HKUST

A Low-Power Low-Voltage Amplifier

ELEC 304 Spring 2010 (Prof. Howard Luong)

Class Project

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I. Design Specifications

Supply Voltage	+/- 1.5 V
Power Consumption	< 1 mW
Low Frequency Gain A_0	> 60 dB
Unity Gain Frequency f_0	> 10 MHz
Slew Rate SR	> 10 V/us
Phase Margin PM	> 60°
CMRR	> 80 dB
Output Swing	> +/- 1.0 V
Load Capacitor C_L	2 pF
Other Requirements	Differential input and single-ended output. Minimize the power consumption

II. Design Comparison

Before venturing deeper into the OP AMP design, it is important to identify the most critical parameter of the specification that have to be achieved, thus selecting the most possible topology for this design. A first order comparison of different topologies is summarized below (Table 1):

Topology	Gain	Unity-Gain Frequency	Output Swing	Slew Rate	Phase Margin	Power	Complexity	Compensation Capacitor
Single-Stage	gm*ro	big	Vdd-3Vdsat	big	90°	1	Simple	N/A
Two-Stage	(gm*ro)^2	small	Vdd-2Vdsat	small	60°	2	Medium	Cc
Telescopic	(gm*ro)^2	big	Vdd-5Vdsat	big	90°	1	Complex	N/A
Folded-Cascode	(gm*ro)^2	big	Vdd-4Vdsat	big	90°	2	Complex	N/A

Table 1. Comparison of possible amplifier architectures across major design specifications [Ref. 1]

III. Design Justification

1. Choice of Topology

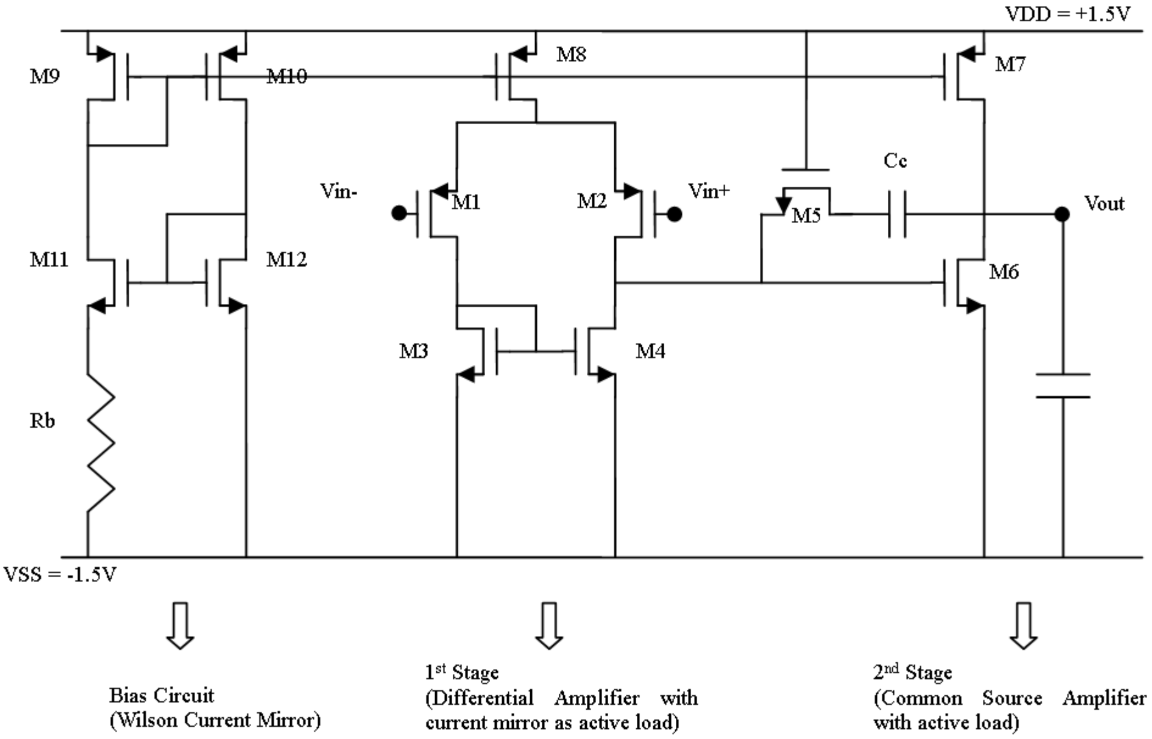
To meet the 60dB gain requirement, a gain on the order of (gm*ro)^2-3 is required, which means we can not choose the simple single-stage approach. All of the remainder three can possibly achieve the Unity Gain frequency and Slew Rate easily. So here the critical parameter is the output swing. It is difficult to get +/- 1.0 V output swing for either telescopic or folded-cascode topologies, even if we assume only 100mV overdrive voltage it hardly leaves any margin for our design. As a result, a two-stage architecture with a differential amplifier as the first stage and a common source amplifier with active load as second stage is favored. Another pro of the two-stage topology is its relative low complexity, especially of its biasing circuit, which gives the other two topologies with complex biasing circuit no significant advantage in terms of power consumption. For the 2 stage topology, a miller compensation capacitor is added to resolve the limitation of phase margin problem, also to increase stability, a transistor operating in triode region is used in series with Cc to eliminate the right half plane zero.

2. Choice of Technology

Although the bipolar junction transistor (BJT) has traditionally been the analog designer's transistor of choice, due largely to its higher transconductance and its higher output impedance (drain-voltage independence) in the switching region, CMOS technology is favored here because characteristics and performance of the devices can be designed by changing the sizes (length and width) of the MOSFETs used. [Ref. 2] Also BiCMOS technology is avoided to reduce fabrication process complexity. The TSMC 0.18um technology is used due to its high transconductance, high output impedance and low threshold voltage as well as small chip area of the device.

IV. Major Design Decisions

1. Circuit description and Schematic



V. Design Methodology

1. Device Characterization

Before starting the design, deveice characterization has been done to extrapolate the physical device parameters of TSMC 0.18um technology. The results are summerized in Table 2 below:

TYPE	W/L	Vth	Id	gm	uCox	Cgs	Cgd	Lambda
NMOS	18u/0.18u	0.484	827.3136u	6.2002m	232.32u	31.7064f	14.94f	0.059
NMOS	5.4u/0.54u	0.440	88.1679u	640.008u	232.29u	22.6058f	4.42f	0.0545
NMOS	1.1u/0.36u	0.450	26.9382u	197.0207u	237.9u	3.2626f	898.79a	0.0635
NMOS	6.66u/0.36u	0.461	149.9208u	1.1509m	238.82u	19.8111f	5.4958f	0.04396
PMOS	10u/1u	-0.418	-24.1208u	159.385u	52.66u	69.57f	7.7811f	0.033
PMOS	3.6u/0.36u	-0.453	-21.8095u	162.57u	60.59u	10.06f	2.76f	0.0525

Table 2. Device Charaterization Results of TSMC 0.18um technology. (|Vgs|=0.7, |Vds|=0.5)

In the following hand calculation, I assume: Vtn=|Vtp|=0.45V, unCox=233u, upCox=53u, Lambda=0.5 for both NMOS and PMOS.

2. Design Flow

Since we have so many different specifications to meet, some inequalities are first derived to give the range of parameters we can design.

Slew Rate

SR > 10 V/us

Slew Rate = $\frac{I_{tail}}{Cc}$ ⇒ (Choosing a very small Cc=500fF to minimize power)

I_{tail} > Slew Rate * Cc = 10 V/us * Cc = 5 uA
To ensure enough margin, design I8=20uA, I1=I2=I3=I4=0.5*I8=10uA.
Expect to get SR=40 V/us.
(After simulation, the SR is far from expectation. This is due to the small Cc I choose and will be explained in detail later.)

Common Mode Rejection Ratio

CMRR > 80 dB = 10000

CMRR = $(2g_{m(dp)} * R_{tail}) * g_{m(mir)} * (R_{o(dp)} // R_{o(mir)})$ [Ref. 3]
To match M1,M2,M3,M4 and reduce systematic offset, design gm1=gm2=gm3=gm4 and I1=I2=I3=I4, so we get:

CMRR = $2 * (\frac{20*gm1}{I8})^2$ > 10000 ⇒ gm1>70.71 uA/V

To ensure enough margin, design gm1=100 uA/V, gm2=gm3=gm4=gm1=100 uA/V.

Then we can determine (W/L)1=(W/L)2= $\frac{g_m^2}{I_8 * uCox}$ = 9.4, (W/L)3=(W/L)4=2.2

Choosing L=5*0.18um=0.9um to increase output resistance and gain, we get:
W1=W2=8.5u, W3=W4=2.12u, L1=L2=L3=L4=0.9u
Expect to get CMRR=20000=86.02 dB

Unity Gain Frequency

UGF > 10 MHz

$w_0 = 2\pi f_0 = \frac{g_{m1}}{Cc}$, since I have designed gm1=100uA/V and Cc=500fF, I expect to get:

ω_0 = 2E08 rad/s, f_0 = 31.8 MHz

Phase Margin

PM > 60°

To get 60° phase margin, the 2nd pole has to be at least 2 ω_0 :

$\frac{g_{m_6}}{C_L} > 2\omega_0$ ⇒ gm6 > 251 uA/V.

To ensure enough margin, design gm6=300 uA/V, and expect to get PM=arctan(f2/GBW)=67.27°

Low Frequency Gain

A_0 > 60 dB

$$A_0 = -g_{m1} * (r_{o2} // r_{o4}) * g_{m6} * (r_{o6} // r_{o7}) = -g_{m1} * \frac{1}{2}\frac{1}{0.05 * I_2} * g_{m6} * \frac{1}{2}\frac{1}{0.05 I_6}$$

Since I have designed gm1=100 uA/V, I2=10 uA, gm6=300 uA/V and assume lamba for both NMOS and PMOS to be 0.05, in order to get a gain of 1000, I6 < 300uA.

But this constrain does not give any lower limit of I6. Based on the principle of reducing power consumption, several I6 values have been tested (5 uA/10uA/20uA/30uA) and finally I6=30 uA was chosen because it satisfies the SR requirements. Why does this one work will be explained in detail later.

From I6=30 uA, gm6=300 uA/V, I can determine (W/L)6=6.46 = (6.15u/0.9u)
(To ensure M6 operate in saturation region and a 200 mV overdrive voltage, W is made a little larger)

Expect to get low frequency gain A0=10000=80 dB

Power Budget	Vdd= 1.5V, Vss= -1.5V, Power Consumption < 1mW

(Vdd-Vss) * I_total < Power ⇒ I_total < 333 uW

Since I have designed I8=20 uA, I7= 30 uA, to minimize power consumption, the bias circuit should be designed such that it takes as less current as possible. So I design I_bias = I9=I10=5 uA.

To get 5 uA biasing current, a Wilson current mirror was used. Design:
Assume the 0.35V overdrive voltage for M9,M10,M8,M7
Vgs=Vgs10=Vgs8=Vgs7=0.8V

(W/L)9=(0.41u/0.36u)=(W/L)10=(W/L)12, (W/L)11=4(W/L)12=(1.6u/0.36u), r_bias=14.4k ohm.

Expect to get 5 uA on both branches.

As I8=4*I9, (W/L)8=4*(W/L)9=(4.08u/0.9u); I7=6*I9, (W/L)7=6*(W/L)9=(6.15u/0.9u).

The total current is: I_total = 5+5+20+30 = 60 uA.
Expect to get 60 uA * 3 V = 0.18 mW power consumption.

Output Swing	Output Swing > +/- 1.0 V

Since the 2nd stage is just a common source amplifier without much headroom, I expect to get the full vdd/vss swing:
Output Swing: +1.5V to -1.5V

Stability Concern	Eliminate the RHP-Zero introduced by Cc

I use a transistor operating in triode region to replace Rz to save chip area. The equivalent Rz we need can be calculated by:

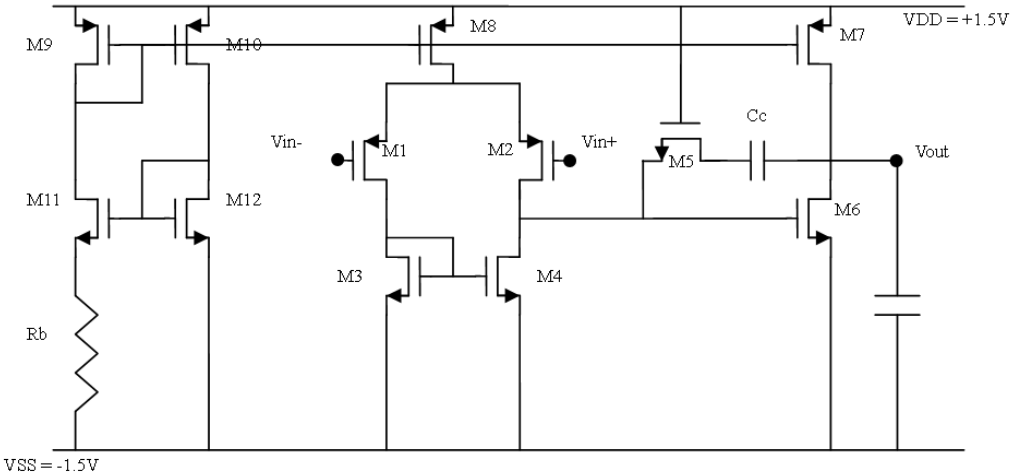
$$R_z = \frac{C_L + Cc}{g_{m_6} * Cc} = 16.667\text{k ohm}$$

$$(W/L)5 = \frac{1}{u_n Cox * Rz * (V_{gs5} - V_{tp})} = 0.1077, \text{ design } (W/L)5 = (0.5u/3.6u)$$

(W has been adjusted a little a bit because of body effect. A large L was chosen because the Zero Compensation failed when (W/L)5=0.05u/0.36u, due to the inexact value of Rz it defined as the size was too small.)

Design flow summary:

1. Assume Cc=500fF.
2. From SR, design I8=20uA, I1=I2=I3=I4=10uA.
3. From CMMR, design gm1=gm2=gm3=gm4=100uA/V, determine (W/L)1,2,3,4.
4. Check whether UGF satisfy the specification.
5. From PM, design gm6=300uA/V.
6. From GAIN, design I6=30uA, determine (W/L)6.
7. Assume Vov=0.35V, design I_bias=I9=I10=5uA. Determine rb, (W/L)7,8,9,10,11,12.
8. Check Power Consumption.
9. Check Output Swing.
10. From CL,Cc,gm6, Determine Rz and (W/L)5.
11. Simulation and check all the results.



Summary of Design Parameters

Parameter	Design Value	Major Constrain Specification	Specification Requirement	Margin
Cc	500 fF	SR		Assuption
I8	20 uA	SR	I8 > 5 uA	+ 300%
I1, I2, I3, I4	0.5*I8 = 10 uA	SR		
gm1, gm2,gm3,gm4	100 uA/V	CMRR UGF	gm1 > 70.71 uA/V gm1 > 31.4 uA/V	+ 41.42 % + 218.47%
I6, I7	30 uA	GAIN SR	I6 < 300 uA I6 can not be too small	+ 900% N/A
gm6	300 uA/V	PM	Gm6 > 251 uA/V	+ 19%
(W/L)1,2	8.5u/0.9u=9.44	gm1,2=100 uA/V I1,I2=10uA		
(W/L)3,4	2.12u/0.9u=2.36	gm3,4=100 uA/V I3,I4=10uA		
(W/L)6	6.15u/0.9u=6.83	gm6=300 uA/V I6=30uA		
(W/L)7	6.15u/0.9u=6.83	I7=30uA		
(W/L)8	4.08u/0.9u=4.53	I8=20uA		
(W/L)9,10,12	0.41u/0.36u=1.14	POWER	I9=I10=5uA	
(W/L)11	1.6u/0.36u=4.44		I_bias=5uA	
Rb	14.4k ohm		I_bias=5uA	
(W/L)5	0.5u/3.6u=0.14	STABILITY		

Table 3. Summary of Design Parameters

Comparision of design expectation and HSPICE simulation

(All specifications are met with minimum power consumption)

Parameter	Design Value	Expect Value	Simulation Value	Difference	Remark
Device Parameters					
gm1,gm2	100 uA/V	100.03 uA/V	100.9627 uA/V	+0.9%	Difference due to inexact mobility value in hand calculation.
gm3,gm4	100 uA/V	104.60 uA/V	106.8866 uA/V	+2.2%	
gm6	300 uA/V	308.61 uA/V	322.9033 uA/V	+4.6%	
I8	20 uA	19.79 uA	20.41 uA	+3.1%	Difference due to the unbalance of two branches of the biasing current circuit.
I1,I2,I3,I4	10 uA	9.89 uA	10.21 uA	+3.2%	
I6,I7	30 uA	29.83 uA	31.45 uA	+5.4%	
I9	5 uA	5 uA	4.98 uA		
I10	5 uA	5 uA	5.47 uA		
Circuit Parameters					
POWER	0.18mW	0.18207mW	0.18695mW	+2.7%	Remark [1]
GAIN	80dB	80.39dB	78.2dB	-27.8%	Remark [2]
UGF	31.83MHz	31.84MHz	38.4 MHz	+20.6%	Remark [3]
SR	40V/us	39.58V/us	12.09V/us	-227%	Remark [4]
PM	67.27°	67.27°	75°	+9.3%	Remark [5]
CMRR	86.02dB	86.20dB	85.59dB	-6.8%	Remark [6]
SWING	+/- 1.5V	+/- 1.5V	+/- 1.5V	0	Remark [7]

Table 4. Comparsion of Design Parameters expectation and HSPICE simulation

(Difference between “Design Value” and “Expect Value” is due to rounding of device width and length in simulation)

3. Remarks & Discussions:

[1] POWER: Refer to Figure 1.

I have been trying to trade-off other slack specifications to push the power consumption to a limit. As the current goes lower, many problems emerge and I have to reconsider other possible solutions. After several interations, I managed to limit the power to only 0.187mW. Comparing to 0.245mW and 0.458mW of my previous designs(another design with 0.12mW power consumption failed to meet the SR requirement), I have reduced the power consumption more than half and used no more than 1/5 of the power budget.

[2] GAIN: Refer to Figure 2.

The gain I got is 78.2dB, which is much higher than the 60dB requirement. Noted that although there is a big discrepancy between the hand-calculation result and simulation result, it mainly sterns from the inaccurate assumpsion, that lamba of both NMOS and PMOS are 0.05 I made before. Also because the gain is very large, a little difference in dB makes it look very huge in linear scale, in fact the calucation result is quite accurate and acceptable. It seems that it may be possible to futhur reduce the power consumption by degrading the gain a little bit. But in fact, it is not very practical because the differential mode gain constitude a large part of the 80dB CMRR, which is one of the most difficult specification for this project. This consideration is later varified by the CMRR simulation.

[3] UGF: Refer to Figure 3.

I got 38.4 MHz UGF, which exceeds the specification. The high UGF (as well as Gain) is due to the small Cc (0.5nF) I choose. A small Cc requires a big gm1, which is also preferrable for high gain and high CMRR. Making Cc small also gives I8 more room because it lesens the SR contrain, thus a smaller I8 as well as power can be achieved. Another reason why the UGF exceeds expectation is because of the benefit of the pole spitting brought by miller compensation.

[4] SR: Refer to Figure 4.

1 got only 12.09V/us slew rate, barely exceeding the requirement. Because I tried to reduce the power as much as possible, the current of the 2nd stage (I6) has to be reduced because I must keep the current of the 1st stage large enough to drive Cc to get enough slew rate. After several simulations, it turns out that in fact the current of the 2nd stage is also affecting the slew rate, which explains the big dicrepancy(-227%) between hand calculation and simulation result. The equation SR=I_tail/Cc is not longer accurate when Cc is very small. The slew rate now is dominated by the 2nd stage, so I6 and C_load as well as other parasitic capacitors such as Cgs, Cgd should all be be taken into account, which makes the accurate estimation very difficult. A rough estimate can be made by equation: SR=I6/C_load, which gives 15 V/us. This is very close to the simulation result. Also it points out the importance to leave margins in analog IC design.

[5] CMRR: Refer to Figure 5.

The CMMR I got is 85.59dB. As I said in [2], the 80dB CMMR is not easy to achieve because the common mode rejection (CMR) is only contributed by the 1st differential stage (the 2nd stage has no contribution). This makes the CMR value not very high, typically from -5 to -10 dB and futhur improvement by scale up the dimention of the devices is not very significant. So we have to get a low frequency gain much higher than the 60 dB requirement to meet the 80 dB CMMR specification.

[6] Output Swing: Refer to Figure 6.

The output swing is +/- 1.5V. As a result of the 2-stage topology with a common source amplifier as 2nd stage, the output swing can be maximized and is only a minor consideration in this design. Other topologies like telescopic and folded-cascode are not easy to achieve the required output swing because the large overhead of the stacked transistors.

VI. HSPICE Simulations & Results

<table>
<tr><td>Power Consumption</td><td>Figure1. Power Consumption: $P = 0.187mW < 1mW$</td></tr>
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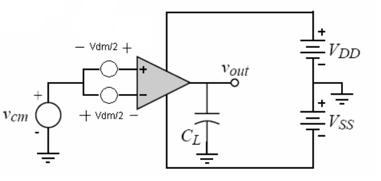

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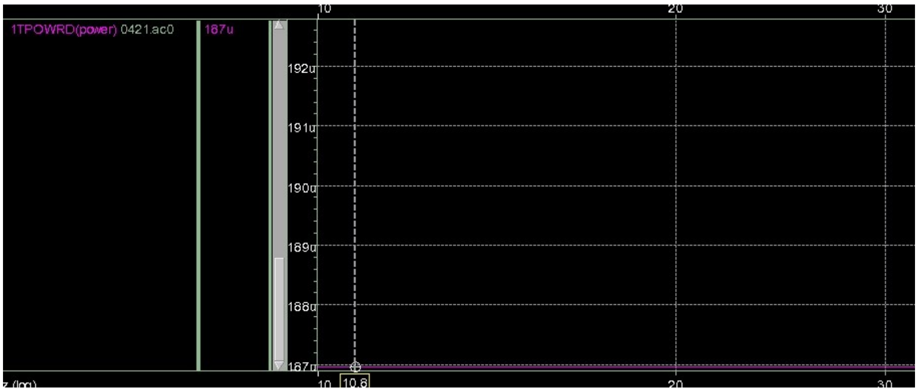

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<tr><td>Gain</td><td>Figure2. Low Frequency Gain: $A0 = 78.2$ dB > 60 dB</td></tr>
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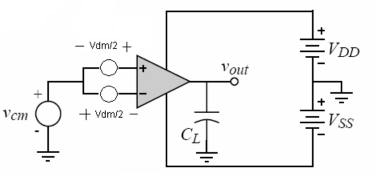

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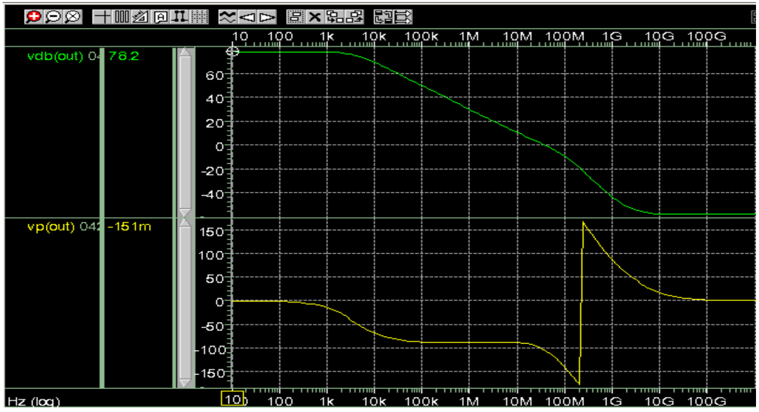

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<tr><td>Unity Gain Frequency
Phase Margin</td><td>Figure3. Unity-Gain Frequency $f0 = 38.4$ MHz > 10 MHz
Phase Margin $PM = 75° > 60°$</td></tr>
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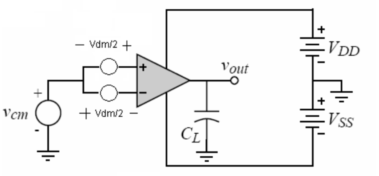

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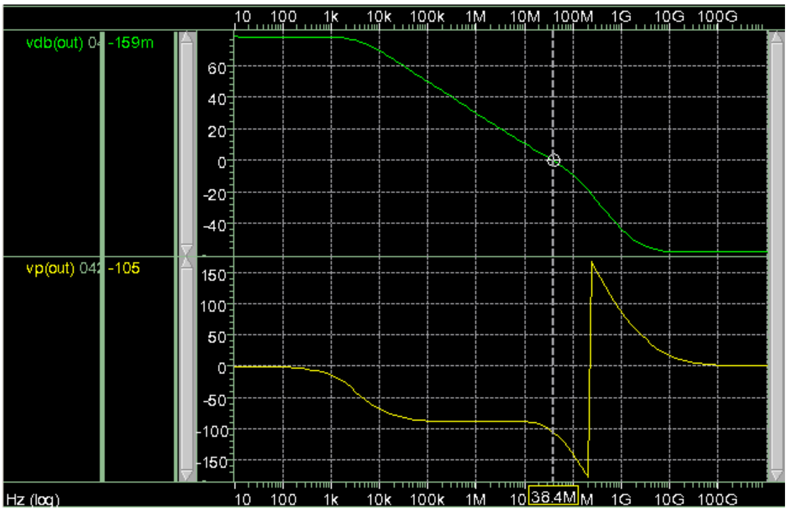

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<tr><td>Slew Rate</td><td>SFigure 4. Slew Rate $SR = 12.09$ V/us > 10 V/us</td></tr>
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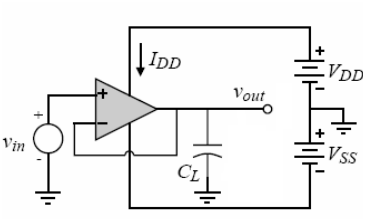
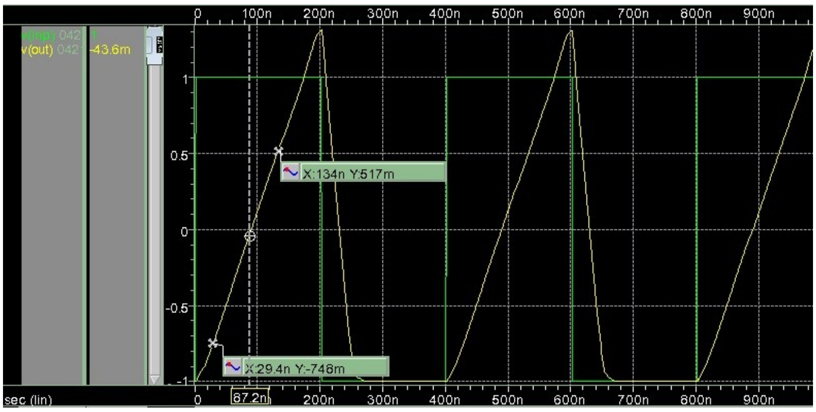
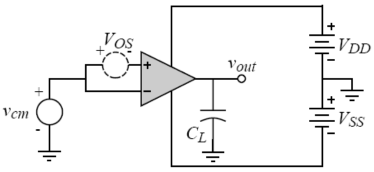
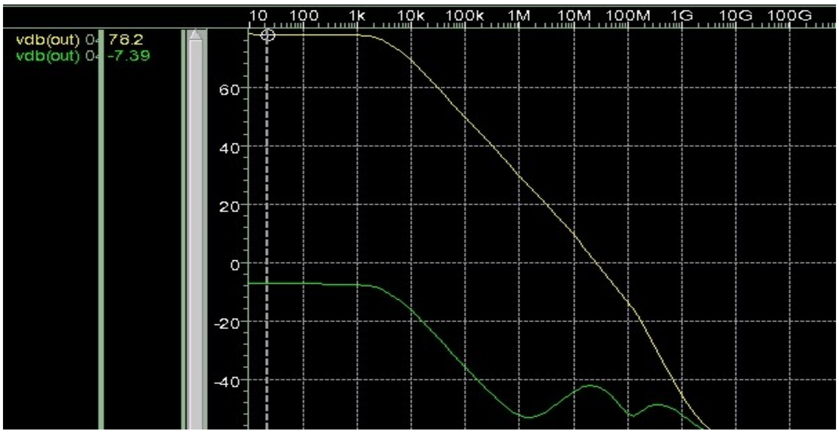
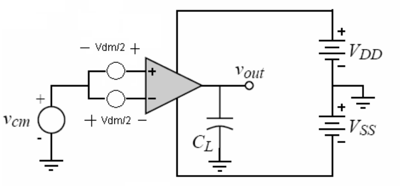
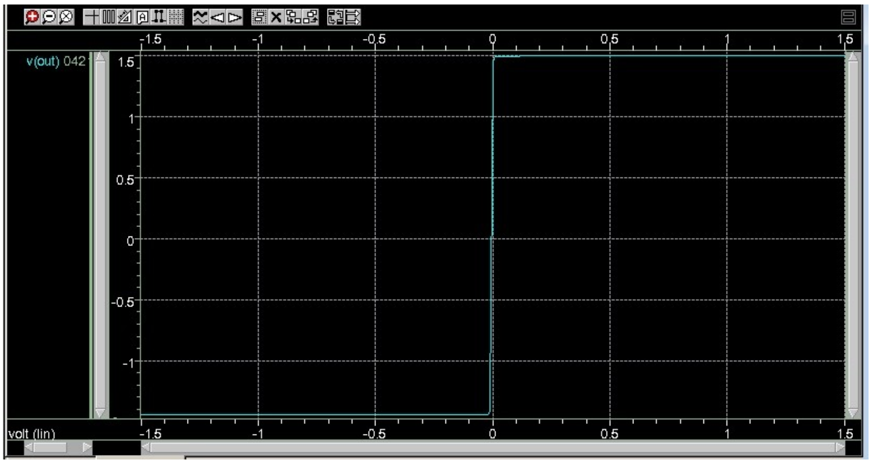
	
Common Mode Rejection Ratio	*Figure 5. Common Mode Rejection Ratio CMRR = 85.59 dB > 80 dB (Gain-dm = 78.2 dB, Gain-cm = -7.39 dB)*
	
Output Swing	*Figure 6. Transfer Function. Output Swing = +/- 1.5 V > +/- 1.0 V*
	

(Setup circuit schematics are taken from "Opamp Design Example")

VII. Project Summary

This is the first time for me to design a complete amplifier with given specifications. Facing so many different specifications, it's very hard to start the design process without some reasonable assumptions because all the requirements are interrelated and there is no obvious origin to start with. As Prof. Howard said, it's important to first make some assumptions and break the loop, and it is necessary to iterate the process several times until all the specifications are met.

The final design met all the specifications with only 0.18mW power consumption. Also I have tried to reduce the chip area by choosing the smallest possible transistors sizes. Further more, transistors with aspect ratio larger than 100/1 are intentionally avoided. To minimize noise, P-transistor input pair has been selected instead of their N type counterparts.

Through this project, I learned the basic process of designing amplifiers. First, I identified the most difficult specification and chose the most promising topology and technology for this project. Because of the large discrepancy of the physical parameters of different technologies, device characterization was done to extrapolate the necessary physical parameters before the design process. Then hand-calculation was employed to determine the range of the possible design parameters. From the ranges of different parameters, I can have a rough idea of which specification is the most critical thus readjusting the design margin allocation. Circuit simulation was followed and several refining iterations were used to get the minimum power consumption. It's also important to point out that device characterization enabled me to estimate the simulation result quite accurately, at the same time speeding up the design process.

VIII. Possible Improvement

Although this design has met all the design specifications with only 1/5 of the power budget, it is far from perfect. Some possible improvements include:

1. Add one more buffer stage, such as a source follower, to reduce the output impedance such that it can deliver voltage much more efficiently.
2. The size of some transistors may be scaled down to save chip area.
3. From the Slew-Rate simulation waveform, the problem of overshoot was observed (about +20%), it may be solved by more accurate compensation and RHP-zero elimination.

IX. Individual Contribution

This work is done by myself individually.

APPENDIX

HSPICE Codes:

```
*two stage operational amplifier
.GLOBAL vdd vss

.include 'cmos018.mod'

.SUBCKT op inn inp out r_bias
m1 e inn d vdd cmosp W=8.5u L=0.9u
m2 f inp d vdd cmosp W=8.5u L=0.9u
m3 e e vss vss cmosn W=2.12u L=0.9u
m4 f e vss vss cmosn W=2.12u L=0.9u
m5 g vdd f vss cmosn W=0.5u L=3.6u
*r5 g f 10k
m6 out f vss vss cmosn W=6.15u L=0.9u
m7 out a vdd vdd cmosp W=6.15u L=0.9u
m8 d a vdd vdd cmosp W=4.08u L=0.9u
m9 a a vdd vdd cmosp W=0.41u L=0.36u
m10 b a vdd vdd cmosp W=0.41u L=0.36u
m11 a b r_bias vss cmosn W=1.6u L=0.36u
m12 b b vss vss cmosn W=0.41u L=0.36u
cc g out 500f
.ENDS

xa inn inp out r_bias op
rb r_bias vss 14.4k
cL out vss 2p

vdd vdd 0 dc 1.5
vss vss 0 dc -1.5

e+ inp 102 100 0 0.5
e- inn 102 100 0 -0.5
vcm 102 0 dc=0
vs 100 0 dc=0  ac=1

*vinn inn 0 dc 1.5 ac 1
*vinp inp 0 dc 1.5



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.ac dec 10 10 1000000meg
.meas ac gain max vdb(out)
.meas ac phase_margin find=vp(out) when vdb(out)=0
.meas ac unit_gain_freq when vdb(out)=0
.probe ac vp(out) vdb(out)
.meas ac power avg power
.end
```

REFERENCE

[1] Howard Luong, Basic Amplifier Design – Summary and Comparison, page 20.

[2] Wikipedia – MOSFET, http://en.wikipedia.org/wiki/MOSFET.

[3] Gray, et al, Analysis and design of analog integrated circuits, 4th edition, page 431.