A Classic Wide Band Operational Amplifier Design

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Abstract

A CMOS wide band operational amplifier is designed based on the classical two stage differential input criteria and simulated using Mentor Graphics tools. A set of design specifications has been taken into account as a benchmark, but it is tried to extend them further where ever possible.

1. Introduction

"CMOS operational amplifiers have become an integral part of many integrated circuit chips fabricated today in a number of application areas. These amplifiers offer a number of advantages in terms of power dissipation, die area, and compatibility with digital circuits when compared with their bipolar counterparts" [1]. The classical two stage op-amp design approach is used which block diagram is shown in Figure 1. The first stage is a differential amplifier with differential voltage gain of A_1. It is followed by another gain stage such as common source with gain of A_2.

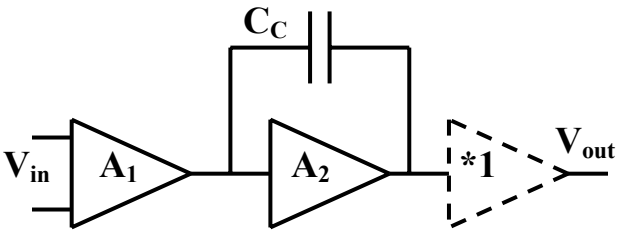


Figure 1. Block Diagram of two-stage opamp

If the op-amp is intended to drive a resistive or large capacitive load, a third unity gain buffer is added but this stage is not needed for purely capacitive loads which is most often the case.

2. Overview

The op-amp circuit diagram is shown in Figure 2 and the design requirements are summarized in Table 1. Transistors M_1 to M_5 make the first stage, which is a differential amplifier with M_1 and M_2 as differential pair, M_3 and M_4 as current mirror and active load, and M_5 as their biasing current source. The second stage consists of M_6 and M_7 which is a PMOS common source amplifier stage with an active load. These to stages must provide a DC gain as high as 85dB. There is no need for a unity gain buffer stage in this design because the load is a fairly small fully capacitivew one. The compensation capacitor C_c builds a local feedback over the second stage as shown in Figure 1. The effect of this capacitor on the first dominant pole is A_2 times its value because of the Miller effect. In other words the function of this capacitor is to increase phase margin by splitting the first and second dominant poles apart. Transistor M_8 operates in triode region to act as a nulling resistor R_z in series with C_c. Finally the biasing branch is a chain of transistors M_9 to M_{12}, connected in series between supply rails to make a multiple voltage divider for biasing current sources and the nulling resistor (M_8).

Table 1. Design Specifications for the opamp

Parameter	Specification
DC Gain	≥85 dB
Input CMR	Supply within 0.75V
Output Swing	Supply within 0.3V
Power Dissipation	250μW
Unity Gain Freq.	50MHz
Settling Time (0±1V)	250nS to 0.1%
CMRR at DC	≥85dB
PSRR	≥85dB at DC ≥40dB at 800KHz
Load Capacitance	2pF
Supply Voltage	±2.5V

3. Design Approach

The design procedure was very close to the approach proposed in [2] with some provisions to satisfy the design specifications which are not covered in that article. The λ equal to 0.4μm technology is utilized which leads to the minimum feature size equal to 0.8μm. Minimum length transistors are chosen trough the design to minimize the stray capacitors as much as possible knowing that this may cause problems due to the channel length modulation effect and process variations. This will be addressed in more detail in discussion section.

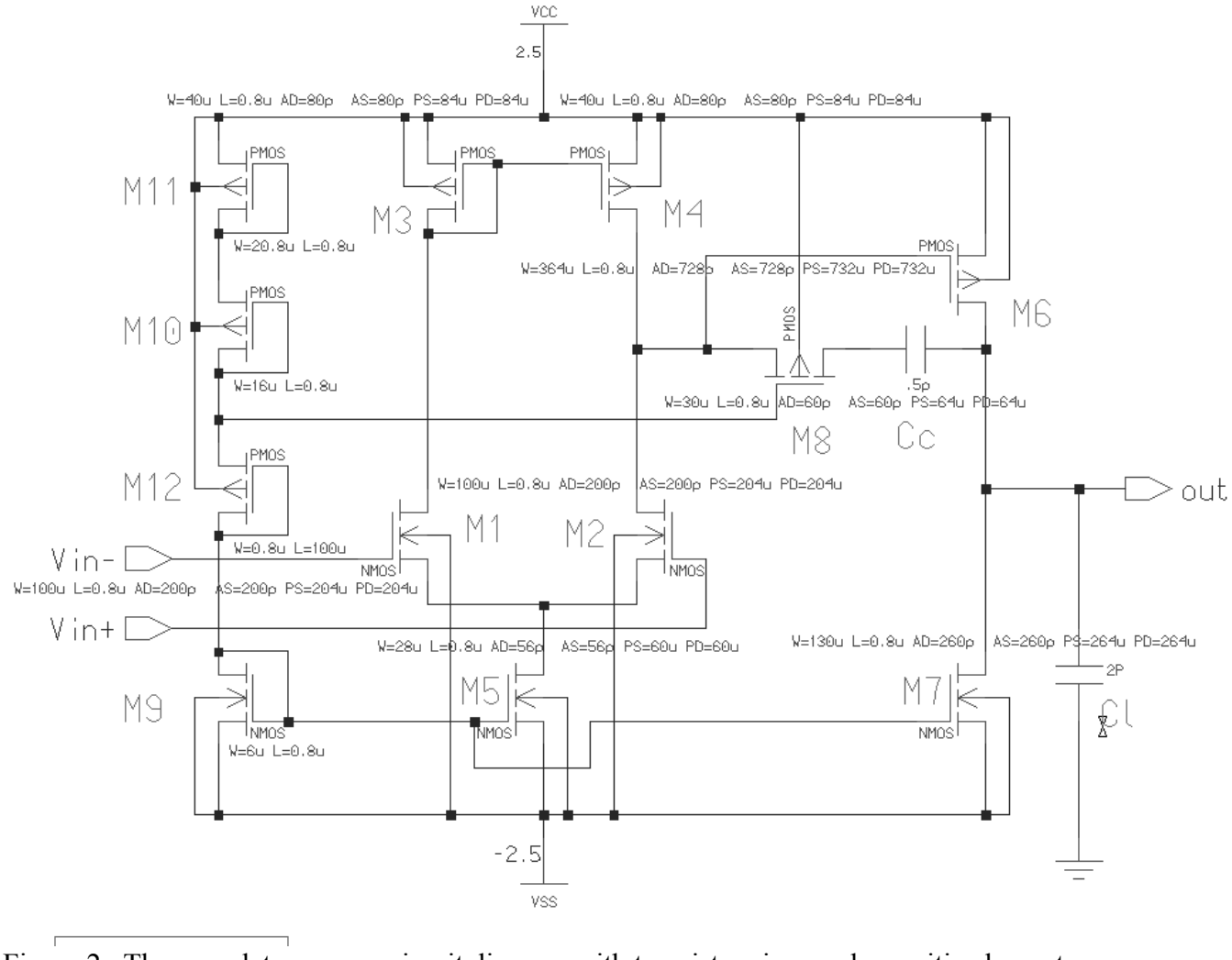


Figure 2. The complete op-amp circuit diagram with transistor sizes and parasitic elements

The are three branches in this circuit which pass current from *VDD* to *VSS*. Since there is power consumption limitation in the specifications but no size limitation, these currents were chosen in advance to be changed later in simulations if needed. To simplify the design it is assumed to have two dominant poles which are splitted apart by the compensation capacitor. The C_c value is chosen 0.5pF according to (1) to give 60° of phase margin.

$$C_c > 0.22C_L \quad \textbf{(1)}$$

This might seem conservative, but later simulations showed that this is needed to compensate for the effects of other parasitic and non-dominant poles and zeros. Based on Equation (2) I_{D5} and C_C define the slew rate which is not stated directly in the specs but it should not take more than 100nS to slew from 0V to ±1V in order to meet the 250nS settling time requirement [3].

$$SR^+ = \frac{I_{D5}}{C_c} > 10^7 V/Sec \quad \textbf{(2)}$$

This condition guaranties the rise time but for the falling step inputs, M_6 cuts off and the load capacitor should be discharged by the second stage current source. This is stated in Equation (3) and defines the minimum value for I_{D7}.

$$SR^- = \frac{I_{D7}}{C_L} > 10^7 V/Sec \quad \textbf{(3)}$$

The biasing branch current is very flexible and later defines M_9, M_5 and M_7 size ratios. So it was chosen 1μA for simplicity. These branch currents should finally satisfy the power consumption constraint:

$$(V_{DD} + V_{SS})(I_{D9} + I_{D5} + I_{D7}) < 250\mu W \quad \textbf{(4)}$$

M_5 and M_3 ratios are basically defined by input *CMR* according to Equations (5) and (6) respectively. Here considering some safety margins might help to compensate for some secondary effects like the body effect and V_{dsat1}. But care must be taken by Equation (7) to verify that the pole of M_3 due to C_{gs3} and C_{gs4} will not be dominant.

$$CMR^- = V_{SS} + V_{T1} + \sqrt{\frac{I_{D5}}{\mu_n C_{ox}(W/L)_5}} \quad \textbf{(5)}$$

$$CMR^+ = V_{DD} - V_{T3} - \sqrt{\frac{I_{D5}}{2\mu_n C_{ox}(W/L)_3}} \quad \textbf{(6)}$$

$$\frac{g_{m3}}{2C_{gs3}} \geq 10GB \quad \textbf{(7)}$$

$$C_{gs3} = 0.67W_3L_3C_{ox}$$

The op-amp gain is controlled by the trans-conductance and output resistance of the two stages as shown in Figure 1.

$$A_v = A_1A_2 = \frac{2g_{m2}g_{m6}}{I_{D5}(\lambda_2 + \lambda_4)I_{D7}(\lambda_6 + \lambda_7)} \quad \textbf{(8)}$$

Since the branch currents are already defined, not much can be done on output resistances but M_2 and M_6 ratios can be set to meet the required gain. This leads to:

$$\left(\frac{W}{L}\right)_2\left(\frac{W}{L}\right)_6 \geq 1600 \quad \textbf{(9)}$$

The dominant poles are also placed by g_{m2} and g_{m6}. To achieve the desired gain-bandwidth and phase margin [2]:

$$g_{m2} = GB*C_c = 157\ \mu mho \quad \textbf{(10)}$$

$$\frac{g_{m6}}{g_{m2}} = 2.2\frac{C_L}{C_c} \quad \textbf{(11)}$$

These two equations define M_2 and M_6 ratios and satisfy (9) as well. 0 Transistor M_4 should be tailored to keep M_6 in saturation region by having the same V_{gs}. This requires to have:

$$\frac{(\frac{W}{L})_4}{(\frac{W}{L})_6} = \frac{I_{D4}}{I_{D6}} \qquad \textbf{(12)}$$

The ratio achieved by (12) should be matched with (6) and (7) to get the desired *CMR* and *GB* respectively.

To achieve a better phase margin as well as higher bandwidth, the RHP zero was moved to LHP and on top of the second pole by inserting a PMOS nulling resistor biased in triode region in series with C_c. The biasing voltage for M_8 was generated by M_{10} and M_{11} which are placed on the same biasing branch as M_9 to save area and power. It can be shown [1] that for this purpose M_8, M_{10} and M_{11} ratios should be chosen according to (13) and (14). The size of one of these transistors can be arbitrarily chosen.

$$(\frac{W}{L})_8 = \sqrt{(\frac{W}{L})_6(\frac{W}{L})_{10}\frac{I_{D6}}{I_{D10}}}(\frac{C_c}{C_c + C_L}) \qquad \textbf{(13)}$$

$$\frac{(\frac{W}{L})_{11}}{(\frac{W}{L})_6} = \frac{I_{D11}}{I_{D6}} \qquad \textbf{(14)}$$

M_{12} is a long transistor which is added in the biasing branch to make the required voltage divider and its ratio can be found so that:

$$V_{gs12} = V_{DD} - V_{SS} - V_{gs9} - V_{gs10} - V_{gs11} \qquad \textbf{(15)}$$

At this stage the design is completed and other design specs can be checked to see if any change of transistor sizes or biasing currents is needed. *CMRR* for this topology can be calculated from Equation (16).

$$CMRR = (1+g_{m2}*r_{o5})\, g_{m4}(r_{o5} \| r_{o4}) \qquad \textbf{(16)}$$

Since the open loop gain was designed over the required value, and the common mode gain is less than 1, the *CMRR* can be easily achieved.

To calculate *PSRR*, the general equation is simplified for DC and 800KHz. Equations (17) to (19) show that at DC, $PSRR^+$ and $PSRR^-$ are much higher than the required value due to higher low frequency gain and at 800KHz the design objective is very close to specifications which can be adjusted through simulations.

$$\begin{aligned} A_{V_0^+} &= g_{m2}g_{m6}r_{o6}(r_2 \| r_4) \\ A_{V_0^-} &= g_{m2}g_{m6}r_{o7}(r_2 \| r_4) \end{aligned} \qquad \textbf{(17)}$$

$$\begin{aligned} \omega_P^+ &= \frac{GB}{A_{V_0^+}} \\ \omega_P^- &= \frac{GB}{A_{V_0^-}} \end{aligned} \qquad \textbf{(18)}$$

$$A_{V_{800K}^+} = A_{V_0^+}\left|\frac{1}{1 + j\frac{\omega_T}{\omega_P^+}}\right|$$

$$A_{V_{800K}^-} = A_{V_0^+}\left|\frac{1}{1 + j\frac{\omega_T}{\omega_P^+}}\right| \qquad \textbf{(19)}$$

$$\omega_T = 2\pi * 800KHz$$

The settling time constraints can be set for this design using the generalized second order system model. But since all of the design parameters were defined by other constraints and settling time is highly sensitive to other parasitic components which can not be included in this simplified design approach, it was decided to deal with it in simulations and fixing it through iterations.

Table 2. Transistor sizes and currents based on hand calculations

Transistor#	Width	Length	Current
M1	39μm	0.8μm	2.5μA
M2	39μm	0.8μm	2.5μA
M3	36μm	0.8μm	2.5μA
M4	36μm	0.8μm	2.5μA
M5	22μm	0.8μm	5μA
M6	300μm	0.8μm	25μA
M7	112μm	0.8μm	25μA
M8	5μm	0.8μm	0
M9	6μm	0.8μm	1μA
M10	16μm	0.8μm	1μA
M11	19μm	0.8μm	1μA
M12	0.8μm	44μm	1μA

Table 2. summarizes the hand design transistor sizes and expected drain currents.

4. Transistor and Bias Summary

Table 3. lists transistors used in this design with their dimensions, biasing parameters, trans-conductance and output conductance after several simulations and changing design parameters to achieve all of the specifications.

5. Op-Amp Performance

Table 4. compares design objectives which was expected after hand calculations and the final design performance after fine tuning the design by several simulations and changing parameters through iterations.

6. Discussion

The original circuit of Figure 2. is not suitable for most of the simulations which are performed to derive op-amp performance. So several elements were added to the original circuit and simulations performed by assigning too high or too low values to these elements to act as open or short circuit according to the configuration of interest. This closed loop op-amp circuit is shown in Figure 3.

One of the most important phenomena which affects the general circuit performance and specifically the overall gain is the channel length modulation. The significance of this effect was noticed after failing to get the gain spec for more than a weak using the Mentor Graphics level 2 models which are

Table 3. Transistors used in this design with their dimensions, biasing parameters, trans-conductance and output conductance.

Transistor#	W(μm)	L(μm)	I_D(μA)	$\lvert V_{GS}(V)\rvert$	$\lvert V_{DS}(V)\rvert$	g_m(mho)	g_{ds}(mho)
M1	100	0.8	2.67	0.891	2.66	4.08e-4	2.72e-7
M2	100	0.8	2.67	0.891	2.66	4.08e-4	2.72e-7
M3	40	0.8	2.67	0.731	0.731	1.72e-4	2.28e-7
M4	40	0.8	2.67	0.731	0.731	1.72e-4	2.28e-7
M5	28	0.8	5.34	0.737	1.609	2.88e-4	6.10e-7
M6	364	0.8	26.8	0.731	2.54	1.77e-3	1.98e-6
M7	130	0.8	26.8	0.737	2.46	1.46e-3	2.79e-6
M8	30	0.8	0	0.801	7.38e-9	2.88e-11	1.01e-4
M9	6	0.8	1.03	0.737	0.737	5.57e-5	1.31e-7
M10	16	0.8	1.03	0.806	0.806	6.81e-5	8.77e-8
M11	20.8	0.8	1.03	0.727	0.727	7.74e-5	8.83e-8
M12	0.8	100	1.03	2.73	2.73	1.09e-6	7.54e-8

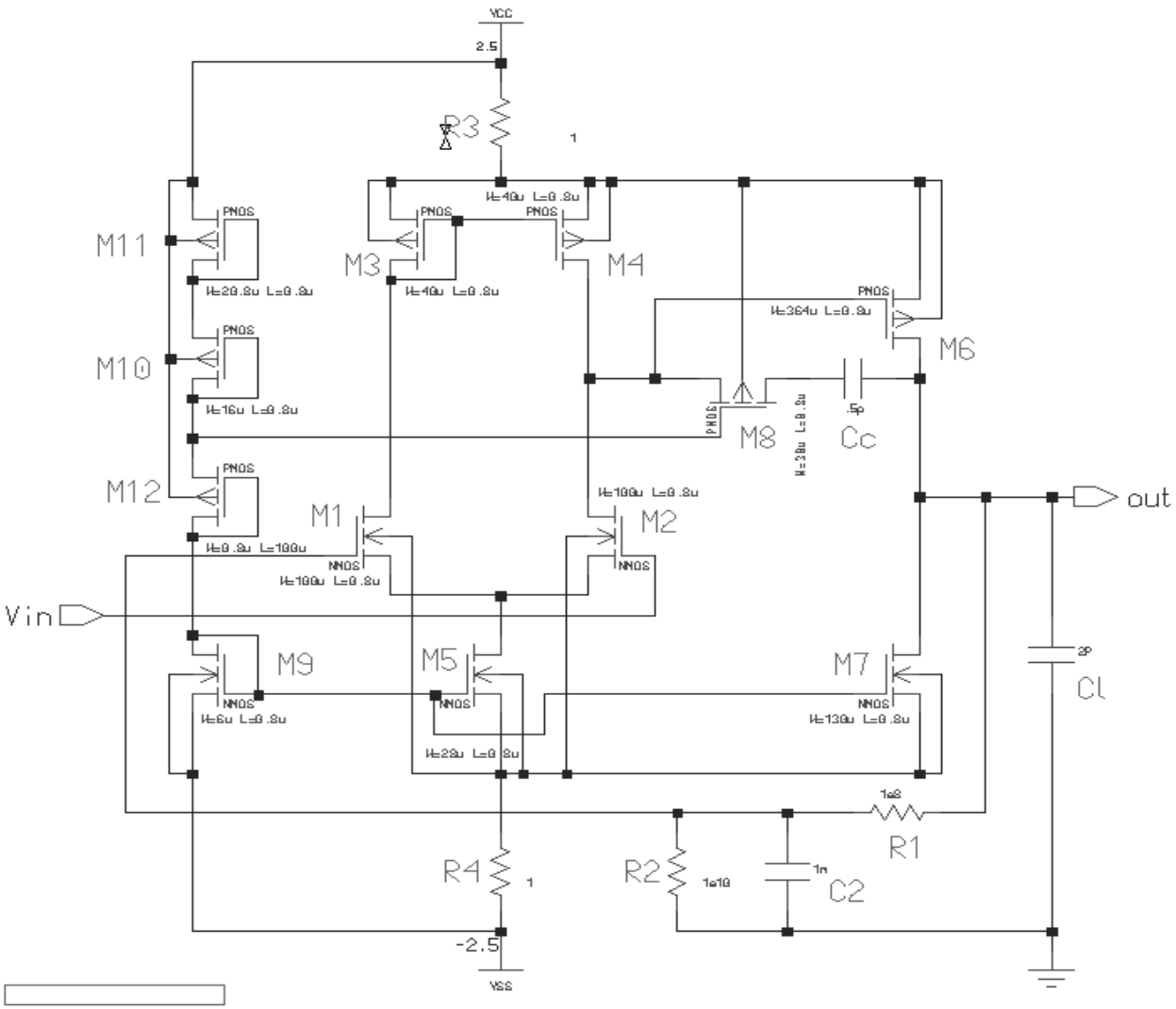


Figure 3. The closed circuit op-amp used for simulations and performance measurement

equal to SPICE level 49 BSIM models. These models include the effects of short channel length and high electric field. The result is that the output resistance of each stage is much less than what is expected from simple long-channel model calculations. A remedy to minimize the effect of channel length modulation and process parameter variation which also has the advantage of a better matched input differential stage is to use larger devices with drawn channel length higher than 1.6μm. But on the other hand, this leads to larger devices which makes the effect of parasitic capacitors worse.

Another effect seen when using higher level models was the second stage "bump" which limits the op-amp band width and makes its compensation much more complicated. This problem arises when the circuit has 4 dominant poles due to parasitic components of the second stage instead of 3 poles which was considered in the simplified small signal model. These poles no longer remain on the real axis, but split apart and make a pair of complex poles. These poles can make the circuit under damped and cause peaking or even oscillation if their real part become less than the first dominant pole [4].

Table 4. Comparison between design specifications, hand design objectives and the simulated performance

Parameter	Specification	Design Objective	Performance
DC Gain	≥85 dB	88.4 dB	106.8 dB
CMR^+	1.75 V	1.75 V	2.46 V
CMR^-	-1.75 V	-1.75 V	-1.80 V
Max Output	2.2 V	2.4 V	2.49 V
Min Output	-2.2 V	-2.4 V	-2.49 V
Power Dissipation	250 μW	155 μW	166 μW
Unity Gain Freq.	50 MHz	50 MHz	76.5 MHz
Settling Time (+1V)	250 nS to 0.1%	-	128 nS
Settling Time (-1V)	250 nS to 0.1%	-	346 nS
Slew Rate	-	1e7 V/Sec	9.8e6 V/Sec
CMRR at DC	≥85dB	102.5 dB	107.14 dB
$PSRR^+$ at DC	≥85dB	106.3 dB	117.1 dB
$PSRR^-$ at DC	≥85dB	102.6 dB	91.8 dB
$PSRR^+$ at 800KHz	≥40dB	36 dB	42.3 dB
$PSRR^-$ at 800KHz	≥40dB	36 dB	40.8 dB
Compensation Cap.	-	0.5 pF	0.5 pF
Offset Voltage	-	-	2.63 μV
Phase Margin	-	60°	49°

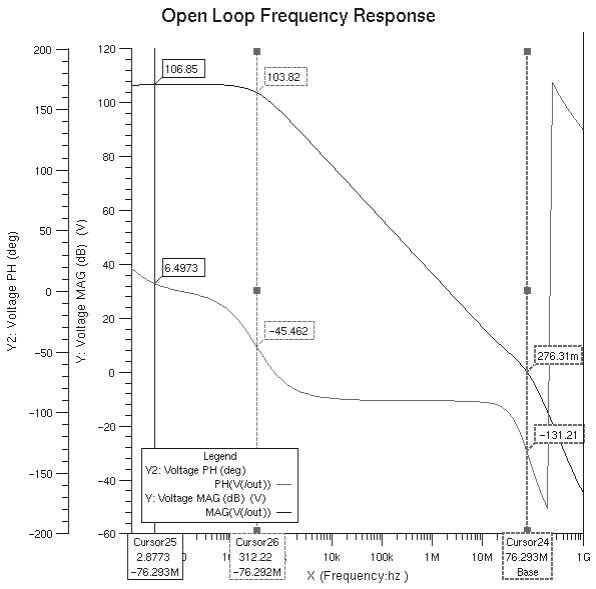
In the rest of this section the method for measuring each parameter is stated separately along with the simulation results.

6.1. Open-loop Frequency Response

To measure the open-loop frequency response of the op-amp, A 1V frequency sweeping AC source is applied to its non-inverting input while its inverting input bias should be DC stabilized. This is done with the circuit shown in Figure 4b in which R_1C_2 time constant is chosen too large in order not to affect the frequency response. In the circuit of Figure 3 *R1* was set to 100MΩ and *C2* to 1000μF. The simulation result is shown in Figure 4a which gives *DC Gain*, *GB*, and *PM* parameters. As discussed in [2] and shown in Equations (8) and (10), Increasing M_1 size ratio increases both gain and bandwidth and as long as the input source is considered ideal, has minimal deteriorating effect. The pole-zero plot of the open-loop circuit is shown in Figure 5. The dominant poles are located at 307.2Hz, 23.3MHz, and 56MHz. The second pole is nulled very well by the LHP zero which is located at 24.37MHz. The frequency distance between this pole-zero doublet has a significant effect on settling time and has discussed in [3].

6.2. Settling Time and Slew Rate

Settling time was simulated and measured by unity gain feedback. Returning to circuit of Figure 3, *R1* was set to 1Ω and *C2* to 1fF which has no effect on closed-circuit performance. The output transient for +1V and –1V step inputs are shown in Figure6a. and 6b. respectively. The input step is applied at T = 1μs in each case and the waveform is magnified to show less than



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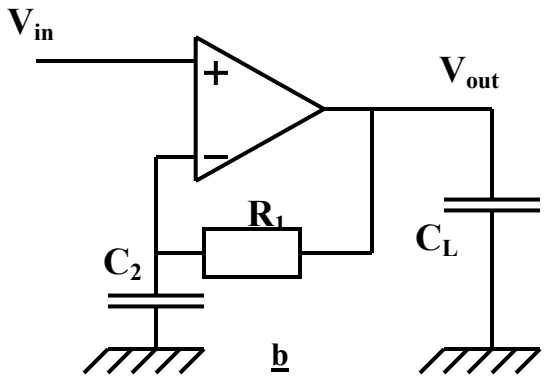


Figure 4. The Open-loop Frequency Response (a) and its measuring circuit. (b)

1mV fluctuations. As stated in section 3 and [3], settling time is composed of two periods. In the first period, output is limited by slew rate and changes from 0V to near its final value (here +1V or –1V). In this period the amplifier acts in a nonlinear fashion. SR^+ is defined in Equation (2) by the current available to charge C_c, but SR^- is mainly limited by the second stage current source which has to discharge C_L as shown in Equation (3).

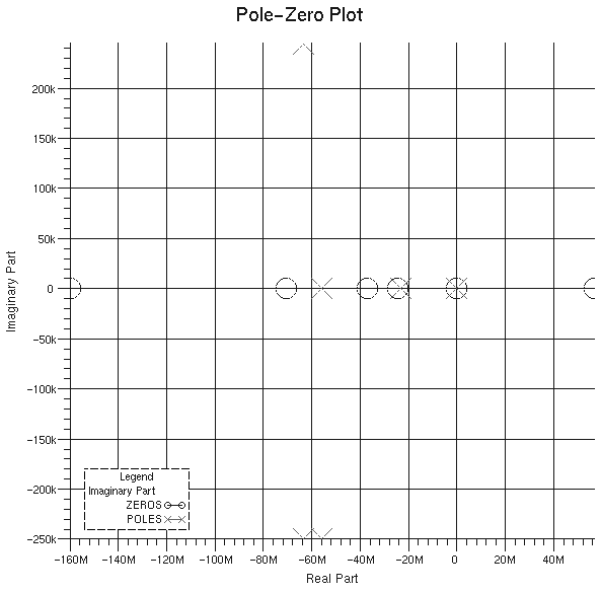
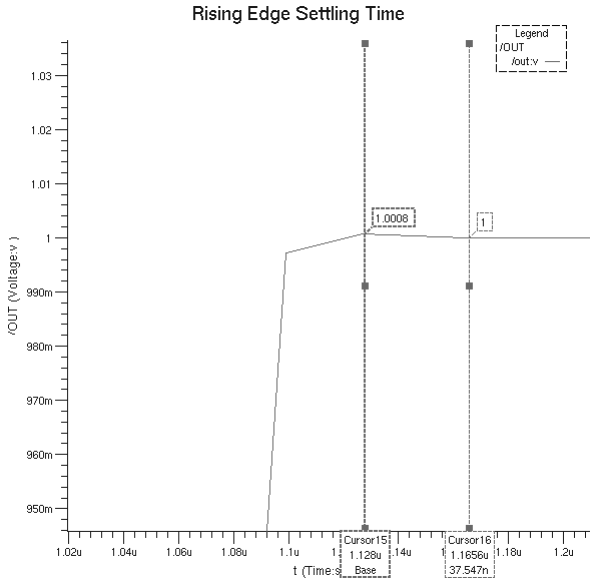


Figure 5. Pole-Zero plot of the open-loop op-amp circuit.

Slew rate was measured using the same unity gain feedback loop and step input. The simulation result is shown in Figure 7 and according to Table 4 matches with design computations very well. In the second portion of settling time the amplifier output is near its final value and acts in a quasi-linear fashion. The second period of settling time is very sensitive to phase margin and the value and distance between the second pole-zero doublet [3] specially when 0.1% of the final value is concerned. To meet this requirement, the first and second branch currents were increased a little by decreasing M_9 ratio and also M_8 and M_{10} ratios were carefully adjusted to achieve an appropriate distance between P_2 and Z_1.



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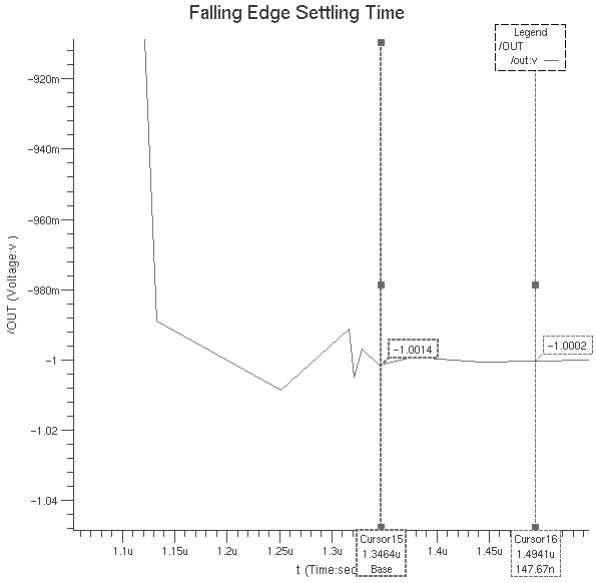

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Figure 6. Rising(a) and Falling(b) edge settling times.

6.3 Common Mode Rejection Ratio

To measure *CMRR* at DC, differential and common mode gains should be known. A_{DM} was measured by the circuit of Figure 4b and gave 106.8 dB at DC. To measure A_{CM}, circuit of Figure 8 was used which value was 0.86 (-1.29dB). This circuit is also useful to measure the op-amp input offset which arises from mismatches between M_4, M_7, and M_6 sizing ratios.

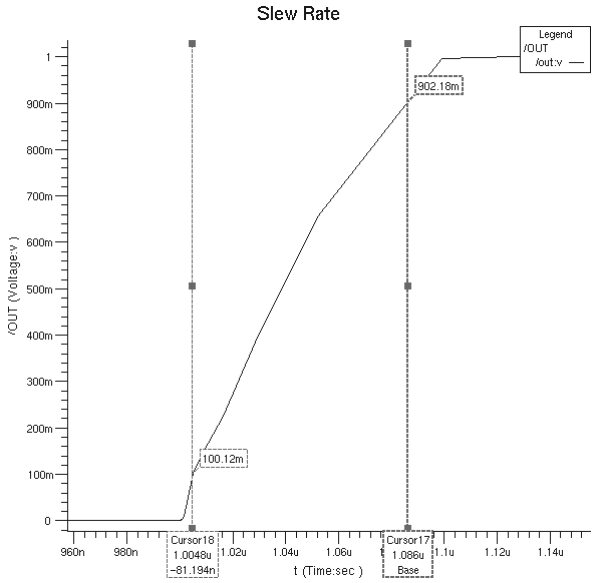


Figure 7. Op-amp step response marked between 10% and 90% of the final value to measure SR^+

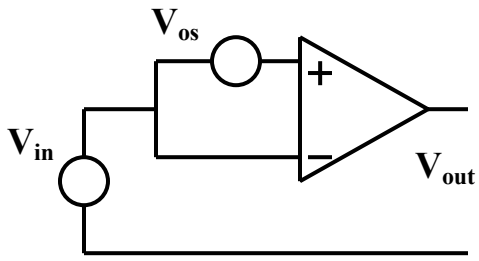


Figure 8. Configuration for simulating A_{CM}.

6.4. Power Supply Rejection Ratio

The biasing circuit used in this op-amp is very susceptible to supply variations because the supply noise directly falls on Vgs and changes the drain current significantly. There are several supply independent biasing techniques which can improve supply rejection. But here to keep the circuit simple and power consumption low, as can be seen in Figure 3, the biasing branch was separated

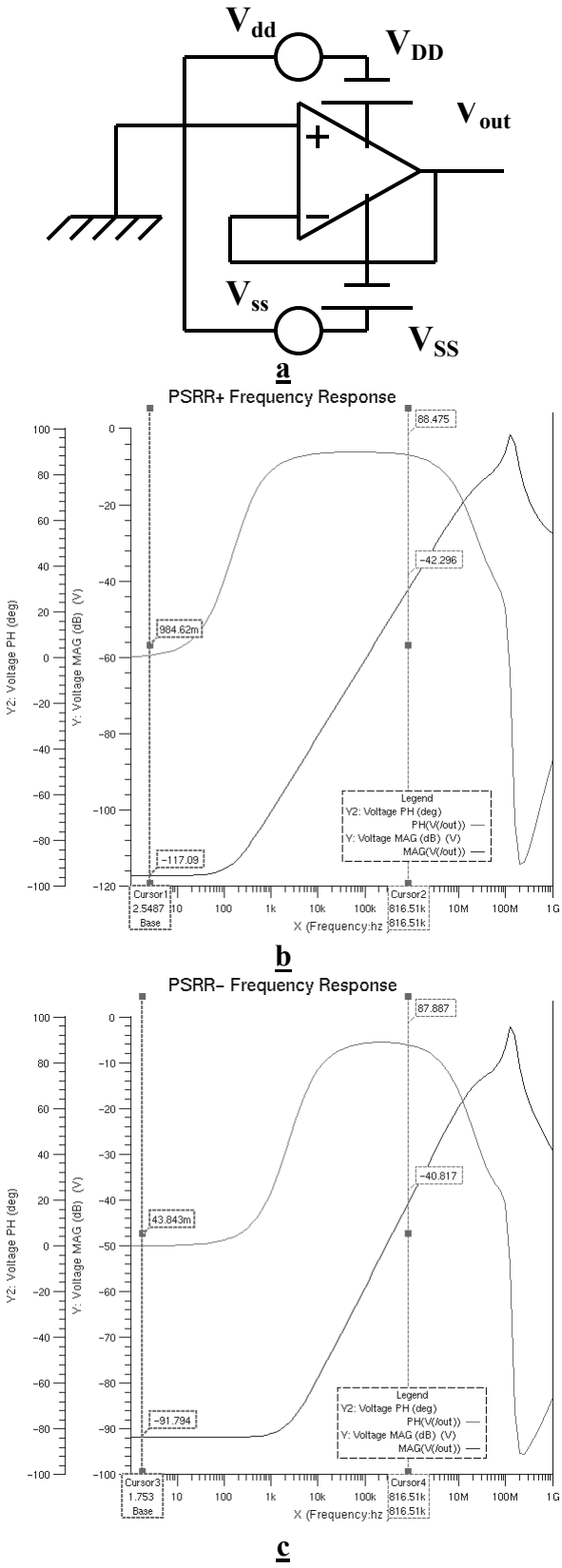


Figure 9 .Configuration for *PSRR* measurement (a) $PSRR^+$ (b) and $PSRR^-$(c) frequency response.

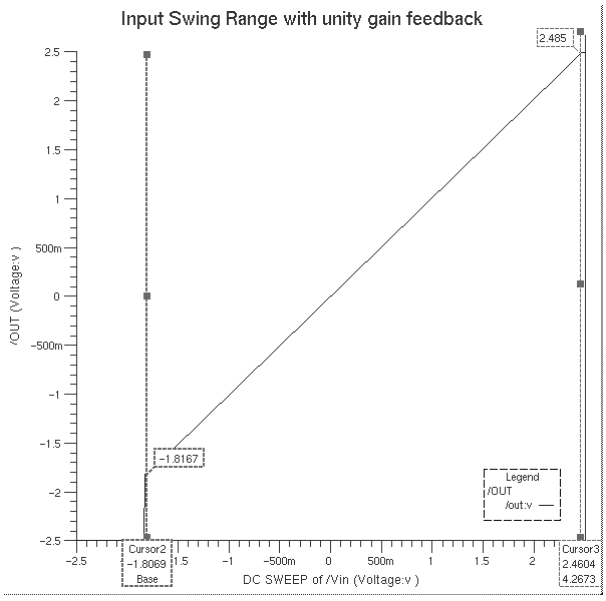
from the rest of the circuit with 1Ω resistors. These resistors help to apply the supply noise only to the first and second stages but not the biasing branch. The circuit used for $PSRR^+$ and $PSRR^-$ measurement is shown in Figure 9a and the simulation results are shown in Figure 9b and 9c respectively. As the input frequency increases, both $PSRR^+$ and $PSRR^-$ decrease because the differential gain decreases but stray capacitors become more conductive and transfer the supply noise to output.

6.5. Common Mode Input and Output Range

Common mode input range is mainly defined by transistors M5 (CMR^-) and M3 (CMR^+) as shown in Equations (5) and (6). To simulate and measure this parameter, the op-amp with unity gain is used. An input source sweeps all the voltages from V_{SS} to V_{DD} while output is monitored. Generally the output swing is larger than the input common range, so when there is unity gain, the output will be limited by the input first. To measure the output swing, A feedback value less than or equal to 2 should be used. In this case limitation will be imposed by the output and not the input. Simulation results are shown in Figure 10a and 10b for the input *CMR* and the output swing respectively. Both of these parameters are above the required design spec and the output almost can swing between the supply rails, due to the large output transistors used in this design.

7. Conclusion

A CMOS wide band operational amplifier is designed using the classical two stage differential input approach. Various parameters are estimated by hand calculations while trying to take as much as required



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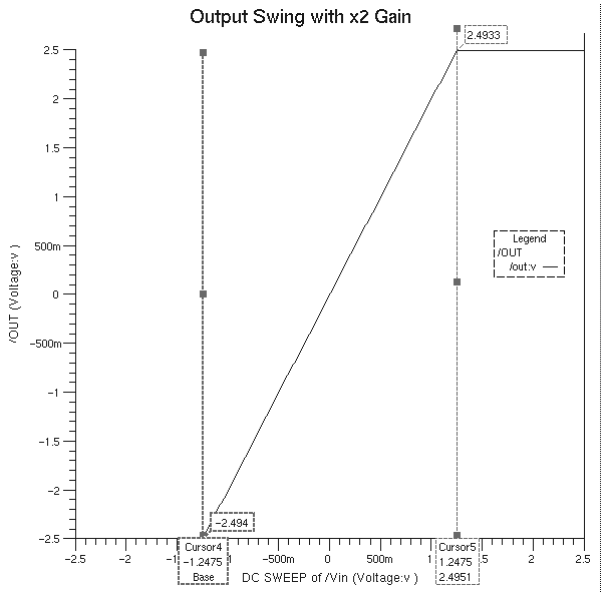

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Figure 10. The input CMR measured by unity gain(a) and the output swing measured by x2 gain.

parameter in to account. Then several simulations have been performed using Mentor Graphics tools to meet all the specs as well as including parasitics.

Through these simulations one can obviously see that how different circuit parameters and design specs affect each other weather directly or indirectly. Improving one aspect might be in expense of degrading the others and finally to achieve a good performance, various parameters should be compromised all together.

Today by invention of different design techniques for amplifier circuits each providing the best performance for a certain application, classical approach might not be as significant as before. For example to drive a fully capacitive load, designing an operational trans-conductance amplifier with only one dominant pole may be much easier, or a wide swing range folded cascode op-amp gives provides much higher gain with over rail to rail *CMR*. But still for a general purpose applications, this approach might be the best.

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