Chapter 1 Homework Solutions

1.1-1 Using Eq. (1) of Sec 1.1, give the base-10 value for the 5-bit binary number 11010 ($b_4\, b_3\, b_2\, b_1\, b_0$ ordering).

From Eq. (1) of Sec 1.1 we have

$$b_{N\text{-}1}\, 2^{-1} + b_{N\text{-}2}\, 2^{-2} + b_{N\text{-}3}\, 2^{-3} + \ldots + b_0\, 2^{-N} = \sum_{i=1}^{N} b_{N-i} 2^{-i}$$

$$1 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4} + 0 \times 2^{-5} = \frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{1}{16} + \frac{0}{32}$$

$$= \frac{16 + 8 + 0 + 2 + 0}{32} = \frac{26}{32} = \frac{13}{16}$$

1.1-2 Process the sinusoid in Fig. P1.2 through an analog sample and hold. The sample points are given at each integer value of t/T.

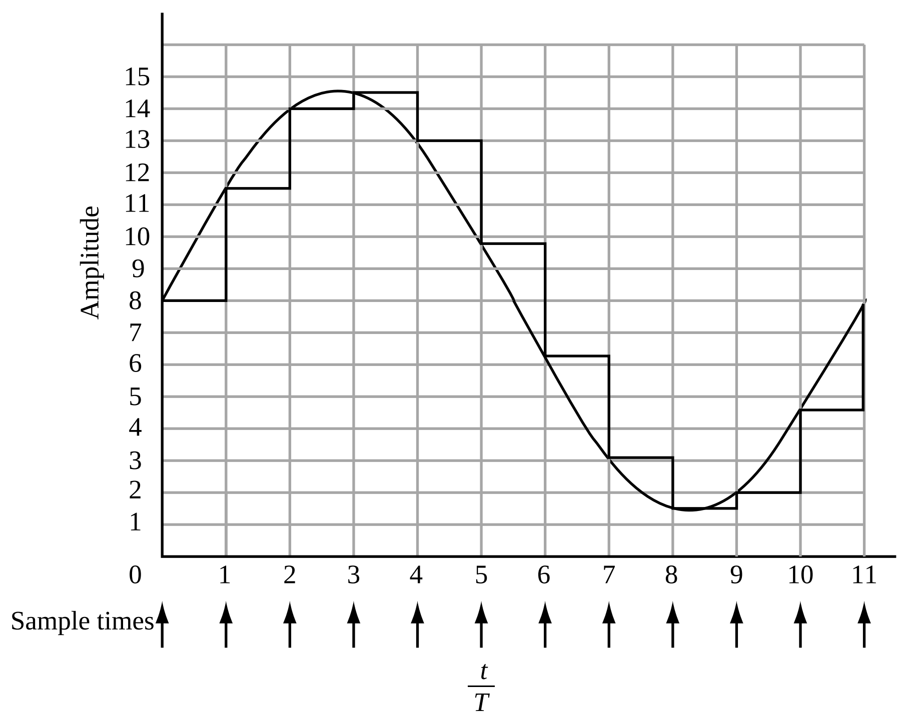


Figure P1.1-2

1.1-3 Digitize the sinusoid given in Fig. P1.2 according to Eq. (1) in Sec. 1.1 using a four-bit digitizer.

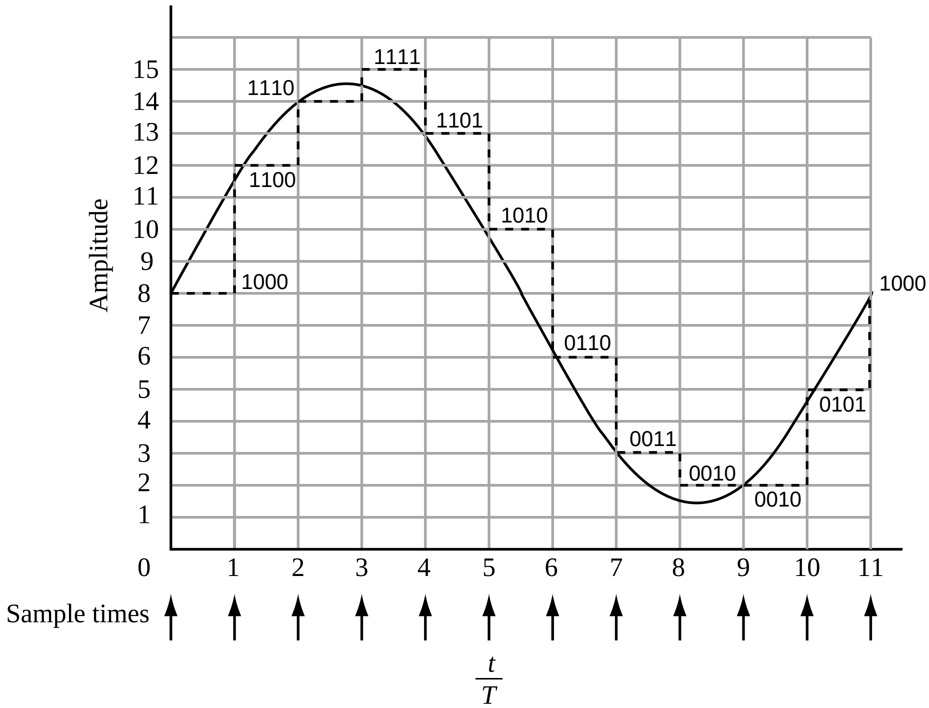


Figure P1.1-3

The figure illustrates the digitized result. At several places in the waveform, the digitized value must resolve a sampled value that lies equally between two digital values. The resulting digitized value could be either of the two values as illustrated in the list below.

Sample Time	4-bit Output
0	1000
1	1100
2	1110
3	1111 or 1110
4	1101
5	1010
6	0110
7	0011
8	0010 or 0001
9	0010
10	0101
11	1000

1.1-4 Use the nodal equation method to find v_{out}/v_{in} of Fig. P1.4.

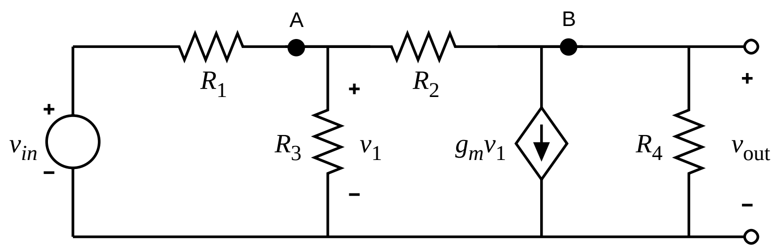


Figure P1.1-4

Node A:

$$0 = G_1(v_1 - v_{in}) + G_3(v_1) + G_2(v_1 - v_{out})$$

$$v_1(G_1 + G_2 + G_3) - G_2(v_{out}) = G_1(v_{in})$$

Node B:

$$0 = G_2(v_{out} - v_1) + g_{m1}(v_1) + G_4(v_{out})$$

$$v_1(g_{m1} - G_2) + v_{out}(G_2 + G_4) = 0$$

$$v_{out} = \frac{\begin{vmatrix} G_1+G_2+G_3 & G_1 v_{in} \\ g_{m1} - G_2 & 0 \end{vmatrix}}{\begin{vmatrix} G_1+G_2+G_3 & -G_2 \\ g_{m1} - G_2 & G_2 + G_4 \end{vmatrix}}$$

$$\frac{v_{out}}{v_{in}} = \frac{G_1(G_2 - g_{m1})}{G_1 G_2 + G_1 G_4 + G_2 G_4 + G_3 G_2 + G_3 G_4 + G_2 g_{m1}}$$

1.1-5 Use the mesh equation method to find v_{out}/v_{in} of Fig. P1.4.

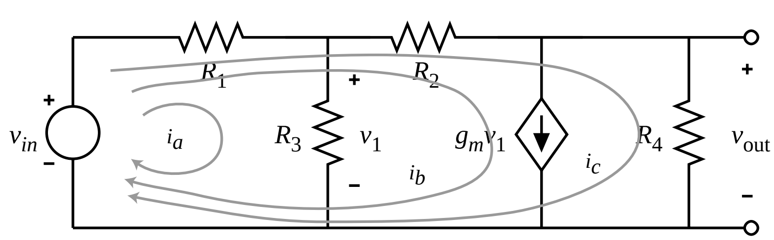


Figure P1.1-5

$$0 = -v_{in} + R_1(i_a + i_b + i_c) + R_3(i_a)$$

$0 = -v_{in} + R_1(i_a + i_b + i_c) + R_2(i_b + i_c) + v_{out}$

$i_c = \dfrac{v_{out}}{R_4}$

$i_b = g_m v_1 = g_m i_a R_3$

$$0 = -v_{in} + R_1\left(i_a + g_m i_a R_3 + \frac{v_{out}}{R_4}\right) + R_3 i_a$$

$$0 = -v_{in} + R_1\left(i_a + g_m i_a R_3 + \frac{v_{out}}{R_4}\right) + R_2\left(g_m i_a R_3 + \frac{v_{out}}{R_4}\right) + v_{out}$$

$$v_{in} = i_a (R_1 + R_3 + g_m R_1 R_2) + v_{out}\frac{R_1}{R_4}$$

$$v_{in} = i_a (R_1 + g_m R_1 R_3 + g_m R_2 R_3) + v_{out}\left(\frac{R_1 + R_2 + R_4}{R_4}\right)$$

$$v_{out} = \frac{\begin{vmatrix} R_1+R_3 + g_m R_1 R_3 & v_{in} \\ R_1 + g_m R_1 R_3 + g_m R_2 R_3 & v_{in} \end{vmatrix}}{\begin{vmatrix} R_1 + R_3 + g_m R_1 R_3 & R_1/R_4 \\ R_1 + g_m R_1 R_3 + g_m R_2 R_3 & (R_1 + R_2 + R_4)/R_4 \end{vmatrix}}$$

$$v_{out} = \frac{v_{in} R_3 R_4 (1 - g_m R_2)}{(R_1 + R_3 + g_m R_1 R_3)(R_1 + R_2 + R_4) - (R_1^2 + g_m R_1^2 R_3 + g_m R_1 R_2 R_3)}$$

$$v_{out} = \frac{v_{in} R_3 R_4 (1 - g_m R_2)}{R_1R_2 + R_1R_4 + R_1R_3 + R_2R_3 + R_3R_4 + g_m R_1 R_3 R_4}$$

$$\frac{v_{out}}{v_{in}} = \frac{R_3 R_4 (1 - g_m R_2)}{R_1R_2 + R_1R_4 + R_1R_3 + R_2R_3 + R_3R_4 + g_m R_1 R_3 R_4}$$

1.1-6 Use the source rearrangement and substitution concepts to simplify the circuit shown in Fig. P1.6 and solve for i_{out}/i_{in} by making chain-type calculations only.

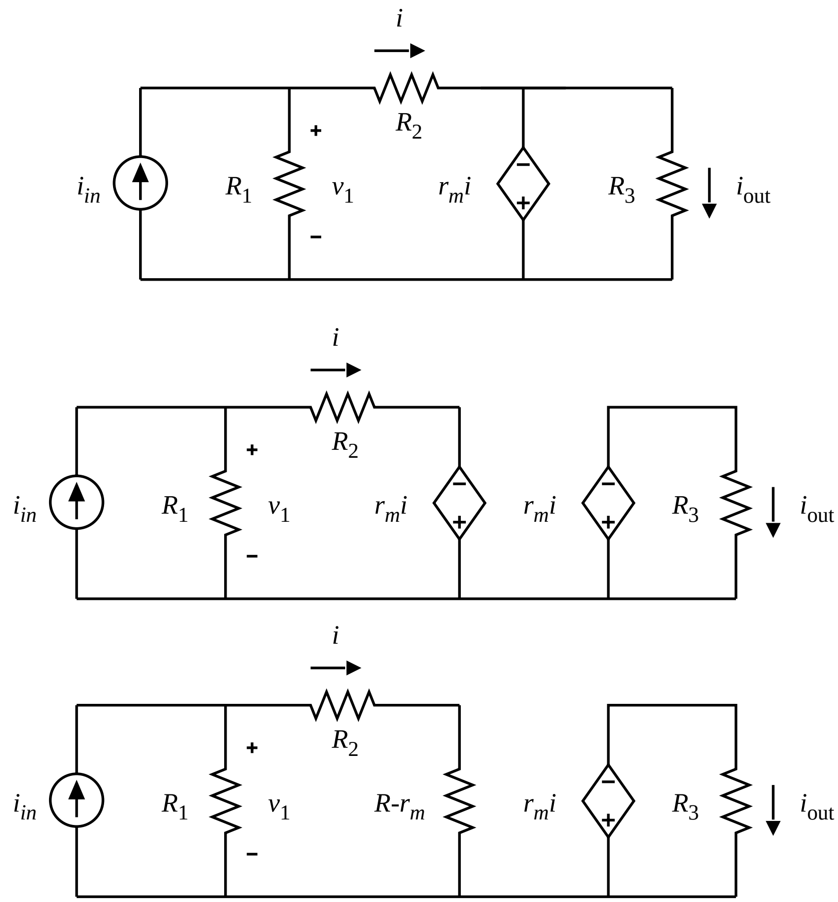


Figure P1.1-6

$$i_{\text{out}} = \frac{-r_m}{R_3}\, i$$

$$i = \frac{R_1}{R + R_1 - r_m}\, i_{\text{in}}$$

$$\frac{i_{\text{out}}}{i_{\text{in}}} = \frac{-r_m\, R_1/R_3}{R + R_1 - r_m}$$

1.1-7 Find v_2/v_1 and v_1/i_1 of Fig. P1.7.

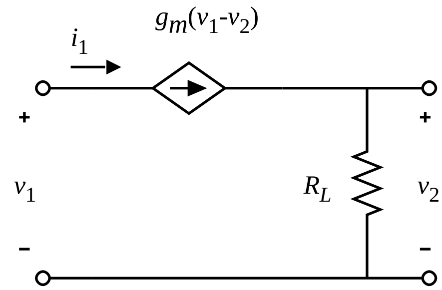


Figure P1.1-7

$$\frac{v_2}{v_1} = g_m\,(v_1 - v_2)\,R_L$$

$$v_2\,(1 + g_m\,R_L\,) = g_m\,R_L\,v_1$$

$$\frac{v_2}{v_1} = \frac{g_m\,R_L}{1 + g_m\,R_L}$$

$$v_2 = i_1\,R_L$$

substituting for v_2 yields:

$$\frac{i_1\,R_L}{v_1} = \frac{g_m\,R_L}{1 + g_m\,R_L}$$

$$\frac{v_1}{i_1} = \frac{R_L(\,1 + g_m\,R_L\,)}{g_m\,R_L}$$

$$\frac{v_1}{i_1} = R_L + \frac{1}{g_m}$$

1.1-8 Use the circuit-reduction technique to solve for v_{out}/v_{in} of Fig. P1.8.

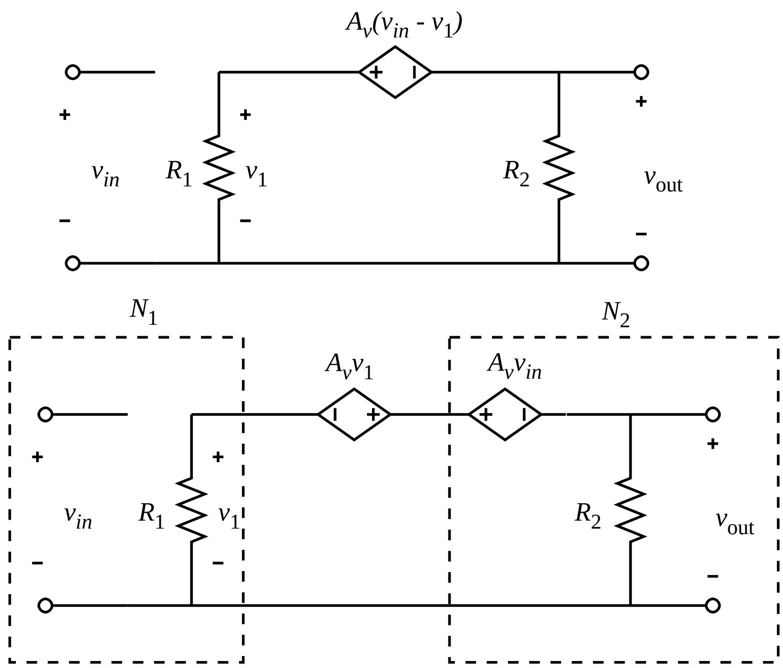


Figure P1.1-8a

Multiply R_1 by $(A_v + 1)$

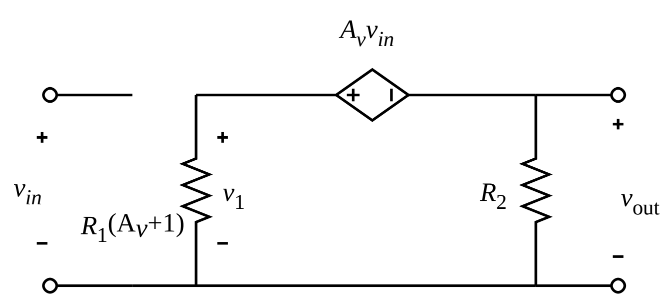


Figure P1.1-8b

$$v_{out} = \frac{-A_v v_{in} R_2}{R_2 + R_1(A_v+1)}$$

$$\frac{v_{out}}{v_{in}} = \frac{-A_v R_2}{R_2 + R_1(A_v+1)}$$

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{\dfrac{-A_v}{-A_v + 1} R_2}{\dfrac{R_2}{A_v + 1} + R_1}$$

As A_v approaches infinity,

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{-R_2}{R_1}$$

1.1-9 Use the Miller simplification concept to solve for v_{out}/v_{in} of Fig. A-3 (see Appendix A).

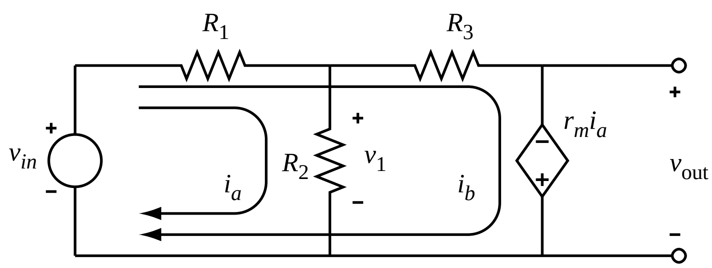


Figure P1.1-9a (Figure A-3 Mesh analysis.)

$$K = \frac{v_{\text{out}}}{v_1} = \frac{-r_m\, i_a}{i_a R_2} = \frac{-r_m}{R_2}$$

$$Z_1 = \frac{R_3}{1 + \dfrac{r_m}{R_2}}$$

$$Z_2 = \frac{R_3 \dfrac{-r_m}{R_2}}{-\dfrac{r_m}{R_2} - 1}$$

$$Z_2 = \frac{r_m \frac{R_3}{R_2}}{\frac{r_m}{R_2} + 1} = \frac{R_3}{\frac{R_2}{r_m} + 1}$$

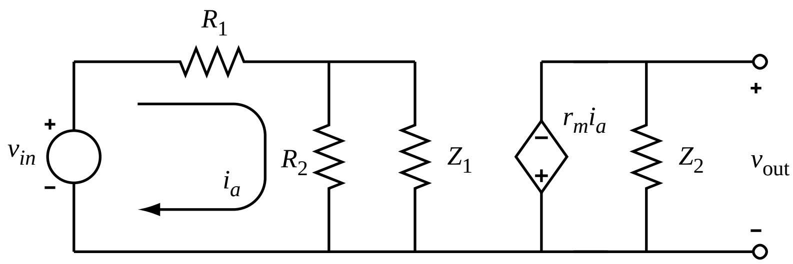


Figure P1.1-9b

$$i_a = \frac{v_{\text{in}}\,(R_2 \parallel Z_1)}{(R_2 \parallel Z_1) + R_1}\left(\frac{1}{R_2}\right)$$

$$v_{\text{out}} = -r_m\, i_a$$

$$v_{\text{out}} = \frac{-v_{\text{in}}\, r_m\,(R_2 \parallel Z_1)}{(R_2 \parallel Z_1) + R_1}\left(\frac{1}{R_2}\right)$$

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{-r_m\,(R_2 \parallel Z_1)}{(R_2 \parallel Z_1) + R_1}\left(\frac{1}{R_2}\right)$$

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{-r_m\, R_3}{(R_1R_2 + R_1R_3 + R_1r_m + R_2R_3)}$$

1.1-10 Find v_{out}/i_{in} of Fig. A-12 and compare with the results of Example A-1.

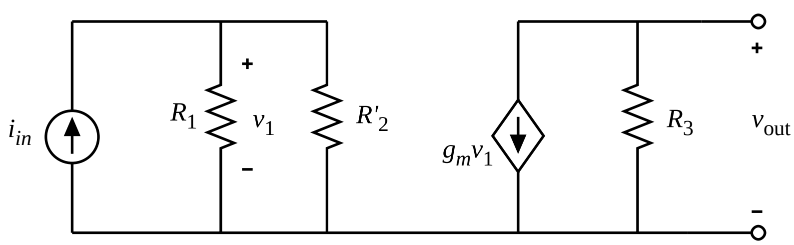


Figure P1.1-10

$$v_1 = i_{\text{in}}\,(R_1 \,\|\, R_2^{'})$$

$$v_{\text{out}} = -g_m v_1\, R_3 = -g_m\, R_3\, i_{\text{in}}\,(R_1 \,\|\, R_2^{'})$$

$$\frac{v_{\text{out}}}{i_{\text{in}}} = -g_m\, R_3 (R_1 \,\|\, R_2^{'})$$

$$R_2^{'} = \frac{R_2}{1 + g_m\, R_3}$$

$$R_1 \,\|\, R_2^{'} = \frac{\dfrac{R_1 R_2}{1 + g_m\, R_3}}{\dfrac{(1 + g_m\, R_3)\, R_1 + R_2}{1 + g_m\, R_3}}$$

$$R_1 \,\|\, R_2^{'} = \frac{R_1 R_2}{(1 + g_m\, R_3)\, R_1 + R_2}$$

$$\frac{v_{\text{out}}}{i_{\text{in}}} = \frac{-g_m\, R_1\, R_2 R_3}{R_1 + R_2 + R_3 + g_m\, R_1 R_3}$$

The A.1-1 result is:

$$\frac{v_{\text{out}}}{i_{\text{in}}} = \frac{R_1\, R_3 - g_m\, R_1\, R_2 R_3}{R_1 + R_2 + R_3 + g_m\, R_1 R_3}$$

if $g_m R_2 >> 1$ then the results are the same.

1.1-11 Use the Miller simplification technique described in Appendix A to solve for the output resistance, v_o/i_o, of Fig. P1.4. Calculate the output resistance not using the Miller simplification and compare your results.

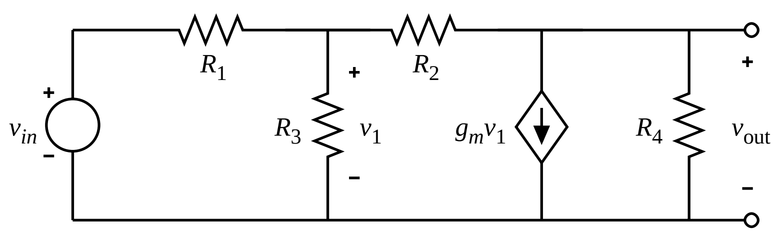


Figure P1.1-11a

Z_o with Miller

$K = -g_m R_4$

$$Z_2 = \frac{-R_2\, g_m\, R_4}{-g_m\, R_4 - 1} = \frac{R_2\, g_m\, R_4}{1 + g_m\, R_4}$$

$$Z_0 = R_4 \parallel Z_2 = \frac{\dfrac{g_m\, R_2\, R_4^2}{1 + g_m\, R_4}}{\dfrac{(1 + g_m\, R_4)\, R_4 + g_m\, R_2\, R_4^2}{1 + g_m\, R_4}}$$

$$Z_0 = R_4 \parallel Z_2 = \frac{g_m\, R_2\, R_4^2}{R_4 + g_m\, R_4\, (\, R_4 + R_2)}$$

Z_o without Miller

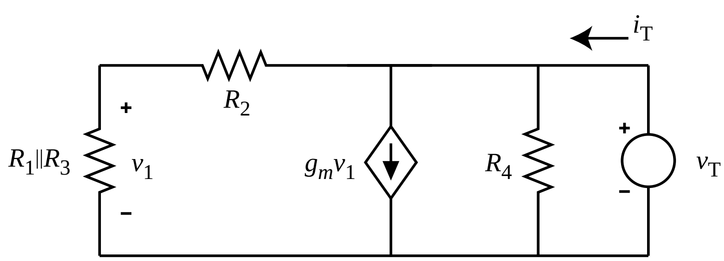


Figure P1.1-11b

$$v_1 = (R_1 \parallel R_3)\left(i + g_m v_1 - \frac{v_T}{R_4}\right)$$

$$v_1\, [1 + g_m\, (R_1 \parallel R_3)] = (\, R_1 \parallel R_3\,)\left(i_T + - \frac{v_T}{R_4}\right)$$

$$(1) \quad v_1 = \frac{(R_1 \parallel R_3)\, (i_T\, R_4 + - v_T)}{R_4\, [1 + g_m\, (R_1 \parallel R_3)]}$$

(2) $$v_1 = \frac{v_T (R_1 \parallel R_3)}{R_1 \parallel R_3 + R_2}$$

Equate (1) and (2)

$$\frac{v_T \ (R_1 \parallel R_3)}{R_1 \parallel R_3 + R_2} = \frac{(R_1 \parallel R_3)\ (i_T R_4 - v_T)}{R_4\ [1 + g_m\ (R_1 \parallel R_3)]}$$

$$\frac{v_T}{R_1 \parallel R_3 + R_2} = \frac{i_T R_4 - v_T}{R_4\ [1 + g_m\ (R_1 \parallel R_3)]}$$

$$v_T \left\{ R_4\ [1 + g_m\ (R_1 \parallel R_3)] + R_2 + R_1 \| R_3 \right\} = i_T R_4\ (R_2 + R_1 \| R_3)$$

$$Z_0 = \frac{R_4\ (R_2 + R_1 \| R_3\ )}{R_2 + R_4 + g_m R_4 (R_1 \| R_3) + R_1 \| R_3}$$

$$Z_0 = \frac{R_4 R_2 + \dfrac{R_1 R_3 R_4}{R_1 + R_3}}{R_2 + R_4 + \dfrac{g_m R_4 R_1 R_3 + R_1 R_3}{R_1 + R_3}}$$

$$Z_0 = \frac{R_4 R_2\ (R_1 + R_3) + R_1 R_3 R_4}{(R_2 + R_4)\ (R_1 + R_3) + R_1 R_3 + g_m R_1 R_3 R_4}$$

$$Z_0 = \frac{R_1 R_2 R_4 + R_2 R_3 R_4 + R_1 R_3 R_4}{R_1 R_2 + R_2 R_3 + R_3 R_4 + R_1 R_4 + R_1 R_3 + g_m R_1 R_3 R_4}$$

1.1-12 Consider an ideal voltage amplifier with a voltage gain of $A_v = 0.99$. A resistance R = 50 kΩ is connected from the output back to the input. Find the input resistance of this circuit by applying the Miller simplification concept.

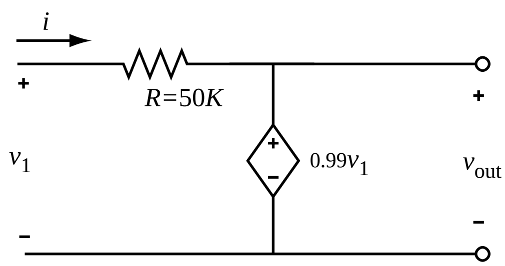


Figure P1.1-12

$$R_{\text{in}} = \frac{R}{1 - K}$$

$K = 0.99$

$$R_{\text{in}} = \frac{50\ K\Omega}{1 - 0.99} = \frac{50\ K\ \Omega}{0.01} = 5\ \text{Meg}\ \Omega$$

Chapter 2 Homework Solutions

Problem 2.1-1
List the five basic MOS fabrication processing steps and give the purpose or function of each step.

Oxidation: Combining oxygen and silicon to form silicondioxide (SiO_2). Resulting SiO_2 formed by oxidation is used as an isolation barrier (e.g., between gate polysilicon and the underlying channel) and as a dielectric (e.g., between two plates of a capacitor).

Diffusion: Movement of impurity atoms from one location to another (e.g., from the silicon surface to the bulk to form a diffused well region).

Ion Implantation: Firing ions into an undoped region for the purpose of doping it to a desired concentration level. Specific doping profiles are achievable with ion implantation which cannot be achieved by diffusion alone.

Deposition: Depositing various films on to the wafer. Used to deposit dielectrics which cannot be grown because of the type of underlying material. Deposition methods are used to lay down polysilicon, metal, and the dielectric between them.

Etching: Removal of material sensitive to the etch process. For example, etching is used to eliminate unwanted polysilicon after it has been laid out by deposition.

Problem 2.1-2
What is the difference between positive and negative photoresist and how is photoresist used?

Positive: Exposed resist changes chemically so that it can dissolve upon exposure to light. Unexposed regions remain intact.

Negative: Unexposed resist changes chemically so that it can dissolve upon exposure to light. Exposed regions remain intact.

Photoresist is used as a masking layer which is paterned appropriately so that certain underlying regions are exposed to the etching process while those regions covered by photoresist are resistant to etching.

Problem 2.1-3
Illustrate the impact on source and drain diffusions of a 7° angle off perpendicular ion implant. Assume that the thickness of polysilicon is 8000 Å and that out diffusion from point of ion impact is 0.07 μm.

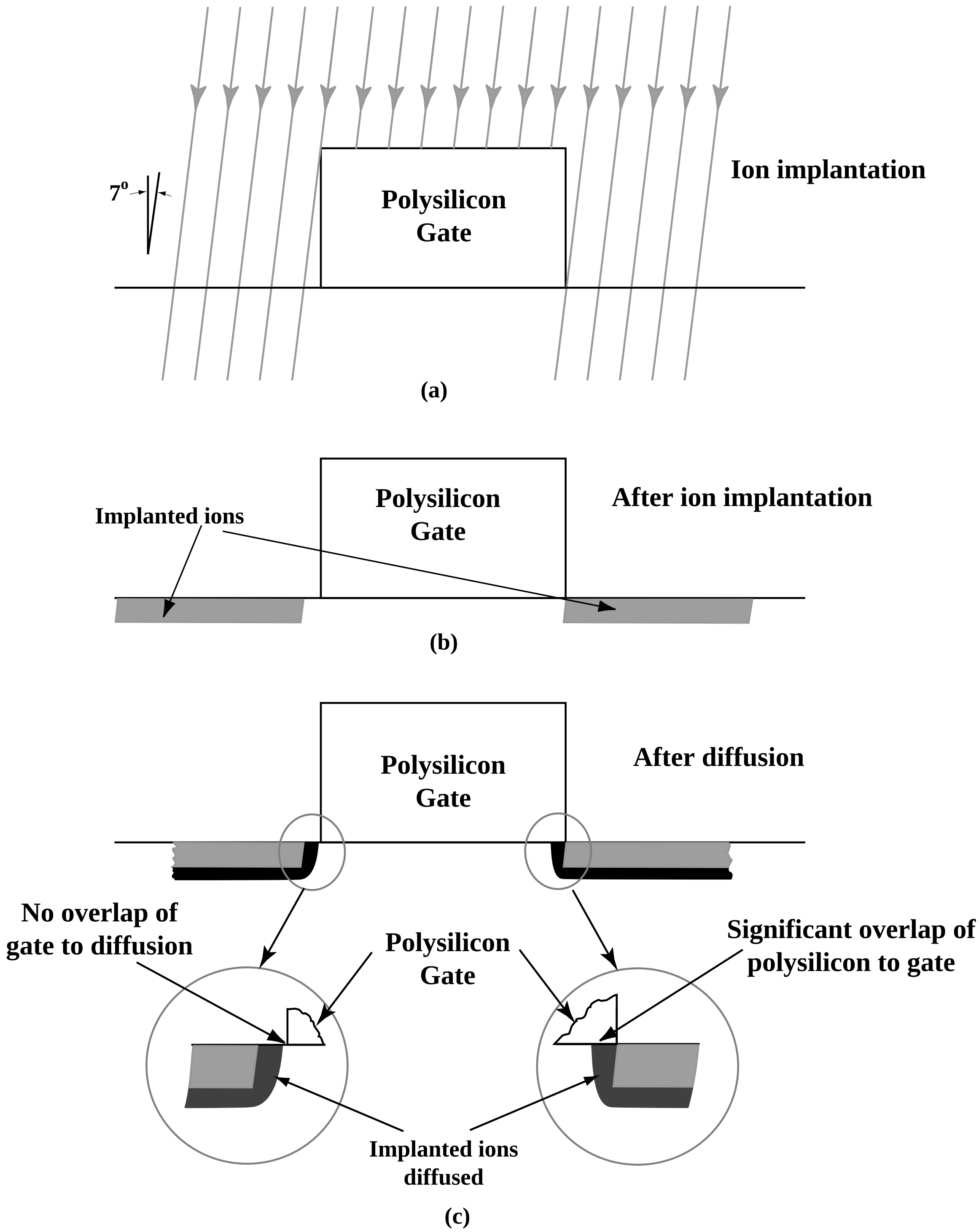


Figure P2.1-3

Problem 2.1-4

What is the function of silicon nitride in the CMOS fabrication process described in Section 2.1

The primary purpose of silicon nitride is to provide a barrier to oxygen so that when deposited and patterned on top of silicon, silicon dioxide does not form below where the silicon nitride exists.

Problem 2.1-5

Give typical thickness for the field oxide (FOX), thin oxide (TOX), n^+ or p^+, p-well, and metal 1 in units of μm.

FOX: ~ 1 μm

TOX: ~ 0.014 μm for an 0.8 μm process

N+/p+: ~ 0.2 μm

Well: ~ 1.2 μm

Metal 1: ~ 0.5 μm

Problem 2.2-1

Repeat Example 2.2-1 if the applied voltage is -2 V.

$N_A = 5 \times 10^{15}/\text{cm}^3,\ N_D = 10^{20}/\text{cm}^3$

$$\phi_o = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = \frac{1.381\times10^{-23}\times300}{1.6\times10^{-19}}\ln\left(\frac{5\times10^{15}\times10^{20}}{(1.45\times10^{10})^2}\right) = 0.9168$$

$$x_n = \left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_A}{qN_D(N_A+N_D)}\right]^{1/2} = \left[\frac{2\times11.7\times8.854\times10^{-14}\ (0.9168+2.0)\ 5\times10^{15}}{1.6\times10^{-19}\times10^{20}\ (\ 5\times10^{15}+10^{20})}\right]^{1/2} = 43.5\times10^{-12}\ \text{m}$$

$$x_p = -\left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_D}{qN_A(N_A+N_D)}\right]^{1/2} = \left[\frac{2\times11.7\times8.854\times10^{-14}\ (0.9168+2.0)\ 10^{20}}{1.6\times10^{-19}\times5\times10^{15}\ (\ 5\times10^{15}+10^{20})}\right]^{1/2} = -0.869\ \mu\text{m}$$

$$x_d = x_n - x_p = 0\ + 0.869\ \mu\text{m} = 0.869\ \mu\text{m}$$

$$C_{j0} = \frac{dQ_j}{dv_D} = A\left[\frac{\varepsilon_{si} q N_A N_D}{2(N_A+N_D)\ (\phi_o)}\right]^{1/2}$$

$$C_{j0} = 1\times10^{-3}\times1\times10^{-3}\left[\frac{11.7\times8.854\times10^{-14}\times1.6\times10^{-19}\times5\times10^{15}\times1\times10^{20}}{2(5\times10^{15}+1\times10^{20})\ (0.917)}\right]^{1/2} = 21.3\ \text{fF}$$

$$C_{j0} = \frac{C_{j0}}{\left(1-\dfrac{\phi_0}{v_D}\right)^{1/2}} = \frac{21.3 \text{ fF}}{\left(1-\dfrac{-2}{0.917}\right)^{1/2}} = 11.94 \text{ fF}$$

Problem 2.2-2
Develop Eq. (2.2-9) using Eqs. (2.2-1), (2.2-7), and (2.2-8).

Eq. 2.2-1

$$x_d = x_n - x_p$$

Eq. 2.2-7

$$x_n = \left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_A}{qN_D(N_A+N_D)}\right]^{1/2}$$

Eq. 2.2-8

$$x_p = -\left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_D}{qN_A(N_A+N_D)}\right]^{1/2}$$

$$x_d = \left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_A^2 + 2\varepsilon_{si}(\phi_o - v_D)N_D^2}{qN_A\,N_D\,(N_A+N_D)}\right]^{1/2}$$

$$x_d = (\phi_o - v_D)^{1/2}\left[\frac{2\varepsilon_{si}\left(N_A^2 + N_D^2\right)}{qN_A\,N_D\,(N_A+N_D)}\right]^{1/2}$$

Assuming that $2N_A\,N_D << (N_A + N_D)^2$

Then

$$x_d = (\phi_o - v_D)^{1/2}\left[\frac{2\varepsilon_{si}(N_A + N_D)^2}{qN_A\,N_D\,(N_A+N_D)}\right]^{1/2}$$

$$x_d = (\phi_o - v_D)^{1/2}\left[\frac{2\varepsilon_{si}(N_A + N_D)}{qN_A\,N_D}\right]^{1/2}$$

Problem 2.2-3
Redevelop Eqs. (2.2-7) and (2.2-8) if the impurity concentration of a pn junction is given by Fig. 2.2-2 rather than the step junction of Fig. 2.2-1(b).

Referring to Figure P2.2-3

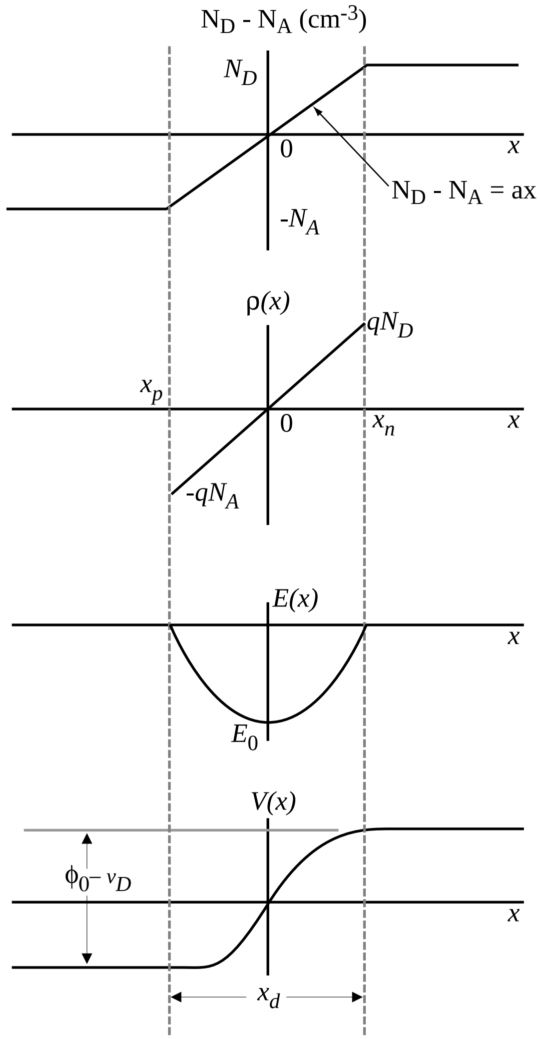


Figure P2.2-3

Using Poisson's equation in one dimension

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\varepsilon}$$

$$\rho(x) = qax\ , \quad when \quad x_p < x < x_n$$

$$\frac{d^2V}{dx^2} = -\frac{qax}{\varepsilon}$$

$$E(x) = -\frac{dV}{dx} = \frac{qa}{2\varepsilon}x^2 + C_1$$

$$E(x_p) = E(x_n) = 0$$

then

$$0 = \frac{qa}{2\varepsilon}x_p^2 + C_1$$

$$C_1 = -\frac{qa}{2\varepsilon}x_p^2$$

$$E(x) = \frac{qa}{2\varepsilon}x^2 - \frac{qa}{2\varepsilon}x_p^2 = \frac{qa}{2\varepsilon}\left(x^2 - x_p^2\right)$$

The voltage across the junction is given as

$$V = -\int_{x_p}^{x_n} E(x)dx = -\frac{qa}{2\varepsilon}\int_{x_p}^{x_n}\left(x^2 - x_p^2\right)dx$$

$$V = -\frac{qa}{2\varepsilon}\left(\frac{x^3}{3} - x_p^2 x\right)\Bigg|_{x_p}^{x_n}$$

$$V = -\frac{qa}{2\varepsilon}\left[\left(\frac{x_n^3}{3} - x_p^2 x_n\right) - \left(\frac{x_p^3}{3} - x_p^2 x_p\right)\right]$$

$$V = -\frac{qa}{2\varepsilon}\left[\left(\frac{x_n^3}{3} - x_p^2 x_n\right) - x_p^3\left(\frac{1}{3} - 1\right)\right] = -\frac{qa}{2\varepsilon}\left[\frac{x_n^3}{3} - x_p^2 x_n + \frac{2}{3}x_p^3\right]$$

Since $-x_p = x_n$

$$V = -\frac{qa}{2\varepsilon}\left[-\frac{x_p^3}{3} + x_p^3 + \frac{2}{3}x_p^3\right] = -\frac{qa}{2\varepsilon}x_p^3\left[-\frac{1}{3} + 1 + \frac{2}{3}\right] = -\frac{qa}{2\varepsilon}x_p^3\left(\frac{4}{3}\right)$$

$$V = -\frac{2qa}{3\varepsilon}x_p^3$$

V represents the barrier potential across the junction, $\phi_0 - V_D$. Therefore

$$\phi_0 - V_D = \frac{2qa}{3\varepsilon} x_p^3$$

$$x_p = -x_n = \left(\frac{3\varepsilon}{2qa}\right)^{1/3} (\phi_0 - V_D)^{1/3}$$

Problem 2.2-4

Plot the normalized reverse current, i_{RA}/i_R, versus the reverse voltage v_R of a silicon pn diode which has $BV = 12$ V and $n = 6$.

$$\frac{i_{RA}}{i_R} = \left[\frac{1}{1-(v_R/BV)^n}\right]$$

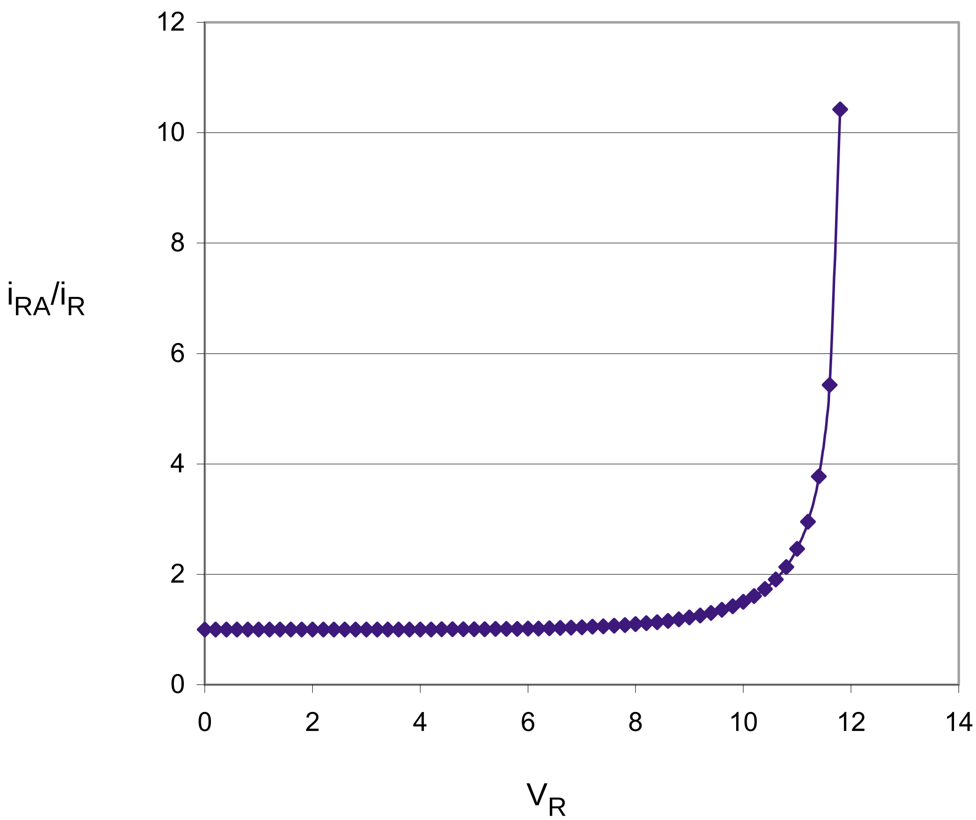


Figure P2.2-4

Problem 2.2-5

What is the breakdown voltage of a pn junction with $N_A = N_D = 10^{16}/\text{cm}^3$?

$$BV \cong \frac{\varepsilon_{si}(N_A + N_D)}{2qN_AN_D} E_{\max}^2$$

$$BV \cong \frac{11.7\times 8.854\times 10^{-14}\,(10^{16} + 10^{16})}{2\times 1.6\times 10^{-19}\times 10^{16}\times 10^{16}}\,(3\times 10^5)^2 = 58.27 \text{ volts}$$

Problem 2.2-6

What change in v_D of a silicon pn diode will cause an increase of 10 (an order of magnitude) in the forward diode current?

$$i_D = I_s\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \cong I_s \exp\left(\frac{v_D}{V_t}\right)$$

$$\frac{10\, i_D}{i_D} = \frac{I_s \exp\left(\frac{v_{D1}}{V_t}\right)}{I_s \exp\left(\frac{v_{D2}}{V_t}\right)} = \frac{\exp\left(\frac{v_{D1}}{V_t}\right)}{\exp\left(\frac{v_{D2}}{V_t}\right)} = \exp\left(\frac{v_{D1} - v_{D2}}{V_t}\right)$$

$$10 = \exp\left(\frac{v_{D1} - v_{D2}}{V_t}\right)$$

$$V_t \ln(10) = v_{D1} - v_{D2}$$

$$25.9 \text{ mV} \times 2.303 = 59.6 \text{ mV} = v_{D1} - v_{D2}$$

$$v_{D1} - v_{D2} = 59.6 \text{ mV}$$

Problem 2.3-1

Explain in your own words why the magnitude of the threshold voltage in Eq. (2.3-19) increases as the magnitude of the source-bulk voltage increases (The source-bulk pn diode remains reversed biased.)

Considering an n-channel device, as the gate voltage increases relative to the bulk, the region under the gate will begin to invert. What happens near the source? If the source is at the same potential as the bulk, then the region adjacent to the edge of the source inverts as the rest of the bulk region under the gate inverts. However, if the source is at a higher potential than the bulk, then a greater gate voltage is required to overcome the electric field induced by the source. While a portion of the region under the gate still inverts, there is no path of current flow to the source because the gate voltage is not large enough to invert right at the source edge. Once the gate is greater than the source and increasing, then the region adjacent to the source can begin to invert and thus provide a current path into the channel.

Problem 2.3-2

If V_{SB} = 2 V, find the value of V_T for the n-channel transistor of Ex. 2.3-1.

$2\phi_F = -0.940$
$\gamma = 0.577$
$V_{T0} = 0.306$

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

$$V_T = 0.306 + 0.577\left(\sqrt{|0.940 + 2|} - \sqrt{|0.940|}\right) = 0.736 \text{ volts}$$

$V_T = 0.736$ volts

Problem 2.3-3

Re-derive Eq. (2.3-27) given that V_T is not constant in Eq. (2.3-22) but rather varies linearly with $v(y)$ according to the following equation.

$V_T = V_{T0} + a\ v(y)$ << correction to book

$$\int_0^L i_D\, dy = \int_0^{v_{DS}} W\mu_n Q_I(y)\ dv(y) = \int_0^{v_{DS}} W\mu_n C_{ox}[v_{GS} - v(y) - V_{T(y)}]\ dv(y)$$

$$V_{T(y)} = V_{T0} + a\, v(y)$$

$$i_D\, \mathrm{L} = \int_0^{v_{DS}} W\mu_n C_{ox}[v_{GS} - v(y) - V_{T0} - a\, v(y)]\ dv(y)$$

$$i_D\, \mathrm{L} = W\mu_n C_{ox} \int_0^{v_{DS}} [v_{GS} - V_{T0} - v(y)\,(1 + a)]\ dv(y)$$

$$i_D\, \mathrm{L} = W\mu_n C_{ox} \left[(v_{GS} - V_{T0})v(y) - (1 + a)\frac{v(y)^2}{2} \right]_0^{v_{DS}}$$

$$i_D = \frac{W\mu_n C_{ox}}{L}\left[(v_{GS} - V_{T0})\, v_{DS} - (1+a)\frac{v_{DS}^{\;2}}{2} \right]$$

Problem 2.3-4

If the mobility of an electron is 500 cm^2/(V·s) and the mobility of a hole is 200 cm^2/(V·s), compare the performance of an n-channel with a p-channel transistor. In particular, consider the value of the transconductance parameter and speed of the MOS transistor.

Since $K' = \mu C_{OX}$, the transconductance of an n-channel transistor will be 2.5 time greater than the transconductance of a p-channel transistor. Remember that mobility will degrade as a function of terminal conditions so transconductance will degrade as well. The speed of a circuit is determined in a large part by the capacitance at the terminals and the transconductance. When terminal capacitances are equal for an n-channel and p-channel transistor of the same dimensions, the higher transconductance of the n-channel results in a faster circuit.

Problem 2.3-5

Using Ex. 2.3-1 as a starting point, calculate the difference in threshold voltage between two devices whose gate-oxide is different by 5% (i.e., t_{ox} = 210 Å).

$$\phi_F(\text{substrate}) = -0.0259 \ln\left[\frac{3\times 10^{16}}{1.45 \times 10^{10}}\right] = -0.377 \text{ V}$$

$$\phi_F(\text{gate}) = 0.0259 \ln\left[\frac{4\times 10^{19}}{1.45 \times 10^{10}}\right] = 0.563 \text{ V}$$

$$\phi_{MS} = \phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.940 \text{ V.}$$

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.9\times 8.854\times 10^{-14}}{210\times 10^{-8}} = 1.644\times 10^{-7}\text{ F/cm}^2$$

$$Q_{b0} = -\left(2\times 1.6\times 10^{-19}\times 11.7\times 8.854\times 10^{-14}\times 2\times 0.377\times 3\times 10^{16}\right)^{1/2}$$

$$= -\,8.66\times 10^{-8}\text{ C/cm}^2.$$

$$\frac{Q_{b0}}{C_{ox}} = \frac{-8.66 \times 10^{-8}}{1.644 \times 10^{-7}} = -0.5268 \text{ V}$$

$$\frac{Q_{SS}}{C_{ox}} = \frac{10^{10} \times 1.60 \times 10^{-19}}{1.644 \times 10^{-7}} = 9.73 \times 10^{-3} \text{ V}$$

$$V_{T0} = -\ 0.940\ +\ 0.754\ +\ 0.5268\ -\ 9.73 \times 10^{-3} =\ 0.331 \text{ V}$$

$$\gamma = \frac{\left[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 3 \times 10^{16}\right]^{1/2}}{1.644 \times 10^{-7}} = 0.607 \quad \text{V}^{1/2}$$

Problem 2.3-6

Repeat Ex. 2.3-1 using $N_A = 7 \times 10^{16}$ cm^{-3}, gate doping, $N_D = 1 \times 10^{19}$ cm^{-3}.

$$\phi_F(\text{substrate}) = -0.0259 \ln\left[\frac{7\times 10^{16}}{1.45\ \times 10^{10}}\right] = -0.3986 \text{ V}$$

$$\phi_F(\text{gate}) = 0.0259 \ln\left[\frac{1 \times 10^{19}}{1.45 \times 10^{10}}\right] = 0.527 \text{ V}$$

$$\phi_{MS}\ = \phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.9256 \text{ V.}$$

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.9 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} = 1.727 \times 10^{-7} \text{ F/cm}^2$$

$$Q_{b0} = -\left(2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 2 \times 0.3986 \times 7 \times 10^{16}\right)^{1/2}$$

$$= -\ 13.6 \times 10^{-8} \text{ C/cm}^2.$$

$$\frac{Q_{b0}}{C_{ox}} = \frac{-13.6 \times 10^{-8}}{1.727 \times 10^{-7}} = -0.7875 \text{ V}$$

$$\frac{Q_{SS}}{C_{ox}} = \frac{10^{10} \times 1.60 \times 10^{-19}}{1.727 \times 10^{-7}} = 9.3 \times 10^{-3} \text{ V}$$

$$V_{T0} = -0.9256 + 0.797 + 0.7875 - 9.3 \times 10^{-3} = 0.6496 \text{ V}$$

$$\gamma = \frac{\left[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 7 \times 10^{16}\right]^{1/2}}{1.727 \times 10^{-7}} = 0.882 \quad \text{V}^{1/2}$$

Problem 2.4-1
Given the component tolerances in Table 2.4-1, design the simple lowpass filter illustrated in Fig P2.4-1 to minimize the variation in pole frequency over all process variations. Pole frequency should be designed to a nominal value of 1MHz. You must choose the appropriate capacitor and resistor type. Explain your reasoning. Calculate the variation of pole frequency over process using the design you have chosen.

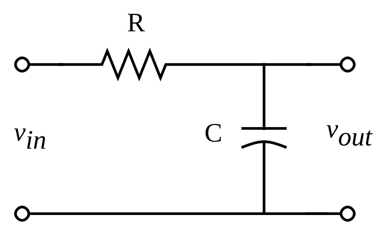


Figure P2.4.1

- To minimize distortion, we would choose minimum voltage coefficient for resistor and capacitor.

- To minimize variation, we choose components with the lowest tolerance.

The obvious choice for the resistor is Polysilicon. The obvious choice for the capacitor is the MOS capacitor. Thus we have the following:

We want $\omega_{-3dB}=2\pi\times10^6 = 1/RC$

C = 2.2 fF/μm^2 to 2.7 fF/μm^2 ; R = 20 Ω/❑ to 40 Ω/❑

Nominal values are
C = 2.45 fF/μm^2 ; R = 30 Ω/❑

In order to minimize total area used, you can do the following:

Set resistor width to 5µm (choosing a different width is OK).
Define:

N = the number of squares for the resistor

A_C = area for the capacitor.

Then:

$R = N \times 30$

$C = A_C \times C'$ (use C' to avoid confusion)

We want:

$$RC = \frac{1}{2\pi\times 10^6}$$

Total area = $A_{tot} = N\times 25 + A_C$

$$A_{tot} = 25\times N + \frac{1.59\times 10^6}{N}$$

To minimize area, set

$$\frac{\partial A_{tot}}{\partial N} = 25 - \frac{1.59\times 10^6}{N^2} = 0$$

$N = 252 \Rightarrow A_C = 6308\ \mu m^2$

Nominal values for R and C:

$R = 7.56\ k\Omega$; $C = 15.45\ pF$

Minimum values for R and C:

$R = 5.04\ k\Omega$; $C = 13.88\ pF$

Maximum values for R and C:

$R = 10.08\ k\Omega$; $C = 17.03\ pF$

Max pole frequency = $\frac{1}{(2\pi)(5.04k)\ (13.88pF)} \Rightarrow 2.275\ MHz$

Min pole frequency = $\frac{1}{(2\pi)(10.08k)\ (17.03pF)} \Rightarrow 927\ kHz$

Problem 2.4-2

List two sources of error that can make the actual capacitor, fabricated using a CMOS process, differ from its designed value.

Sources of error are:

- Variations in oxide thickness between the capacitor plates
- Dimensional variations of the plates due to the tolerance in
  - Etch
  - Mask
- Registration error (between layers)

Problem 2.4-3
What is the purpose of the n^+ implantation in the capacitor of Fig. 2.4-1(a)?

The implant is required to form a diffusion with a doping similar to that of the drain and source. As the voltage across the capacitor varies, depleting the bottom plate of carriers causes the capacitor to have a voltage coefficient which can have a bad effect on analog performance. With a highly-doped diffusion below the top plate, voltage coefficient is minimized.

Problem 2.4-4
Consider the circuit in Fig. P2.4-4. Resistor R_1 is an n-well resistor with a nominal value of 10 kΩ when the voltage at both terminals is 3 V. The input voltage, v_{in}, is a sine wave with an amplitude of 2 VPP and a dc component of 3 V. Under these conditions, the value of R_1 is given as

$$R_1 = R_{nom}\left[1 + K\left(\frac{v_{in} + v_{out}}{2}\right)\right]$$

where R_{nom} is 10K and the coefficient K is the voltage coefficient of an n-well resistor and has a value of 10K ppm/V. Resistor R_2 is an ideal resistor with a value of 10 kΩ. Derive a time-domain expression for v_{out}. Assume that there are no frequency dependencies.

TBD

Problem 2.4-5
Repeat problem 21 using a P+ diffused resistor for R_1. Assume that a P+ resistor's voltage coefficient is 200 ppm/V. The n-well in which R1 lies, is tied to a 5 volt supply.

TBD

Problem 2.4-6
Consider problem 2.4-5 again but assume that the n-well in which R1 lies is not connected to a 5 volt supply, but rather is connected as shown in Fig. P2.4-6.

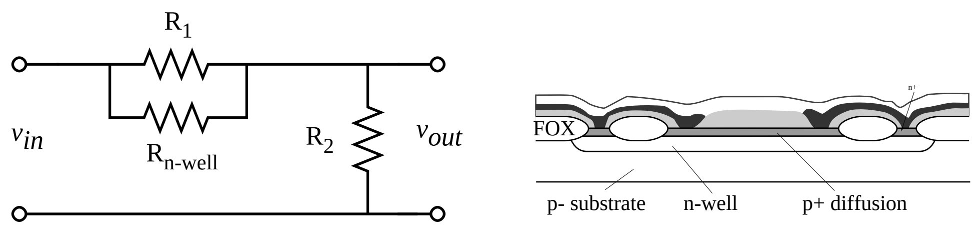
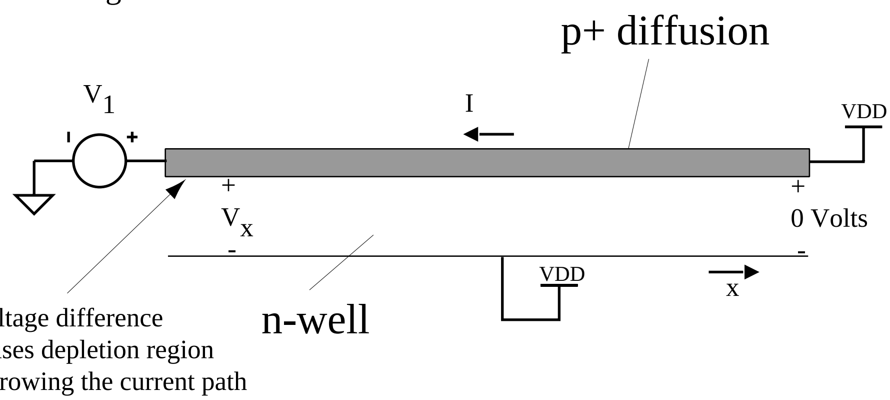
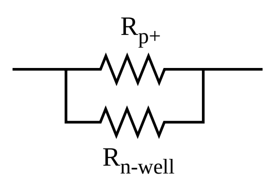


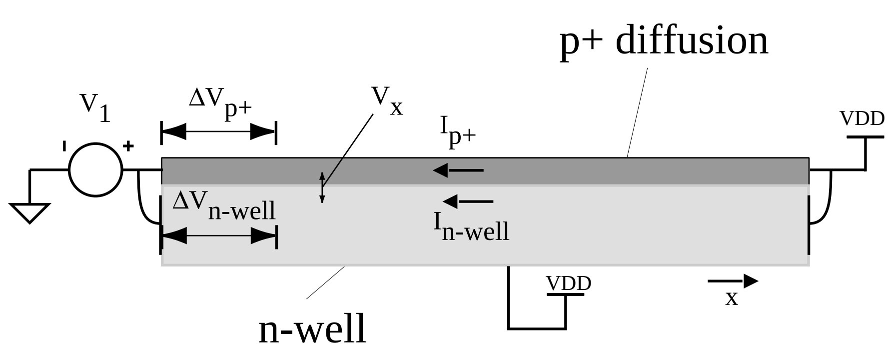
Figure P2.4-6

Voltage effects a resistor's value when the voltage between any point along the current path in the resistor and the material in which it lies. The voltage difference causes a depletion region to form in the resistor, thus increasing its resistance. This idea is illustrated in the diagram below.



In order to keep the depletion region from varying along the direction of the current path, the potential of the material below the p+ diffusion (n-well in this case) must vary in the same way as the potential of the p+ diffusion. This is accomplished by causing current to flow in the underlying material (n-well) in parallel with the current in the p+ diffusion as illustrated below.





It is easy to see that if $\Delta V_{p+} = \Delta V_{n\text{-}well}$ then $V_X = 0$. Thus by attaching the n-well in parallel with the desired current path, the effects of voltage coefficient of the p+ material are eliminated. There is a second-order effect due to the fact that the n-well resistor will have a voltage coefficient due to the underlying material (p- substrate) tied to ground. Even with this non-ideal effect, significant improvement is achieved by this method.

Problem 2.5-1

Assume $v_D = 0.7$ V and find the fractional temperature coefficient of I_s and v_D.

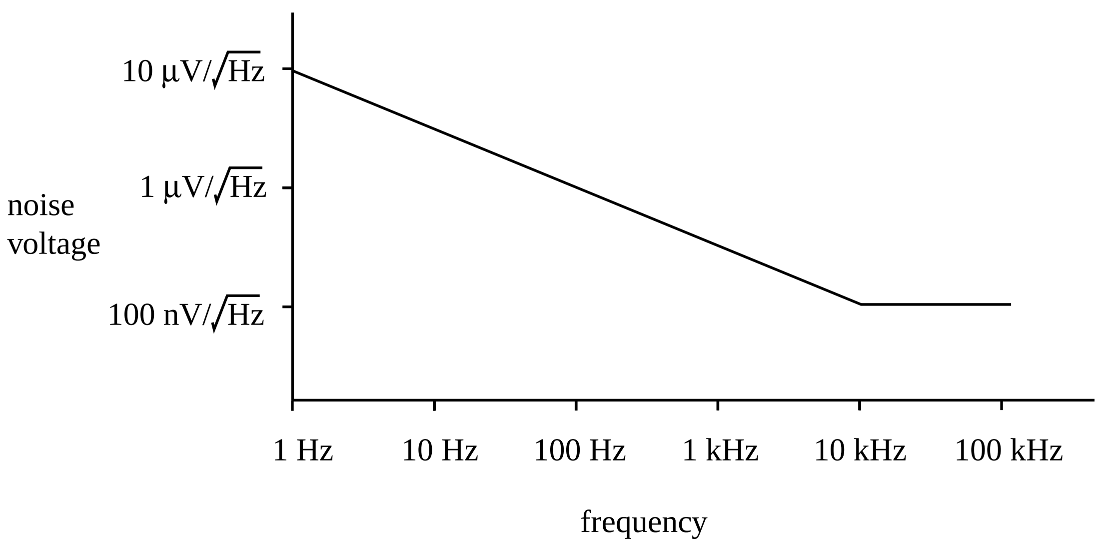
$$\frac{1}{I_S}\frac{dI_S}{dT} = \frac{3}{T} + \frac{1}{T}\frac{V_{Go}}{V_t} = \frac{3}{300} + \frac{1}{300}\,\frac{1.205}{0.0259} = 0.1651$$

$$\frac{dv_D}{dT} = -\left[\frac{V_{Go}\; 1.942\times 10^{-3}\; v_D}{T}\right] - \frac{3V_t}{T} = -\left[\frac{1.205-0.7}{300}\right] - \frac{3\times 0.0259}{300} = 1.942\times 10^{-3}$$

$$\frac{1}{v_D}\frac{dv_D}{dT} = \frac{1.942\times 10^{-3}}{0.7} = 2.775\times 10^{-3}$$

Problem 2.5-2

Plot the noise voltage as a function of the frequency if the thermal noise is 100 nV/$\sqrt{\text{Hz}}$ and the junction of the 1/*f* and thermal noise (the 1/*f* noise corner) is 10,000 Hz.



Problem 2.6-1

Given the polysilicon resistor in Fig. P2.6-1 with a resistivity of $\rho = 8\times10^{-4}$ Ω-cm, calculate the resistance of the structure. Consider only the resistance between contact edges. $\rho_S = 50$ Ω/ ❑

Fix problem: Eliminate . $\rho_S = 50$ Ω/ ❑ because it conflicts with $\rho = 8\times10^{-4}$ Ω-cm

$$R = \frac{\rho L}{W\mathrm{T}} = \frac{8\times10^{-4} \times 3\times10^{-4}}{1\times10^{-4} \times 8000\times10^{-8}} = 30\ \Omega$$

Problem 2.6-2

Given that you wish to match two transistors having a W/L of 100µm/0.8µm each. Sketch the layout of these two transistors to achieve the best possible matching.

Best matching is achieved using the following principles:

- unit matching
- common centroid
- photolithographic invariance

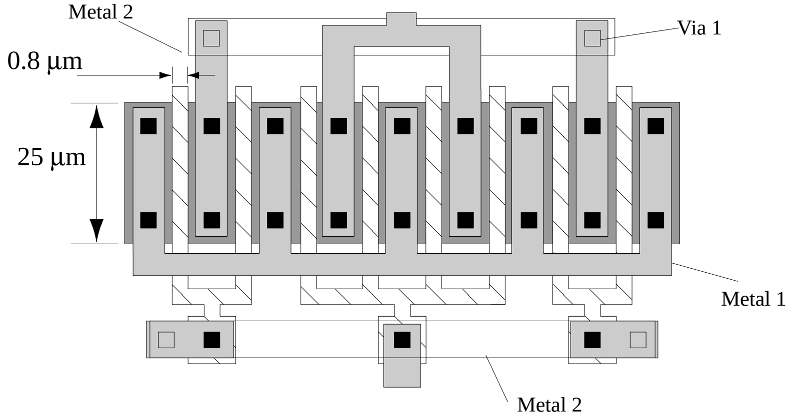


Figure P2.6-2

Problem 2.6-3

Assume that the edge variation of the top plate of a capacitor is 0.05µm and that capacitor top plates are to be laid out as squares. It is desired to match two equal capacitors to an accuracy of 0.1%. Assume that there is no variation in oxide thickness. How large would the capacitors have to be to achieve this matching accuracy?

Since capacitance is dominated by the area component, ignore the perimeter (fringe) component in this analysis. The units in the analysis that follows is micrometers.

$C = C_{\mathrm{AREA}}\,(\mathrm{d} \pm 0.05)^2$

where d is one (both) sides of the square capacitor.

$$\frac{C_1}{C_1} = \frac{(\mathrm{d} + 0.05)^2}{(\mathrm{d} - 0.05)^2} = 1.001$$

$$\frac{C_1}{C_1} = \frac{(\mathrm{d} + 0.05)^2}{(\mathrm{d} - 0.05)^2} = 1.001$$

$$\mathrm{d}^2 + 0.1\mathrm{d} + 0.05^2 = 1.001\left(\mathrm{d}^2 - 0.1\mathrm{d} + 0.05^2\right)$$

Solving this quadratic yields

d = 200.1

Problem 2.6-4
Show that a circular geometry minimizes perimeter-to-area ratio for a given area requirement. In your proof, compare against rectangle and square.

$$A_{\mathrm{circle}} = \pi r^2$$

$$A_{\mathrm{square}} = d^2$$

if $A_{\mathrm{square}} = A_{\mathrm{circle}}$

then

$$r = \frac{d\sqrt{\pi}}{\pi}$$

$$\frac{P_{\mathrm{circle}}}{P_{\mathrm{square}}} = \frac{2d\sqrt{\pi}}{4d} = \frac{\sqrt{\pi}}{2} < 1$$

Ideally, $\dfrac{C_{\mathrm{perimeter}}}{C_{\mathrm{area}}} = 0$, so since $\dfrac{P_{\mathrm{circle}}}{P_{\mathrm{square}}} < 1$, the impact of perimeter on a circle is less than on a square.

Problem 2.6-5
Show analytically how the Yiannoulos-path technique illustrated in Fig. 2.6-5 maintains a constant area-to-perimeter ratio with non-integer ratios.

Area of one unit is:

$$A_u = L^2$$

Total area = $N \times A_u$

Total periphery = 2(N + 1)

$$C_{Total} = K_A \times N \times A_u + K_P \times 2(N+1)$$

where K_A and K_P represent area and perimeter capacitance (per unit area and per unit length) respectively.

Consider two capacitors with different numbers of units but drawn following the template shown in Fig. 2.6-5(a). Their ratio would be

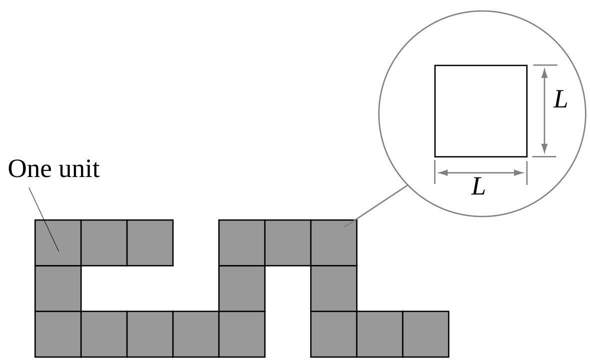


Figure P2.6-5 (a)

$$\frac{C_1}{C_2} = \frac{K_A \times N_1 \times A_u + K_P \times 2(N_1+1)}{K_A \times N_2 \times A_u + K_P \times 2(N_2+1)}$$

The ratio of the area and peripheral components by themselves are

$$\left(\frac{C_1}{C_2}\right)_{AREA} = \frac{K_A \times N_1 \times A_u}{K_A \times N_2 \times A_u} = \frac{N_1}{N_2}$$

$$\left(\frac{C_1}{C_2}\right)_{PER} = \frac{K_P \times 2(N_1+1)}{K_P \times 2(N_2+1)} = \frac{N_1+1}{N_2+1}$$

$$\frac{N_1+1}{N_2+1} \neq \frac{N_1}{N_2} \text{ unless } N_1 = N_2$$

Therefore, the structure in Fig. P2.6-5(a) cannot achieve constant area to perimeter ratio.

Consider Fig. P2.6-5(b).

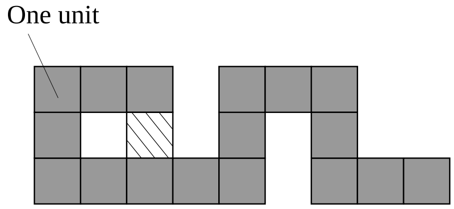


Figure P2.6-5 (b)

Total area = $(N + 1) \times A_u$

Total periphery = $2(N + 1)$ (as before)

Notice what has happened. By adding the extra unit area, two peripheral units are eliminated but two additional ones are added resulting in no change in total periphery. However, one additional area has been added. Thus

$$\frac{C_1}{C_2} = \frac{K_A \times (N_1 + 1) \times A_u + K_P \times 2(N_1 + 1)}{K_A \times (N_2 + 1) \times A_u + K_P \times 2(N_2 + 1)}$$

The ratio of the area and peripheral components by themselves are

$$\left(\frac{C_1}{C_2}\right)_{AREA} = \frac{K_A \times (N_1 + 1) \times A_u}{K_A \times (N_2 + 1) \times A_u} = \frac{N_1 + 1}{N_2 + 1}$$

$$\left(\frac{C_1}{C_2}\right)_{PER} = \frac{K_P \times 2(N_1 + 1)}{K_P \times 2(N_2 + 1)} = \frac{N_1 + 1}{N_2 + 1}$$

$$\frac{N_1 + 1}{N_2 + 1} = \frac{N_1 + 1}{N_2 + 1} \quad !!!$$

Problem 2.6-6

Design an optimal layout of a matched pair of transistors whose W/L are 8μm/1μm. The matching should be photolithographic invariant as well as common centroid.

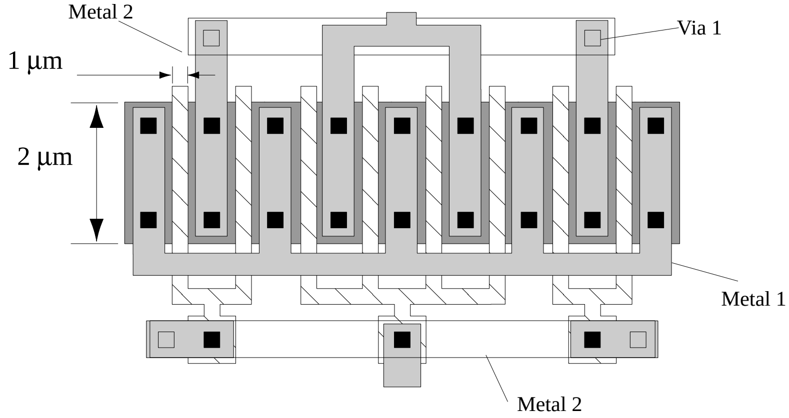


Figure P2.6-6

Problem 2.6-7

Figure P2.6-7 illustrates various ways to implement the layout of a resistor divider. Choose the layout that BEST achieves the goal of a 2:1 ratio. Explain why the other choices are not optimal.

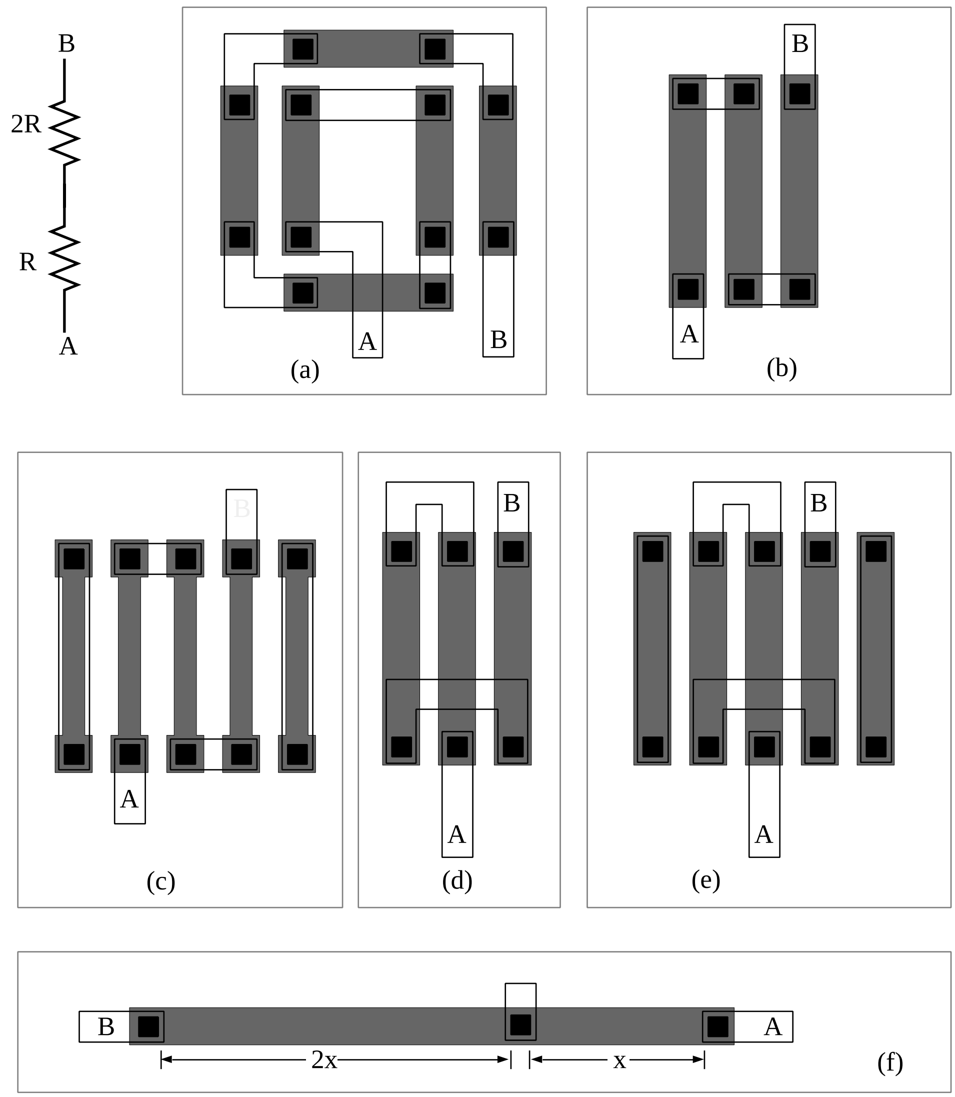


Figure P2.6-7

Option A suffers the following:

- Orientation of the 2R resistor is partly orthogonal to the 1R resistor. Matched resistors should have the same orientation.
- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.

Option B suffers the following:

- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.
- Resistors do not share a common centroid as they should.

Option C suffers the following:

- Resistors do not share a common centroid as they should.
- Uncertainty is introduced with the additional notch at the contact head.

Option D suffers the following:

- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.

Option E suffers the following:

- Nothing

Option F suffers the following:

- Violates the unit-matching principle
- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.
- Resistors do not share a common centroid as they should.

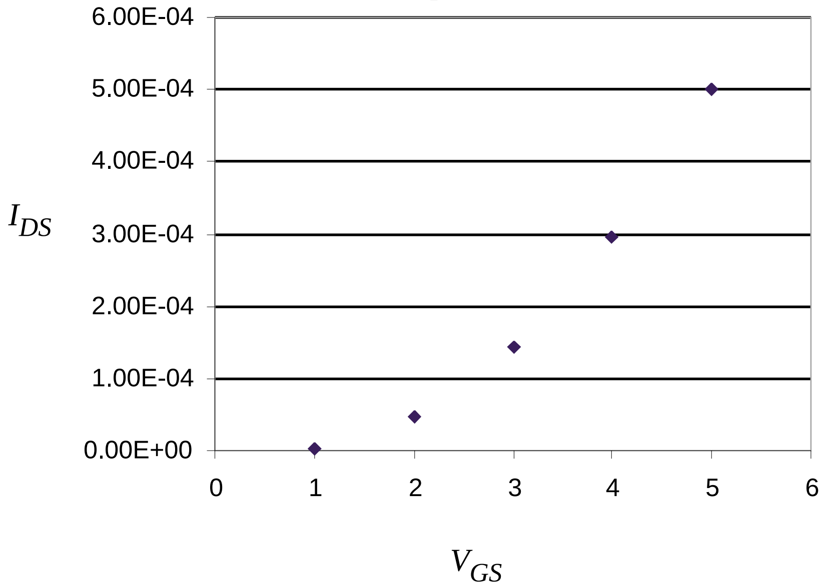
	Unit Matching	Etch Comp.	Orientation	Common Centroid
(a)	Yes	No	No	Yes
(b)	Yes	No	Yes	No
(c)	Yes	Yes	Yes	No
(d)	Yes	No	Yes	Yes
(e)	Yes	Yes	Yes	Yes
(f)	No	No	Yes	No

Clearly, option (e) is the best choice.

Chapter 3 Homework Solutions

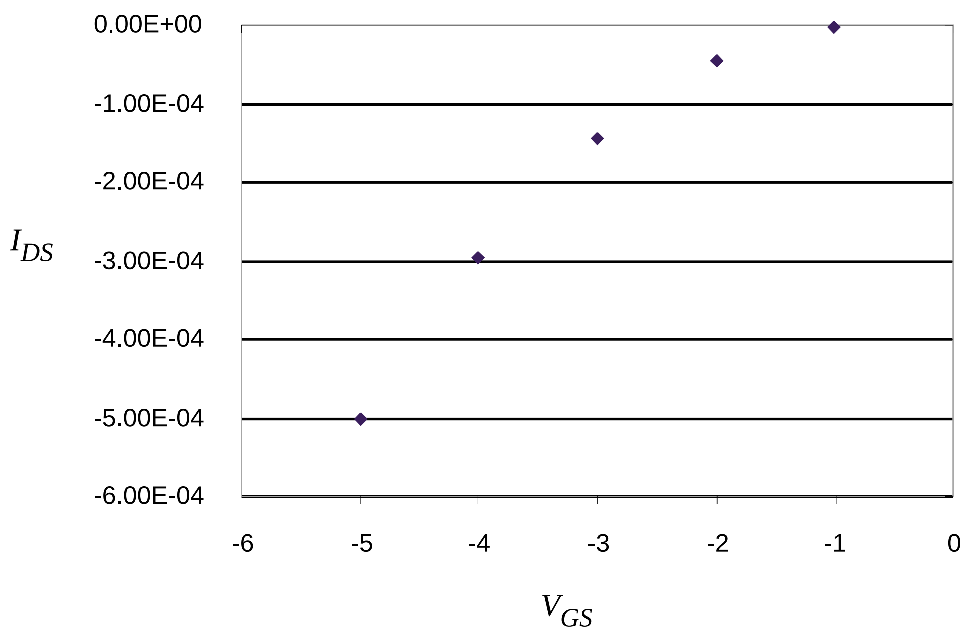
Problem 3.1-1

Sketch to scale the output characteristics of an enhancement n-channel device if $V_T = 0.7$ volt and $I_D = 500\ \mu$A when $V_{GS} = 5$ V in saturation. Choose values of $V_{GS} = 1$, 2, 3, 4, and 5 V. Assume that the channel modulation parameter is zero.



Problem 3.1-2

Sketch to scale the output characteristics of an enhancement p-channel device if $V_T = -0.7$ volt and $I_D = -500\ \mu$A when $V_{GS} = -1$, -2, -3, -4, and -6 V. Assume that the channel modulation parameter is zero.



Problem 3.1-3
In Table 3.1-2, why is γ_P greater than γ_N for a n-well, CMOS technology?
The expression for γ is:

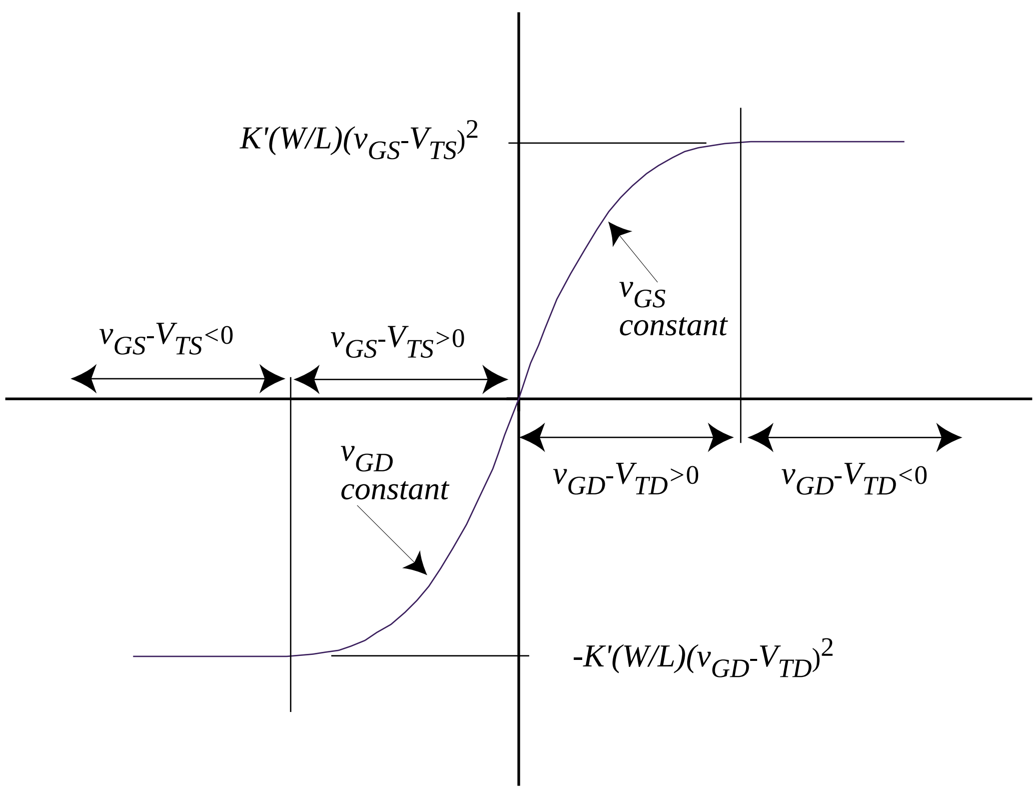
$$\gamma = \frac{\sqrt{2\varepsilon_{si}\, q\, N_{SUB}}}{C_{ox}}$$

Because γ is a function of substrate doping, a higher doping results in a larger value for γ. In general, for an nwell process, the well has a greater doping concentration than the substrate and therefore devices in the well will have a larger γ.

Problem 3.1-4
A large-signal model for the MOSFET which features symmetry for the drain and source is given as

$$i_D = K'\frac{W}{L}\left\{[(v_{GS} - V_{TS})^2\, u(v_{GS} - V_{TS})] - [(v_{GD} - V_{TD})^2\, u(v_{GD} - V_{TD})]\right\}$$

where $u(x)$ is 1 if x is greater than or equal to zero and 0 if x is less than zero (step function) and V_{TX} is the threshold voltage evaluated from the gate to X where X is either S (Source) or D (Drain). Sketch this model in the form of i_D versus v_{DS} for a constant value of v_{GS} ($v_{GS} > V_{TS}$) and identify the saturated and nonsaturated regions. Be sure to extend this sketch for both positive and negative values of v_{DS}. Repeat the sketch of i_D versus v_{DS} for a constant value of v_{GD} ($v_{GD} > V_{TD}$). Assume that both V_{TS} and V_{TD} are positive.



Problem 3.1-5

Equation (3.1-12) and Eq. (3.1-18) describe the MOS model in nonsaturation and saturation region, respectively. These equations do not agree at the point of transition between saturation and nonsaturation regions. For hand calculations, this is not an issue, but for computer analysis, it is. How would you change Eq. (3.1-18) so that it would agree with Eq. (3.1-12) at $v_{DS} = v_{DS}$ (sat)?

$$i_D = K'\frac{W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right]v_{DS} \tag{3.1-12}$$

$$i_D = K'\ \frac{W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS}),\quad 0 < (v_{GS} - V_T) \le v_{DS} \tag{3.1-18}$$

What happens to Eq. 3.1-12 at the point where saturation occurs?

$$i_D = K'\frac{W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}\,(sat)}{2}\right]v_{DS}(sat)$$

$$v_{DS}\,(sat) = v_{GS} - V_T$$

then

$$i_D = K'\frac{W}{L}\left[(v_{GS} - V_T)\ v_{DS}(sat) - \frac{v_{DS}^2\,(sat)}{2}\right]$$

$$i_D = K'\frac{W}{L}\left[(v_{GS} - V_T)\ (v_{GS} - V_T) - \frac{(v_{GS} - V_T)^2}{2}\right]$$

$$i_D = K'\frac{W}{L}\left[(\ v_{GS} - V_T)\ ^2 - \frac{(v_{GS} - V_T)^2}{2}\right] = K'\frac{W}{L}\left[\frac{(v_{GS} - V_T)^2}{2}\right]$$

$$i_D = K'\frac{W}{L}\left[\frac{(v_{GS} - V_T)^2}{2}\right]$$

which is not equal to Eq.(3.1-18) because of the channel-length modulation term.

Since Eq. (3.1-18) is valid only during saturation when $v_{DS} > v_{DS}(sat)$ we can subtract $v_{DS}(sat)$ from the v_{DS} in the channel-length modulation term. Doing this results in the following modification of Eq. (3.1-18).

$$i_D = K'\ \frac{W}{2L}(v_{GS} - V_T)^2\left[1 + \lambda\,(v_{DS}\ -\ v_{DS}(sat))\right]\ ,\quad 0 < (v_{GS} - V_T) \le v_{DS}$$

When $v_{DS} = v_{DS}(sat)$, this expression agrees with the non-saturation equation at the point of transition into saturation. Beyond saturation, channel-length modulation is applied to the difference in v_{DS} and $v_{DS}(sat)$.

Problem 3.2-1
Using the values of Tables 3.1-1 and 3.2-1, calculate the values of CGB, CGS, and CGD for a MOS device which has a W of 5 μm and an L of 1 μm for all three regions of operation.

We will need LD in these calculations. LD can be approximated from the value given for CGSO in Table 3.2-1.

$$LD = \frac{220 \times 10^{-12}}{24.7 \times 10^{-4}} \cong 89 \times 10^{-9}$$

Off

$$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{\text{eff}})(L_{\text{eff}}) + 2\text{CGBO}(L_{\text{eff}})$$

$$W_{\text{eff}} = 5\ \mu\text{m}$$

$$L_{\text{eff}} = 1\ \mu\text{m - } 2{\times}89\text{ nm} = 822 \times 10^{-9}$$

$$C_{GB} = 24.7 \times 10^{-4} \times (5{\times}\ 10^{-6})(\ 822 \times 10^{-9}) + 2{\times}700 \times 10^{-12}{\times}822 \times 10^{-9}$$

$$C_{GB} = 11.3 \times 10^{-15}\text{ F}$$

$$C_{GS} = C_1 \cong C_{ox}(\text{LD})(W_{\text{eff}}) = \text{CGSO}(W_{\text{eff}})$$

$$C_{GS} = (\ 220 \times 10^{-12})\ (\ 5 \times 10^{-6}) = 1.1 \times 10^{-15}$$

$$C_{GD} = C_2 \cong C_{ox}(\text{LD})(W_{\text{eff}}) = \text{CGDO}(W_{\text{eff}})$$

$$C_{GD} = (\ 220 \times 10^{-12})\ (\ 5 \times 10^{-6}) = 1.1 \times 10^{-15}$$

Saturation

$$C_{GB} = 2C_5 = \text{CGBO}\ (L_{\text{eff}})$$

C_{GB} = 700×10^{-12} (822×10^{-9}) = 575×10^{-18}

C_{GS} = CGSO(W_{eff}) + 0.67C_{ox}(W_{eff})(L_{eff})

$C_{GS} = 220 \times 10^{-12} \times 5 \times 10^{-6} + 0.67 \times 24.7 \times 10^{-4} \times 822 \times 10^{-9} \times 5 \times 10^{-6}$

$C_{GS} = 7.868 \times 10^{-15}$

$C_{GD} = C_3 \cong C_{ox}$(LD)($W_{\mathrm{eff}}$) = CGDO($W_{\mathrm{eff}}$)

C_{GD} = CGDO(W_{eff}) = $220 \times 10^{-12} \times 5 \times 10^{-6} = 1.1 \times 10^{-15}$

Nonsaturated

$C_{GB} = 2C_5$ = CGBO (L_{eff})

C_{GB} = CGBO (L_{eff}) = $700 \times 10^{-12} \times 822 \times 10^{-9} = 574 \times 10^{-18}$

C_{GS} = (CGSO + 0.5$C_{ox}L_{\mathrm{eff}}$)W_{eff}

$C_{GS} = (220 \times 10^{-12} + 0.5 \times 24.7 \times 10^{-4} \times 822 \times 10^{-9}) \times 5 \times 10^{-6} = 6.18 \times 10^{-15}$

C_{GD} = (CGDO + 0.5$C_{ox}L_{\mathrm{eff}}$)W_{eff}

$C_{GD} = (220 \times 10^{-12} + 0.5 \times 24.7 \times 10^{-4} \times 822 \times 10^{-9}) \times 5 \times 10^{-6} = 6.18 \times 10^{-15}$

Problem 3.2-2

Find C_{BX} at V_{BX} = 0 V and 0.75 V of Fig. P3.7 assuming the values of Table 3.2-1 apply to the MOS device where FC = 0.5 and PB = 1 V. Assume the device is n-channel and repeat for a p-channel device.

Change problem to read: "|V_{BX} |= 0 V and 0.75 V (with the junction always reverse biased)…"

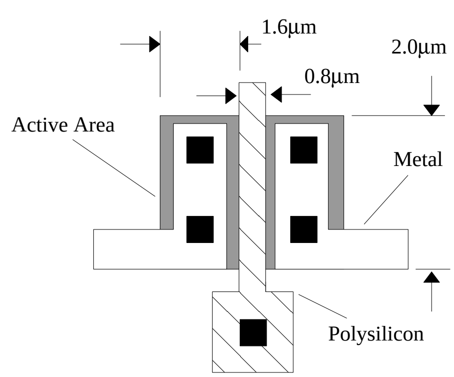


Figure P3.2-2

$AX = 1.6 \times 10^{-6} \times 2.0 \times 10^{-6} = 3.2 \times 10^{-12}$
$PX = 2\times 1.6 \times 10^{-6} + 2.0 \times 2.0 \times 10^{-6} = 7.2 \times 10^{-6}$

NMOS case:

$$C_{BX} = \frac{(\mathrm{CJ})(\mathrm{AX})}{\left[1 - \left(\frac{v_{BX}}{\mathrm{PB}}\right)\right]^{\mathrm{MJ}}} + \frac{(\mathrm{CJSW})(\mathrm{PX})}{\left[1 - \left(\frac{v_{BX}}{\mathrm{PB}}\right)\right]^{\mathrm{MJSW}}}$$

$$C_{BX} = \frac{(770 \times 10^{-6})(\ 3.2 \times 10^{-12})}{\left[1 - \left(\frac{0}{\mathrm{PB}}\right)\right]^{\mathrm{MJ}}} + \frac{(380 \times 10^{-12})(\ 7.2 \times 10^{-6})}{\left[1 - \left(\frac{0}{\mathrm{PB}}\right)\right]^{\mathrm{MJSW}}} = 5.2 \times 10^{-15}$$

PMOS case:

$$C_{BX} = \frac{(560 \times 10^{-6})(\ 3.2 \times 10^{-12})}{\left[1 - \left(\frac{0}{\mathrm{PB}}\right)\right]^{\mathrm{MJ}}} + \frac{(350 \times 10^{-12})(\ 7.2 \times 10^{-6})}{\left[1 - \left(\frac{0}{\mathrm{PB}}\right)\right]^{\mathrm{MJSW}}} = 4.31 \times 10^{-15}$$

$|v_{BX}|$ = 0.75 volts reverse biased

NMOS case:

$$C_{BX} = \frac{(\mathrm{CJ})(\mathrm{AX})}{\left[1 - \left(\frac{v_{BX}}{\mathrm{PB}}\right)\right]^{\mathrm{MJ}}} + \frac{(\mathrm{CJSW})(\mathrm{PX})}{\left[1 - \left(\frac{v_{BX}}{\mathrm{PB}}\right)\right]^{\mathrm{MJSW}}},$$

$$C_{BX} = \frac{(770 \times 10^{-6})(\ 3.2 \times 10^{-12})}{\left[1 - \left(\frac{-0.75}{1}\right)\right]^{0.5}} + \frac{(380 \times 10^{-12})(\ 7.2 \times 10^{-6})}{\left[1 - \left(\frac{-0.75}{1}\right)\right]^{0.38}}$$

$$C_{BX} = \frac{2.464 \times 10^{-15}}{1.323} + \frac{2.736 \times 10^{-15}}{1.237} = 4.07 \times 10^{-15}$$

PMOS case:

$$C_{BX} = \frac{(560 \times 10^{-6})(\ 3.2 \times 10^{-12})}{\left[1 - \left(\frac{-0.75}{1}\right)\right]^{0.5}} + \frac{(350 \times 10^{-12})(\ 7.2 \times 10^{-6})}{\left[1 - \left(\frac{-0.75}{1}\right)\right]^{0.35}}$$

$$C_{BX} = \frac{1.79 \times 10^{-15}}{1.323} + \frac{2.52 \times 10^{-15}}{1.216} = 3.425 \times 10^{-15}$$

Problem 3.2-3

Calculate the value of C_{GB}, C_{GS}, and C_{GD} for an n-channel device with a length of 1 μm and a width of 5 μm. Assume V_D = 2 V, V_G = 2.4 V, and V_S = 0.5 V and let V_B = 0 V. Use model parameters from Tables 3.1-1, 3.1-2, and 3.2-1.

$$LD = \frac{220 \times 10^{-12}}{24.7 \times 10^{-4}} \cong 89 \times 10^{-9}$$

$$L_{\text{eff}} = \text{L - } 2 \times \text{LD} = 1 \times 10^{-6} - 2 \times 89 \times 10^{-9} = 822 \times 10^{-9}$$

$$V_T = V_{T0} + \gamma[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}]$$

$$V_T = 0.7 + 0.4\,[\sqrt{0.7 + 0.5} - \sqrt{0.7}] = 0.803$$

$v_{GS} - v_T$ =2.4 – 0.5 – 0.803 = 1.096 < v_{DS} thus saturation region

$$C_{GB} = \text{CGBO } x\ L_{eff} = 700 \times 10^{-12} \times 822 \times 10^{-9} = 0.575 \text{ fF}$$

$$C_{GS} = \text{CGSO}(W_{\text{eff}}) + 0.67C_{ox}(W_{\text{eff}})(L_{\text{eff}})$$

$$C_{GS} = 220 \times 10^{-12} \times 5 \times 10^{-6} + 0.67 \times 24.7 \times 10^{-4} \times 822 \times 10^{-9} \times 5 \times 10^{-6}$$

$$C_{GS} = 7.868 \times 10^{-15}$$

$$C_{GD} = C_3 \cong C_{ox}(\text{LD})(W_{\text{eff}}) = \text{CGDO}(W_{\text{eff}})$$

$$C_{GD} = \text{CGDO}(W_{\text{eff}}) = 220 \times 10^{-12} \times 5 \times 10^{-6} = 1.1 \times 10^{-15}$$

Problem 3.3-1

Calculate the transfer function $v_{out}(s)/v_{in}(s)$ for the circuit shown in Fig. P3.3-1. The W/L of M1 is 2µm/0.8µm and the W/L of M2 is 4µm/4µm. Note that this is a small-signal analysis and the input voltage has a dc value of 2 volts.

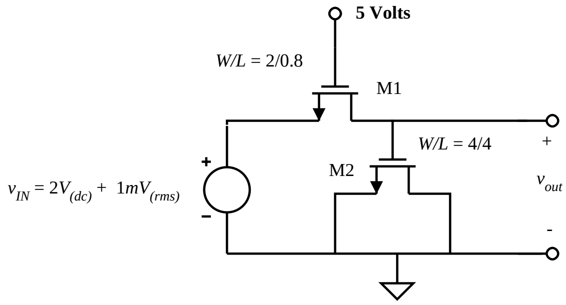


Figure P3.3-1

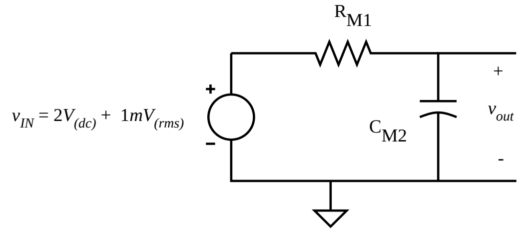


Figure P3.3-1b

$$\frac{v_{\text{out}}(s)}{v_{\text{IN}}(s)} = \frac{1/SC_{\text{M2}}}{R_{\text{M1}} + 1/SC_{\text{M2}}} = \frac{1}{SC_{\text{M2}}R_{\text{M1}} + 1}$$

$$V_{T1} = V_{T0} + \gamma[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}]$$

$$V_{T1} = 0.7 + 0.4\,[\sqrt{0.7 + 2.0} - \sqrt{0.7}] = 1.02$$

$$R_{\text{M1}} = \frac{1}{K'(W/L)_{\text{M1}}\,(v_{GS1} - V_{T1})} = 1.837\ \text{k}\Omega$$

$$C_{\text{M2}} = W_{\text{M2}} \times L_{\text{M2}} \times C_{\text{ox}} = 4 \times 10^{-6} \times 4 \times 10^{-6} \times 24.7 \times 10^{-4} = 39.52 \times 10^{-15}$$

$$R_{\text{M1}}C_{\text{M2}} = 1.837\ \text{k}\Omega \times 39.52 \times 10^{-15} = 72.6 \times 10^{-12}$$

$$\frac{v_{\text{out}}(s)}{v_{\text{IN}}(s)} == \frac{1}{\dfrac{S}{13.77 \times 10^{9}} + 1}$$

Problem 3.3-2

Design a low-pass filter patterened after the circuit in Fig. P3.3-1 that achieves a -3dB frequency of 100 KHz.

$$\frac{1}{2\pi RC} = 100{,}000$$

There is more than one answer to this problem because there are two free parameters.
Use the resistance from Problem 3.3-1.

$R_{M1} = \ 1.837\ \text{k}\Omega$

$$C_{M2} = \frac{1}{2\pi\times 1.837\times 10^{3}\times 1\times 10^{5}} = \ 866.4\ \text{pF}$$

Choose $W = L$

$$C_{M2} = W_{M2}\times L_{M2}\times C_{ox} = W_{M2}^{2}\times 24.7\times 10^{-4} = 866.4\times 10^{-12}$$

$$W_{M2}^{2} = 350.8\times 10^{-9}$$

$$W_{M2} = 592\times 10^{-6}$$

Problem 3.3-3
Repeat Examples 3.3-1 and 3.3-2 if the W/L ratio is 100 μm/10 μm.
Problem correction: Assume λ = 0.01.

Repeat of Example 3.3-1

N-Channel Device

$$g_m = \sqrt{(2K'W/L)|I_D|}$$

$$g_m = \sqrt{2\times 110\times 10^{-6}\times 10\times 50\times 10^{-6}} = 332\times 10^{-6}$$

$$g_{mbs} = g_m\frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}}$$

$$g_{mbs} = 332\times 10^{-6}\frac{0.4}{2(0.7+2.0)^{1/2}} = 40.4\times 10^{-6}$$

$$g_{ds} = \ I_D\,\lambda$$

$$g_{ds} = 50\times 10^{-6}\times 0.01 = 500\times 10^{-9}$$

P-Channel Device

$$g_m = \sqrt{(2K'W/L)|I_D|}$$

$$g_m = \sqrt{2 \times 50 \times 10^{-6} \times 10 \times 50 \times 10^{-6}} = 224 \times 10^{-6}$$

$$g_{mbs} = g_m \frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}}$$

$$g_{mbs} = 224 \times 10^{-6} \frac{0.57}{2(0.8+2.0)^{1/2}} = 38.2 \times 10^{-6}$$

$$g_{ds} = I_D \lambda$$

$$g_{ds} = 50 \times 10^{-6} \times 0.01 = 500 \times 10^{-9}$$

Repeat of Example 3.3-2

N-Channel Device

$$g_m = \beta V_{DS} = 110 \times 10^{-6} \times 10 \times 1 = 1.1 \times 10^{-3}$$

$$g_{mbs} = \frac{\beta\gamma V_{DS}}{2(2|\phi_F| + V_{SB})^{1/2}} = \frac{110 \times 10^{-6} \times 0.4 \times 1 \times 10}{2(0.7+2)^{1/2}} = 134 \times 10^{-6}$$

$$V_T = V_{T0} + \gamma[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}]$$

$$V_T = 0.7 + 0.4\,[\sqrt{0.7 + 2.0} - \sqrt{0.7}] = 1.02$$

$$g_{ds} = \beta(V_{GS} - V_T - V_{DS}) = 10 \times 110 \times 10^{-6}\,(5 - 1.02 - 1) = 3.28 \times 10^{-3}$$

P-Channel Device

$$g_m = \beta V_{DS} = 50 \times 10^{-6} \times 10 \times 1 = 500 \times 10^{-6}$$

$$g_{mbs} = \frac{\beta\gamma V_{DS}}{2(2|\phi_F| + V_{SB})^{1/2}} = \frac{50 \times 10^{-6} \times 0.57 \times 1 \times 10}{2(0.8+2)^{1/2}} = 85.2 \times 10^{-6}$$

$$|V_T| = |V_{T0}| + \gamma[\sqrt{2|\phi_F| + v_{BS}} - \sqrt{2|\phi_F|}]$$

$$|V_T| = 0.7 + 0.57\,[\sqrt{0.8 + 2.0} - \sqrt{0.8}] = 1.144$$

$$g_{ds} = \beta(V_{GS} - V_T - V_{DS}) = 10 \times 50 \times 10^{-6} (5 - 1.144 - 1) = 1.428 \times 10^{-3}$$

Problem 3.3-4

Find the complete small-signal model for an n-channel transistor with the drain at 4 V, gate at 4 V, source at 2 V, and the bulk at 0 V. Assume the model parameters from Tables 3.1-1, 3.1-2, and 3.2-1, and $W/L = 10\ \mu\text{m}/1\ \mu\text{m}$.

$$V_T = V_{T0} + \gamma[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}]$$

$$V_T = 0.7 + 0.4\,[\sqrt{0.7 + 2.0} - \sqrt{0.7}] = 1.02$$

$$I_D = \frac{K'W}{2L}(v_{GS} - v_T)^2 (1 + \lambda v_{DS}) = \frac{110 \times 10^{-6} \times 10}{2}(2 - 1.02)^2(1 + 0.4 \times 2) = 570 \times 10^{-6}$$

$$g_m = \sqrt{(2K'W/L)|I_D|}$$

$$g_m = \sqrt{2 \times 110 \times 10^{-6} \times 10 \times 570 \times 10^{-6}} = 1.12 \times 10^{-3}$$

$$g_{mbs} = g_m \frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}}$$

$$g_{mbs} = 1.12 \times 10^{-3} \frac{0.4}{2(0.7+2.0)^{1/2}} = 136 \times 10^{-6}$$

$$g_{ds} = I_D\,\lambda$$

$$g_{ds} = 570 \times 10^{-6} \times 0.04 = 22.8 \times 10^{-9}$$

$$LD = \frac{220 \times 10^{-12}}{24.7 \times 10^{-4}} \cong 89 \times 10^{-9}$$

$$L_{\text{eff}} = \text{L} - 2 \times \text{LD} = 1 \times 10^{-6} - 2 \times 89 \times 10^{-9} = 822 \times 10^{-9}$$

$$C_{GB} = \text{CGBO}\ x\ L_{eff} = 700 \times 10^{-12} \times 822 \times 10^{-9} = 0.575\ \text{fF}$$

$$C_{GS} = \text{CGSO}(W_{\text{eff}}) + 0.67C_{ox}(W_{\text{eff}})(L_{\text{eff}})$$

$C_{GS} = 220 \times 10^{-12} \times 10 \times 10^{-6} + 0.67 \times 24.7 \times 10^{-4} \times 822 \times 10^{-9} \times 10 \times 10^{-6}$

$C_{GS} = 15.8 \times 10^{-15}$

$C_{GD} = \mathrm{CGDO}(W_{\mathrm{eff}})$

$C_{GD} = \mathrm{CGDO}(W_{\mathrm{eff}}) = 220 \times 10^{-12} \times 10 \times 10^{-6} = 2.2 \times 10^{-15}$

Problem 3.3-5
Consider the circuit in Fig P3.3-5. It is a parallel connection of *n* mosfet transistors. Each transistor has the same length, *L*, but each transistor can have a different width, *W*. Derive an expression for *W* and *L* for a single transistor that replaces, and is equivalent to, the multiple parallel transistors.

The expression for drain current in saturation is:

$$I_D = \frac{K'W}{2L}\left(v_{GS} - v_T \right)^2 (1 + \lambda\, v_{DS})$$

For multiple transistors with the same drain, gate, and source voltage, the drain current can be expressed simply as

$$I_{D(\mathrm{i})} = \left(\frac{W}{L}\right)_{\mathrm{i}} \left(v_{GS} - v_T \right)^2 (1 + \lambda\, v_{DS})$$

The drain current in each transistor is additive to the total current, thus

$$I_{D(\mathrm{TOTAL})} = \left(v_{GS} - v_T \right)^2 (1 + \lambda\, v_{DS}) \left[\sum \left(\frac{W}{L}\right)_{\mathrm{i}} \right]$$

Since the lengths are the same, we have

$$I_{D(\mathrm{TOTAL})} = \frac{1}{L}\left(v_{GS} - v_T \right)^2 (1 + \lambda\, v_{DS}) \left[\sum W_{\mathrm{i}} \right]$$

Problem 3.3-6
Consider the circuit in Fig P3.3-6. It is a series connection of *n* mosfet transistors. Each transistor has the same width, *W*, but each transistor can have a different length, *L*. Derive an expression for *W* and *L* for a single transistor that replaces, and is equivalent to, the multiple parallel transistors. When using the simple model, you must ignore body effect.

Error in problem statement : replace “parallel” with “series”

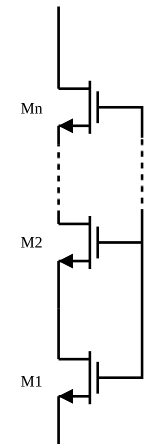
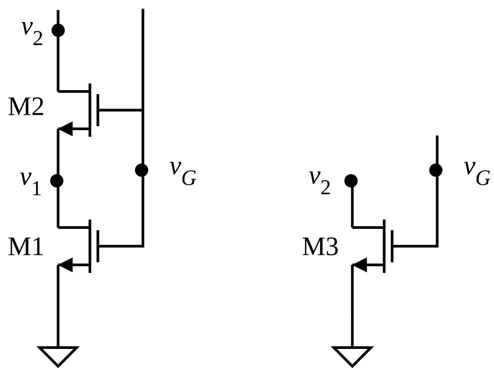


Figure P3.3-6

Assume that all devices are in the non-saturation region.

Consider the case for two transistors in series as illustrated below.



The drain current in M1 is

$$i_1 = \frac{K'W}{L}\left[(v_{GS} - V_T)\, v_{DS} - \frac{v_{DS}^2}{2}\right]$$

$$i_1 = \beta_1\left[(v_{GS} - V_T)\, v_1 - \frac{v_1^2}{2}\right] = \beta_1\left[(v_G - V_T)\, v_1 - \frac{v_1^2}{2}\right]$$

$$i_1 = \beta_1\left[\; V_{\text{on}}\, v_1 - \frac{v_1^2}{2}\right]$$

where

$V_{on} = v_G - V_T$

$$v_1 = V_{on} - \sqrt{V_{on}^2 - \frac{2i_1}{\beta_1}}$$

$$v_1^2 = 2V_{on} - 2V_{on}\sqrt{V_{on}^2 - \frac{2i_1}{\beta_1}} - \frac{2i_1}{\beta_1}$$

The drain current in M2 is

$$i_2 = \beta_2\left[(v_G - v_1 - V_T)(v_2 - v_1) - \frac{(v_2 - v_1)^2}{2}\right]$$

$$i_2 = \beta_2\left[(V_{on} - v_1)(v_2 - v_1) - \frac{(v_2 - v_1)^2}{2}\right]$$

$$i_2 = \beta_2\left[V_{on}\, v_2 - V_{on} v_1 + \frac{v_1^2}{2} - \frac{v_2^2}{2}\right]$$

Substitue the earlier expression for v_1 and equate the drain currents (drain currents must be equal)

$$i_2 = \frac{\beta_1\,\beta_2}{\beta_1 + \beta_2}\left[V_{on}\, v_2 - \frac{v_2^2}{2}\right]$$

The expression for the current in M3 is

$$i_3 = \beta_3\left[(v_{GS} - V_T)\, v_2 - \frac{v_2^2}{2}\right] = \beta_3\left[V_{on}\, v_2 - \frac{v_2^2}{2}\right]$$

The drain current in M3 must be equivalent to the drain current in M1 and M2, thus

$$\beta_3 = \frac{\beta_1\,\beta_2}{\beta_1 + \beta_2} = \left(\frac{1}{\beta_1} + \frac{1}{\beta_2}\right)^{-1} = \left(\frac{L_1}{K'W_1} + \frac{L_2}{K'W_2}\right)^{-1}$$

Since the widths are equal and the transconductances are equal

$$\beta_3 = \frac{1}{K'W}(L_1 + L_2)$$

This analysis is easily extended to address any number of transistors (repeat the analysis with M3 and another transistor in series with it—two at a time)

$$L_{\mathrm{EQUIVALENT}} = \sum_{0}^{\mathrm{i}} L_{\mathrm{i}}$$

Problem 3.5-1

Calculate the value for V_{ON} for n MOS transistor in weak inversion assuming that *fs* and *fn* can be approximated to be unity (1.0).

Assume (from Level 1 parameters):

GAMMA = 0.4
PHI = 0.7
COX = 24.7×10^{-4} F/m^2
$v_{SB} = 0$

NFS = 7×10^{15} (m^{-2}) from Table 3.4-1

$$v_{on} = V_T + fast$$

where

$$fast = \frac{kT}{q}\left[1 + \frac{q \times NFS}{\mathrm{COX}} + \frac{\mathrm{GAMMA} \times f_s\,(\mathrm{PHI} + v_{SB})^{1/2} + f_n\,(\mathrm{PHI} + v_{SB})}{2(\mathrm{PHI} + v_{SB})}\right]$$

if

$$f_s = f_n = 1$$

$$fast = \frac{kT}{q}\left[1 + \frac{q \times NFS}{\mathrm{COX}} + \frac{\mathrm{GAMMA} \times (\mathrm{PHI} + v_{SB})^{1/2} + (\mathrm{PHI} + v_{SB})}{2(\mathrm{PHI} + v_{SB})}\right]$$

$$fast = 0.0259\left[1 + \frac{1.6 \times 10^{-19} \times 7 \times 10^{15}}{24.7 \times 10^{-4}} + \frac{0.4 \times (0.7 + 0)^{1/2} + (0.7 + 0)}{2(0.7 + 0)}\right]$$

$fast = 0.0259\,(1 + .453 + 0.739) = 56.77 \times 10^{-3}$

$v_{on} = V_T + fast = 0.0259 + 56.77 \times 10^{-3} = 82.67 \times 10^{-3}$

Problem 3.5-2

Develop an expression for the small signal transconductance of a MOS device operating in weak inversion using the large signal expression of Eq. (3.5-5).

$$i_D \cong \frac{W}{L} I_{DO} \exp\left(\frac{v_{GS}}{n(kT/q)}\right)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L}\left(\frac{1}{n(kT/q)}\right) I_{DO} \exp\left(\frac{v_{GS}}{n(kT/q)}\right) = \frac{I_D}{n(kT/q)}$$

Problem 3.5-3

Another way to approximate the transition from strong inversion to weak inversion is to find the current at which the weak-inversion transconductance and the strong-inversion transconductance are equal. Using this method and the approximation for drain current in weak inversion (Eq. (3.5-5)), derive an expression for drain current at the transition between strong and weak inversion.

$$g_m = \frac{W}{L}\left(\frac{1}{n(kT/q)}\right) I_{DO} \exp\left(\frac{v_{GS}}{n(kT/q)}\right) = \sqrt{(2K'W/L)I_D}$$

$$\left(\frac{W}{L}\right)^2 \left(\frac{1}{n(kT/q)}\right)^2 I_{DO}^2 \exp\left(\frac{2v_{GS}}{n(kT/q)}\right) = (2K'W/L)I_D$$

$$I_D = \left(\frac{1}{2K'}\right)\left(\frac{W}{L}\right)\left(\frac{I_{DO}}{n(kT/q)}\right)^2 \exp\left(\frac{2v_{GS}}{n(kT/q)}\right)$$

$$I_D = \left(\frac{1}{2K'}\right) I_{DO}\left(\frac{1}{n(kT/q)}\right)^2 \exp\left(\frac{v_{GS}}{n(kT/q)}\right) \times \left(\frac{W}{L}\right) I_{DO} \exp\left(\frac{v_{GS}}{n(kT/q)}\right)$$

$$I_D = \left(\frac{1}{2K'}\right) I_{DO}\left(\frac{1}{n(kT/q)}\right)^2 \exp\left(\frac{v_{GS}}{n(kT/q)}\right) \times I_D$$

$$2K'\,[n(kT/q)]^2 = I_{DO} \exp\left(\frac{v_{GS}}{n(kT/q)}\right) = \frac{I_D}{W/L}$$

$$I_D = 2K'\frac{W}{L}[n(kT/q)]^2$$

Problem 3.6-1

Consider the circuit illustrated in Fig. P3.6-1. (a) Write a SPICE netlist that describes this circuit. (b) Repeat part (a) with M2 being 2μm/1μm and it is intended that M3 and M2 are ratio matched, 1:2.

Part (a)

```
Problem 3.6-1 (a)
M1 2 1 0 0 nch W=1u L=1u
M2 2 3 4 4 pch w=1u L=1u
M3 3 3 4 4 pch w=1u L=1u
R1 3 0 50k
Vin 1 0 dc 1
Vdd 4 0 dc 5
.MODEL nch NMOS VTO=0.7 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.MODEL pch PMOS VTO=-0.7 KP=50U GAMMA=0.57 LAMBDA=0.05 PHI=0.8

.op
.end
```

Part (b)

```
Problem 3.6-1 (b)
M1 2 1 0 0 nch W=1u L=1u
M2 2 3 4 4 pch w=1u L=1u M=2
M3 3 3 4 4 pch w=1u L=1u
R1 3 0 50k
Vin 1 0 dc 1
Vdd 4 0 dc 5
.MODEL nch NMOS VTO=0.7 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.MODEL pch PMOS VTO=-0.7 KP=50U GAMMA=0.57 LAMBDA=0.05 PHI=0.8

.op
.end
```

Problem 3.6-2

Use SPICE to perform the following analyses on the circuit shown in Fig. P3.6-1: (a) Plot v_{OUT} versus v_{IN} for the nominal parameter set shown. (b) Separately, vary K' and V_T by +10% and repeat part (a)—four simulations.

Parameter	N-Channel	P-Channel	Units
V_T	0.7	-0.7	V
K'	110	50	μA/V^2
l	0.04	0.05	V^{-1}

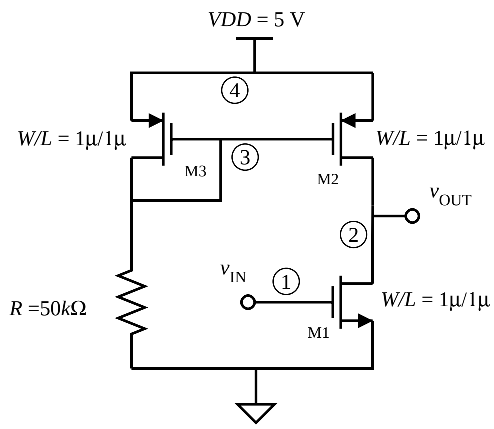
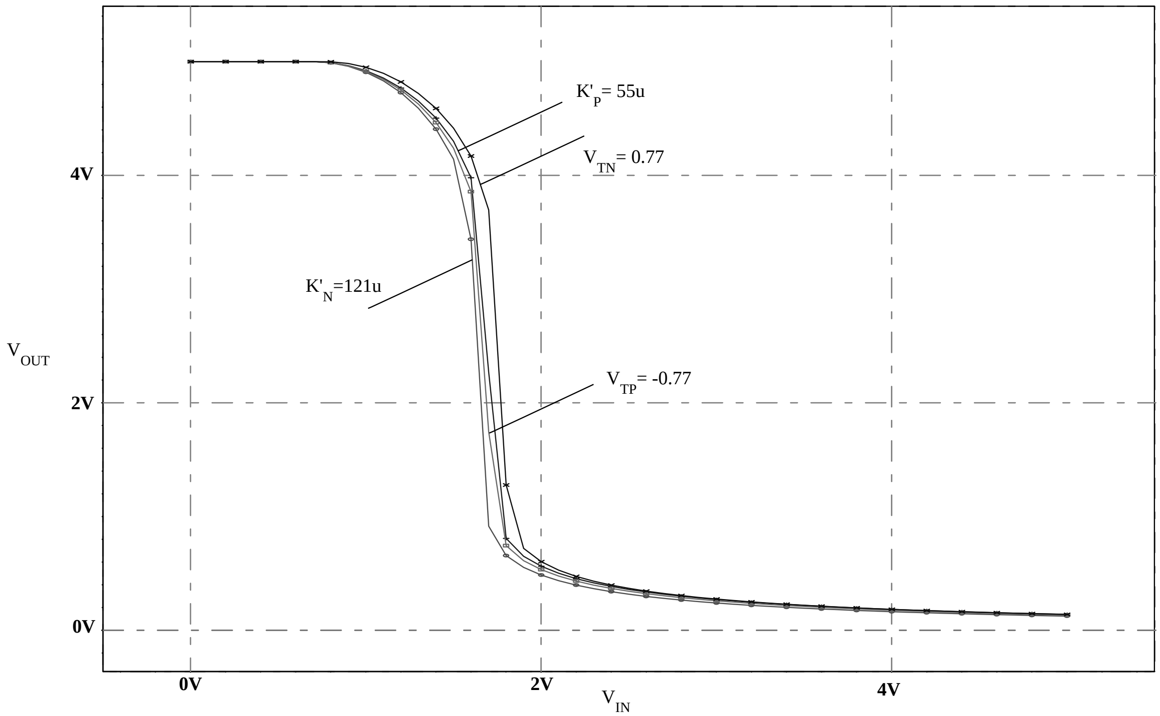


Figure P3.6-1

```
Problem 3.6-2
M1 2 1 0 0 nch W=1u L=1u
M2 2 3 4 4 pch w=1u L=1u
M3 3 3 4 4 pch w=1u L=1u
R1 3 0 50k
Vin 1 0 dc 1
Vdd 4 0 dc 5
*.MODEL nch NMOS VTO=0.7 KP=110U  LAMBDA=0.04
*.MODEL pch PMOS VTO=-0.7 KP=50U  LAMBDA=0.05
*
*.MODEL nch NMOS VTO=0.77 KP=110U  LAMBDA=0.04
*.MODEL pch PMOS VTO=-0.7 KP=50U  LAMBDA=0.05
*
*.MODEL nch NMOS VTO=0.7 KP=110U  LAMBDA=0.04
*.MODEL pch PMOS VTO=-0.77 KP=50U  LAMBDA=0.05
*
*.MODEL nch NMOS VTO=0.7 KP=121U  LAMBDA=0.04
*.MODEL pch PMOS VTO=-0.7 KP=50U  LAMBDA=0.05
*
.MODEL nch NMOS VTO=0.7 KP=110U  LAMBDA=0.04
.MODEL pch PMOS VTO=-0.7 KP=55U  LAMBDA=0.05
.dc vin 0 5 .1
.probe
.end
```



Problem 3.6-3

Use SPICE to plot i_2 as a function of v_2 when i_1 has values of 10, 20, 30, 40, 50, 60, and 70 μA for Fig. P3.6-3. The maximum value of v_2 is 5 V. Use the model parameters of V_T = 0.7 V and K' = 110 μA/V^2 and λ = 0.01 V^{-1}. Repeat with λ = 0.04 V^{-1}.

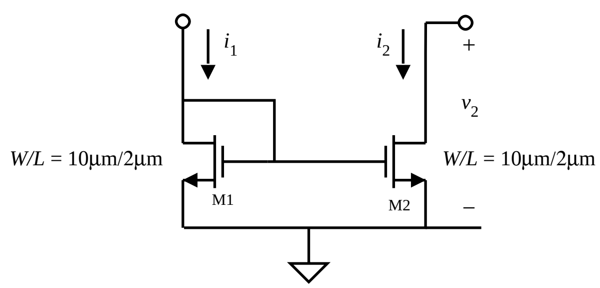
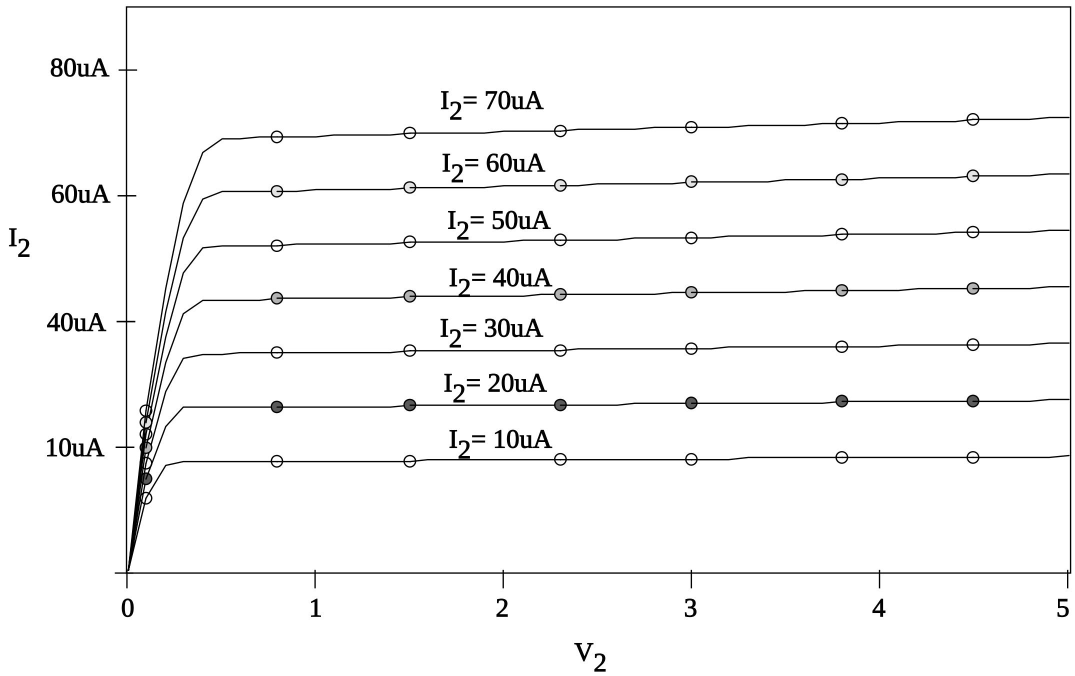


Figure P3.6-3

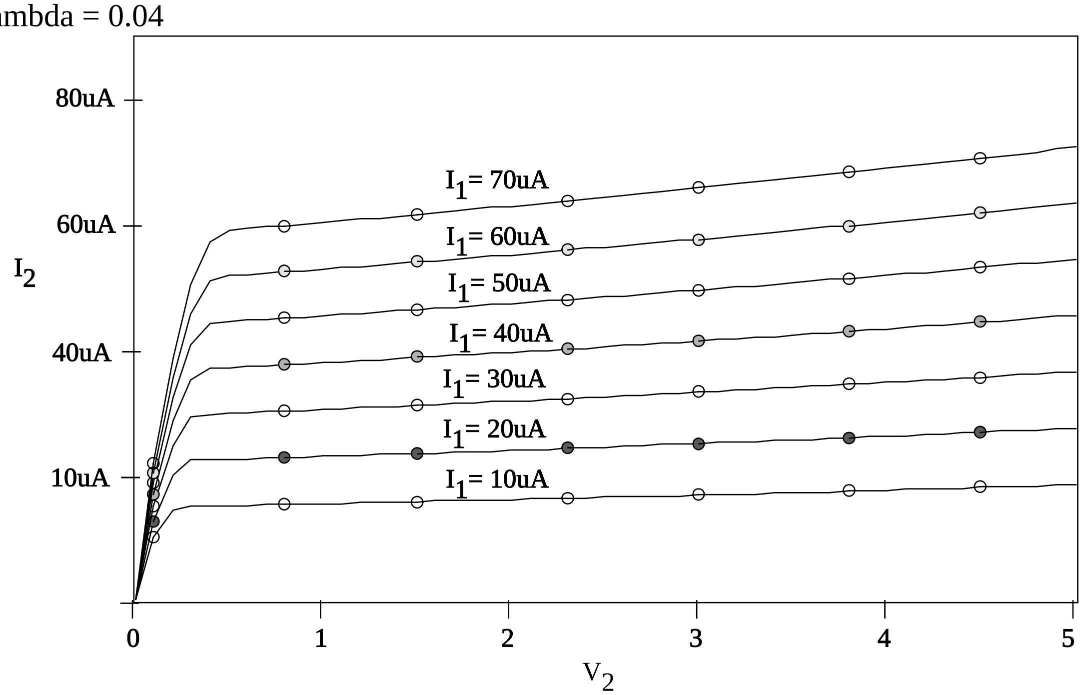
```
p3.6-3
M1 1  1  0  0 nch  l = 2u  w = 10u
M2 2  1  0  0 nch  l = 2u  w = 10u
I1 0  1 DC 0
V1 3  0 DC 0
V_I2 3  2 DC 0

.MODEL nch NMOS VTO=0.7 KP=110U  LAMBDA=0.01 GAMMA = 0.4 PHI = 0.7
*.MODEL nch NMOS VTO=0.7 KP=110U  LAMBDA=0.04 GAMMA = 0.4 PHI = 0.7
.dc V1 0 5 .1 I1 10u 80u 10u
.END
```

Lambda = 0.01



Lambda = 0.04

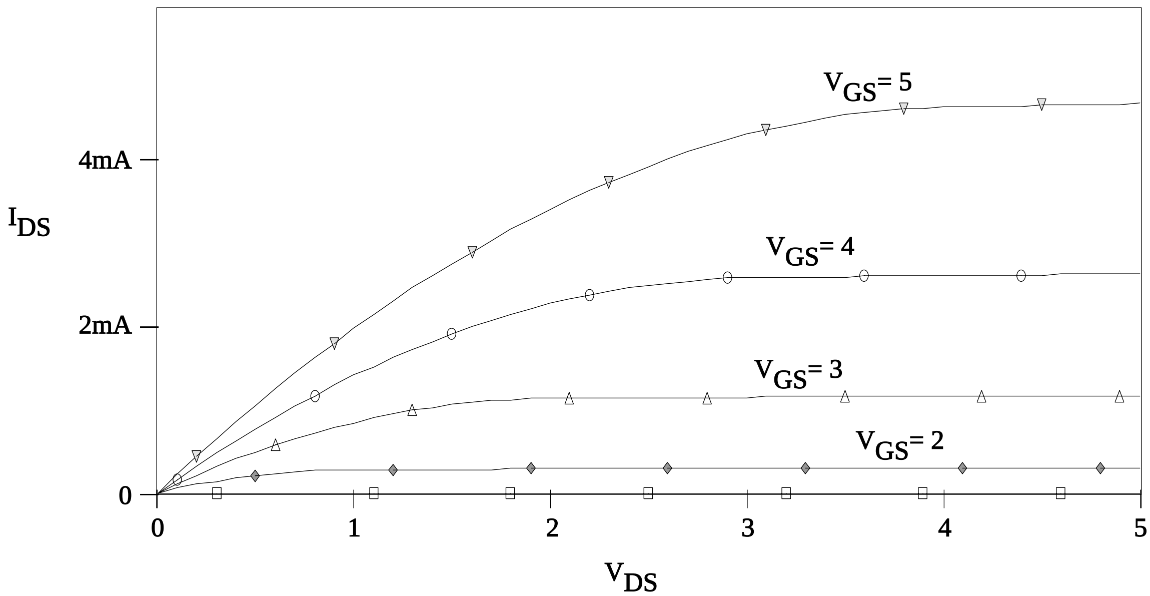


Problem 3.6-4

Use SPICE to plot i_D as a function of v_{DS} for values of v_{GS} = 1, 2, 3, 4 and 5 V for an n-channel transistor with V_T = 1 V, K' = 110 μA/V^2, and l = 0.04 V^{-1}. Show how SPICE can be used to generate and plot these curves simultaneously as illustrated by Fig. 3.1-3.

```
p3.6-4
M1 2  3  0  0 nch  l = 1u  w = 5u
```

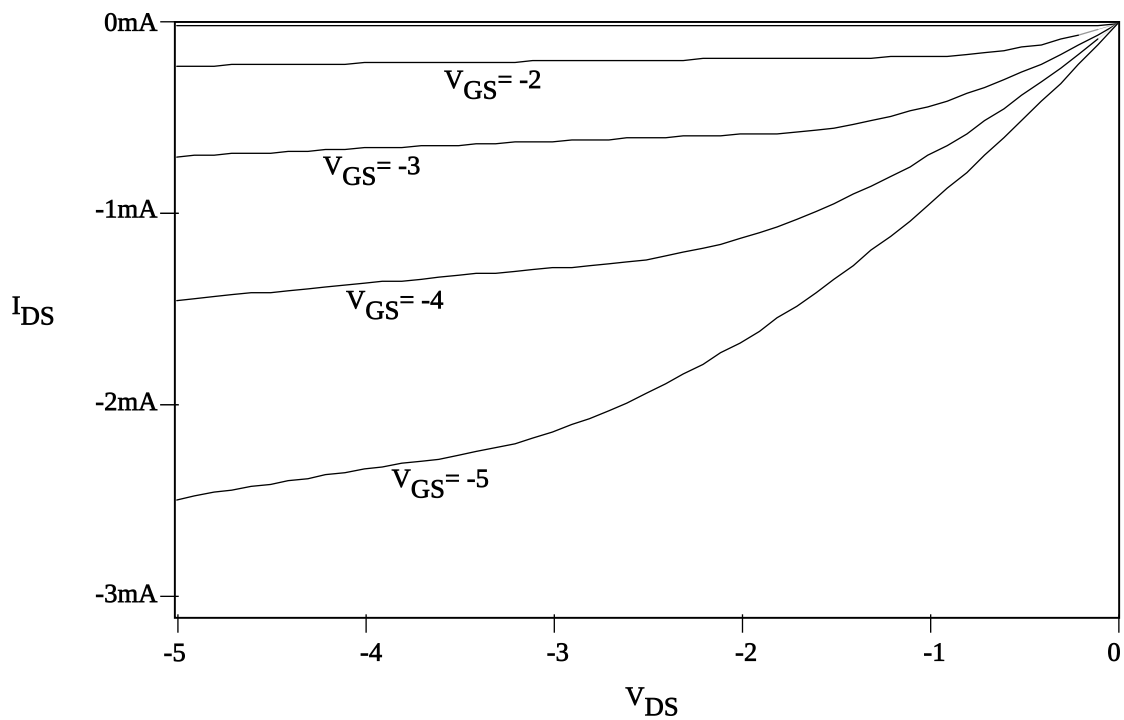
```
VGS 3  0 DC 0
VDS 4  0 DC 0
V_IDS 4  2 DC 0
.MODEL nch NMOS VTO=1 KP=110U  LAMBDA=0.01 GAMMA = 0.4 PHI = 0.7
.dc VDS 0 5 .1 VGS 0 5 1
.END
```



Problem 3.6-5

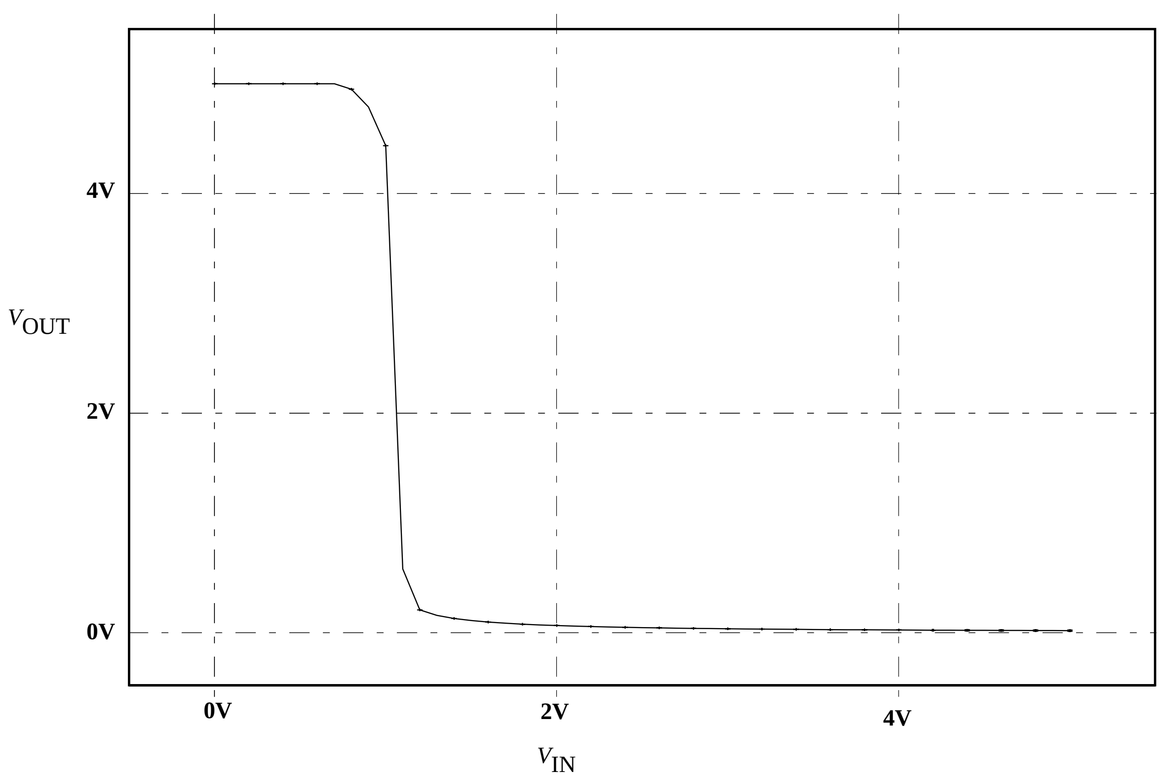
Repeat Example 3.6-1 if the transistor of Fig. 3.6-5 is a PMOS having the model parameters given in Table 3.1-2.

```
p3.6-5
V_IDS 5  2 DC 0
VGS 3  0 DC 0
VDS 5  0 DC 0
M1 2  3  0  0 pch  l = 1u  w = 5u
.MODEL pch PMOS VTO=-0.7   KP=50U  LAMBDA=0.051 GAMMA = 0.57 PHI = 0.8
.dc VDS 0 -5 -.1 VGS 0 -5 -1
.END
```

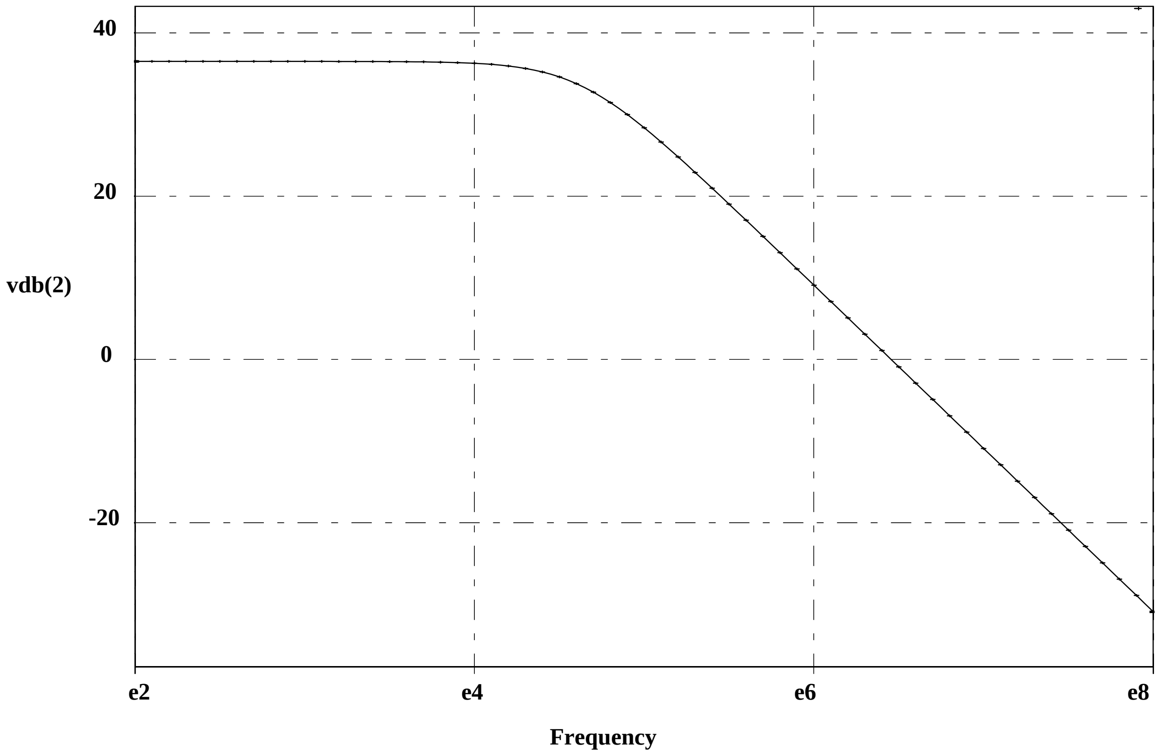


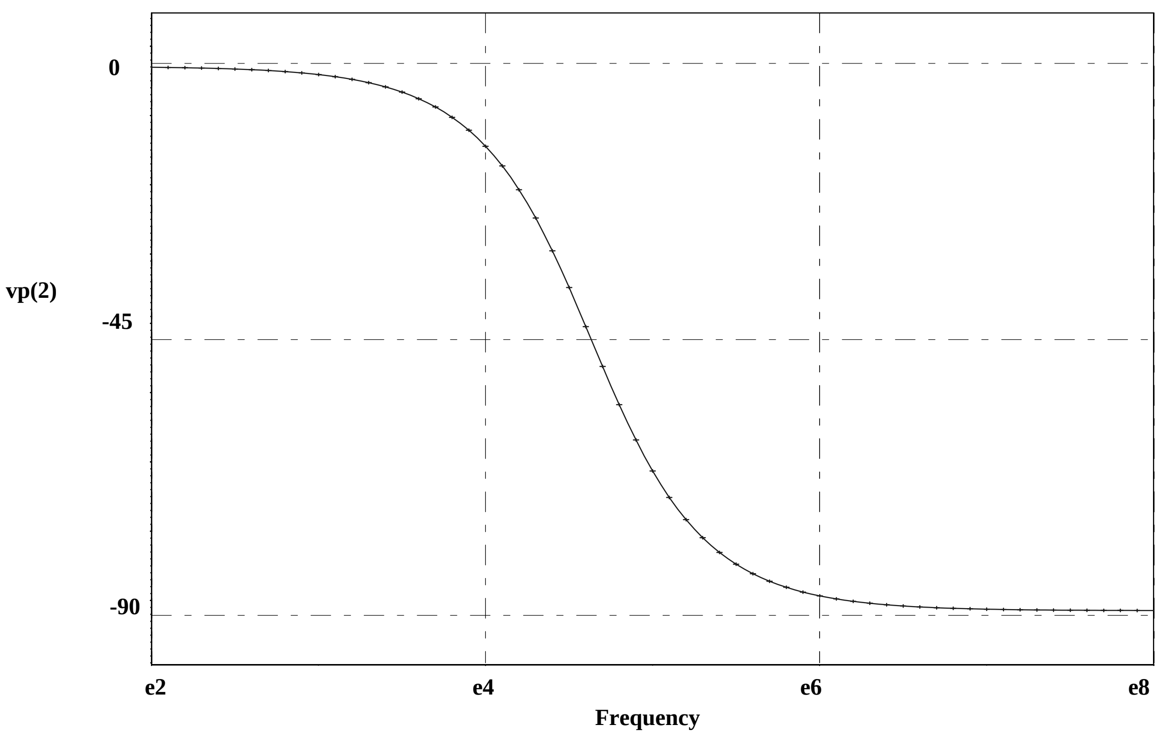
Problem 3.6-6

Repeat Examples 3.6-2 through 3.6-4 for the circuit of Fig. 3.6-2 if R1 = 200 KΩ.

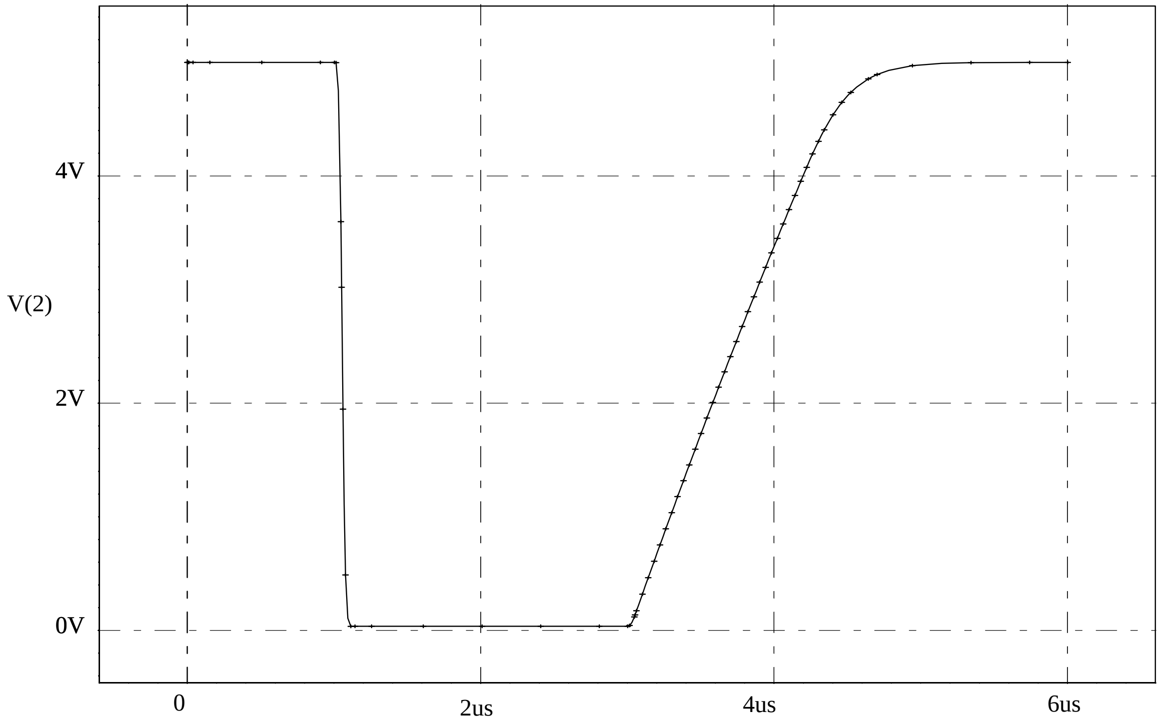


AC Analysis





Transient Analysis


4V
V(2)
2V
0V
0
2us
4us
6us

Chapter 4 Homework Solutions

Problem 4.1-1

Using SPICE, generate a set of parametric I-V curves similar to Fig. 4.1-3 for a transistor with a W/L = 10/1. Use model parameters from Table 3.1-2.

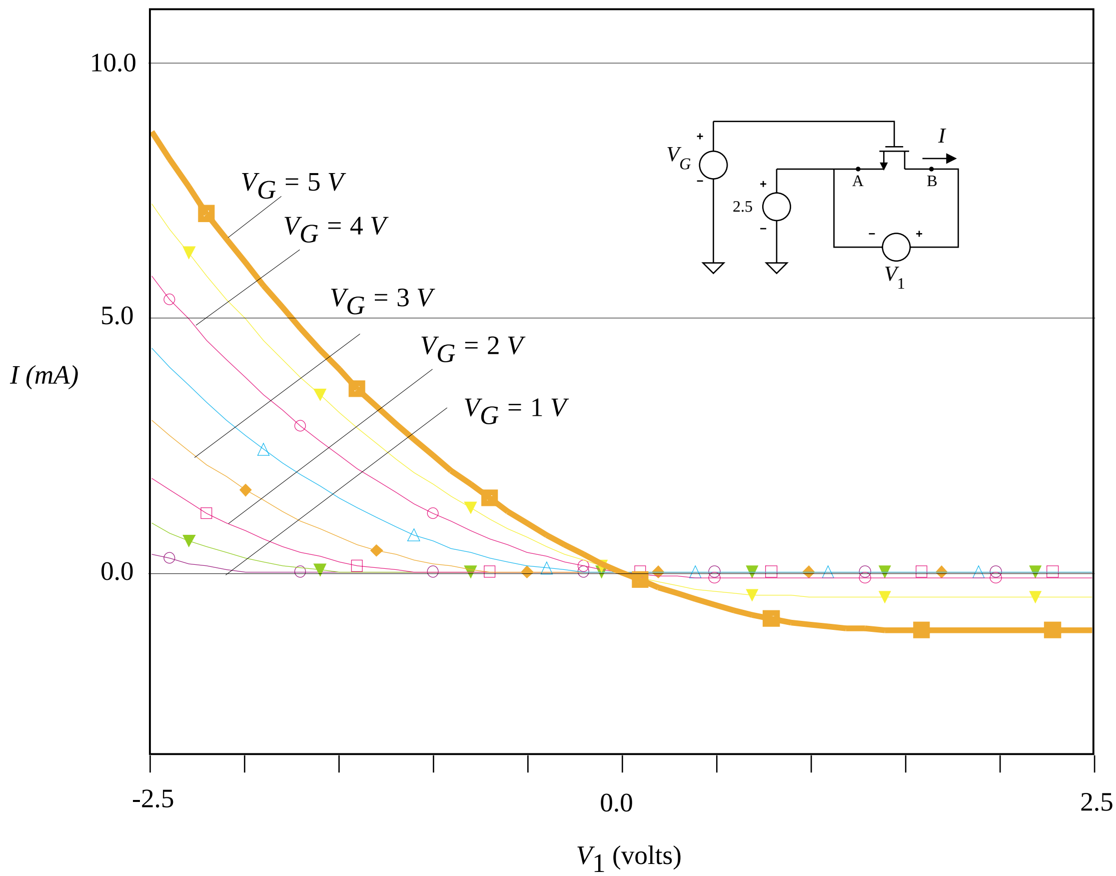


Figure P4.1-1

Problem 4.1-2

The circuit shown in Fig. P4.1-2 illustrates a single-channel MOS resistor with a W/L of 2µm/1µm. Using Table 3.1-2 model parameters, calculate the small-signal on resistance of the MOS transistor at various values for V_S and fill in the table below.

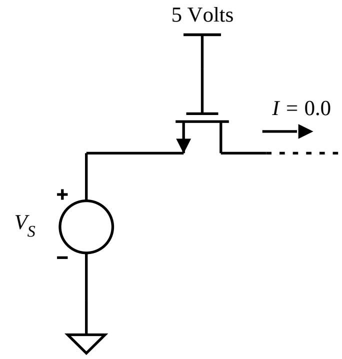


Figure P4.1-2

The equation for threshold voltage with absolute values so that it can be applied to n-channel or p-channel transistors without confusion.

$$|V_T| = |V_{T0}| + \gamma\left[\sqrt{2|\phi_F| + |v_{SB}|} - \sqrt{2|\phi_F|}\right]$$

$$r_{ON} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{L}{K'W(|V_{GS}| - |V_T|)} \text{ (when } V_{DS} = 0)$$

For n-channel device,

$$V_{T0} = 0.7$$

$$\gamma = 0.4$$

$$2|\phi_F| = 0.7$$

The table below shows the value of V_{GS} and V_{SB} for each value of V_S

V_S (volts)	V_{GS} (volts)	V_{SB} (volts)
0.0	5	0
1.0	4	1
2.0	3	2
3.0	2	3
4.0	1	4
5.0	0	5

Using $V_S = 0$, calculate V_T

$$|V_T| = |V_{T0}| + \gamma\left[\sqrt{2|\phi_F| + |v_{SB}|} - \sqrt{2|\phi_F|}\right] = 0.7 + 0.4[\sqrt{0.7 + 0.0} - \sqrt{0.7}] = 0.7$$

Calculate r_{on}

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{110\mu \times 2(5 - 0.7 - 0)} = 1057\ \Omega$$

Repeat for $V_S = 1$

$$|V_T| = 0.7 + 0.4[\sqrt{0.7 + 1.0} - \sqrt{0.7}] = 0.887$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{110\mu \times 2(4 - 0.887 - 0)} = 1460\ \Omega$$

Repeat for $V_S = 2$

$$|V_T| = 0.7 + 0.4[\sqrt{0.7 + 2.0} - \sqrt{0.7}] = 1.023$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{110\mu \times 2(3 - 1.023 - 0)} = 2299\ \Omega$$

Repeat for $V_S = 3$

$$|V_T| = 0.7 + 0.4[\sqrt{0.7 + 3.0} - \sqrt{0.7}] = 1.135$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{110\mu \times 2(2 - 1.135 - 0)} = 5253\ \Omega$$

Repeat for $V_S = 4$

$$|V_T| = 0.7 + 0.4[\sqrt{0.7 + 4.0} - \sqrt{0.7}] = 1.233$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{110\mu \times 2(1 - 1.233 - 0)} = -19549\ \Omega$$

The negative sign means that the device is off due to the fact that $V_{GS} < V_T$

Thus

$$r_{\mathrm{ON}} = \text{infinity}$$

Repeat for $V_S = 5$

$$|V_T| = 0.7 + 0.4[\sqrt{0.7+5.0} - \sqrt{0.7}] = 1.320$$

$$r_{ON} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{110\mu \times 2(0 - 1.320 - 0)} = -3442\ \Omega$$

The negative sign means that the device is off due to the fact that $V_{GS} < V_T$

Thus

$$r_{ON} = \text{infinity}$$

Summary:

V_S (volts)	R (ohms)
0.0	1057
1.0	1460
2.0	2299
3.0	5253
4.0	infinity
5.0	infinity

Problem 4.1-3

The circuit shown in Fig. P4.1-3 illustrates a single-channel MOS resistor with a W/L of 4µm/1µm. Using Table 3.1-2 model parameters, calculate the small-signal on resistance of the MOS transistor at various values for V_S and fill in the table below. Note that the most positive supply voltage is 5 volts.

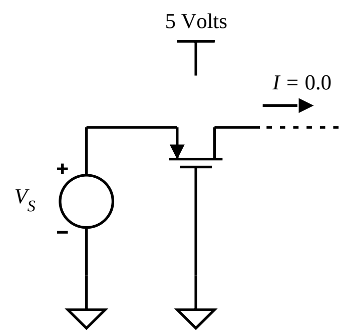


Figure P4.1-3

The equation for threshold voltage with absolute values so that it can be applied to n-channel or p-channel transistors without confusion.

$$|V_T| = |V_{T0}| + \gamma\left[\sqrt{2|\phi_F| + |v_{SB}|} - \sqrt{2|\phi_F|}\right]$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)}$$

For p-channel device,

$|V_{T0}| = 0.7$

K' = 50μ

$\gamma = 0.57$

$2|\phi_F| = 0.8$

The table below shows the value of V_{GS} and V_{SB} for each value of V_S

V_S (volts)	V_{GS} (volts)	V_{BS} (volts)
0.0	0	5
1.0	1	4
2.0	2	3
3.0	3	2
4.0	4	1
5.0	5	0

Using V_S = 5, calculate V_T

$$|V_T| = |V_{T0}| + \gamma\left[\sqrt{2|\phi_F| + |v_{SB}|} - \sqrt{2|\phi_F|}\right] = 0.7 + 0.57[\sqrt{0.8 + 0.0} - \sqrt{0.8}] = 0.7$$

Calculate r_{on}

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{50\mu \times 4(5 - 0.7 - 0)} = 1163\ \Omega$$

Repeat for $V_S = 4$

$$|V_T| = 0.7 + 0.57[\sqrt{0.8 + 1.0} - \sqrt{0.8}] = 0.955$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{50\mu \times 4(4 - 0.955 - 0)} = 1642\ \Omega$$

Repeat for $V_S = 3$

$$|V_T| = 0.7 + 0.57[\sqrt{0.8 + 2.0} - \sqrt{0.8}] = 1.144$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{50\mu \times 4(3 - 1.144 - 0)} = 2694\ \Omega$$

Repeat for $V_S = 2$

$$|V_T| = 0.7 + 0.4[\sqrt{0.8 + 3.0} - \sqrt{0.8}] = 1.301$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{50\mu \times 4(2 - 1.301 - 0)} = 7145\ \Omega$$

Repeat for $V_S = 1$

$$|V_T| = 0.7 + 0.57[\sqrt{0.8 + 4.0} - \sqrt{0.8}] = 1.439$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{50\mu \times 4(1 - 1.439 - 0)} = -11390\ \Omega$$

The negative sign means that the device is off due to the fact that $V_{GS} < V_T$

Thus

$$r_{\mathrm{ON}} = \text{infinity}$$

Repeat for $V_S = 0$

$$|V_T| = 0.7 + 0.57[\sqrt{0.8 + 5.0} - \sqrt{0.8}] = 1.563$$

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{1}{50\mu \times 4(0 - 1.563 - 0)} = 3199\ \Omega$$

The negative sign means that the device is off due to the fact that $V_{GS} < V_T$

Thus

$$r_{\mathrm{ON}} = \text{infinity}$$

Summary:

V_S (volts)	R (ohms)
0.0	infinity
1.0	infinity
2.0	7145
3.0	2694
4.0	1642
5.0	1163

Problem 4.1-4

The circuit shown in Fig. P4.3 illustrates a complementary MOS resistor with an n-channel W/L of 2µm/1µm and a p-channel W/L of 4µm/1µm. Using Table 3.1-2 model parameters, calculate the small-signal on resistance of the complementary MOS resistor at various values for V_S and fill in the table below. Note that the most positive supply voltage is 5 volts.

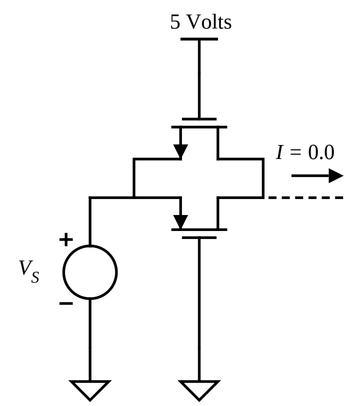


Figure P4.3

Summary for n-channel device from Problem 4.1-2:

V_S (volts)	R (ohms)
0.0	1057
1.0	1460
2.0	2299
3.0	5253
4.0	infinity
5.0	infinity

Summary for p-channel device from Problem 4.1-3:

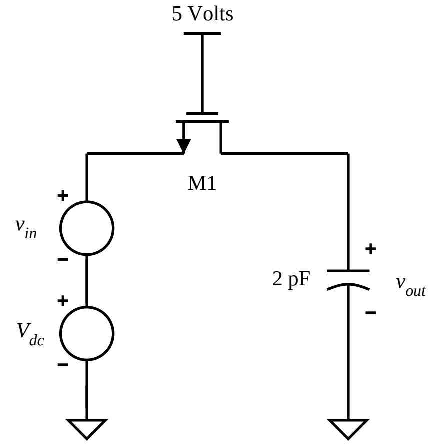
V_S (volts)	R (ohms)
0.0	infinity
1.0	infinity
2.0	7145
3.0	2694
4.0	1642
5.0	1163

Table showing both and their parallel combination:

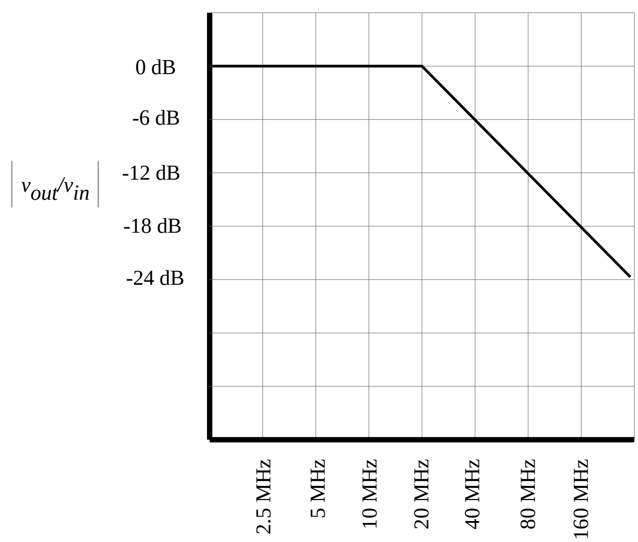
V_S (volts)	R (ohms), n-channel	R (ohms), p-channel	R (ohms), parallel
0.0	1057	infinity	1057
1.0	1460	infinity	1460
2.0	2299	7145	1739
3.0	5253	2694	1781
4.0	infinity	1642	1642
5.0	infinity	1163	1163

Problem 4.1-5

For the circuit in Figure P4.1-5(a) assume that there are NO capacitance parasitics associated with M1. The voltage source v_{in} is a small-signal value whereas voltage source V_{dc} has a dc value of 3 volts. Design M1 to achieve the frequency response shown in Figure P4.1-5(b).



(a)



(b)

Figure P4.4

f(-3 dB) = 20 MHz, thus w = 40π M rad/s
Note that since no dc current flows through the transistor, the dc value of the drain-source voltage is zero.

$$r_{\mathrm{ON}} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{L}{K'W(|V_{GS}| - |V_T|)}$$

Then

$$\frac{1}{\mathrm{RC}} = \frac{K'W(|V_{GS}| - |V_T|)}{\mathrm{LC}} = 40\ \pi\ \mathrm{M\ rad/s}$$

$$\frac{W}{L} = \frac{C \times 40\ \pi\ \times 10^{6}}{K'(|V_{GS}| - |V_T|)}$$

Calculate VT due to the back bias.

$$V_T\ = V_{T0} + \gamma\left(\sqrt{|2\phi_f| + |v_{bs}|}\ - \sqrt{|2\phi_f|}\right) = 0.7 + 0.4\left(\sqrt{0.7 + 3.0}\ - \sqrt{0.7}\right) = 1.135$$

$$\frac{W}{L} = \frac{40\ \pi \times 10^{6}\ \times\ 2 \times 10^{-12}}{110 \times 10^{-6}\ (2 - 1.135)} = 2.64$$

Problem 4.1-6

Using the result of Problem 4, calculate the frequency response resulting from changing the gate voltage of M1 to 4.5 volts. Draw a Bode diagram of the resulting frequency response.

$$r_{ON} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T| - |V_{DS}|)} = \frac{L}{K'W(|V_{GS}| - |V_T|)}$$

Calculate VT due to the back bias (same as previous problem).

$$V_T\ = V_{T0} + \gamma\left(\sqrt{|2\phi_f| + |v_{bs}|}\ - \sqrt{|2\phi_f|}\right) = 0.7 + 0.4\left(\sqrt{0.7 + 3.0}\ - \sqrt{0.7}\right) = 1.135$$

$$r_{ON} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{K'W(|V_{GS}| - |V_T|)}$$

$$r_{ON}\ = \frac{1}{110 \times 10^{-6} \times 2.64(4.5 - 3 - 1.135)} == 9434\ \Omega$$

$$\omega(\text{-3 } dB) = \frac{1}{r_{ON}C} = \frac{1}{9.434 \times 10^{3} \times 2 \times 10^{-12}}\ =\ 53 \times 10^{6}\ \text{ rad/s}$$

$$f(\text{-3 } dB) =\ 8.44 \times 10^{6}\ \text{ Hz}$$

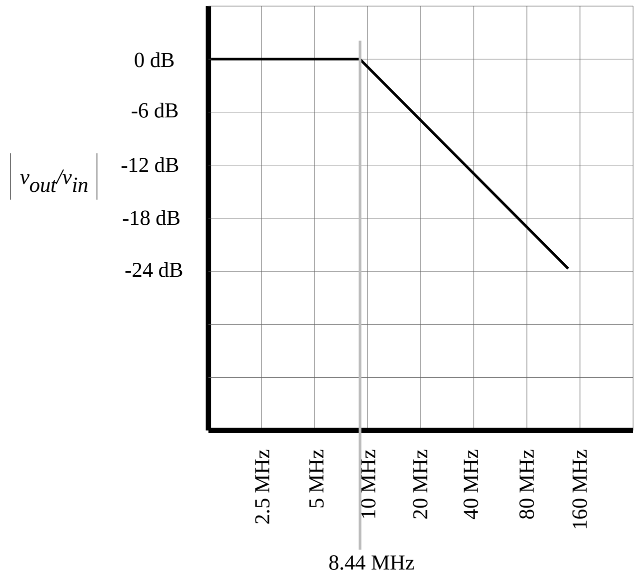


Figure P4.1-6

Problem 4.1-7

Consider the circuit shown in Fig. P4.1-7 Assume that the *slow regime* of charge injection is valid for this circuit. Initially, the charge on C_1 is zero. Calculate v_{OUT} at time t_1 after ϕ_1 pulse occurs. Assume that CGS0 and CGD0 are both 5 fF. C_1=30 fF. You cannot ignore body effect. L = 1.0 μm and W = 5.0 μm.

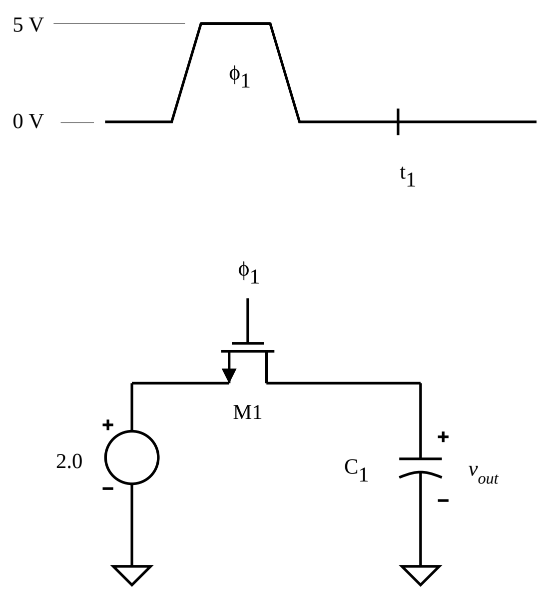


Figure P4.1-7

CHANGE PROBLEM:

Use model parameters from Table 3.1-2 and 3.2-1 as required

$U = 5 \times 10^8$

The equation for the slow regime is given as

$$V_{error} = \left(\frac{W \cdot \mathrm{CGD0} + \frac{C_{channel}}{2}}{C_L} \right) \sqrt{\frac{\pi U C_L}{2\beta}} + \frac{W \cdot \mathrm{CGD0}}{C_L} (V_S + V_T - V_L)$$

and

$V_S = 2.0$ volts

$V_L = 0.0$ volts

V_T is calculated below

The source of the transistor is at 2.0 volts, so the threshold for the switch must be calculated with a back-gate bias of 2.0 volts.

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_f| + |v_{bs}|} - \sqrt{|2\phi_f|}\right) = 0.7 + 0.4\left(\sqrt{0.7 + 2.0} - \sqrt{0.7}\right) = 1.023$$

$V_T = 1.023$

$$C_{channel} = W \times L \times C_{ox} = 5 \times 10^{-6} \times 1 \times 10^{-6} \times 24.7 \times 10^{-4} = 12.35 \times 10^{-15}\ \mathrm{F}$$

$$V_{HT} = V_H - V_S - V_T = 5 - 2 - 1.023 = 1.98$$

Verify slow regime:

$$\frac{\beta V_{HT}^2}{2C_L} = \frac{110 \times 10^{-6} \times 3.91}{2 \times 30 \times 10^{-15}} = 7.17 \times 10^9 >> 5 \times 10^8 \text{ thus slow regime}$$

$$V_{error} = \left(\frac{W \cdot \mathrm{CGD0} + \frac{C_{channel}}{2}}{C_L} \right) \sqrt{\frac{\pi U C_L}{2\beta}} + \frac{W \cdot \mathrm{CGD0}}{C_L} (V_S + V_T - V_L)$$

$$V_{error} = \left(\frac{5 \times 10^{-6} \times 220 \times 10^{-12} + \frac{12.35 \times 10^{-15}}{2}}{30 \times 10^{-15}} \right) \times$$

$$\times\sqrt{\frac{\pi\times 5\times 10^{8}\times 30\times 10^{-15}}{2\times 110\times 10^{-6}}}+\frac{5\times 10^{-6}\cdot 220\times 10^{-12}}{30\times 10^{-15}}(2+1.023-0)=0.223$$

$V_{out}(\mathrm{t1}) = 2.0 - V_{error} = 2.0 - 0.223 = 1.777$

Problem 4.1-8

In Problem 4.1-7, how long must ϕ_1 remain high for C_1 to charge up to 99% of the desired final value (2.0 volts)?

$$r_{\mathrm{ON}}=\frac{1}{\partial I_D/\partial V_{DS}}=\frac{L}{K'W(|V_{GS}|-|V_T|)}$$

$$r_{\mathrm{ON}}=\frac{1}{5\times 110\times 10^{-6}\times(3-1.135)}=972.3\ \Omega$$

$$r_{\mathrm{ON}}\,C_1 = 972.3\times 30\times 10^{-15} = 29.2\text{ ps}$$

$$v_{\mathrm{O}}(\mathrm{t})\,C_1 = 2\times(\ 1-\mathrm{e}^{-t/RC}\ ) = 0.99\times 2.0$$

$$\mathrm{e}^{-t/RC}\ ) = 0.01$$

$$t = -\mathrm{RC}\ln(0.01) = 134.3\text{ ps}$$

Problem 4.1-9

In Problem 4.1-7, the charge feedthrough could be reduced by reducing the size of M1. What impact does reducing the size (W/L) of M1 have on the requirements on the width of the ϕ_1 pulse width?

The width of ϕ_1 must increase since a decrease in size (and thus feedthrough) increases resistance and thus the time required to charge the capacitor to the desired final value.

Problem 4.1-10

Considering charge feedthrough due to slow regime only, will reducing the magnitude of the ϕ_1 pulse impact the resulting charge feedthrough? What impact does reducing the magnitude of the ϕ_1 pulse have on the accuracy of the voltage transfer to the output?

Reducing the magnitude does not effect the result of feedthrough in the slow regime because all of the charge except residual channel charge (at the point where the device turns off) returns to the voltage source. Decreasing the magnitude does effect the accuracy because the time required to charge the capacitor is increased due to higher resistance when the device is on.

Problem 4.1-11

Repeat Example 4.1-1 with the following conditions. Calculate the effect of charge feedthrough on the circuit shown in Fig. 4.1-9 where V_S = 1.5 volts, C_L = 150 fF, W/L = 1.6µm/0.8µm, and V_G is given for two cases illustrated below. The fall time is 0.1ns instead of 8ns.

Case 1: 0.1ns fall time

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_f| + |v_{bs}|} - \sqrt{|2\phi_f|}\right) = 0.7 + 0.4\left(\sqrt{0.7 + 1.5} - \sqrt{0.7}\right) = 0.959$$

$$V_{HT} = V_H - V_S - V_T = 5 - 1.5 - 0.959 = 2.541$$

$$U = \frac{V_H}{t} = \frac{5}{0.1 \times 10^{-9}} = 50 \times 10^9$$

$$\frac{\beta V_{HT}^2}{2C_L} = \frac{2{\times}110 \times 10^{-6} \times 2.541^2}{2 \times 150 \times 10^{-15}} = 4.735 \times 10^9 << 50 \times 10^9 \text{ thus fast mode}$$

$$C_{channel} = W \times L \times C_{ox} = 1.6 \times 10^{-6} \times 0.8 \times 10^{-6} \times 24.7 \times 10^{-4} = 3.162 \times 10^{-15}\ \mathrm{F}$$

$$V_{error} = \left(\frac{W{\cdot}\mathrm{CGD0} + \frac{C_{channel}}{2}}{C_L}\right)\left(V_{HT} - \frac{\beta V_{HT}^3}{6U\, C_L}\right) + \frac{W{\cdot}\mathrm{CGD0}}{C_L}\left(V_S + V_T - V_L\right)$$

$$V_{error} = \left(\frac{1.6 \times 10^{-6} \times 220 \times 10^{-12} + \frac{3.162 \times 10^{-15}}{2}}{150 \times 10^{-15}}\right)\left(2.541 - \frac{220 \times 10^{-6} \times 2.541^3}{6{\times}50 \times 10^9 \times 150 \times 10^{-15}}\right) +$$

$$+ \frac{1.6 \times 10^{-6} \times{\cdot}220 \times 10^{-12}}{150 \times 10^{-15}}(1.5 + 0.96 - 0)$$

$$V_{error} = (12.89 \times 10^{-3})\,(2.46) + 1.267 \times 10^{-3} = 32.98 \times 10^{-3}$$

$$V_{out}(\mathrm{t1}) = 2.0 - V_{error} = 2.0 - 32.98 \times 10^{-3} = 1.967$$

Case 2: 8ns fall time

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_f| + |v_{bs}|} - \sqrt{|2\phi_f|}\right) = 0.7 + 0.4\left(\sqrt{0.7 + 1.5} - \sqrt{0.7}\right) = 0.959$$

$$V_{HT} = V_H - V_S - V_T = 5 - 1.5 - 0.959 = 2.541$$

$$v_G = V_H - Ut$$

$$U = \frac{V_H}{t} = \frac{5}{8 \times 10^{-9}} = 625 \times 10^6$$

$$\frac{\beta V_{HT}^2}{2C_L} = \frac{2 \times 110 \times 10^{-6} \times 6.457}{2 \times 150 \times 10^{-15}} = 4.735 \times 10^9 >> 625 \times 10^6 \text{ thus slow regime}$$

$$V_{error} = \left(\frac{W \cdot \text{CGD0} + \frac{C_{channel}}{2}}{C_L}\right)\sqrt{\frac{\pi U C_L}{2\beta}} + \frac{W \cdot \text{CGD0}}{C_L}(V_S + V_T - V_L)$$

and

$V_S = 1.5$ volts

$V_L = 0.0$ volts

$$C_{channel} = W \times L \times C_{ox} = 1.6 \times 10^{-6} \times 0.8 \times 10^{-6} \times 24.7 \times 10^{-4} = 3.162 \times 10^{-15} \text{ F}$$

$$V_{error} = \left(\frac{W \cdot \text{CGD0} + \frac{C_{channel}}{2}}{C_L}\right)\sqrt{\frac{\pi U C_L}{2\beta}} + \frac{W \cdot \text{CGD0}}{C_L}(V_S + V_T - V_L)$$

$$V_{error} = \left(\frac{1.6 \times 10^{-6} \times 220 \times 10^{-12} + \frac{3.162 \times 10^{-15}}{2}}{150 \times 10^{-15}}\right) \times$$

Error!

$$V_{out}(\text{t1}) = 2.0 - V_{error} = 2.0 - 0.0163 = 1.984$$

Problem 4.1-12

Figure P4.1-12 illustrates a circuit that contains a charge-cancellation scheme. Design the size of M2 to minimize the effects of charge feedthrough. Assume slow regime.

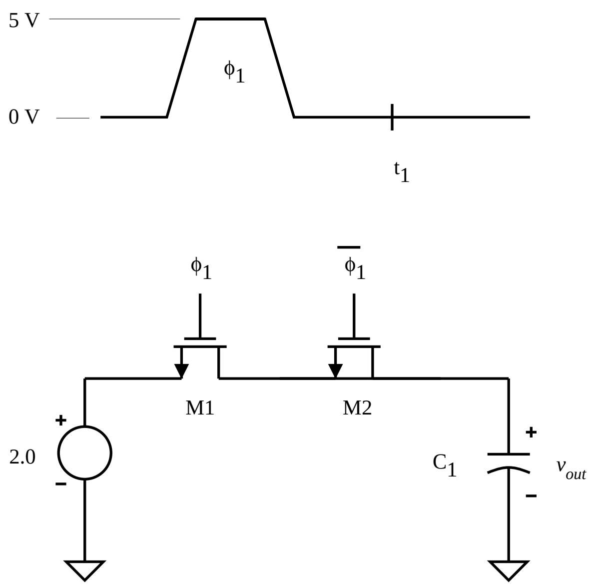


Figure P4.1-12

When U is small, the expression for the charge feedthrough due to M1 in the slow regime can be approximated as

$$V_{error} = \left(\frac{W \cdot \text{CGD0} + \frac{C_{channel}}{2}}{C_L}\right)\sqrt{\frac{\pi U C_L}{2\beta}} + \frac{W \cdot \text{CGD0}}{C_L}(V_S + V_T - V_L)$$

$$V_{error} \cong \frac{W \cdot \text{CGD0}}{C_L}(V_S + V_T - V_L)$$

Because M2 is driven by the inversion of ϕ_1 , charge is injected in the opposite direction from that of M1. The charge injected is due to the overlap capacitance and due to the channel capacitance. The overlap capacitance from the drain or source is simply

$$C_{overlap} = W \cdot \text{CGD0}$$

Because both the drain and the source are involved, the charge injected from both must be added.

Capacitance due to the channel once M2 channel inverts is simply

$C_{channel} = W \cdot L \cdot C_{ox}$

Consider the voltage on C_1 due to charge injected from the overlap and the channel separately.

The error voltage due to overlap is approximated to be

$$V_{error\_overlap} \cong \frac{2 \cdot W \cdot \mathrm{CGD0}}{C_L}(V_S + V_T - V_L)$$

Notice the factor of "2" to account for the overlap from the drain and the source.

The error voltage due to the channel is approximated to be

$$V_{error\_channel} \cong \frac{C_{channel}}{C_L}(5 - V_S - V_T)$$

where the "5" comes from the maximum value of $\overline{\phi_1}$.

If V_L is zero, then the total error voltage due to M2 alone is approximately

$$V_{error\_M2} \cong \frac{2 \cdot W_2 \cdot \mathrm{CGD0}}{C_L}(V_S + V_T) + \frac{C_{channel}}{C_L}(5 - V_S - V_T)$$

Since the error voltage due to M2 is in the opposite direction to that due to M1 then to minimize the overall effect due to charge injection, the error due to M1 and M2 should be made equal. Therefore

$$\frac{W_1 \cdot \mathrm{CGD0}}{C_L}(V_S + V_T) = \frac{2 \cdot W_2 \cdot \mathrm{CGD0}}{C_L}(V_S + V_T) + \frac{C_{channel}}{C_L}(5 - V_S - V_T)$$

$$(W_1 \cdot \mathrm{CGD0})(V_S + V_T) = (2 \cdot W_2 \cdot \mathrm{CGD0})(V_S + V_T) + C_{channel\_M2}(5 - V_S - V_T)$$

$$(W_1 \cdot \mathrm{CGD0})(V_S + V_T) = (2 \cdot W_2 \cdot \mathrm{CGD0})(V_S + V_T) + W_2 L_2 C_{OX}(5 - V_S - V_T)$$

$$W_1 = 2 \cdot W_2 + \frac{W_2 L_2 C_{OX}(5 - V_S - V_T)}{\mathrm{CGD0}(V_S + V_T)}$$

$$W_1 = W_2\left(2 + \frac{L_2 C_{OX}(5 - V_S - V_T)}{\mathrm{CGD0}(V_S + V_T)}\right)$$

$$W_2 = W_1 \left(2 + \frac{L_2 C_{OX} (5 - V_S - V_T)}{\text{CGD0}\,(V_S + V_T)} \right)^{-1}$$

Design L_2 to be the minimum allowed device length and calculate W_2.

Problem 4.3-1

Figure P4.3-1 illustrates a source-degenerated current source. Using Table 3.1-2 model parameters calculate the output resistance at the given current bias.

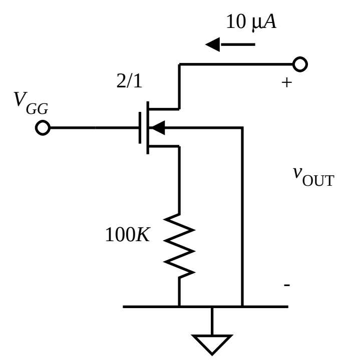
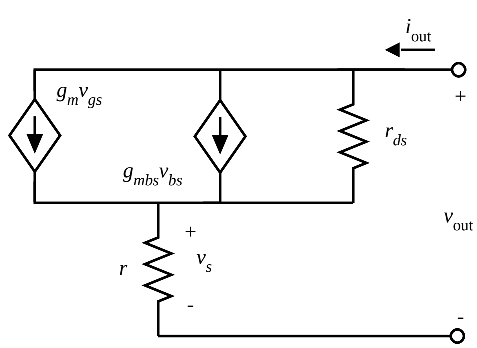


Figure P4.3-1

The small-signal model of this circuit is shown below



First calculate dc terminal conditions.

$I_D = 10\ \mu\text{A}$

$V_S = I_D \times \text{R} = 10 \times 10^{-6} \times 100 \times 10^{3} = 1$ volt

$V_S = V_{SB}$

$$r_{\text{out}} = \frac{v_{\text{out}}}{i_{\text{out}}} = r + r_{ds} + [(g_m + g_{mbs})r_{ds}]r \cong (g_m r_{ds})r$$

$$g_m \cong \sqrt{(2K'W/L)|I_D|} = \sqrt{2\times 110\times10^{-6} \times 2/1 \times 10\times10^{-6}} = 66.3 \times10^{-6}$$

$$g_{mbs} = g_m \frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}} = 66.3\times10^{-6} \frac{0.4}{2(0.7 + 1)^{1/2}} = 10.17\times10^{-6}$$

$$g_{ds} \cong I_D\, \lambda = 10\times10^{-6} \times 0.04 = 400\times10^{-9}$$

$$r_{ds} = \frac{1}{g_{ds}} = 2.5\times10^{6}$$

thus

$$r_{\text{out}} = 100 \times 10^{3} + 2.5\times10^{6} + [(66.3 \times10^{-6} + 10.17\times10^{-6})\ 2.5\times10^{6}]\ 100 \times 10^{3} = 21.7\times10^{6}$$

$$r_{\text{out}} = 21.7\times10^{6}$$

Problem 4.3-2

Calculate the minimum output voltage required to keep device in saturation in Problem 4.3-1.

The minimum voltage across drain and source while remaining in saturation is V_{ON}

$$V_{ON} = \sqrt{\frac{2i_D}{\beta}} = \sqrt{\frac{2 \times 10 \times10^{-6}}{2 \times 110 \times10^{-6}}} = \sqrt{\frac{10}{110}} = 0.302$$

The minimum drain voltage is

$V_{D(min)} = V_{S(min)} + V_{ON} = 1 + 0.302 = 1.302$

Problem 4.3-3

Using the cascode circuit shown in Fig. P4.3-3, design the W/L of M1 to achieve the same output resistance as the circuit in Fig. P4.3-1. Ignore body effect.

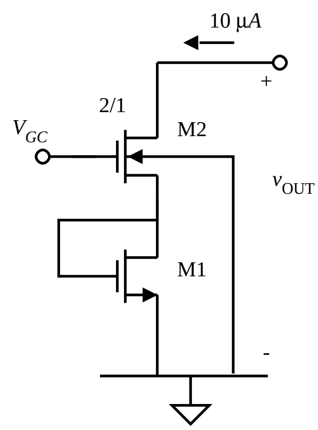


Figure P4.3-3

$$r_{DS1} = \frac{1}{g_{m1}}$$

$$\frac{1}{g_m} = 100\ \text{k}\Omega$$

$$g_{m1} = \frac{1}{100\ \text{k}\Omega} \cong \sqrt{2K'(W/L)_1 I_D} = \sqrt{2\times 110\times10^{-6} \times 10\times10^{-6}}\,\sqrt{(\text{W/L})_1}$$

$$\left(\frac{\text{W}}{\text{L}}\right)_1 = \left(\frac{10^{-5}}{\sqrt{2\times 110\times10^{-6} \times 10\times10^{-6}}}\right)^2 = \frac{1}{22}$$

From the previous problem,

$$g_{m2} = 66.3 \times10^{-6}$$

$$r_{ds2} = 2.5\times10^{6}$$

Note that the terminal conditions of M2 must change in order to support the larger gate voltage required on M1. This will be addressed in the next problem.

Problem 4.3-4

Calculate the minimum output voltage required to keep device in saturation in Problem 4.3-3. Compare this result with that of Problem 4.3-2. Which circuit is a better choice in most cases?

First calculate the gate voltage of M1

$$V_{GS1} = \sqrt{\frac{2I_D}{K'(W/L)}} + V_T = \sqrt{\frac{20\ \mu}{110\ \mu\ (1/22)}} + 0.7 = 2.7$$

From Problem 4.3-2, V_{ON2} = 0.302

Therefore, the minimum output voltage to keep devices in saturation is

$V_{\text{out}}(min) = V_{GS1} + V_{ON2} = 2.7 + .302 = 3.02$

In for the circuit in problem 4.3-2, the minimum output voltage is lower than the circuit in 4.3-3 and is thus generally a better choice.

Problem 4.3-5

Calculate the output resistance and the minimum output voltage, while maintaining all devices in saturation, for the circuit shown in Fig. P4.3-5. Assume that I_{OUT} is actually 10µA. Simulate this circuit using SPICE LEVEL 3 model (Table 3.4-1) and determine the actual output current, I_{OUT}. Use Table 3.1-2 for device model information.

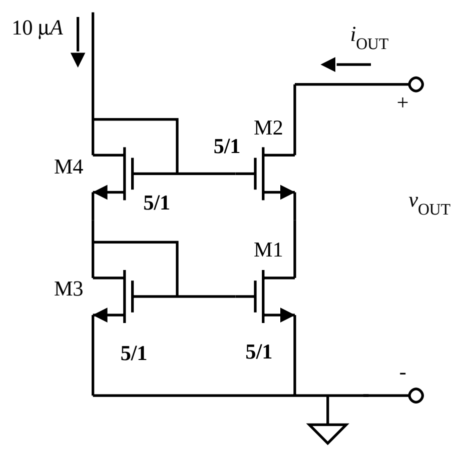


Figure P4.3-5

First calculate node voltages and currents.

Assume a near perfect current mirror so that the current in all devices is 10 µA.

Calculate node voltages.

$$V_{GS3} = V_{G3} = \sqrt{\frac{2i_D}{\beta}} + V_T = \sqrt{\frac{2 \times 10 \times 10^{-6}}{5 \times 110 \times 10^{-6}}} + 0.7 = \sqrt{\frac{20}{550}} + 0.7 = 0.891$$

$V_{SB2} = V_{G3} = 0.891$

$V_{DS1} = V_{G3} + V_{GS4} - V_{GS2}$ because all devices are matched.

$g_{m2} = g_{m4} \cong \sqrt{(2K'W/L)|I_D|} = \sqrt{2\times 110\times10^{-6} \times5/1 \times 10\times10^{-6}} = 104.9 \times10^{-6}$

$g_{mbs2} = g_{mbs4} = g_{m2} \dfrac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}} = 104.9 \times10^{-6} \dfrac{0.4}{2(0.7 + 0.891)^{1/2}} = 16.63\times10^{-6}$

$r_{out} = \dfrac{v_{out}}{i_{out}} = r_{ds1} + r_{ds2} + [(g_{m2} + g_{mbs2})r_{ds2}]\, r_{ds1}$

$g_{ds1} = g_{ds2} \cong I_D\, \lambda = 10\times10^{-6} \times 0.04 = 400\times10^{-9}$

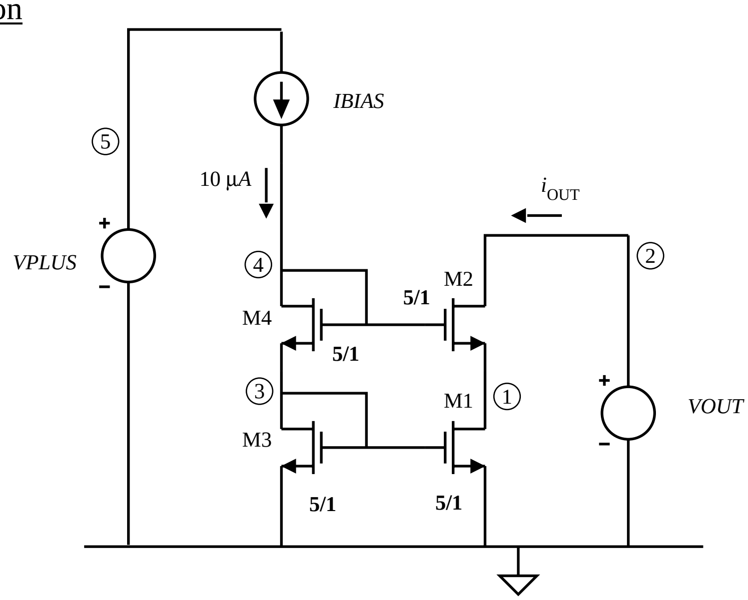
$r_{ds1} = r_{ds2} = \dfrac{1}{g_{ds}} = 2.5\times10^{6}$

$r_{out} = r_{ds1} + r_{ds2} + [(g_{m2} + g_{mbs2})r_{ds2}]\, r_{ds1} = 2.5\times10^{6} + 2.5\times10^{6}$

$r_{out} = 2.5\times10^{6} + 2.5\times10^{6} + [(104.9 \times10^{-6} + 16.63\times10^{-6})\, 2.5\times10^{6}]\, 2.5\times10^{6}$

$r_{out} = 764\times10^{6}$

Spice Simulation



Spice simulation circuit

```
Problem 4.3-5
M4 4 4 3 0 nch w=5u l=1u
M3 3 3 0 0 nch w=5u l=1u
M2 2 4 1 0 nch w=5u l=1u
```

```
m1 1 3 0 0 nch w=5u l=1u
ibias 5 4 10u
vplus 5 0 5
vout 2 0 3
.op
.model nch  NMOS
+ LEVEL        =            3
+ VTO          =         0.70
+ UO           =          660
+ TOX          =     1.40E-08
+ NSUB         =        3E+16
+ XJ           =       2.0e-7
+ LD           =      1.6E-08
+ NFS          =        7e+11
+ VMAX         =        1.8e5
+ DELTA        =         2.40
+ ETA          =          0.1
+ KAPPA        =         0.15
+ THETA        =          0.1
+ CGDO         =     2.20E-10
+ CGSO         =     2.20E-10
+ CGBO         =     7.00E-10
+ MJ           =         0.50
+ CJSW         =     3.50E-10
+ MJSW         =         0.38

.model pch  PMOS
+ LEVEL        =            3
+ VTO          =        -0.70
+ UO           =          210
+ TOX          =     1.40E-08
+ NSUB         =      6.00e16
+ XJ           =       2.0e-7
+ LD           =      1.5E-08
+ NFS          =        6E+11
+ VMAX         =       2.00e5
+ DELTA        =         1.25
+ ETA          =          0.1
+ KAPPA        =          2.5
+ THETA        =          0.1
+ CGDO         =     2.20E-10
+ CGSO         =     2.20E-10
+ CGBO         =     7.00E-10
+ MJ           =         0.50
.end

                  DC Operating Point Analysis, 27 deg C
                        Fri Aug 30 23:00:34 2002
-----------------------------------------------------------------------
                 >>>    i(vout)  = -1.0157e-005
                        i(vplus) = -1.0000e-005
                        v(0)     =  0.0000e+000
                        v(1)     =  8.5259e-001
                        v(2)     =  3.0000e+000
                        v(3)     =  8.1511e-001
                        v(4)     =  1.7609e+000
                        v(5)     =  5.0000e+000
```

Problem 4.3-6

Calculate the output resistance, and the minimum output voltage, while maintaining all devices in saturation, for the circuit shown in Fig. P4.3-6. Assume that I_{OUT} is actually 10µA. Simulate this circuit using SPICE Level 3 model (Table 3.4-1) and determine the actual output current, I_{OUT}. Use Table 3.1-2 for device model information.

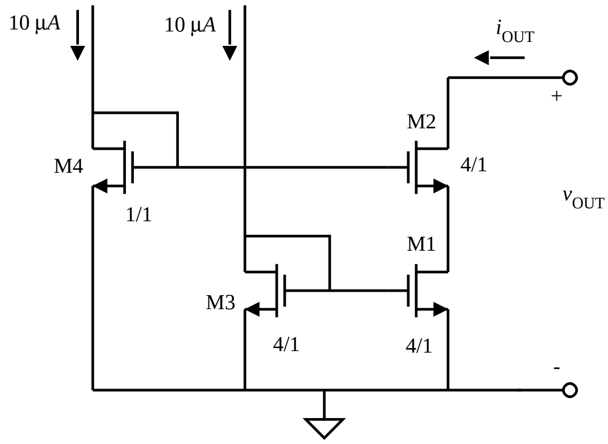


Figure P4.3-6

First calculate node voltages and currents.

Assume a near perfect current mirror so that the current in all devices is 10 microamps.

Calculate node voltages.

$$V_{GS4} = V_{G4} = \sqrt{\frac{2i_D}{\beta}} + V_T = \sqrt{\frac{2 \times 10 \times 10^{-6}}{1 \times 110 \times 10^{-6}}} + 0.7 = \sqrt{\frac{20}{110}} + 0.7 = 1.126$$

$$V_{GS3} = V_{G3} = \sqrt{\frac{2i_D}{\beta}} + V_T = \sqrt{\frac{2 \times 10 \times 10^{-6}}{4 \times 110 \times 10^{-6}}} + 0.7 = \sqrt{\frac{20}{440}} + 0.7 = 0.913$$

--

VGS of M2 must be solved taking into account the back-bias voltage and its effect on threshold voltage. The following equations relate to M2 terminals (subscripts dropped for simplicity)

$$V_{GS} = V_G - V_S = \sqrt{\frac{2i_D}{\beta}} + V_{T0} + \gamma\left(\sqrt{|2\phi_f| + v_{SB}} - \sqrt{|2\phi_f|}\right)$$

Noting that the bulk terminal is ground we get

$$V_G - V_S = \sqrt{\frac{2i_D}{\beta}} + V_{T0} + \gamma\left(\sqrt{|2\phi_f| + v_S} - \sqrt{|2\phi_f|}\right)$$

$$V_G - V_S - \sqrt{\frac{2i_D}{\beta}} - V_{T0} + \gamma\sqrt{|2\phi_f|} = \gamma\left(\sqrt{|2\phi_f| + v_S}\right)$$

$$V_G - \sqrt{\frac{2i_D}{\beta}} - V_{T0} + \gamma\sqrt{|2\phi_f|} - V_S = \gamma\left(\sqrt{|2\phi_f| + v_S}\right)$$

$$A - V_S = \gamma\left(\sqrt{|2\phi_f| + v_S}\right)$$

where

$$A = V_G - \sqrt{\frac{2i_D}{\beta}} - V_{T0} + \gamma\sqrt{|2\phi_f|}$$

$$(A - V_S)^2 = \gamma^2\left(|2\phi_f| + v_S\right)$$

$$A^2 - 2AV_S + V_S^2 = \gamma^2\left(|2\phi_f| + v_S\right)$$

$$V_S^2 - V_S(2A + \gamma^2) + A^2 - \gamma^2\left(|2\phi_f|\right) = 0$$

Now solving numerically:

$$A = V_G - \sqrt{\frac{2i_D}{\beta}} - V_{T0} + \gamma\sqrt{|2\phi_f|} = 1.126 - \sqrt{\frac{20}{440}} - 0.7 + 0.4\sqrt{0.7} = 0.5475$$

$$V_S^2 - V_S\,[2(0.5475) + 0.4^2] + 0.5475^2 - 0.4^2(0.7) = 0$$

$$V_S^2 - V_S\,(1.255) + 0.1877 = 0$$

$$V_S = 0.1736$$

$$V_{ON} = \sqrt{\frac{2i_D}{\beta}} = \sqrt{\frac{20}{440}} = 0.2132$$

$$V_{OUT}(min) = V_{ON} + V_S = 0.2132 + 0.1736 = 0.3868$$

Small signal calculation of output resistance:

$$g_{m1} = g_{m2} \cong \sqrt{(2K'W/L)|I_D|} = \sqrt{2\times 110\times10^{-6}\times 4/1 \times 10\times10^{-6}} = 93.81\times10^{-6}$$

$$g_{mbs2} = g_{m2}\frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}} = 93.81\times10^{-6}\frac{0.4}{2(0.7+0.1736)^{1/2}} = 20.07\times10^{-6}$$

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds1} + r_{ds2} + [(g_{m2} + g_{mbs2})r_{ds2}]\, r_{ds1}$$

$$g_{ds1} = g_{ds2} \cong I_D\,\lambda = 10\times10^{-6}\times 0.04 = 400\times10^{-9}$$

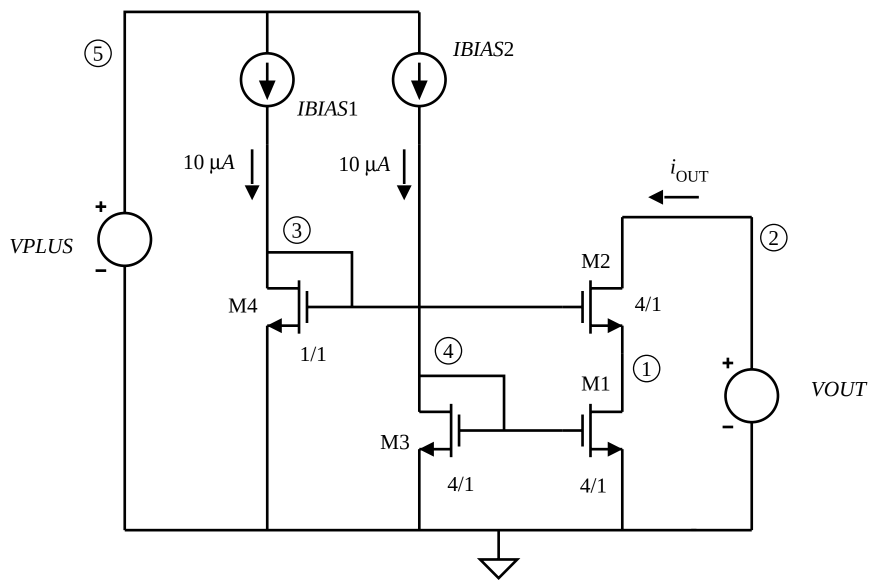
$$r_{ds1} = r_{ds2} = \frac{1}{g_{ds}} = 2.5\times10^{6}$$

$$r_{out} = r_{ds1} + r_{ds2} + [(g_{m2} + g_{mbs2})r_{ds2}]\, r_{ds1} = 2.5\times10^{6} + 2.5\times10^{6}$$

$$r_{out} = 2.5\times10^{6} + 2.5\times10^{6} + [(93.81\times10^{-6} + 20.07\times10^{-6})\, 2.5\times10^{6}]\, 2.5\times10^{6}$$

$$r_{out} = 717\times10^{6}$$

Spice Simulation



Spice simulation circuit

```
Problem 4.3-6
M4 3 3 0 0 nch w=1u l=1u
M3 4 4 0 0 nch w=4u l=1u
M2 2 3 1 0 nch w=4u l=1u
m1 1 4 0 0 nch w=4u l=1u
ibias1 5 3 10u
ibias2 5 4 10u
vplus 5 0 5
vout 2 0 3
.op
```

```
.model nch  NMOS
+ LEVEL       =          3
+ VTO         =       0.70
+ UO          =        660
+ TOX         =   1.40E-08
+ NSUB        =      3E+16
+ XJ          =     2.0e-7
+ LD          =    1.6E-08
+ NFS         =     7e+11
+ VMAX        =      1.8e5
+ DELTA       =       2.40
+ ETA         =        0.1
+ KAPPA       =       0.15
+ THETA       =        0.1
+ CGDO        =   2.20E-10
+ CGSO        =   2.20E-10
+ CGBO        =   7.00E-10
+ MJ          =       0.50
+ CJSW        =   3.50E-10
+ MJSW        =       0.38

.model pch  PMOS
+ LEVEL       =          3
+ VTO         =      -0.70
+ UO          =        210
+ TOX         =   1.40E-08
+ NSUB        =    6.00e16
+ XJ          =     2.0e-7
+ LD          =    1.5E-08
+ NFS         =      6E+11
+ VMAX        =     2.00e5
+ DELTA       =       1.25
+ ETA         =        0.1
+ KAPPA       =        2.5
+ THETA       =        0.1
+ CGDO        =   2.20E-10
+ CGSO        =   2.20E-10
+ CGBO        =   7.00E-10
+ MJ          =       0.50
.end
```

```
                          Problem 4.3-6
                DC Operating Point Analysis, 27 deg C
                    Mon Sep 02 16:24:37 2002
-------------------------------------------------------------------------
             >>>   i(vout)  = -8.1815e-006
                   i(vplus) = -2.0000e-005
                   v(0)     =  0.0000e+000
                   v(1)     =  3.2664e-001
                   v(2)     =  3.0000e+000
                   v(3)     =  1.1450e+000
                   v(4)     =  8.4156e-001
                   v(5)     =  5.0000e+000
```

Problem 4.3-7

Design M3 and M4 of Fig. P4.3-7 so that the output characteristics are identical to the circuit shown in Fig. P4.3-6. It is desired that I_{OUT} is ideally 10μA.

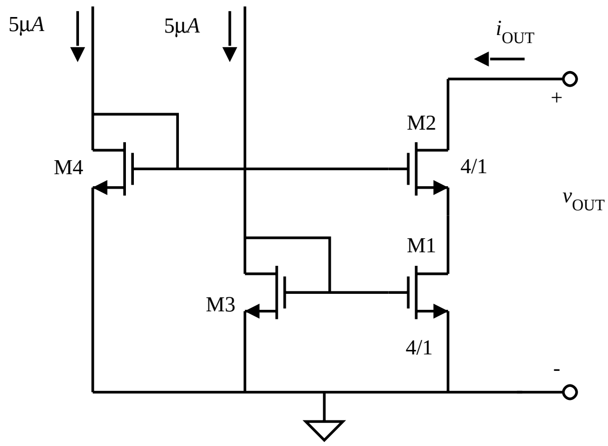


Figure P4.3-7

By comparison with the circuit in P4.3-6, the output transistors are identical but the bias currents are halved. In order to achieve the same gate voltages on M1 and M2, the W/L of M3 and M4 must be half of those in Fig P4.3-6. This is illustrated in the following equations.

$$V_{GS} = \sqrt{\frac{2i_D}{K'(W/L)}} + V_T$$

$$V_{GS}\,(5\mu\text{A}) = \sqrt{\frac{2(5\mu\text{A})}{K'(W/L)_{5\mu\text{A}}}} + V_T = V_{GS}\,(10\mu\text{A}) = \sqrt{\frac{2(10\mu\text{A})}{K'(W/L)_{10\mu\text{A}}}} + V_T$$

$$\sqrt{\frac{2(5\mu\text{A})}{K'(W/L)_{5\mu\text{A}}}} = \sqrt{\frac{2(10\mu\text{A})}{K'(W/L)_{10\mu\text{A}}}}$$

$$\frac{5\mu\text{A}}{(W/L)_{5\mu\text{A}}} = \frac{10\mu\text{A}}{(W/L)_{10\mu\text{A}}}$$

$$\frac{(W/L)_{10\mu\text{A}}}{(W/L)_{5\mu\text{A}}} = \frac{10\mu\text{A}}{5\mu\text{A}} = 2$$

$$(W/L)_{10\mu\text{A}} = 2(W/L)_{5\mu\text{A}}$$

Thus for Fig. 4.3-7

$$(W/L)_4 = 1/2$$

$$(W/L)_3 = 2/1$$

Problem 4.3-8

For the circuit shown in Fig. P4.3-8, determine I_{OUT} by simulating it using SPICE Level 3 model (Table 3.4-1). Use Table 3.1-2 for device model information. Compare the results with the SPICE results from Problem 4.3-6.

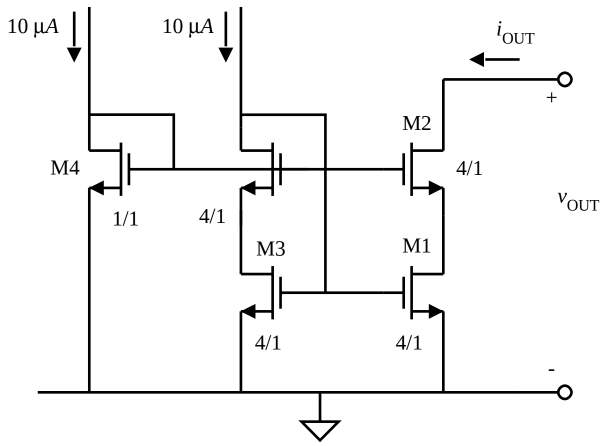
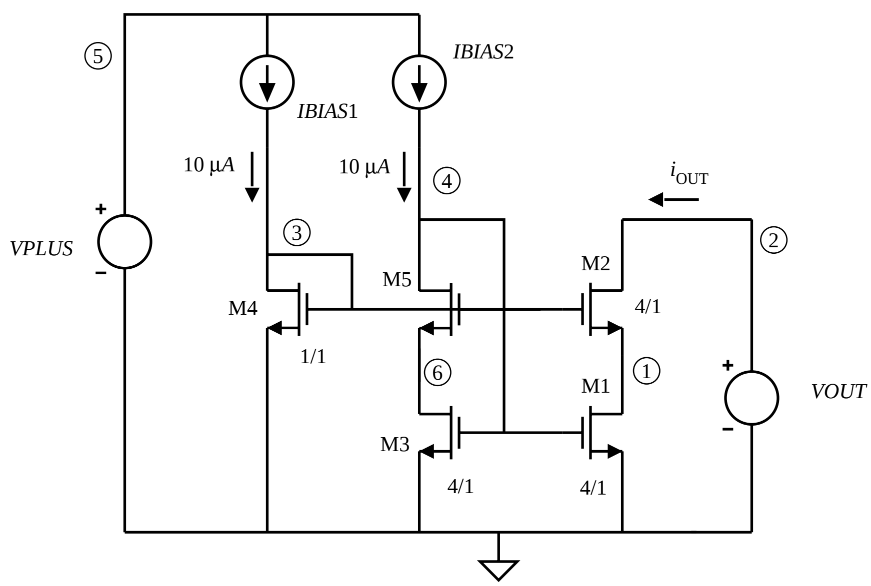


Figure P4.3-8



Spice simulation circuit

```
Problem 4.3-8
M5 4 3 6 0 nch w=4u l=1u
M4 3 3 0 0 nch w=1u l=1u
M3 6 4 0 0 nch w=4u l=1u
M2 2 3 1 0 nch w=4u l=1u
m1 1 4 0 0 nch w=4u l=1u
ibias1 5 3 10u
ibias2 5 4 10u
vplus 5 0 5
vout 2 0 3
```

```
.op
.model nch  NMOS
+ LEVEL       =           3
+ VTO         =        0.70
+ UO          =         660
+ TOX         =    1.40E-08
+ NSUB        =       3E+16
+ XJ          =      2.0e-7
+ LD          =     1.6E-08
+ NFS         =      7e+11
+ VMAX        =       1.8e5
+ DELTA       =        2.40
+ ETA         =         0.1
+ KAPPA       =        0.15
+ THETA       =         0.1
+ CGDO        =    2.20E-10
+ CGSO        =    2.20E-10
+ CGBO        =    7.00E-10
+ MJ          =        0.50
+ CJSW        =    3.50E-10
+ MJSW        =        0.38

.model pch  PMOS
+ LEVEL       =           3
+ VTO         =       -0.70
+ UO          =         210
+ TOX         =    1.40E-08
+ NSUB        =     6.00e16
+ XJ          =      2.0e-7
+ LD          =     1.5E-08
+ NFS         =      6E+11
+ VMAX        =      2.00e5
+ DELTA       =        1.25
+ ETA         =         0.1
+ KAPPA       =         2.5
+ THETA       =         0.1
+ CGDO        =    2.20E-10
+ CGSO        =    2.20E-10
+ CGBO        =    7.00E-10
+ MJ          =        0.50
.end
```

```
                           Problem 4.3-8
                 DC Operating Point Analysis, 27 deg C
                        Mon Sep 02 18:01:39 2002
-----------------------------------------------------------------------
                        i(vout)  = -1.0233e-005
                        i(vplus) = -2.0000e-005
                        v(0)     =  0.0000e+000
                        v(1)     =  3.0942e-001
                        v(2)     =  3.0000e+000
                        v(3)     =  1.1450e+000
                        v(4)     =  8.6342e-001
                        v(5)     =  5.0000e+000
                        v(6)     =  2.4681e-001
```

Notice that the output current is more accurate than that simulated in problem 4.3-6. This is because M3 and M1 have more closely matched terminal conditions.

Problem 4.4-1

Consider the simple current mirror illustrated in Fig. P4.20. Over process, the absolute variations of physical parameters are as follows:

Width variation	+/- 5%
Length variation	+/- 5%
K' variation	+/- 5%
V_T variation	+/- 5mV

Assuming that the drain voltages are identical, what is the minimum and maximum output current measured over the process variations given above.

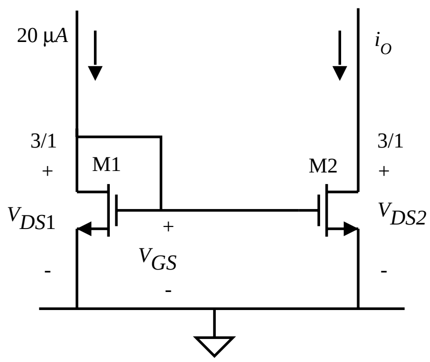


Figure P4.4-1

$$i_D = K'\frac{W}{L}(v_{GS} - V_T)^2$$

and

$$v_{GS} = \sqrt{\frac{2i_D}{K'(W/L)}} + V_T$$

Thus, combining these expressions for the circuit in Fig. P4.4-1,

$$i_O = K'_2\left(\frac{W}{L}\right)_2 (v_{GS2} - V_{T2})^2$$

$$i_O = K'_2\left(\frac{W}{L}\right)_2 \left(\sqrt{\frac{2\times 20\times 10^{-6}}{K'_1(W/L)_1}} + V_{T1} - V_{T2}\right)^2$$

Minimum and Maximum occurs under the following conditions

	K'_1	K'_2	$(W/L)_1$	$(W/L)_2$	V_{T1}	V_{T2}
$i_O(min)$	*Max*	*Min*	*Max*	*Min*	*Min*	*Max*

$i_O(max)$	*Min*	*Max*	*Min*	*Max*	*Max*	*Min*

Substituting in the expression for drain current yields:

	K'_1	K'_2	$(W/L)_1$	$(W/L)_2$	V_{T1}	V_{T2}
27.82 µ	115.5 µ	104.5 µ	3.316	2.714	0.695	0.705
56.93 µ	104.5 µ	115.5 µ	2.714	3.316	0.705	0.695

Problem 4.4-2

Consider the circuit in Fig. P4.21 where a single MOS diode (M2) drives two current mirrors (M1 and M3). A signal (v_{sig}) is present at the drain of M3 (due to other circuitry not shown). What is the effect of v_{sig} on the signal at the drain of M1, v_{OUT} ? Derive the transfer function v_{sig}(s)/ v_{OUT}(s). You must take into account the gate-drain capacitance of M3 but you can ignore the gate-drain capacitance of M1. Given that I_{BIAS}=10µA, W/L of all transistors is 2µm/1µm, and using the data from Table 3.1-2 and Table 3.2-1, calculate v_{OUT} for v_{sig} =100mV at 1MHz.

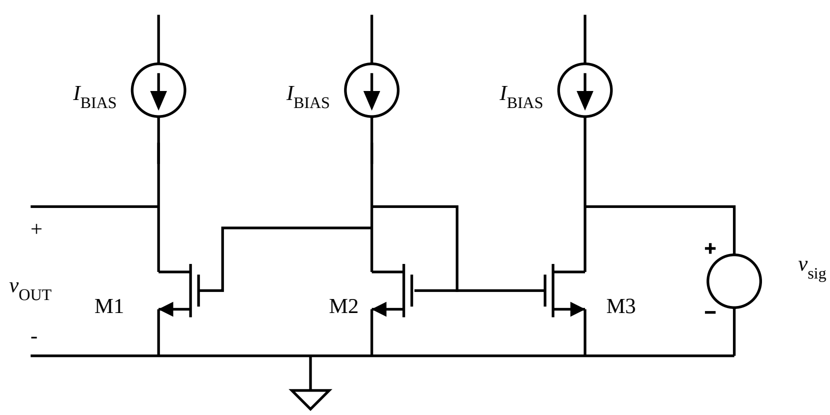
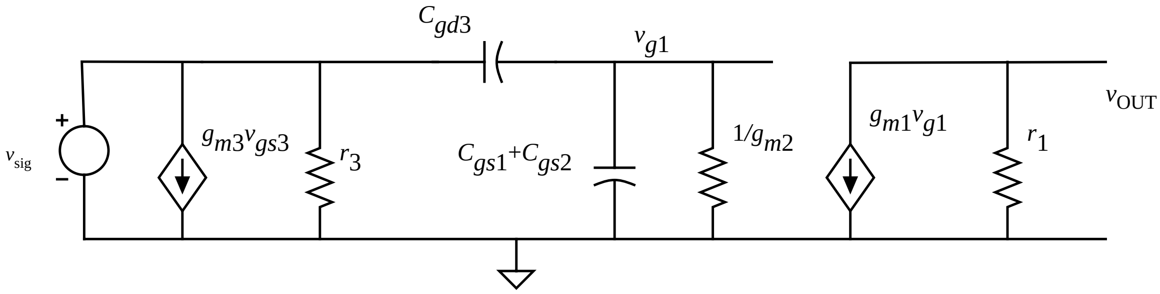
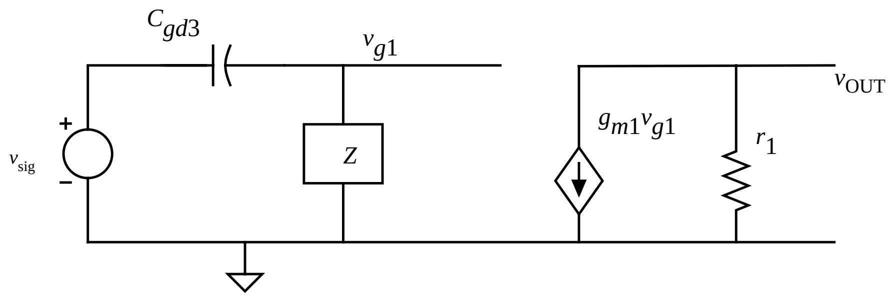


Figure P4.4-2

The small-signal model for Fig. 4.4-2 is





$$v_{g1} = v_{sig}\left(\frac{Z}{Z + 1/sC_{gd3}}\right)$$

$$v_{OUT} = -g_{m1}\, r_1\, v_{g1} = -g_{m1}\, r_1 \left(\frac{Z\, v_{sig}}{Z + 1/sC_{gd3}}\right)$$

$$\frac{v_{OUT}}{v_{sig}} = -g_{m1}\, r_1 \left(\frac{s\ C_{gd3}}{s\,(C_{gd3}+C_{gs1}+C_{gs2}) + g_{m1}}\right)$$

$$\left|\frac{v_{OUT}(\omega)}{v_{sig}\,(\omega)}\right| = -g_{m1}\, r_1 \left(\frac{\omega\ C_{gd3}}{\sqrt{[\omega\,(C_{gd3}+C_{gs1}+C_{gs2})]^2 + g_{m1}^2}}\right)$$

The transfer function has the following poles and zeros.

$$\omega_p = \left(\frac{g_{m1}}{C_{gd3} + C_{gs1} + C_{gs2}}\right)$$

$$\omega_z = \frac{g_{m1}}{C_{gd3}}$$

$$r_1 = \frac{1}{\lambda i_d} = \frac{1}{0.04 \times 10 \times 10^{-6}} = 2.5 \times 10^6$$

$$g_{m1} = \sqrt{2K'(W/L)i_D} = \sqrt{2 \times 110 \times 10^{-6} \times 2 \times 10 \times 10^{-6}} = 66.33 \times 10^{-6}$$

$$C_{gs1} = \frac{2}{3} C_{ox} \times W \times L + \text{CGSO} \times W = 3.29 \text{ fF} + 0.44 \text{ fF} = 3.73 \text{ fF}$$

$$C_{gs1} = C_{gs2}$$

$$C_{gd3} = \text{CGSO} \times W = 0.44 \text{ fF}$$

Substituting numerical values yields:

$$\left|\frac{v_{\text{OUT}}(\omega)}{v_{sig}(\omega)}\right| = 66.33 \times 10^{-6} \times 2.5 \times 10^{6} \times$$

$$\times \left(\frac{6.28 \times 10^{6} \times 0.44 \times 10^{-15}}{\sqrt{[6.28 \times 10^{6}\ (0.44 \times 10^{-15} + 3.73 \times 10^{-15} + 3.73 \times 10^{-15})]^{2} + (66.33 \times 10^{-6})^{2}}}\right)$$

$$\left|\frac{v_{\text{OUT}}(\omega)}{v_{sig}(\omega)}\right| = 6.91 \times 10^{-3} \text{ at } \omega = 6.28 \text{ Mrps}$$

For v_{sig} = 100 mV

$$v_{\text{OUT}} = v_{sig} \times 6.91 \times 10^{-3} = 100 \times 10^{-3} \times 6.91 \times 10^{-3} = 691\ \mu\text{V}$$

Problem 4.5-1

Show that the sensitivity of the reference circuit shown in Fig. 4.5-2(b) is unity.

$$\frac{\beta_P}{2}\left[V_{DD} - V_{REF} - |V_{TP}|\right]^2 = \frac{\beta_N}{2}\left[V_{REF} - V_{TN}\right]^2$$

$$\left(\frac{\beta_P}{\beta_N}\right)^{1/2}\left(V_{DD} - V_{REF} - |V_{TP}|\right) = \left(V_{REF} - V_{TN}\right)$$

$$V_{REF} = \frac{\left(\frac{\beta_P}{\beta_N}\right)^{1/2}\left(V_{DD} - |V_{TP}|\right) + V_{TN}}{1 + \left(\frac{\beta_P}{\beta_N}\right)^{1/2}}$$

When:

$\beta_P = \beta_N$, $|V_{TP}| = V_{TN}$

then

$$v_{REF} = \frac{v_{DD}}{2}$$

$$\frac{\partial V_{REF}}{\partial\, V_{DD}} = ??$$

Use a small-signal model to simplify analysis.

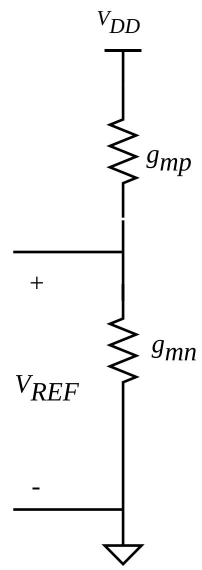


Figure P4.5-1

$$\frac{\partial V_{REF}}{\partial V_{DD}} = \frac{v_{REF}}{v_{DD}}$$

$$\frac{\partial V_{REF}}{\partial V_{DD}} = \frac{1/g_{mN}}{1/g_{mN} + 1/g_{mP}} = \frac{g_{mP}}{g_{mN} + g_{mP}}$$

$$\frac{\partial V_{REF}}{\partial V_{DD}} = \frac{\sqrt{2\beta_P\, I_D}}{\sqrt{2\beta_P\, I_D} + \sqrt{2\beta_N\, I_D}} = \frac{\sqrt{I_D}}{\sqrt{I_D} + \sqrt{I_D}} = 1/2$$

$$\underset{\mathrm{V}_{DD}}{\overset{\mathrm{V}_{\mathrm{REF}}}{\mathrm{S}}} = \left(\frac{\partial V_{\mathrm{REF}}}{\partial V_{DD}}\right)\left(\frac{V_{DD}}{V_{\mathrm{REF}}}\right) = \left(\frac{1/2}{1/2}\right) = 1$$

Problem 4.5-2

Fig P4.5-2 illustrates a reference circuit that provides an interesting reference voltage output. Derive a symbolic expression fo V_{REF} .

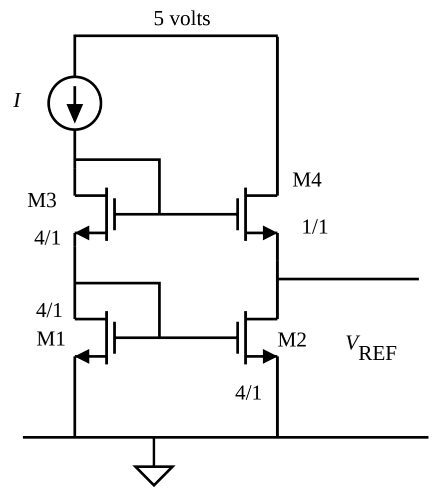


Fig. P4.5-2

$$V_{GS1} + V_{GS3} - V_{GS4} = V_{\text{REF}}$$

$$V_{\text{REF}} = V_{ON1} + V_{T1} + V_{ON3} + V_{T3} - V_{ON4} - V_{T4}$$

$$V_{T4} = V_{T3}$$

$$V_{ON1} = V_{ON3}$$

$$V_{ON4} = 2V_{ON3}$$

$$V_{\text{REF}} = 2V_{ON1} + V_{T1} + V_{T3} - 2V_{ON1} - V_{T3} = V_{T1}$$

$$V_{\text{REF}} = V_{T1}$$

Problem 4.5-3

Figure P4.5-3 illustrates a current reference. The W/L of M1 and M2 is 100/1. The resistor is made from n-well and its nominal value is 400kΩ at 25 °C. Using Table 3.1-2 and an n-well resistor with a sheet resistivity of 1kΩ/sq. ± 40% and temperature coefficient of 8000 ppm/°C, calculate the total variation of output current seen over process, temperature of 0 to 70 °C, and supply voltage variation of ± 10%. Assume that the temperature coefficient of the threshold voltage is –2.3 mV/°C.

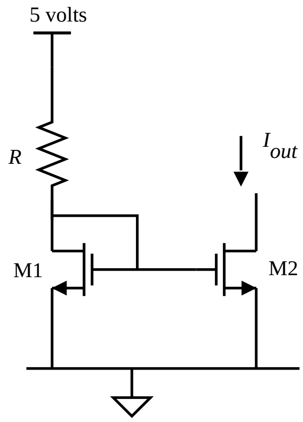


Fig. P4.5-3

$$I_{\mathrm{REF}} = \frac{V_{DD} - \sqrt{\frac{2I_{REF}}{\beta}} + V_T}{R}$$

$$\frac{1}{R}\sqrt{\frac{2I_{REF}}{\beta}} = \frac{V_{DD} - V_T}{R} - I_{REF}$$

Define $V = V_{DD} - V_T$

$$\frac{2I_{REF}}{\beta} = (V - I_{REF}R)^2$$

$$I_{REF}^2 R^2 - 2I_{REF}\left(VR + \frac{1}{\beta}\right) + V^2 = 0$$

$$I_{REF}^2 - 2I_{REF}\left(\frac{V}{R} + \frac{1}{\beta R^2}\right) + \frac{V^2}{R^2} = 0$$

$$I_{REF} = \frac{V}{R} + \frac{1}{\beta R^2} \pm \frac{1}{R}\sqrt{\frac{2V}{\beta R} + \frac{1}{\beta^2 R^2}}$$

$$I_{REF} = \frac{V_{DD} - V_T}{R} + \frac{1}{\beta R^2} \pm \frac{1}{R}\sqrt{\frac{2(V_{DD} - V_T)}{\beta R} + \frac{1}{\beta^2 R^2}}$$

$R_{min}(25°\mathrm{C}) = 500\mathrm{k}\Omega \times (1 - 0.4) = 300\mathrm{k}\Omega$

$R_{max}(25°\mathrm{C}) = 500\mathrm{k}\Omega \times (1 + 0.4) = 700\mathrm{k}\Omega$

$R(T) = R(T_0) \times (1 + \mathrm{TC}\times\Delta T)$

$R_{min}(0\ °C) = R_{min}(25\ C) \times (1 + 8000\times10^{-6} \times -25) = 300 \times 0.8 = 240k\Omega$

$R_{max}(70\ °C) = R_{max}(25\ C) \times (1 + 8000\times10^{-6} \times 45) = 700 \times 1.36 = 952k\Omega$

$V_{T(min)}\ (25°C) = 0.7 - 0.15 = 0.55$

$V_{T(max)}\ (25°C) = 0.7 + 0.15 = 0.85$

$V_{T(min)}\ (70°C) = 0.55 - 45 \times 0.0023 = 0.4465$

$V_{T(max)}\ (0°C) = 0.85 + 25 \times 0.0023 = 0.9075$

$K'_{(max)}\ (25°C) = 110 \times 10^{-6} \times 1.1 = 121 \times 10^{-6}$

$K'_{(min)}\ (25°C) = 110 \times 10^{-6} \times 0.9 = 99 \times 10^{-6}$

$$K'\ (T) = K'\ (T_0) \times \left(\frac{T}{T_0}\right)^{-1.5}$$

$$K'_{(min)}\ (70°C) = 99 \times 10^{-6} \times \left(\frac{343}{298}\right)^{-1.5} = 80.17 \times 10^{-6}$$

$$K'_{(max)}\ (0°C) = 121 \times 10^{-6} \times \left(\frac{273}{298}\right)^{-1.5} = 138 \times 10^{-6}$$

Minimum and Maximum occurs under the following conditions

	K'	V_T	V_{DD}	R
$I_{REF(min)}$	*Max*	*Max*	*Min*	*Max*
$I_{REF(max)}$	*Min*	*Min*	*Max*	*Min*

	K'	V_T	V_{DD}	R
$I_{REF(min)}$	80.17×10^{-6}	0.9075	4.5	952 K
$I_{REF(max)}$	138×10^{-6}	0.4465	5.5	240 K

Plugging in these minimums and maximums yields the following over process and temperature:

$$I_{REF(min)} = 3.81 \times 10^{-6}$$

$$I_{REF(max)} = 21.3 \times 10^{-6}$$

Problem 4.5-4

Figure 4.5-4 illustrates a current reference circuit. Assume that M3 and M4 are identical in size. The sizes of M1 and M2 are different. Derive a symbolic expression for the output current I_{out} .

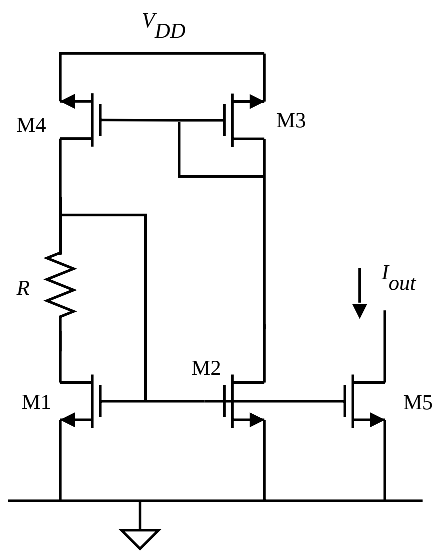


Fig. P4.5-4

Assume that M3 and M4 make a perfect current mirror, as does M2 and M5.

$$V_{GS2} - V_{GS1} + IR = 0$$

$$V_{T1} + V_{ON1} - V_{T2} - V_{ON2} = IR$$

$$IR = V_{ON1} - V_{ON2} = \sqrt{\frac{2i_D}{K'(W/L)_1}} - \sqrt{\frac{2i_D}{K'(W/L)_2}}$$

$$IR = \sqrt{\frac{2i_D}{K'}} \left(\sqrt{\frac{1}{(W/L)_1}} - \sqrt{\frac{1}{(W/L)_2}} \right)$$

$$I = \frac{1}{R}\sqrt{\frac{2i_D}{K'}}\left(\sqrt{\frac{1}{(W/L)_1}} - \sqrt{\frac{1}{(W/L)_2}}\right)$$

Problem 4.5-5

Find the small-signal output resistance of Fig. 4.5-3(b) and Fig. 4.5-4(b).

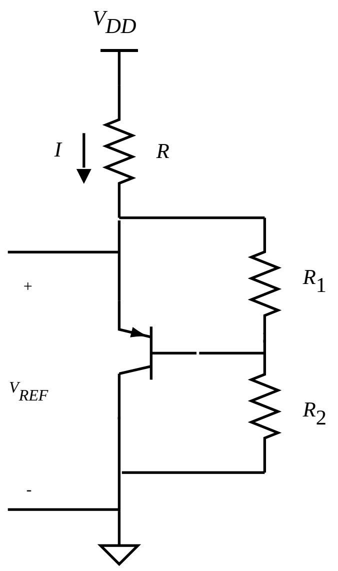


Figure 4.5-3(b)

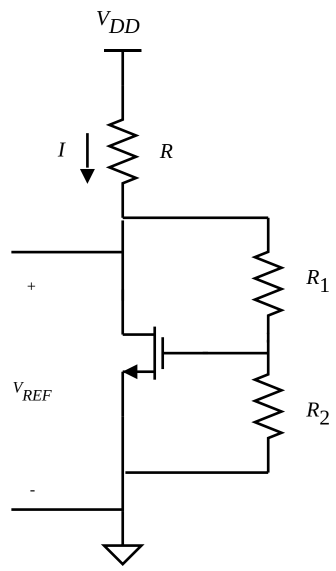
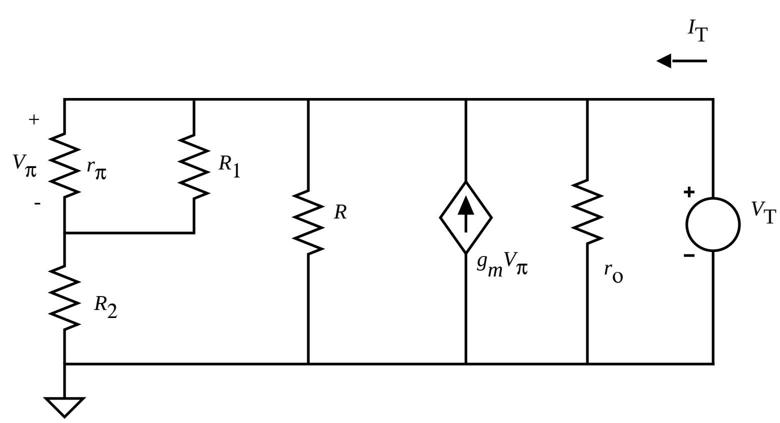
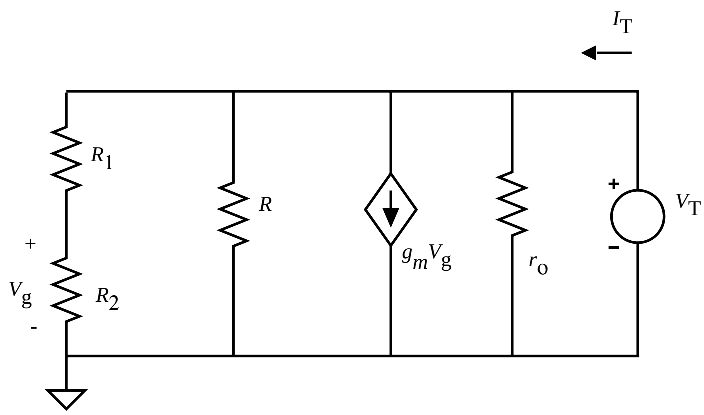


Figure 4.5-4(b)





Part a:

$$v_\pi = v_t\left(\frac{r_\pi \| R_1}{r_\pi \| R_1 + R_2}\right)$$

$$i_t = \left(\frac{v_t}{r_\pi \| R_1 + R_2}\right) + \left(\frac{v_t}{R}\right) + g_m v_\pi + \frac{v_t}{r_o}$$

$$i_t = v_t\left[\left(\frac{1}{r_\pi \| R_1 + R_2}\right) + \left(\frac{1}{R}\right) + \left(\frac{g_m (r_\pi \| R_1)}{r_\pi \| R_1 + R_2}\right) + \frac{1}{r_o}\right]$$

$$\frac{v_t}{i_t} = \left[\frac{R\, r_o\, (r_\pi \| R_1 + R_2)}{R\, r_o + r_o\,(r_\pi \| R_1 + R_2) + R\, r_o\, g_m\,(r_\pi \| R_1) + R\,(r_\pi \| R_1 + R_2)}\right]$$

if $r_\pi \| R_1 >> R_2$ then

$$\frac{v_t}{i_t} = \frac{1}{g_m}$$

Part b:

$$v_G = v_t\left(\frac{R_2}{R_1 + R_2}\right)$$

$$i_t = g_m v_G + \frac{v_t}{r_o} + \frac{v_t}{R} + \frac{v_t}{R_1 + R_2}$$

$$\frac{i_t}{v_t} = \frac{g_m R_2}{R_1 + R_2} + \frac{1}{r_o} + \frac{1}{R} + \frac{1}{R_1 + R_2}$$

if $R_2 >> R_1$ then

$$\frac{i_t}{v_t} = g_m + \frac{1}{r_o} + \frac{1}{R} + \frac{1}{R_2}$$

if $g_m >> \frac{1}{R_2}, g_m >> \frac{1}{r_o}, g_m >> \frac{1}{R}$ then

$$\frac{i_t}{v_t} = g_m$$

Problem 4.5-6

Using the reference circuit illustrated in Fig. 4.5-3(b), design a voltage reference having V_{REF}=2.5 when V_{DD}=5.0. Assume that I_S = 1 fA and β_F=100. Evaluate the sensitivity of V_{REF} with respect to V_{DD}.

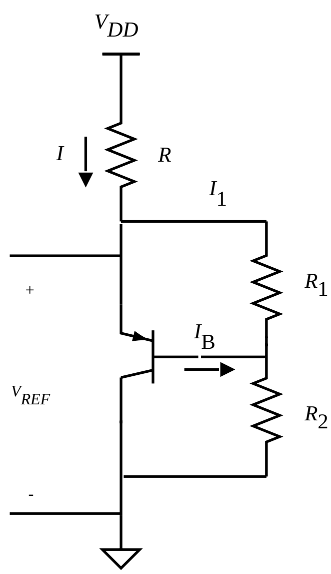


Figure 4.5-3 (b)

$IR = 2.5$
Choose R = 250 kΩ, I = 10µA

$I = I_1 + I_E$

choose I_E = 1 µA, and I_1 = 9 µA

With β=100, base current is insignificant and will be ignored.

$$I_1 = \frac{2.5}{R_1 + R_2} = 9\ \mu\text{A} = \frac{2.5}{R_1 + R_2}$$

$$R_1 + R_2 = 277.8\ \text{k}\Omega$$

$$V_{\text{REF}} = I_1 R_2 + V_{\text{EB}}$$

$$2.5 = 9\ \mu\text{A}\ R_2 + 0.0259 \times \ln\left(\frac{1\ \mu\text{A}}{1\ \text{fA}}\right)$$

$$R_2 = 218.1\ \text{k}\Omega$$

$$R_1 = 59.64\ \text{k}\Omega$$

$$V_{EB} = \frac{V_{REF}\, R_1}{R_1 + R_2}$$

$$V_{\text{REF}} = V_{EB}\frac{R_1 + R_2}{R_1} = \left(\frac{R_1 + R_2}{R_1}\right) V_t \ln\left(\frac{V_{DD} - V_{\text{REF}}}{R\, I_S}\right)$$

$$S_{V_{DD}}^{V_{\text{REF}}} = \left(\frac{\partial V_{\text{REF}}}{\partial V_{DD}}\right)\left(\frac{V_{DD}}{V_{\text{REF}}}\right) = \left(\frac{V_{DD}}{V_{\text{REF}}}\right) V_t \left(\frac{R\, I_S}{V_{DD} - V_{\text{REF}}}\right)\left(\frac{1}{R\, I_S}\right)\left(\frac{R_1 + R_2}{R_1}\right)$$

$$S_{V_{DD}}^{V_{\text{REF}}} = \left(\frac{V_{DD}}{V_{\text{REF}}}\right) V_t \left(\frac{1}{V_{DD} - V_{\text{REF}}}\right)\left(\frac{R_1 + R_2}{R_1}\right)$$

$$S_{V_{DD}}^{V_{\text{REF}}} = \left(\frac{5}{2.5}\right) 0.0259 \left(\frac{1}{2.5}\right)\left(\frac{277.8}{59.64}\right) = 0.0965$$

Problem 4.6-1

An improved bandgap reference generator is illustrated in Fig. P4.6-1. Assume that the devices M1 through M5 are identical in W/L. Further assume that the area ratio for the bipolar transistors is 10:1. Design the components to achieve an output reference voltage of 1.262 V. Assume that the amplifier is ideal. What advantage, if any, is there in stacking the bipolar transistors?

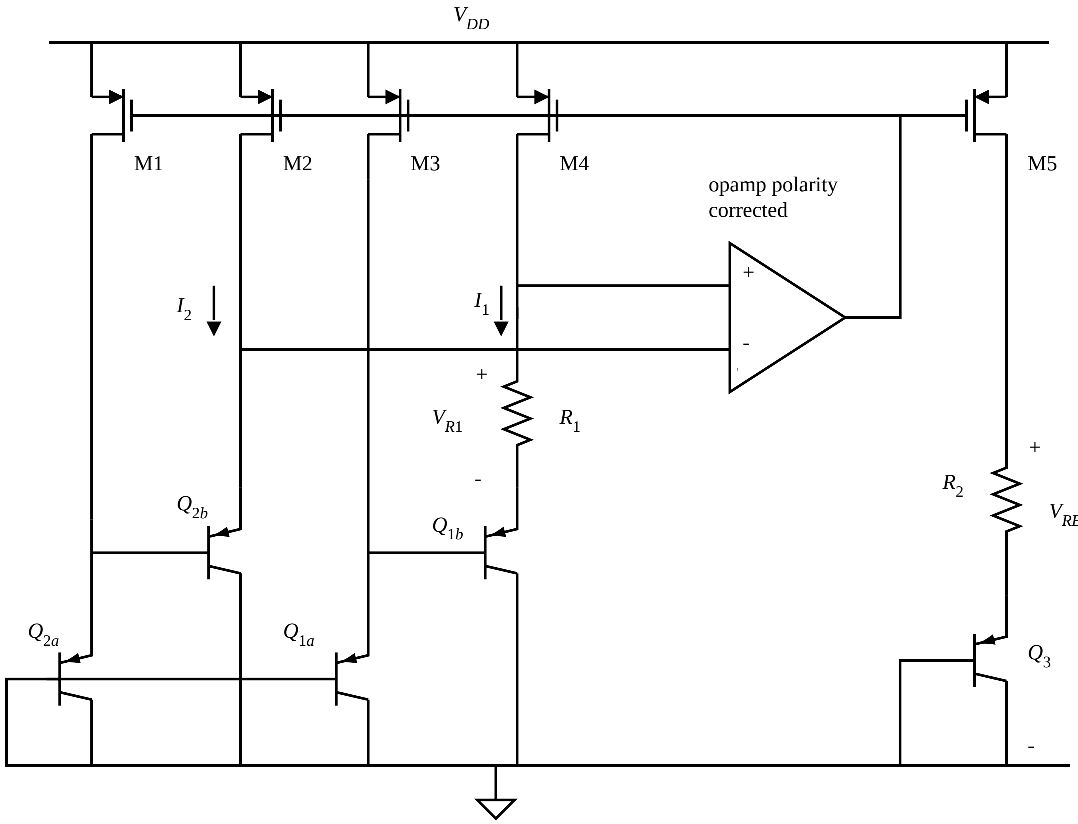


Figure P4.6-1

$$V_{\mathrm{REF}}\Big|_{T=T0} = V_{G0} + V_{t0}\,(\gamma - \alpha) = 1.262 \text{ @ } 300\text{ K}$$

$$KV_{t0} = V_{G0} - V_{BE0} + V_{t0}\,(\gamma - \alpha)$$

$$K = \left(\frac{R_2}{R_1}\right)\ln(10) = \frac{V_{G0} - V_{BE0} + V_{t0}\,(\gamma - \alpha)}{V_{t0}}$$

$$V_{BE0} = \frac{kT}{q}\ln\left(\frac{I}{I_S}\right)$$

$$I = \frac{\Delta V_{BE}}{R_1} = 1\ \mu\text{A}$$

$$R_1 = \frac{0.0259\ \ln(10)}{1\ \mu\text{A}} = 59.64\ \text{k}\Omega$$

$$K = \frac{1.205 - 0.53 + 0.0259(2.2)}{0.0259} = 28.26 \text{ k}\Omega = \left(\frac{R_2}{R_1}\right) \ln (10)$$

$R_2 = 732 \text{ k}\Omega$

Stacking bipolar transistors reduces sensitivity to amplifier offset.

Problem 4.6-2

In an attempt to reduce the noise output of the reference circuit shown in Fig. P4.6-1, a capacitor is placed on the gate of M5. Where should the other side of the capacitor be connected and why?

The other end of the capacitor should be connected to V_{DD}. At high frequencies, the capacitor is a small-signal short circuit. Therefore, high-frequency noise on V_{DD} also appears at the gate of M5 and thus is not amplified by M5. If on the other hand, the capacitor was connected to ground, noise on V_{DD} would appear as v_{GS} of M5 and thus be amplified to the output.

Problem 4.6-3

In qualitative terms, explain the effect of low Beta for the bipolar transistors in Fig. P4.6-1?

In our analysis, we assume that

$$I_E = I_S \, e^{(V_{BE}/V_t)}$$

but in reality, this is the expression for I_C .

If β is large, then the approximation is warranted, but if not, the performance will deviate from the ideal.

Problem 4.6-4

Consider the circuit shown in Fig. P4.6-4. It is a variation of the circuit shown in Fig. P4.6-1. What is the purpose of the circuit made up of M6-M9 and Q4?

This circuit performs base-current compensation so that none of the base currents in Q_{1b} and Q_{2b} flow into Q_{1a} and Q_{2a} respectively.

Problem 4.6-5

Extend Example 4.6-1 to the design of a temperature-independent current based upon the circuit shown in Fig. 4.6-4. The temperature coefficient of the resistor, R_4, is +1500 ppm/°C.

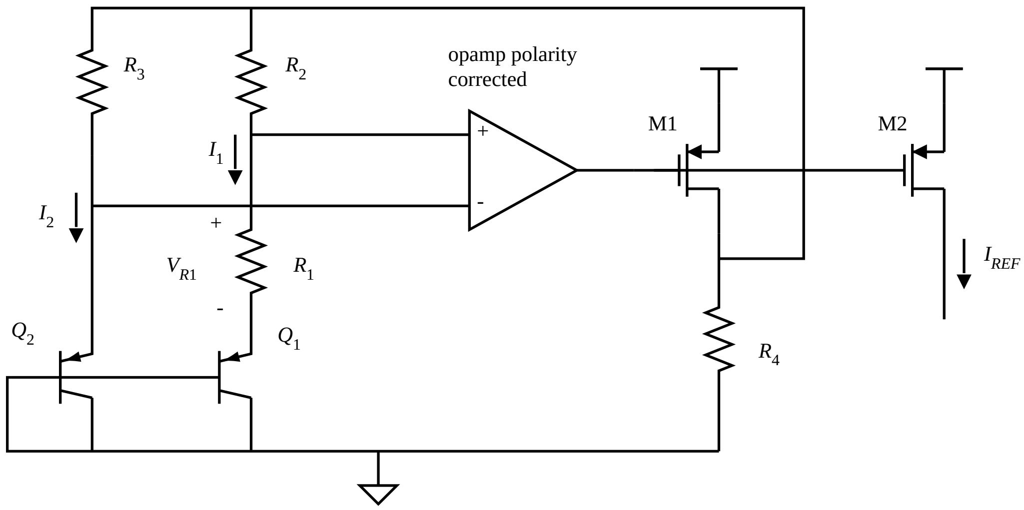


Figure P4.6-5

$$\left(\frac{A_{e1}}{A_{e2}}\right) = 10$$

$V_{eb} = 0.7$, $R_2 = R_3$, $V_t = 26$ mV , $TC_4 = 1500$ ppm/°C

$V_{G0} = 1.205$, $\gamma = 3.2$, $\alpha = 1$, $T_0 = 27$ °C

Since the amp forces $V^+ = V^-$, then $I_1 = I_2$

$$I_{\text{REF}} = I_4 + 2\, I_1 = \frac{V_{\text{REF}}}{R_4} + 2\, I_1$$

$$I_1 = \frac{\Delta V_{be}}{R_1} = \frac{1}{R_1}\frac{kT}{q}\ln(10)$$

We want

$$\left.\frac{\partial I_{\text{REF}}}{\partial T} = 0\right|_{\text{T} = \text{T}_0}$$

$$\frac{\partial I_{\text{REF}}}{\partial T} = \frac{\partial}{\partial T}\left(\frac{V_{\text{REF}}}{R_4}\right) + \frac{\partial}{\partial T}(2\, I_1)$$

$$2\frac{\partial I_1}{\partial T} = \left(\frac{2K}{q}\right)\frac{\ln(10)}{R_1}$$

$$\frac{\partial}{\partial T}\left(\frac{V_{\text{REF}}}{R_4}\right) = \frac{\dfrac{\partial V_{\text{REF}}}{\partial T} R_4 - V_{\text{REF}} \dfrac{\partial R_4}{\partial T}}{R_4^2}$$

$$\frac{\partial R_4}{\partial T} = \frac{\partial}{\partial T}(R_4 + R_4 \text{TC}_4 \Delta \text{T}) = R_4 \text{TC}_4$$

$$\frac{\partial V_{\text{REF}}}{\partial T} = K\left(\frac{V_{t0}}{T_0}\right) + \frac{V_{BE0} - V_{G0}}{T_0} + \frac{(\alpha - \gamma)V_{t0}}{T_0}$$

$$\frac{\partial I_{\text{REF}}}{\partial T} = \frac{1}{R_4}\left[K\left(\frac{V_{t0}}{T_0}\right) + \frac{V_{BE0} - V_{G0}}{T_0} + \frac{(\alpha - \gamma)V_{t0}}{T_0}\right] - \frac{V_{\text{REF}}}{R_4}\text{TC}_4 + \left(\frac{2K}{q}\right)\frac{\ln(10)}{R_1}$$

$$\text{K} = \frac{R_2}{R_1}\ln\left(\frac{A_{\text{e1}}}{A_{\text{e2}}}\right) = \frac{R_2}{R_1}\ln(10)$$

choose $\dfrac{R_2}{R_1} = 10$ then $K = 23.03$

$$I_1 = \frac{\Delta V_{\text{BE}}}{R_1} = \frac{\text{kT}}{\text{q}}\left[\frac{\ln(10)}{R_1}\right] = 2\ \mu\text{A}$$

thus

$\boxed{R_1 = 29.93\ \text{k}\Omega \text{, and } R_2 = 299.3\ \text{k}\Omega}$

assume that $V_{\text{REF}} = 1.262$ and solve for R_4

$$R_4 = \frac{T_0\, R_1}{2\, V_t \ln(10)}\left[\frac{V_{G0} - V_{BE0}}{T_0} + \frac{(\gamma - \alpha)V_{t0}}{T_0} - K\left(\frac{V_{t0}}{T_0}\right) + \frac{V_{\text{REF}}\,\text{TC}_4\, T_0}{T_0}\right]$$

$$R_4 = \frac{R_1}{2\, V_t \ln(10)}\left[(V_{G0} - V_{BE0}) + (\gamma - \alpha)V_{t0} - K\ V_{t0} + V_{\text{REF}}\,\text{TC}_4\, T_0\right]$$

$\boxed{R_4 = 250 \times 10^3 \times 0.153 = 3825\ \Omega}$

$$I_{\text{REF}} = \frac{V_{\text{REF}}}{R_4} + 2\,I_1 = 4 \times 10^{-6} + \frac{1.262}{3825} = 333.9 \times 10^{-6}$$

CHAPTER 5 – HOMEWORK SOLUTIONS

Problem 5.1-01

Assume that M2 in Fig. 5.1-2 is replaced by a 10kΩ resistor. Use the graphical technique illustrated in this figure to obtain a voltage transfer function of M1 with a 10kΩ load resistor. What is the maximum and minimum output voltages if the input is taken from 0V to 5V?

Solution

A computer generated plot of this problem is shown below.

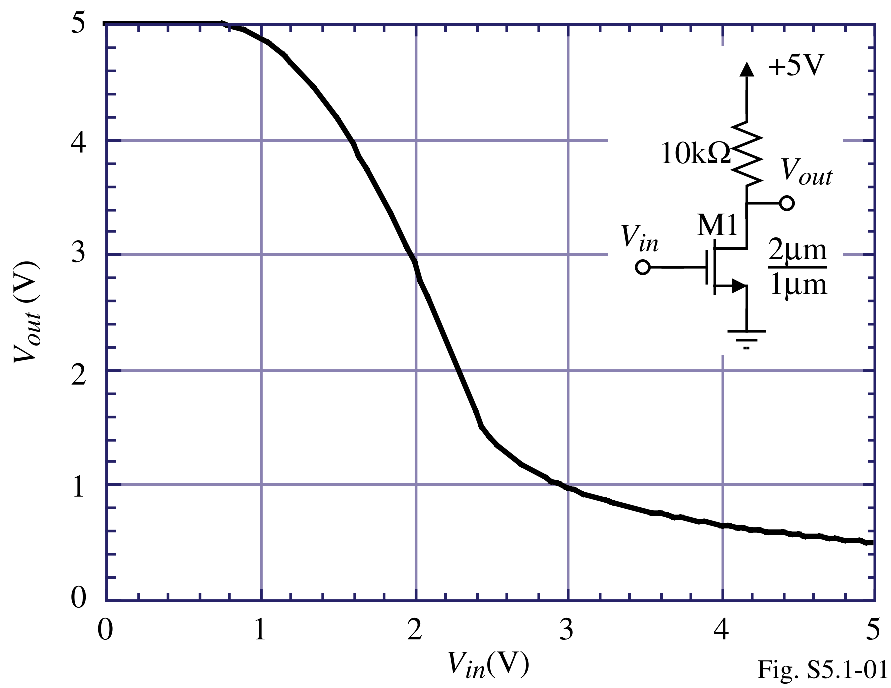


Fig. S5.1-01

The maximum output is obviously equal to 5V. The minimum output requires the following calculation assuming that M1 is in the active region.

$$110\text{x}10^{-6}\cdot 2[(5-0.7)v_{out} - 0.5v_{out}^2] = \frac{5- v_{out}}{10\text{k}\Omega}$$

$$4.3\ v_{out} - v_{out}^2 = \frac{5-v_{out}}{2.22} \quad \rightarrow \qquad v_{out}^2 - 9.5\ v_{out} + 4.504 = 0$$

This gives,

$$v_{out}\ (\text{min}) = 4.25 \pm 4.2945 = \underline{0.5\text{V}}$$

Problem 5.1-02

Using the large-signal model parameters of Table 3.1-2, use Eqs. (1) and (5) to calculate the values of v_{OUT}(max) and v_{OUT}(min). Compare with the results shown on Fig. 5.1-2 on the voltage transfer function curve.

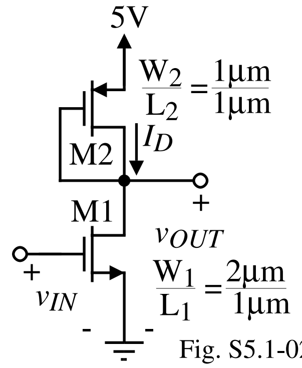


Fig. S5.1-02

Solution

From Eq. (5.1-1), $V_{out}(\max)$ can be calculated as

$$V_{out}(\max) = V_{DD} - |V_{Tp}| = \underline{\underline{4.3\ \text{V}}}$$

From Eq. (5.1-5), $V_{out}(\min)$ can be calculated as

$$V_{out}(\min) = V_{DD} - V_T - \frac{(V_{DD} - V_T)}{\sqrt{1 + \dfrac{\beta_2}{\beta 1}}}$$

$$V_{out}(\min) = 5 - 0.7 - \frac{(5-0.7)}{\sqrt{1 + \dfrac{(50)(1)}{(110)(5)}}} = \underline{\underline{0.183\ \text{V}}}$$

Problem 5.1-03

What value of β_1/β_2 will give a voltage swing of 70% of V_{DD} if V_T is 20% of V_{DD}? What is the small-signal voltage gain corresponding to this value of β_1/β_2?

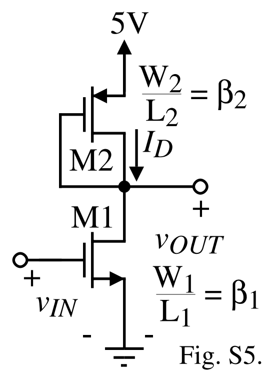


Fig. S5.1-03

Solution

Given $V_T = 0.2V_{DD}$ and $(V_{out}(\max) - V_{out}(\min)) = 0.7V_{DD}$

From Eq. (5.1-1) and (5.1-5)

$$V_{out}(\max) - V_{out}(\min) = \frac{(V_{DD} - V_T)}{\sqrt{1 + \dfrac{\beta_2}{\beta_1}}}$$

or, $$0.7V_{DD} = \frac{(V_{DD} - 0.2V_{DD})}{\sqrt{1 + \dfrac{\beta_2}{\beta_1}}} \quad \rightarrow \quad \left(1 + {\beta_2}/{\beta_1}\right) = \left(\frac{8}{7}\right)^2 \quad \rightarrow \quad {\beta_2}/{\beta_1} = \underline{0.306}$$

The small-signal voltage gain can be given by $$A_v \cong -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{\beta_1}{\beta_2}} = \underline{\underline{-1.8\ \text{V/V}}}$$

Problem 5.1-04

What value of V_{in} will give a current in the active load inverter of 100μA if W_1/L_1 = 5μm/1μm and W_2/L_2 = 2μm/1μm? For this value of V_{in}, what is the small-signal voltage gain and output resistance?

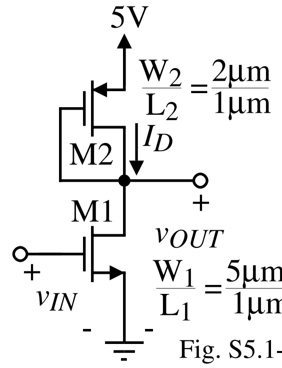


Fig. S5.1-04

Solution

Assuming M_1 is operated in saturation

$$I_{D1} = K_N'\left(\frac{W}{L}\right)_1\left(\frac{(V_{in}-V_T)^2}{2}\right)$$

or, $$100\mu = (110\mu)(5)\left(\frac{(V_{in}-0.7)^2}{2}\right) \qquad \rightarrow V_{in} = \underline{\underline{1.303\text{V}}}$$

The small-signal gain can be given by $$A_v \cong -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{(K_N')}{(K_P')}\left(\frac{W}{L}\right)_1\left(\frac{L}{W}\right)_2} = \underline{\underline{-2.345\text{ V/V}}}$$

The output resistance can be given by $$R_{out} \cong \frac{1}{g_{m2}} = \underline{\underline{7.07\text{ k}\Omega}}$$

Problem 5.1-05

Repeat Ex. 5.1-1 if the drain current in M1 and M2 is 50μA.

Solution

From Eqs. (5.1-1) and (5.1-5) we get

$$v_{OUT}(\max) = \underline{\underline{4.3\text{V}}}$$

$$v_{OUT}(\min) = 5 - 0.7 - \frac{5\text{-}0.7}{\sqrt{1 + (50\cdot 1/110\cdot 2)}} = \underline{\underline{0.418\text{ V}}}$$

From Eq. (5.1-7) we get,

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1}+g_{ds2}+g_{m2}} = \frac{148.3}{2.0 + 2.5 + 70.71} = \underline{\underline{-1.972\text{ V/V}}}$$

From Eq. (5.1-8) we get,

$$R_{out} = \frac{1}{g_{ds1}+g_{ds2}+g_{m2}} = \frac{10^6}{2.0 + 2.5 + 70.71} = \underline{\underline{13.296\text{ k}\Omega}}$$

The zero is at,

$$z_1 = \frac{g_{m1}}{C_{gd1}} = \frac{148.3\mu\text{S}}{0.5\text{ff}} = \underline{\underline{2.966\text{x}10^{11}\text{ rads/sec}}} \rightarrow 47.2\text{ GHz}$$

The pole is at,

$$p_1 = -\omega_{\text{-3dB}} = \frac{1}{R_{out}(C_{bd1}+C_{bd2}+C_{gs2}+C_L)} = \frac{1}{(13.296\text{k}\Omega)(1.0225\text{pF})}$$

$$= \underline{\underline{73.555\text{x}10^6\text{ rads/sec}}}. \rightarrow 11.71\text{ MHz}$$

Problem 5.1-06

Assume that *W*/*L* ratios of Fig. P5.1-6 are W_1/L_1 = 2μm/1μm and $W_2/L_2 = W_3/L_3 = W_4/L_4$ = 1μm/1μm. Find the dc value of V_{in} that will give a dc current in M1 of 110μA. Calculate the small signal voltage gain and output resistance of Fig. P5.1-6 using the parameters of Table 3.1-2.

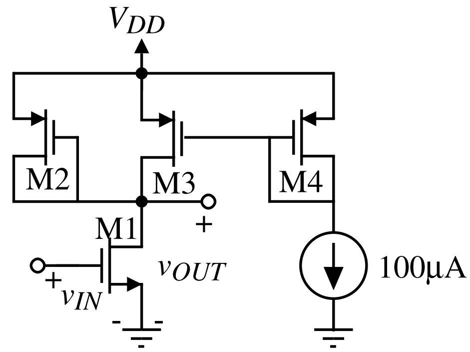


Figure P5.1-6

Solution

Assuming all transistors are in saturation and ideal current mirroring

$$I_{D1} = K_N'\left(\frac{W}{L}\right)_1\left(\frac{(V_{in}-V_T)^2}{2}\right)$$

or, $$110\mu = (110\mu)(2)\left(\frac{(V_{in}-0.7)^2}{2}\right) \quad \rightarrow \quad V_{in} = \underline{1.7\text{V}}$$

The small-signal voltage gain can be given by

$$A_V \cong -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{K_N'}{K_P'}\left(\frac{W}{L}\right)_1\left(\frac{L}{W}\right)_2\left(\frac{I_{D1}}{I_{D2}}\right)} = \underline{\underline{-6.95\text{ V/V}}}$$

where, $I_{D3} = I_{D4} = 100\ \mu A$, and $I_{D2} = 10\ \mu A$.

The output resistance can be given by

$$R_{out} \cong \frac{1}{g_{m2}} = \underline{\underline{31.6\text{ k}\Omega}}$$

Problem 5.1-07

Find the small-signal voltage gain and the -3dB frequency in Hertz for the active-load inverter, the current source inverter and the push-pull inverter if W_1 = 2µm, L_1 = 1µm, W_2 = 1µm, L_2 = 1µm and the dc current is 50µA. Assume that C_{gd1} = 4fF, C_{bd1} = 10fF, C_{gd2} = 4fF, C_{bd2} = 10fF and C_L = 1pF.

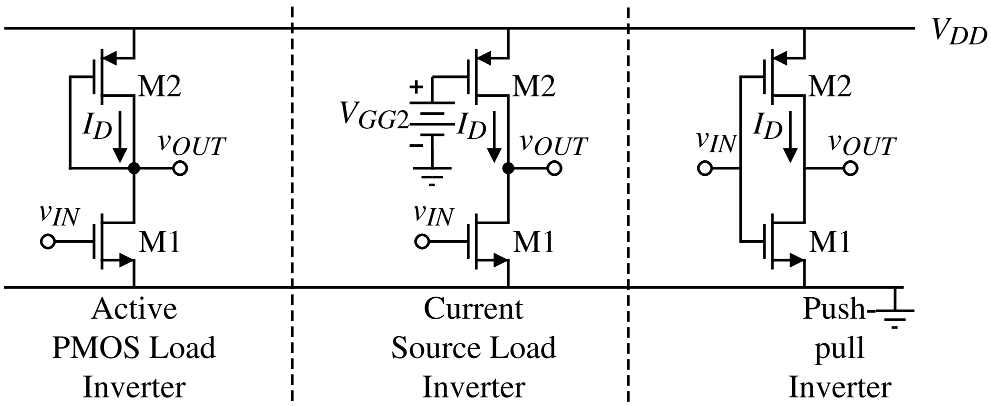


Figure 5.1-1 Various types of inverting CMOS amplifiers.

Solution

1. Active load inverter

The output resistance can be given by

$$R_{out} \cong \frac{1}{g_{m2}} = \frac{1}{\sqrt{2(50\mu)(1)(50\mu)}} = \underline{\underline{14.14\ \text{k}\Omega}}$$

The total output capacitance can be given by

$$C_{out} = C_L + C_{gs2} + C_{bd2} + C_{gd1} + C_{bd1} = \underline{\underline{1.029\ \text{pF}}}$$

The –3 dB frequency can be given by

$$f_{-3dB} = \frac{1}{2\pi R_{out} C_{out}} = \underline{\underline{10.9\ \text{MHz}}}$$

2. Current-source inverter

The output resistance can be given by

$$R_{out} \cong \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{I_D(\lambda_N + \lambda_P)} = \underline{\underline{222.22\ \text{k}\Omega}}$$

The total output capacitance can be given by

$$C_{out} = C_L + C_{gd2} + C_{bd2} + C_{gd1} + C_{bd1} = \underline{\underline{1.028\ \text{pF}}}$$

The –3 dB frequency can be given by

$$f_{-3dB} = \frac{1}{2\pi R_{out} C_{out}} = \underline{\underline{0.697\ \text{MHz}}}$$

Problem 5.1-07 - Continued

3. Push-pull inverter

The output resistance can be given by

$$R_{out} \cong \frac{1}{g_{ds1}+g_{ds2}} = \frac{1}{I_D(\lambda_N+\lambda_P)} = \underline{\underline{222.22\ \text{k}\Omega}}$$

The total output capacitance can be given by

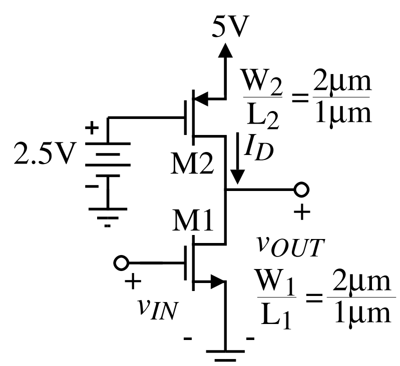
$$C_{out} = C_L + C_{gd2} + C_{bd2} + C_{gd1} + C_{bd1} = \underline{\underline{1.028\ \text{pF}}}$$

The –3 dB frequency can be given by

$$f_{-3dB} = \frac{1}{2\pi R_{out}C_{out}} = \underline{\underline{0.697\ \text{MHz}}}$$

Problem 5.1-08

What is the small-signal voltage gain of a current-sink inverter with $W_1 = 2\mu\text{m}$, $L_1 = 1\mu\text{m}$, $W_2 = L_2 = 1\ \mu\text{m}$ at I_D = 0.1, 5 and 100 μA? Assume that the parameters of the devices are given by Table 3.1-2.



1. $I_D = 0.1\ \mu A$

$$g_{m1} = \frac{I_{D1}}{n_p V_t} = \frac{(0.1\mu)}{(2.5)(26m)} = 1.538\ \mu\text{S}$$

$$A_v = -\frac{g_{m1}}{(g_{ds1}+g_{ds2})} = -\frac{g_{m1}}{I_D(\lambda_N+\lambda_P)} = \underline{\underline{-\ 170.9\ \text{V/V}}}$$

2. $I_D = 5\ \mu A$

$$g_{m1} = \sqrt{2K_P'\left(\frac{W}{L}\right)_1 I_{D1}} = 31.62 = 31.62\ \mu\text{S}$$

$$A_v = -\frac{g_{m1}}{(g_{ds1}+g_{ds2})} = -\frac{g_{m1}}{I_D(\lambda_N+\lambda_P)} = \underline{\underline{-\ 70.27\ \text{V/V}}}$$

3. $I_D = 100\ \mu A$

$$g_{m1} = \sqrt{2K_P'\left(\frac{W}{L}\right)_1 I_{D1}} = 141.42\ \mu S$$

$$A_v = -\frac{g_{m1}}{(g_{ds1}+g_{ds2})} = -\frac{g_{m1}}{I_D(\lambda_N+\lambda_P)} = \underline{\underline{-15.71\ \text{V/V}}}$$

Problem 5.1-09

A CMOS amplifier is shown. Assume M1 and M2 operate in the saturation region. a.) What value of V_{GG} gives 100µA through M1 and M2? b.) What is the DC value of v_{IN}? c.) What is the small signal voltage gain, v_{out}/v_{in}, for this amplifier? d.) What is the -3dB frequency in Hz of this amplifier if $C_{gd} = C_{gd} = 5fF$, $C_{bs} = C_{bd} = 30fF$, and $C_L = 500fF$?

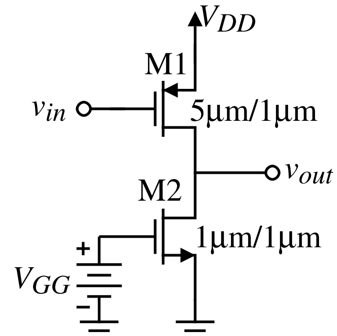


Figure P5.1-9

Solution

a) $V_{GG} = V_{T2} + V_{dsat2}$

$$V_{GG} = V_{T2} + \sqrt{\frac{2I_{D2}}{K_N'(W/L)_2}} = \underline{\underline{2.05\text{ V}}}$$

b) $$V_{in} = V_{DD} - V_{T1} - \sqrt{\frac{2I_{D1}}{K_P'(W/L)_1}} = \underline{\underline{3.406\text{ V}}}$$

c) $$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{(g_{ds1} + g_{ds2})} = \underline{\underline{-24.85\text{ V/V}}}$$

d) $$f_{-3dB} = \frac{(g_{ds1} + g_{ds2})}{2\pi(C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L)} = \underline{\underline{2.51\text{ MHz}}}.$$

Problem 5.1-10

A current-source load amplifier is shown. (a.) If $C_{BDN} = C_{BDP}$ = 100fF, $C_{GDN} = C_{GDP}$ = 50fF, $C_{GSN} = C_{GSP}$ = 100fF, and C_L = 1pF, find the -3dB frequency in Hertz. (b.) If Boltzmann's constant is $1.38\text{x}10^{-23}$ Joules/°K, find the equivalent input thermal noise voltage of this amplifier at room temperature (ignore bulk effects, $\eta = 0$).

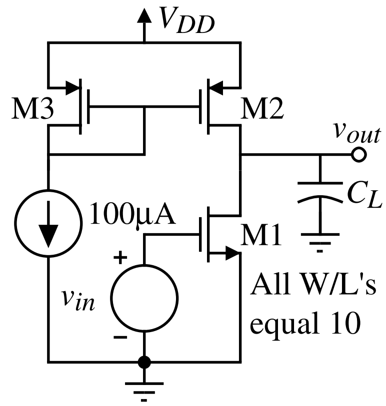


Fig. P5.1-10

Solutions

(a.) The -3dB frequency is equivalent to the magnitude of the output pole which is given as

$$\omega_{\text{-3dB}} = \frac{1}{R_{out}C_{out}} \quad \text{where } R_{out} = \frac{1}{g_{ds1}+g_{ds2}} = \frac{1}{100\mu\text{A}(0.04+0.05)} = \frac{1}{9\text{x}10^{-6}} = 111\text{k}\Omega$$

$$C_{out} = C_{gd1}+C_{bd1}+C_{gd2}+C_{bd2}+C_L = 0.05 + 0.05 + 0.1 + 0.1 +1 \text{ pF} = 1.3\text{pF}$$

$$\therefore\ \omega_{\text{-3dB}} = \frac{1}{0.111\text{M}\Omega\cdot 1.3\text{pF}} = 6.923\text{x}10^6 \text{ rads/sec.} \rightarrow \boxed{f_{\text{-3dB}} = 1.102 \text{ MHz}}$$

(b.) The noise voltage at the output can be written as

$$\overline{e_{no}}^2 = \overline{e_{n1}}^2\left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right)^2 + \overline{e_{n2}}^2\left(\frac{g_{m2}}{g_{ds1}+g_{ds2}}\right)^2$$

Reflecting this noise voltage back to the input gives the equivalent input noise as,

$$\overline{e_{ni}}^2 = \overline{e_{n1}}^2\left[1+\left(\frac{g_{m2}}{g_{m1}}\right)^2\left(\frac{e_{n2}}{e_{n1}}\right)^2\right] = \overline{e_{n1}}^2\left[1+\left(\frac{g_{m2}}{g_{m1}}\right)^2\left(\frac{\frac{8kT}{3g_{m2}}}{\frac{8kT}{3g_{m1}}}\right)\right] = \overline{e_{n1}}^2\left(1+\frac{g_{m2}}{g_{m1}}\right)$$

where

$$g_{m1} = \sqrt{\frac{2I_DK_N\text{W}_1}{\text{L}_1}} = 469\mu\text{S},\ g_{m2} = \sqrt{\frac{2I_DK_P\text{W}_2}{\text{L}_2}} = 316\mu\text{S},$$

and $$\overline{e_{n1}}^2 = \frac{8kT}{3\text{g}_{m1}} = \frac{8\cdot 1.38\text{x}10^{-23}\cdot 300}{3\cdot 469\text{x}10^{-6}} = 2.354\text{x}10^{-17}\ \text{V}^2/\text{Hz}$$

$$\boxed{\overline{e_{ni}}^2 = 2.354\text{x}10^{-17}\cdot 1.6738 = 3.94\text{x}10^{-17}\text{V}^2/\text{Hz} \rightarrow \overline{e_{ni}} = 6.277\text{nV}/\sqrt{\text{Hz}}}$$

Problem 5.1-11

Six inverters are shown. Assume that $K_N' = 2K_P'$ and that $\lambda_N = \lambda_P$, and that the dc bias current through each inverter is equal. Qualitatively select, without using extensive calculations, which inverter(s) has/have (a.) the largest ac small signal voltage gain, (b.) the lowest ac small signal voltage gain, (c.) the highest ac output resistance, and (d.) the lowest ac output resistance. Assume all devices are in saturation.

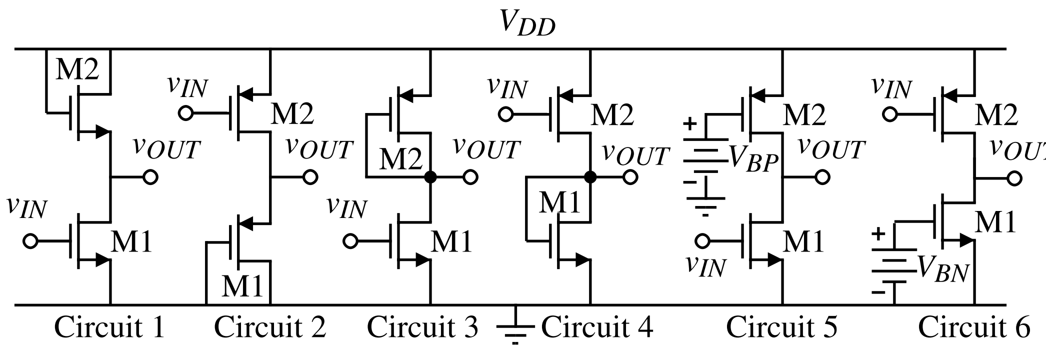


Figure P5.1-11

Solution

	Circuit 1	Circuit 2	Circuit 3	Circuit 4	Circuit 5	Circuit 6
g_m	$g_{mN}=\sqrt{2}\,g_{mP}$	g_{mP}	$g_{mN}=\sqrt{2}\,g_{mP}$	g_{mP}	$g_{mN}=\sqrt{2}\,g_{mP}$	g_{mP}
R_{out}	$\approx\frac{1}{g_{mN}+g_{mbN}}$ $=\frac{0.707}{g_{mP}+g_{mbP}}$	$\approx\frac{1}{g_{mP}+g_{mbP}}$	$\approx\frac{1}{g_{mP}}$	$\approx\frac{1}{g_{mN}}$ $\approx\frac{0.707}{g_{mP}}$	$\frac{1}{g_{dsN}+g_{dsP}}$ $=$ $\frac{1}{g_{dsP}(1+\sqrt{2})}$	$\frac{1}{g_{dsN}+g_{dsP}}$ $=$ $\frac{1}{g_{dsP}(1+\sqrt{2})}$
|Gain|	$\frac{g_{mP}}{g_{mP}+g_{mbP}}$	$\frac{g_{mP}}{g_{mP}+g_{mbP}}$	$\sqrt{2}$	$\frac{1}{\sqrt{2}}$	$\frac{\sqrt{2}\,g_{mP}}{g_{dsP}(1+\sqrt{2})}$	$\frac{g_{mP}}{g_{dsP}(1+\sqrt{2})}$

(a.) Circuit 5 has the highest gain.
(b.) Circuit 4 has the lowest gain (assuming normal values of g_m/g_{mb}).
(c.) Circuits 5 and 6 have the highest output resistance.
(d.) Circuit 1 has the lowest output resistance.

Problem 5.1-12

Derive the expression given in Eq. (5.1-29) for the CMOS push-pull inverter of Fig. 5.1-8. If $C_{gd1} = C_{gd2}$ = 5fF, $C_{bd1} = C_{bd2}$ = 50fF, C_L = 10 pF, and I_D = 200 μA, find the small-signal voltage gain and the −3 dB frequency if $W_1/L_1 = W_2/L_2$ = 5 of the CMOS push-pull inverter of Fig. 5.1-8.

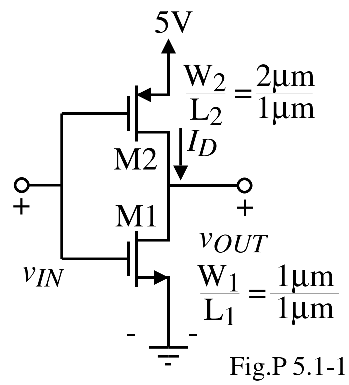


Fig.P 5.1-12

Solution

The effective transconductance can be given by

$$g_{m,eff} = g_{m1} + g_{m2} = \sqrt{2I_D}\left[\sqrt{K_N'\left(\frac{W}{L}\right)_1} + \sqrt{K_P'\left(\frac{W}{L}\right)_2}\right]$$

The output conductance can be given by

$$g_{out} = (g_{ds1} + g_{ds2}) = I_D(\lambda_1 + \lambda_2)$$

Thus, the small-signal gain becomes

$$A_v = -\frac{g_{m,eff}}{g_{out}}$$

$$A_v = -\sqrt{\frac{2}{I_D}}\left[\frac{\sqrt{K_N'\left(\frac{W}{L}\right)_1} + \sqrt{K_P'\left(\frac{W}{L}\right)_2}}{(\lambda_1 + \lambda_2)}\right] \qquad \text{Eq. (5.1-29)}$$

For $I_D = 200 \ \mu A$

$$A_v = -43.63 = \underline{\underline{-43.63\text{ V/V}}}$$

The total capacitance at the output node is

$$C_{total} = \left(C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L\right) = 10.11\text{ pF}.$$

Thus, the –3 dB frequency is

$$f_{-3dB} = \frac{g_{out}}{2\pi C_{total}} = \underline{\underline{283.36\text{ kHz}}}.$$

Problem 5.1-13

For the active-resistor load inverter, the current-source load inverter, and the push-pull inverter compare the active channel area assuming the length is 1μm if the gain is to be −1000 at a current of $I_D = 0.1\ \mu$A and the PMOS transistor has a *W*/*L* of 1.

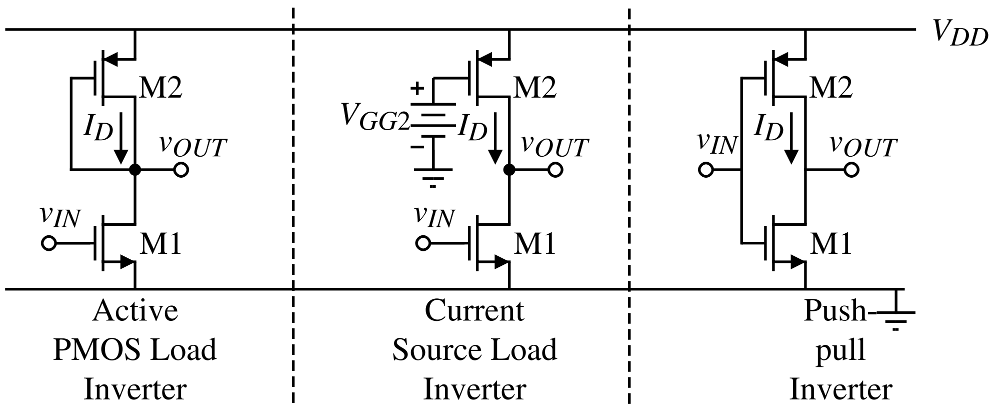


Figure 5.1-1 Various types of inverting CMOS amplifiers.

Soluton

Given, $I_D = 10\ \ \mu A$, and $A_v = -100$ V/V

a) Active-resistor load inverter

$$A_v \cong -\frac{g_{m1}}{g_{m2}} \quad\rightarrow\quad 100 = \sqrt{\frac{K_N'(W/L)_1}{K_P'(1)}} \quad\rightarrow\quad \frac{W_1}{L_1} = 4546$$

Active area = 4546·1 + 5·1 = 4551 μm²

b) Current-source load inverter

$$A_v = -\frac{g_{m1}}{(g_{ds1}+g_{ds2})} \quad\rightarrow\quad 100 = \sqrt{\frac{2K_N'(W/L)_1}{I_D(\lambda_1+\lambda_2)^2}} \quad\rightarrow\quad \frac{W_1}{L_1} = 3.64$$

Active area = 3.64·1 + 5·1 = 8.64 μm²

c) Push-pull inverter

$$A_v = -\frac{(g_{m1}+g_{m2})}{(g_{ds1}+g_{ds2})} \rightarrow \quad 100 = \sqrt{\frac{2K_N'(W/L)_1 + 2K_P'(1/1)}{I_D(\lambda_1+\lambda_2)^2}} \quad\rightarrow \frac{W_1}{L_1} = 1.55$$

Active area = 1.55·1 + 5·1 = 4.55 μm²

Problem 5.1-14

For the CMOS push-pull inverter shown, find the small signal voltage gain, A_v, the output resistance, R_{out}, and the -3dB frequency, f_{-3dB} if I_D = 200μA, $W_1/L_1 = W_2/L_2 = 5$, $C_{gd1} = C_{gd2}$ = 5fF, $C_{bd1} = C_{bd2}$ = 30fF, and C_L = 10pF.

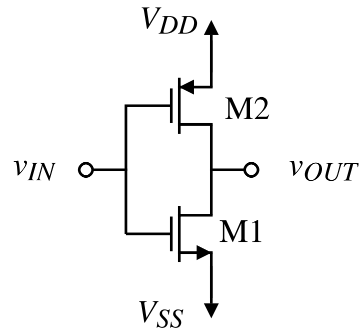


Fig. P5.1-14

Solution

The small-signal model for this problem is shown below.

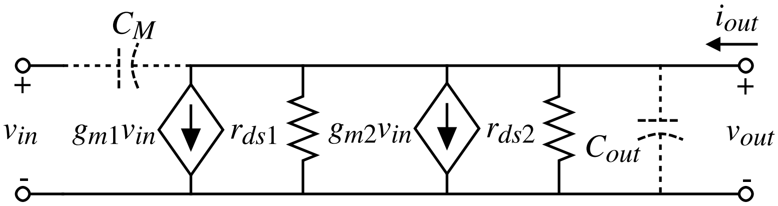


Fig. S5.1-14

Summing the currents at the output (ignoring the capacitors) gives,

$$g_{m1}v_{in} + g_{ds1}v_{out} + g_{m2}v_{in} + g_{ds2}v_{out} = 0$$

Solving for the voltage gain gives,

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}} = -\frac{\sqrt{2\frac{W_1}{L_1}I_DK_N}+\sqrt{2\frac{W_2}{L_2}I_DK_P}}{I_D(\lambda_N+\lambda_P)} = -\sqrt{\frac{2}{I_D}}\ \frac{\sqrt{\frac{W_1}{L_1}K_N}+\sqrt{\frac{W_2}{L_2}K_P}}{\lambda_N+\lambda_P}$$

$$\frac{v_{out}}{v_{in}} = A_v = -\sqrt{\frac{2}{200\text{x}10^{-6}}}\ \frac{\sqrt{5\cdot110\text{x}10^{-6}}+\sqrt{5\cdot50\text{x}10^{-6}}}{0.05+0.04} = -(100)(0.436) = -43.63\text{V/V}$$

∴ A_v = $\underline{\underline{-43.63\text{V/V}}}$

The output resistance is found by setting v_{in} = 0 and solving for v_{out}/i_{out}.

R_{out} is simply expressed as,

$$R_{out} = \frac{1}{g_{ds1}+g_{ds2}} = \frac{1}{I_D(\lambda_N+\lambda_P)} = \frac{1}{200\text{x}10^{-6}(0.05+0.04)} = 55.55\text{k}\Omega$$

∴ R_{out} = $\underline{\underline{55.55\text{k}\Omega}}$

From Eq. (5.1-26) we can solve for the –3dB frequency as

$$\omega_{-3\text{dB}} = \omega_1 = \frac{g_{ds1}+g_{ds2}}{C_{gd1}+C_{gd2}+C_{bd1}+C_{bd2}+C_L} = \frac{1}{R_{out}(C_{gd1}+C_{gd2}+C_{bd1}+C_{bd2}+C_L)}$$

$$= \frac{1}{55.55\text{x}10^{-3}(\text{ 5fF + 5fF + 30fF + 30fF + 10pF })} \approx \frac{1}{55.55\text{x}10^{3}\cdot10\text{x}10^{-12}} = 1.8\text{x}10^{6}\text{ rad/s}$$

∴ $\omega_{-3\text{dB}} = 1.8\text{x}10^6$ rad/s $\rightarrow$ $f_{-3\text{dB}}$ = $\underline{\underline{286.5\text{ kHz}}}$

Problem 5.2-01

Use the parameters of Table 3.1-2 to calculate the small-signal, differential-in, differential-out transconductance g_{md} and voltage gain A_v for the n-channel input, differential amplifier when I_{SS} = 100 μA and $W_1/L_1 = W_2/L_2 = W_3/L_3 = W_4/L_4 = 1$ assuming that all channel lengths are equal and have a value of 1μm. Repeat if $W_1/L_1 = W_2/L_2 = 10W_3/L_3 = 10W_4/L_4 = 10$.

Solution

Referring to Fig. 5.2-5 and given that

a) $$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 1$$

Differential-in differential-out transconductance is given by

$$g_{md} = g_{m1} = g_{m2} = \sqrt{K_N'\left(\frac{W}{L}\right)_1 I_{SS}} = \underline{\underline{104.8\ \mu\text{S}}}$$

Small-signal voltage gain is given by

$$A_v = \frac{g_{m2}}{\left(g_{ds2} + g_{ds4}\right)} = \frac{2g_{m2}}{I_{SS}\left(\lambda_2 + \lambda_4\right)} = \underline{\underline{23.31\ \text{V/V}}}$$

b) $$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 10\left(\frac{W}{L}\right)_3 = 10\left(\frac{W}{L}\right)_4 = 10$$

$$g_{md} = g_{m1} = g_{m2} = \underline{\underline{331.4\ \mu\text{S}}}$$

$$A_v = \frac{g_{m2}}{\left(g_{ds2} + g_{ds4}\right)} = \underline{\underline{36.82\ \text{V/V}}}$$

Problem 5.2-02

Repeat the previous problem for the p-channel input, differential amplifier.

Solution

Referring to Fig. 5.2-7 and given that

(a.) $\left(\dfrac{W}{L}\right)_1 = \left(\dfrac{W}{L}\right)_2 = \left(\dfrac{W}{L}\right)_3 = \left(\dfrac{W}{L}\right)_4 = 1$

Differential-in differential-out transconductance is given by

$$g_{md} = g_{m1} = g_{m2} = \sqrt{K_P^{'}\left(\frac{W}{L}\right)_1 I_{SS}} = \underline{\underline{70.71\ \mu\text{S}}}$$

Small-signal voltage gain is given by

$$A_v = \frac{g_{m2}}{\left(g_{ds2}+g_{ds4}\right)} = \frac{2g_{m2}}{I_{SS}\left(\lambda_2+\lambda_4\right)} = \underline{\underline{15.7\text{ V/V}}}$$

(b.) $\left(\dfrac{W}{L}\right)_1 = \left(\dfrac{W}{L}\right)_2 = 10\left(\dfrac{W}{L}\right)_3 = 10\left(\dfrac{W}{L}\right)_4 = 10$

$$g_{md} = g_{m1} = g_{m2} = \underline{\underline{223.6\ \mu\text{S}}}$$

$$A_v = \frac{g_{m2}}{\left(g_{ds2}+g_{ds4}\right)} = \underline{\underline{24.84\text{ V/V}}}$$

Problem 5.2-03

Develop the expressions for V_{IC}(max) and V_{IC}(min) for the p-channel input differential amplifier of Fig. 5.2-7.

Solution

The maximum input common-mode input is given by

$$V_{IC}(\text{max}) = V_{DD} - \left(|V_{T1}| + V_{dsat1} + V_{dsat5}\right)$$

or, $$\underline{\underline{V_{IC}(\text{max}) = V_{DD} - \left(|V_{T1}| + \sqrt{\frac{I_{DD}}{K_P^{'}(W/L)_1}} + \sqrt{\frac{2I_{DD}}{K_P^{'}(W/L)_5}}\right)}}$$

The minimum input common-mode input is given by

$$V_{IC}(\text{min}) = V_{SS} - |V_{T1}| + V_{T3} + V_{dsat3}$$

or, $$\underline{\underline{V_{IC}(\text{min}) = V_{SS} - |V_{T1}| + V_{T3} + \sqrt{\frac{I_{DD}}{K_N^{'}(W/L)_3}}}}$$

Problem 5.2-04

Find the maximum input common mode voltage, v_{IC}(max) and the minimum input common mode voltage, v_{IC}(min) of the n-channel input, differential amplifier of Fig. 5.2-5. Assume all transistors have a W/L of 10µm/1µm, are in saturation and I_{SS} = 10µA. What is the input common mode voltage range for this amplifier?

Solution

The maximum input common-mode input is given by

$$V_{IC}(\max) = V_{DD} + V_{T1} - V_{T3} - V_{dsat3}$$

or, $$V_{IC}(\max) = V_{DD} + V_{T1} - V_{T3} - \sqrt{\frac{I_{SS}}{K_P'(W/L)_3}} = \underline{\underline{4.86\text{ V}}}$$

The minimum input common-mode input is given by

$$V_{IC}(\min) = V_{SS} + V_{T1} + V_{dsat1} + V_{dsat5}$$

or, $$V_{IC}(\min) = V_{SS} + V_{T1} + \sqrt{\frac{I_{SS}}{K_N'(W/L)_1}} + \sqrt{\frac{2I_{SS}}{K_N'(W/L)_5}} = \underline{\underline{0.93\text{ V}}}$$

So, the input common-mode range becomes

$$ICMR = V_{IC}(\max) - V_{IC}(\min) = \underline{\underline{3.93\text{ V}}}$$

Problem 5.2-05

Find the small signal voltage gain, v_o/v_i, of the circuit in the previous problem if $v_{in} = v_1 - v_2$. If a 10pF capacitor is connected to the output to ground, what is the -3dB frequency for $V_{io}(j\omega)/V_{IN}(j\omega)$ in Hertz? (Neglect any device capacitance.)

Solution

Small-signal voltage gain is given by

$$A_v = \frac{g_{m2}}{(g_{ds2} + g_{ds4})} = \frac{2g_{m2}}{I_{SS}(\lambda_2 + \lambda_4)} = \underline{\underline{233.1\text{ V/V}}}$$

The –3 dB frequency is given by

$$f_{-3dB} \cong \frac{(g_{ds2} + g_{ds4})}{2\pi C_L} = \frac{I_{SS}(\lambda_2 + \lambda_4)}{4\pi C_L} = \underline{\underline{7.16\text{ kHz}}}.$$

Problem 5.2-06

For the CMOS differential amplifier of Fig. 5.2-5, find the small signal voltage gain, v_{out}/v_{in}, and the output resistance, R_{out}, if I_{SS} = 10µA, V_{DD} = 2.5V and $v_{in} = v_{gs1}-v_{gs2}$. If the gates of M1 and M2 are connected together, find the minimum and maximum common mode input voltage if all transistors must remain in saturation (ignore bulk effects).

Solution

Small-signal model for calculations:

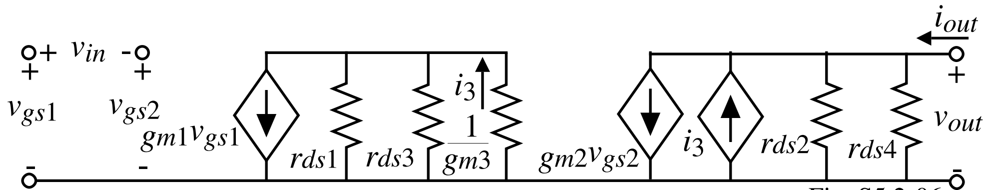


Fig. S5.2-06

$$R_{out} = \frac{1}{g_{ds2}+g_{ds4}} = \frac{1}{(0.04+0.05)5\mu\text{A}} = \underline{\underline{2.22\text{ M}\Omega}}$$

$$v_{out} = \left(\frac{g_{m1}g_{m3}r_{p1}}{1+g_{m3}r_{p1}}v_{gs1} - g_{m2}v_{gs2}\right)R_{out} \approx (g_{m1}v_{gs1}-g_{m2}v_{gs2})R_{out} = g_{m1}R_{out}v_{in}$$

$$\therefore \frac{v_{out}}{v_{in}} = g_{m1}R_{out} = g_{m2}R_{out}, \qquad g_{m1}= g_{m2} = \sqrt{2\cdot 110\cdot 5\cdot 2})\ \mu\text{S} = 46.9\ \mu\text{S}$$

$$\frac{v_{out}}{v_{in}} = 46.9\mu\text{S}\cdot 2.22\text{M}\Omega = \underline{\underline{104.1\text{ V/V}}}$$

Common mode input range:

$$V_{icm}(\text{max}) = V_{DD} - V_{SG3} + V_{TN} = 2.5 - \left(\sqrt{\frac{2\cdot 5}{50\cdot 2}}+0.7\right) + 0.7 = 2.5 - 0.3162 = \underline{\underline{2.184\text{ V}}}$$

$$V_{icm}(\text{min}) = 0+V_{DS5}(\text{sat})+V_{GS1}=\sqrt{\frac{2\cdot 10}{110\cdot 2}}\left(\sqrt{\frac{2\cdot 5}{110\cdot 2}}+0.7\right) = 0.3015+0.9132$$

$$= \underline{\underline{1.2147\text{ V}}}$$

Problem 5.2-07

Find the value of the unloaded differential-transconductance gain, g_{md}, and the unloaded differential-voltage gain, A_v, for the p-channel input differential amplifier of Fig. 5.2-7 when I_{SS} = 10 microamperes and I_{SS} = 1 microampere. Use the transistor parameters of Table 3.1-2.

Solution

Assuming all transistors have W/L = 1

a) Given, $I_{SS} = 10\ \mu A$

$$g_{md} = \sqrt{K_P'\left(\frac{W}{L}\right)_1 I_{SS}} = \underline{\underline{22.36\ \mu\text{S}}} \qquad A_v = \frac{g_{md}}{\left(g_{ds2} + g_{ds4}\right)} = \frac{2g_{md}}{I_{SS}\left(\lambda_2 + \lambda_4\right)} = \underline{\underline{49.69\ \text{V/V}}}$$

b) Given, $I_{SS} = 1\ \mu A$

$$g_{md} = \sqrt{K_P'\left(\frac{W}{L}\right)_1 I_{SS}} = \underline{\underline{7.07\ \mu\text{S}}} \qquad A_v = \frac{g_{md}}{\left(g_{ds2} + g_{ds4}\right)} = \frac{2g_{md}}{I_{SS}\left(\lambda_2 + \lambda_4\right)} = \underline{\underline{157.11\ \text{V/V}}}$$

Problem 5.2-08

What is the slew rate of the differential amplifier in the previous problem if a 100 pF capacitor is attached to the output?

Solution

Slew rate can be given as

$$SR = \frac{I_{SS}}{C_L}$$

For $I_{SS} = 10\ \mu A$ and $C_L = 100$ pF

$$SR = \frac{I_{SS}}{C_L} = \underline{\underline{0.1\ \text{V}/\mu\text{s}}}$$

For $I_{SS} = 1\ \mu A$ and $C_L = 100$ pF

$$SR = \frac{I_{SS}}{C_L} = \underline{\underline{0.01\ \text{V}/\mu\text{s}}}$$

Problem 5.2-09

Assume that the current mirror of Fig. 5.2-5 has an output current that is 5% larger than the input current. Find the small signal common-mode voltage gain assuming that I_{SS} is 100μA and the W/L ratios are 2μm/1μm for M1, M2 and M5 and 1μm/1μm for M3 and M4.

Solution

Given that

$$I_{D4} = (1.05)I_{D3} \quad \text{or,} \quad I_{D2} = (1.05)I_{D1}$$

This mismatch in currents in the differential input pair will result in an input offset voltage.

Now, $I_{D1} + I_{D2} = I_{SS}$

So,

$$I_{D1} \cong (0.49)I_{SS} \text{ and } I_{D2} \cong (0.51)I_{SS}$$

To calculate the common-mode voltage gain, let us assume a small signal voltage v_s applied to both the gates of the differential input pair.

The small-signal output current i_{out} is given by

$$i_{out} = (i_{D4} - i_{D2})$$

where,

$$i_{D4} \cong \left(\frac{0.5g_{ds5}}{g_{m3}} g_{m4}\right)v_s$$

$$i_{D2} \cong (0.5g_{ds5})v_s$$

So,

$$i_{out} = (i_{D4} - i_{D2}) = (0.5g_{ds5})\left(\frac{g_{m4}}{g_{m3}} - 1\right)v_s$$

The output conductance can be given as

$$g_{out} \cong g_{ds4} \qquad \text{as } M_2 \text{ and } M_5 \text{ form a cascode structure.}$$

Thus,

$$v_{out} = \frac{i_{out}}{g_{out}} \cong \frac{g_{ds5}}{2g_{ds4}}\left(\frac{g_{m4}}{g_{m3}} - 1\right)v_s$$

or, $$\frac{v_{out}}{v_s} = \frac{g_{ds5}}{2g_{ds4}}\left(\frac{g_{m4}}{g_{m3}} - 1\right)$$

or, $$\frac{v_{out}}{v_s} = \frac{I_{SS}(\lambda_5)}{I_{SS}(\lambda_4)}\left(\sqrt{\frac{I_{D4}}{I_{D3}}} - 1\right)$$

or, $$\frac{v_{out}}{v_s} = 0.02 \text{ V/V}$$

Thus, the small-signal common-mode gain is approximately 0.02 V/V

Problem 5.2-10

Use the parameters of Table 3.1-2 to calculate the differential-in-to-single-ended-output voltage gain of Fig. 5.2-9. Assume that I_{SS} is 50 microamperes.

Solution

Let, the aspect ratio of all the transistors be 1.

The small-signal differential-in single-ended out voltage gain is given by

$$A_v = \frac{g_{m1}}{2g_{m3}} = \sqrt{\frac{K_N^{'}}{4K_P^{'}}\frac{\left(W/L\right)_1}{\left(W/L\right)_3}} = \underline{\underline{0.74\text{ V/V}}}$$

Problem 5.2-11

Perform a small-signal analysis of Fig. 5.2-10 that does not ignore r_{ds1}. Compare your results with Eq. (5.2-27).

Solution

Referring to Fig. 5.2-10

Applying KVL

$$v_{ic} - v_{gs1} = \left(g_{m1}v_{gs1}\right)2r_{ds5} + \left(\frac{v_o - \left(v_{ic} - v_{gs1}\right)}{r_{ds1}}\right)2r_{ds5}$$

or, $$v_{gs1}\left\{r_{ds1} + 2r_{ds5}\left(1 + g_{m1}r_{ds1}\right)\right\} + v_o\left(2r_{ds5}\right) = v_{ic}\left(r_{ds1} + 2r_{ds5}\right) \quad (1)$$

Also, applying KCL

$$\frac{-v_o}{\left(1/g_{m3} + r_{ds3}\right)} = g_{m1}v_{gs1} + \left(\frac{v_o - \left(v_{ic} - v_{gs1}\right)}{r_{ds1}}\right)$$

or, $$v_{gs1} = \frac{\left\{v_{ic} - v_o\left(1 + g_{m3}r_{ds1}\right)\right\}}{\left(1 + g_{m1}r_{ds1}\right)} \quad (2)$$

Putting Eq. (2) in Eq. (1), and assuming $g_{m1}r_{ds1} >> 1$

$$\frac{\left\{v_{ic} - v_o\left(1 + g_{m3}r_{ds1}\right)\right\}}{\left(1 + g_{m1}r_{ds1}\right)}\left(2r_{ds5}\left(1 + g_{m1}r_{ds1}\right)\right) + v_o\left(2r_{ds5}\right) = v_{ic}\left(r_{ds1} + 2r_{ds5}\right)$$

or, $$-v_o\left(g_{m3}r_{ds1}\right)2r_{ds5} = v_{ic}r_{ds1}$$

or, $$\frac{v_o}{v_{ic}} = -\frac{1}{\left(g_{m3}2r_{ds5}\right)}$$

Problem 5.2-12

Find the expressions for the maximum and minimum input voltages, v_{G1}(max) and v_{G1}(min) for the n-channel differential amplifier with enhancement loads shown in Fig. 5.2-9.

Solution

$$V_{G1}(\text{min}) = V_{T1} + V_{dsat1} + V_{dsat5}$$

or, $$V_{G1}(\text{min}) = V_{T1} + \sqrt{\frac{I_{SS}}{K_N'(W/L)_1}} + \sqrt{\frac{2I_{SS}}{K_N'(W/L)_5}}$$

$$V_{G1}(\text{max}) = V_{DD} + V_{T1} - V_{T3} + V_{dsat3}$$

or, $$V_{G1}(\text{max}) = V_{DD} + V_{T1} - V_{T3} + \sqrt{\frac{I_{SS}}{K_P'(W/L)_3}}$$

Problem 5.2-13

If all the devices in the differential amplifier of Fig. 5.2-9 are saturated, find the worst-case input offset voltage, V_{OS}, if $|V_{Ti}| = 1 \pm 0.01$ volts and $\beta_i = 10^{-5} \pm 5 \times 10^{-7}$ amperes/volt^2. Assume that

$$\beta_1 = \beta_2 = 10\beta_3 = 10\beta_4$$

and

$$\frac{\Delta\beta_1}{\beta_1} = \frac{\Delta\beta_2}{\beta_2} = \frac{\Delta\beta_3}{\beta_3} = \frac{\Delta\beta_4}{\beta_4}$$

Carefully state any assumptions that you make in working this problem.

Solution

Referring to the figure

$$V_{GS1} = V_{T1} + V_{dsat1}$$

or, $$V_{GS1} = V_{T1} + \sqrt{\frac{2I_{D1}}{\beta_1}}$$

$$V_{GS2} = V_{T2} + V_{dsat2}$$

or, $$V_{GS2} = V_{T2} + \sqrt{\frac{2I_{D2}}{\beta_2}}$$

The input-offset voltage can de defined as

$$|V_{OS}| = |V_{GS1} - V_{GS2}|$$

or, $$|V_{OS}| = |V_{T1} - V_{T2}| + \left|\sqrt{\frac{2I_{D1}}{\beta_1}} - \sqrt{\frac{2I_{D1}}{\beta_2}}\right|$$

Considering the transistors M_3 and M_4, mismatches in these two transistors would cause an offset voltage between the output nodes. But, if it is assumed that this offset voltage between the output nodes is small as compared to the drain-to-source voltages of the transistors M_1 and M_2, then

$$V_{DS1} \cong V_{DS2}$$

Thus, it is assumed here that

$$I_{D1} = I_{D2} = I$$

So, the input-offset voltage becomes

$$|V_{OS}| = |V_{T1} - V_{T2}| + \left|\sqrt{\frac{2I}{\beta_1}} - \sqrt{\frac{2I}{\beta_2}}\right|$$

Assuming $I = 50\ \mu A$, the worst-case input offset voltage can be given by

$$|V_{os}| = (1.01 - 0.99) + \left[\sqrt{\frac{2(50\mu)}{0.95(10\mu)}} - \sqrt{\frac{2(50\mu)}{1.05(10\mu)}}\right]$$

or, $V_{OS}(\text{max}) = \underline{\underline{0.18 \text{ V}}}$

Problem 5.2-14

Repeat Example 5.2-1 for a p-channel input, differential amplifier.

Solution

The best way to do this problem is to use the equations for the n-channel, source-coupled pair with opposite type transistor parameters and then subtract the result from 5V.

Eq. (5.2-15) gives

$$V_{IC}(\text{max}) = 4 - \left(\sqrt{\frac{2\cdot 50\mu\text{A}}{99\mu\text{A/V}^2\cdot 1}} + 0.85\right) + 0.55 = 4 - 1.855 + 0.55 = 2.695 \text{ volts}$$

Subtracting from 5V gives

$$V_{IC}(\text{min}) = 5 - 2.695 = \underline{\underline{2.305\text{ V}}}$$

and Eq. (5.2-17) gives

$$V_{IC}(\text{min}) = 0 + 0.2 + \left(\sqrt{\frac{2\cdot 50\mu\text{A}}{45\mu\text{A/V}^2\cdot 5}} + 0.85\right) = 0.2 + 1.517 = 1.717 \text{ volts}$$

Subtracting from 5 V gives,

$$V_{IC}(\text{max}) = 5 - 1.717 = \underline{\underline{3.282\text{ V}}}$$

Therefore, the worst-case input common-mode range is $\underline{\underline{0.978\text{V}}}$ with a nominal 5V power supply.

Problem 5.2-15

Five different CMOS differential amplifier circuits are shown in Fig. P5.12-15. Use the intuitive approach of finding the small signal current caused by the application of a small signal input, v_{in}, and write by inspection the approximate small signal output resistance, R_{out}, seen looking back into each amplifier and the approximate small signal, differential voltage gain, v_{out}/v_{in}. Your answers should be in terms of g_{mi} and g_{dsi}, i = 1 through 8. (If you have to work out the details by small signal model analysis, this problem will take too much time.)

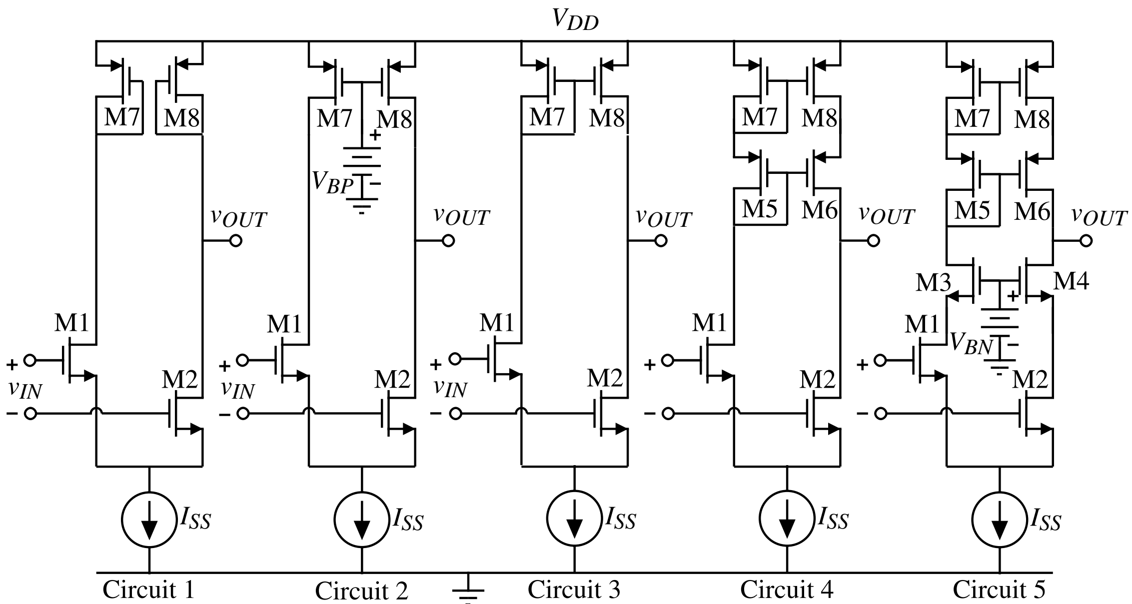


Figure P5.2-15

Solution

Assume $g_{m1} = g_{m2}$ otherwise multiply the gain of circuits 1 and 2 by $\dfrac{g_{m2}}{g_{m1}+g_{m2}}$.

Circuit	R_{out}	v_{out}/v_{in}
1	$\dfrac{1}{g_{ds2}+g_{m8}+g_{ds8}}$	$\dfrac{g_{m1}g_{m2}}{(g_{m1}+g_{m2})(g_{ds8}+g_{m8}+g_{ds8})} = \dfrac{0.5g_{m2}}{g_{ds2}+g_{m8}+g_{ds8}}$
2	$\dfrac{1}{g_{ds2}+g_{ds8}}$	$\dfrac{g_{m1}g_{m2}}{(g_{m1}+g_{m2})(g_{ds2}+g_{ds8})} = \dfrac{0.5g_{m2}}{g_{ds2}+g_{ds8}}$
3	$\dfrac{1}{g_{ds2}+g_{ds8}}$	$\dfrac{g_{m1}+g_{m2}}{2(g_{ds2}+g_{ds8})}$
4	$\dfrac{1}{g_{ds2}+\dfrac{g_{ds6}g_{ds8}}{g_{m6}}} = \dfrac{g_{m6}}{g_{ds6}g_{ds8}+g_{m6}g_{ds2}}$	$\dfrac{(g_{m1}+g_{m2})g_{m6}}{2(g_{m6}g_{ds2}+g_{ds6}g_{ds8})}$
5	$\dfrac{g_{m4}g_{m6}}{g_{ds2}g_{m6}g_{ds4}+g_{m6}g_{ds4}g_{ds8}}$	$\dfrac{(g_{m1}+g_{m2})g_{m4}g_{m6}}{2(g_{ds2}g_{m6}g_{ds4}+g_{m6}g_{ds4}g_{ds8})}$

Problem 5.2-16

If the equivalent input-noise voltage of each transistor of the differential amplifier of Fig. 5.2-5 is 1n$V/\sqrt{\text{Hz}}$ find the equivalent input noise voltage for this amplifier if W_1/L_1 = W_2/L_2 = 2 μm/1 μm, W_3/L_3 = W_4/L_4 = 1 μm/1 μm and I_{SS} = 50 μA. What is the equivalent output noise current under these conditions?

Solution

From Equation. (5.2-39)

$$e_{eq}^2 = e_{n1}^2 + e_{n2}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(e_{n3}^2 + e_{n4}^2\right)$$

or, $$e_{eq}^2 = 2e_n^2\left(1 + \left(\frac{g_{m3}}{g_{m1}}\right)^2\right) = 2.455e_n^2$$

Given

$$e_n = 1 \ nV/\sqrt{Hz}$$

Thus,

$$e_{eq.} = \underline{\underline{1.567 \text{ nV}/\sqrt{\text{Hz}}}}$$

The equivalent output noise current is given by

$$i_{to}^2 = g_{m1}^2 e_{eq}^2$$

or, $$i_{to} = \underline{\underline{164 \text{ fA}/\sqrt{\text{Hz}}}}$$

<u>Problem 5.2-17</u>

Use the small-signal model of the differential amplifier using a current mirror load given in Fig. 5.2-8(a) and solve for the ac voltage at the sources of M1 and M2 when a differential input signal, v_{id}, is applied. What is the reason that this voltage is not zero?

Solution

Neglecting the current source i_3 in the figure, let us assume that

$$v_{g1} = -v_{g2} = \frac{v_{id}}{2}$$

Applying nodal analysis, we will get the following three equations

$$(g_{m1} + g_{ds1})v_{s1} = g_{m1}v_{g1} + (g_{m3} + g_{ds1})v_{D3} \quad (1)$$

$$(g_{m2} + g_{ds2})v_{s1} = g_{m2}v_{g2} + (g_{ds2} + g_{ds4})v_{out} \quad (2)$$

$$(g_{m1} + g_{m2} + g_{ds1} + g_{ds2} - g_{ds5})v_{s1} = g_{m1}v_{g1} + g_{m2}v_{g2} + g_{ds1}v_{D3} + g_{ds2}v_{out} \quad (3)$$

Now, assuming $g_m >> g_{ds}$, $g_{m1} = g_{m2}$, $g_{ds1} = g_{ds2}$, and $v_{g1} = -v_{g2} = \frac{v_{id}}{2}$

$$v_{s1} = \frac{g_{ds1}v_{D3} + g_{ds2}v_{out}}{(g_{m1} + g_{m2} + g_{ds1} + g_{ds2} - g_{ds5})}$$

or, $$v_{s1} = \frac{g_{ds1}v_{D3} + g_{ds2}v_{out}}{(2g_{m1} + 2g_{ds1} - g_{ds5})}$$

Substituting from Equations (1) and (2), we get

$$v_{s1} = \frac{g_{m1}\left(0.25 - \frac{g_{ds1}}{g_{m3}}\right)}{\left(0.75g_{m1} + g_{ds1}\left(2 - \frac{g_{m1}}{g_{m3}}\right) - g_{ds5}\right)} v_{id}$$

The value of v_{s1} is non-zero because the loads (M3 and M4) seen by the input transistors (M1 and M2) at their drains are different.

Problem 5.2-18

The circuit shown Fig. P5.2-18 called a folded-current mirror differential amplifier and is useful for low values of power supply. Assume that all W/L values of each transistor is 100.

a.) Find the maximum input common mode voltage, v_{IC}(max) and the minimum input common mode voltage, v_{IC}(min). Keep all transistors in saturation for this problem.

b.) What is the input common mode voltage range, ICMR?

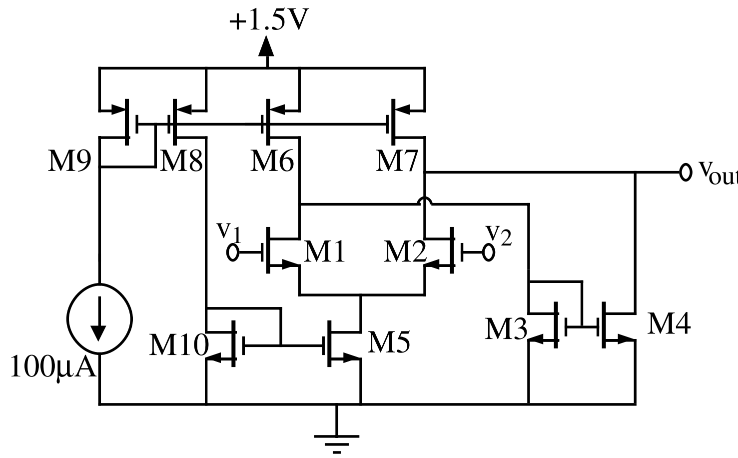


Fig. P5.2-18

c.) Find the small signal voltage gain, v_o/v_{in}, if $v_{in} = v_1 - v_2$.

d.) If a 10 pF capacitor is connected to the output to ground, what is the -3dB frequency for $V_o(j\omega)/V_{in}(j\omega)$ in Hertz? (Neglect any device capacitance.)

Solution

a.) $v_1(\max) = V_{DD} - V_{DS6}(\text{sat}) + V_{TN} = 1.5 - \sqrt{\dfrac{200}{50\cdot 100}} + 0.7 = 1.5 - 0.2 + 0.7$

$\therefore \boxed{v_1(\max) = 2\text{V}}$

$$v_1(\min) = 0 + V_{DS5}(\text{sat}) + V_{GS1}(50\mu\text{A}) = \sqrt{\frac{2\cdot 100}{110\cdot 100}} + \left(\sqrt{\frac{2\cdot 50}{110\cdot 100}} + 0.7\right)$$

$$= 0.1348 + 0953 + 0.7 = 0.9302\text{V} \Rightarrow \boxed{v_1(\min) = 0.9302\text{V}}$$

b.) $\boxed{\text{ICMR} = v_1(\max) - v_1(\min) = 1.0698\text{V}}$

c.) Using intuitive analysis approach gives:

$$i_{d1} = g_{m1}\left(\frac{v_{in}}{2}\right) \Rightarrow i_{d3} = -g_{m1}\left(\frac{v_{in}}{2}\right) \Rightarrow i_{d4} = -g_{m1}\left(\frac{v_{in}}{2}\right)$$

Also,

$$i_{d2} = -g_{m2}\left(\frac{v_{in}}{2}\right). \quad \therefore \; v_{out} = -R_{out}(i_{d2} + i_{d4})$$

However, $R_{out} = r_{ds2}||r_{ds4}||r_{ds7} = \dfrac{1}{g_{ds2}+g_{ds4}+g_{ds7}} \Rightarrow \dfrac{v_{out}}{v_{in}} = \dfrac{g_{m1}}{g_{ds2}+g_{ds4}+g_{ds7}}$

$$g_{m1} = \sqrt{2\cdot 50\cdot 110\cdot 100} = 1049\mu\text{S}, \; g_{ds2} = g_{ds4} = 0.04\cdot 50 = 2\mu\text{S}$$

and $g_{ds7} = 0.05\cdot 100 = 5\mu\text{S}$

$$\therefore \boxed{\frac{v_{out}}{v_{in}} = \frac{1049}{7} = 149.8\text{V/V}}$$

d.) $\omega_{-3dB} = \dfrac{1}{R_{out}10\text{pF}} = \dfrac{7\text{x}10^{-6}}{10\text{x}10^{-12}} = 0.7\text{x}10^{6} \rightarrow \therefore \boxed{f_{-3dB} = 111.4\text{kHz}}$

<u>Problem 5.2-19</u>

Find an expression for the equivalent input noise voltage of Fig. P5.2-18, $\overline{v_{eq}^2}$, in terms of the small signal model parameters and the individual equivalent input noise voltages, $\overline{v_{ni}^2}$, of each of the transistors (i = 1 through 7). Assume M1 and M2, M3 and M4, and M6 and M7 are matched.

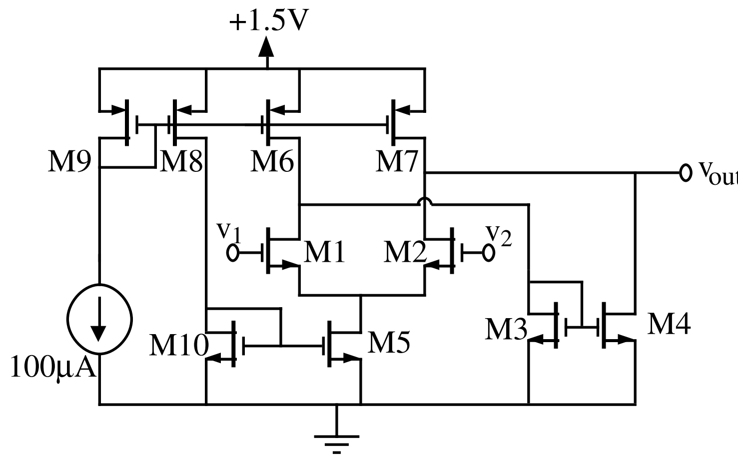
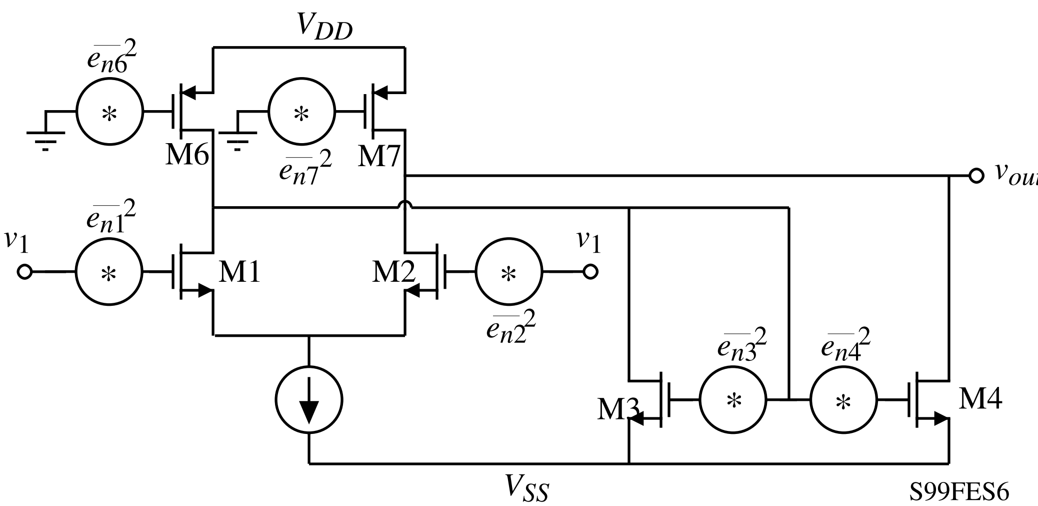


Fig. P5.2-18

<u>Solution</u>

Equivalent noise circuit:



$$\overline{e_{out}^2} = (g_{m1}^2\overline{e_{n1}^2} + g_{m2}^2\overline{e_{n2}^2} + g_{m3}^2\overline{e_{n3}^2} + g_{m4}^2\overline{e_{n4}^2} + g_{m5}^2\overline{e_{n6}^2} + g_{m6}^2\overline{e_{n7}^2})R_{out}^2$$

$$\overline{e_{eq}^2} = \frac{\overline{e_{out}^2}}{(g_{m1}R_{out})^2} = \overline{e_{n1}^2} + \overline{e_{n2}^2} + \left(\frac{g_{m1}}{g_{m3}}\right)^2(\overline{e_{n3}^2} + \overline{e_{n4}^2}) + \left(\frac{g_{m1}}{g_{m6}}\right)^2(\overline{e_{n6}^2} + \overline{e_{n7}^2})$$

If M1 through M2 are matched then $g_{m1} = g_{m3}$ and we get

$$\overline{e_{eq}^2} = 4\overline{e_{n1}^2} + 2\left(\frac{g_{m1}}{g_{m6}}\right)^2\overline{e_{n6}^2}$$

Problem 5.2-20

Find the small signal transfer function $V_3(s)/V_{in}(s)$ of Fig. P5.2-20, where $V_{in} = V_1 - V_2$, for the capacitors shown in algebraic form (in terms of the small signal model parameters and capacitance). Evaluate the low-frequency gain and all zeros and poles if $I = 200\mu A$ and $C_1 = C_2 = C_3 = C_4 = 1pF$. Let all W/L = 10.

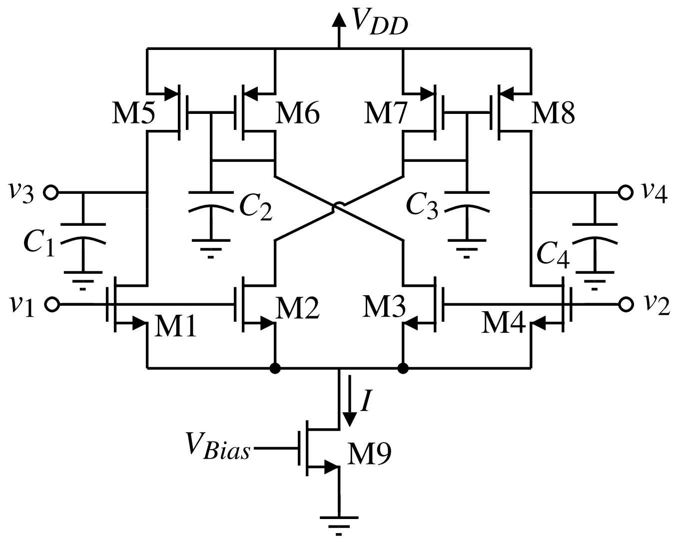


Fig. P5.2-20

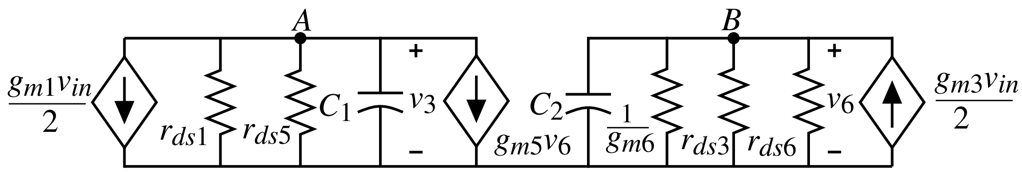
Solution

Small-signal model:L

$\Sigma i_A = 0$: ($G_{out} = g_{ds1} + g_{ds5}$)

$$0.5g_{m1}v_{in} + sC_1v_3 + G_{out}v_3 + g_{m5}v_6 = 0$$

$\Sigma i_B = 0$: $\quad sC_2v_6 + g_{m6}v_6 = 0.5g_{m3}v_{in} = 0 \quad \rightarrow \quad v_6 = \left(\frac{0.5g_{m3}}{sC_2 + g_{m6}}\right)v_6$



From the first equation we get,

$$v_3(sC_1 + G_{out}) + g_{m5}\left(\frac{0.5g_{m3}}{sC_2 + g_{m6}}\right)v_{in} + 0.5g_{m1}v_{in} = 0$$

Solving for v_3 gives,

$$\boxed{\frac{v_3}{v_{in}} = \left(\frac{-0.5g_{m1}}{sC_1 + G_{out}}\right)\left(\frac{sC_2 + g_{m5} + g_{m6}}{sC_2 + g_{m6}}\right)} \qquad \text{When } s \rightarrow 0, \quad \frac{v_3}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds5}}$$

$g_{mN} = \sqrt{2\cdot 50\mu A\cdot 110x10^{-6}\cdot 10} = 331.6\mu S$, $g_{mP} = \sqrt{2\cdot 50\mu A\cdot 50x10^{-6}\cdot 10} = 223.6\mu S$,

$r_{dsN} = \dfrac{1}{0.04\cdot 50x10^{-6}} = 0.5M\Omega$, and $r_{dsP} = \dfrac{1}{0.05\cdot 50x10^{-6}} = 0.4M\Omega$

$$\therefore \quad \frac{v_3}{v_{in}} = -\,g_{mN}\cdot R_{out} = -(331.6)(0.5||0.4) = \underline{\underline{-73.69\text{ V/V}}}$$

Poles are at,

$$p_1 = \frac{-1}{R_{out}C_1} = \frac{-1}{22.22k\Omega\cdot 1pF} = \underline{-4.5x10^6\text{rad/s}} \;\&\; p_2 = \frac{-g_{m6}}{C_2} = \frac{-223.6\mu S}{1pF} = \underline{-223.6\text{ x}10^6\text{ rad/s}}$$

A zero is at, $z_1 = \dfrac{-(g_{m5} + g_{m6})}{C_2} = \dfrac{-(223.6\mu S + 223.6\mu S)}{1pF} = \underline{\underline{-447.2\text{ x}10^6\text{ rad/s}}}$

Problem 5.2-21

For the differential-in, differential-out amplifier of Fig. 5.2-13, assume that all W/L values are equal and that each transistor has approximately the same current flowing through it. If all transistors are in the saturation region, find an algebraic expression for the voltage gain, v_{out}/v_{in}, and the differential output resistance, R_{out}, where $v_{out} = v_3\text{-}v_4$ and $v_{in} = v_1\text{-}v_2$. R_{out} is the resistance seen between the output terminals.

Solution

$$\frac{v_{out}}{v_{in}} = \frac{(v_3 - v_4)}{(v_1 - v_2)} = -\frac{g_{m1}}{(g_{ds1} + g_{ds3})}$$

or, $$\frac{v_{out}}{v_{in}} = -\sqrt{\frac{2K_N'\left(W/L\right)_1}{I_{BIAS}(\lambda_1 + \lambda_3)^2}}$$

Considering differential output voltage swing, the output resistance can be given by

$$R_{out} = \frac{1}{(g_{ds1} + g_{ds3})} + \frac{1}{(g_{ds2} + g_{ds4})}$$

or, $$R_{out} = \frac{2}{(g_{ds1} + g_{ds3})} = \frac{2}{I_{BIAS}(\lambda_1 + \lambda_3)}$$

Problem 5.2-22

Derive the maximum and minimum input common mode voltage for Fig. 5.2-15 assuming all transistors remain in saturation. What is the minimum power supply voltage, V_{DD}, that will give zero common input voltage range?

Solution

The minimum input common-mode voltage is given by

$$V_{IC}(\text{min}) = V_{T1} + V_{dsat1} + V_{dsat5}$$

The maximum input common-mode voltage is given by

$$V_{IC}(\text{max}) = V_{DD} + V_{T1} - V_{dsat3}$$

Assuming all the V_{dsat} voltages to be the same, the minimum supply voltage for zero input common mode can be given by

$$V_{IC}(\text{max}) - V_{IC}(\text{min}) = 0$$

or, $$(V_{DD} + V_{T1} - V_{dsat3}) - (V_{T1} + V_{dsat1} + V_{dsat5}) = 0$$

or, $$\underline{\underline{V_{DD} \approx 3V_{ds}(\text{sat})}}$$

Problem 5.2-23

Find the slew rate, *SR*, of the differential amplifier shown where the output is differential (ignore common-mode stability problems). Repeat this analysis if the two current sources, $0.5I_{SS}$, are replaced by resistors of R_L.

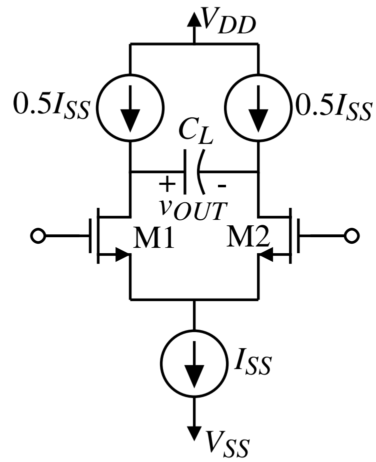


Fig. P5.2-23

Solution

a.) Slew rate of the differential output amplifier with constant current source loads.

Under large signal swing conditions, the maximum current that can be carried by each of the two transistors M_1 and M_2 is I_{SS}. Due to the presence of constant current sources as loads, the maximum charging or discharging current through C_L would be $0.5I_{SS}$. Thus, the slew rate can be given by

$$\boxed{SR = \frac{I_{SS}}{2C_L}}$$

b.) Slew rate of the differential output amplifier with resistive loads.

In presence of resistive loads, the maximum charging or discharging current through C_L would be I_{SS}. Thus, the slew rate can be given by

$$\boxed{SR = \frac{I_{SS}}{C_L}}$$

Problem 5.2-24

If all the devices in the differential amplifier shown in Fig. 5.2-5 are saturated, find the worst-case input-offset voltage V_{OS} using the parameters of Table 3.1-2. Assume that $10(W_4/L_4 = 10(W_3/L_3) = W_2/L_2 = W_1/L_1 = 10\ \mu\text{m}/10\ \mu\text{m}$. State and justify any assumptions used in working this problem.

Solution

The offset voltage between the input terminals is given by

$$|V_{os}| = |V_{GS1} - V_{GS2}|$$

The drain current equations are

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1} - V_{T1})^2$$

$$I_{D2} = \frac{\beta_2}{2}(V_{GS2} - V_{T2})^2$$

or, $$|V_{os}| = |V_{GS1} - V_{GS2}| = \left|(V_{T2} - V_{T1}) + \sqrt{\frac{2I_{D1}}{\beta_1}} - \sqrt{\frac{2I_{D2}}{\beta_2}}\right|$$

Mismatches would cause $I_{D1} \neq I_{D2}$. But, to simplify the problem, it can be assumed that $I_{D1} = I_{D2} = 0.5I_{SS}$. Under this assumption and considering the mismatches in V_T and β only, the worst-case input-offset voltage (from Table 3.1-2) can be given by

$$|V_{os}| = \left|0.3 + \sqrt{\frac{I_{SS}}{0.9\beta}} - \sqrt{\frac{I_{SS}}{1.1\beta}}\right|$$

Assuming

$$I_{SS} = 100\ \ \mu A$$

$$|V_{os}| = 0.3 + \sqrt{\frac{100\mu}{0.9(110\mu)(10/10)}} - \sqrt{\frac{100\mu}{1.1(110\mu)(10/10)}}\ \ = \underline{\underline{0.48\text{ V}}}$$

Problem 5.3-01

Calculate the small-signal voltage gain for the cascode amplifier of Fig. 5.3-2 assuming that the dc value of v_{IN} is selected to keep all transistors in saturation. Compare this value with the slope of the voltage transfer function given in this figure.

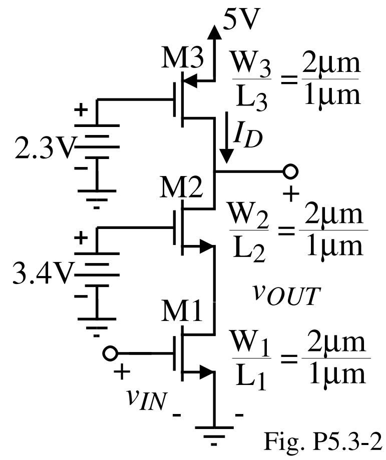


Fig. P5.3-2

Solution

The small-signal voltage gain can be approximated as

$$A_v \cong -\frac{g_{m1}}{g_{ds3}}$$

or, $$A_v \cong -\sqrt{\frac{2K_N'(W/L)_1}{I_{D3}\lambda_3^2}}$$

I_D is calculated from M3 as,

$$I_D = \frac{K_P'W_2}{2L_2}(V_{SG3}-|V_{TP}|)^2 = 50\cdot(2.7-0.7)^2\ \mu A = 200\mu A$$

$$\therefore \quad A_v = \sqrt{\frac{2K_N'(W_1/L_1)}{I_D\lambda_N^2}} = \sqrt{\frac{2\cdot 50\cdot 2}{200\cdot 0.05\cdot 0.05}} = \underline{\underline{-20\ V/V}}$$

From the transfer characteristics, the small-signal gain is approximately -10 V/V.

Problem 5.3-02

Show how to derive Eq. (5.3-6) from Eqs. (5.3-3) through (5.3-5). Hint: Assume that V_{GG2}-V_{T2} is greater than v_{DS1} and express Eq. (5.3-4) as $i_{D2} \approx \beta_2(V_{GG2}\text{-}V_{T2})v_{DS2}$. Solve for v_{OUT} as $v_{DS1} + v_{DS2}$ and simplify accordingly.

Solution

From Eqs. (5.3-3) through (5.3-5)

$$I_{D1} \cong \beta_1(V_{DD} - V_{T1})V_{ds1}$$

$$I_{D2} \cong \beta_2(V_{GG2} - V_{ds1} - V_{T2})(V_{out} - V_{ds1})$$

$$I_{D3} = 0.5\beta_3(V_{DD} - V_{GG3} - |V_{T3}|)^2$$

Assuming, when V_{in} is taken to V_{DD}, the magnitudes of V_{ds1} and V_{out} are small.
Equating $I_{D1} = I_{D3}$

$$\beta_1(V_{DD} - V_{T1})V_{ds1} = 0.5\beta_3(V_{DD} - V_{GG3} - |V_{T3}|)^2$$

or, $$V_{ds1} = \frac{0.5\beta_3(V_{DD} - V_{GG3} - |V_{T3}|)^2}{\beta_1(V_{DD} - V_{T1})} \tag{1}$$

Equating $I_{D1} = I_{D2}$

$$\beta_1(V_{DD} - V_{T1})V_{ds1} = \beta_2(V_{GG2} - V_{ds1} - V_{T2})(V_{out} - V_{ds1})$$

or, $$(V_{DD} - V_{T1})V_{ds1} = (V_{GG2} - V_{T2})(V_{out} - V_{ds1})$$

or, $$V_{ds1} = \frac{V_{out}(V_{GG2} - V_{T2})}{(V_{DD} + V_{GG2} - V_{T1} - V_{T2})} \tag{2}$$

From Eqs. (1) and (2), the minimum output voltage is given by

$$\boxed{V_{out}(\min) = \frac{\beta_3}{2\beta_1}\left(V_{DD} - V_{GG3} - |V_{T3}|\right)^2\left[\frac{1}{(V_{DD} - V_{T1})} + \frac{1}{(V_{GG2} - V_{T2})}\right]}$$

Problem 5.2-03

Redrive Eq. (5.3-6) accounting for the channel modulation where pertinent.

Solution

From Eqs. (5.3-3) through (5.3-5)

$$I_{D1} \cong \beta_1 (V_{DD} - V_{T1}) V_{ds1}$$

$$I_{D2} \cong \beta_2 (V_{GG2} - V_{ds1} - V_{T2})(V_{out} - V_{ds1})$$

$$I_{D3} = 0.5\beta_3 (V_{DD} - V_{GG3} - |V_{T3}|)^2 (1 + \lambda_3 (V_{DD} - V_{out}))$$

Assuming, when V_{in} is taken to V_{DD}, the magnitudes of V_{ds1} and V_{out} are small.

Equating $I_{D1} = I_{D3}$

$$\beta_1 (V_{DD} - V_{T1}) V_{ds1} = 0.5\beta_3 (V_{DD} - V_{GG3} - |V_{T3}|)^2 (1 + \lambda_3 (V_{DD} - V_{out}))$$

or, $$V_{ds1} = \frac{0.5\beta_3 (V_{DD} - V_{GG3} - |V_{T3}|)^2 (1 + \lambda_3 (V_{DD} - V_{out}))}{\beta_1 (V_{DD} - V_{T1})} \qquad (1)$$

Equating $I_{D1} = I_{D2}$

$$\beta_1 (V_{DD} - V_{T1}) V_{ds1} = \beta_2 (V_{GG2} - V_{ds1} - V_{T2})(V_{out} - V_{ds1})$$

or, $$(V_{DD} - V_{T1}) V_{ds1} = (V_{GG2} - V_{T2})(V_{out} - V_{ds1})$$

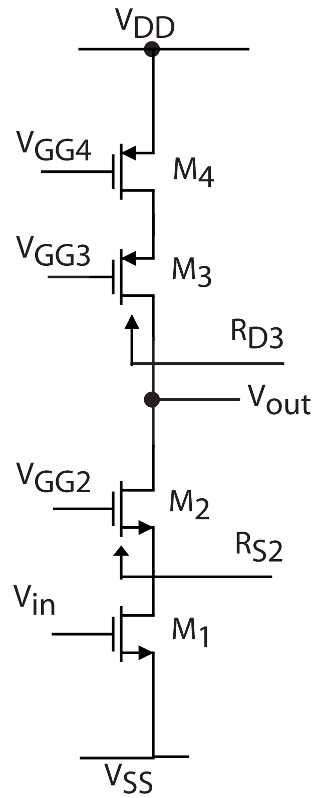
or, $$V_{ds1} = \frac{V_{out}(V_{GG2} - V_{T2})}{(V_{DD} + V_{GG2} - V_{T1} - V_{T2})} \qquad (2)$$

From Eqs. (1) and (2), assuming $V_{DD} - V_{out} \cong V_{DD}$, the minimum output voltage is given by

$$\boxed{V_{out}(\text{min}) = \frac{\beta_3}{2\beta_1}\left(V_{DD} - V_{GG3} - |V_{T3}|\right)^2 \left[\frac{1}{(V_{DD} - V_{T1})} + \frac{1}{(V_{GG2} - V_{T2})}\right](1 + \lambda_3 V_{DD})}$$

Problem 5.3-04

Show that the small signal input resistance looking in the source of M2 of the cascode amplifier of Fig. 5.3-1 is equal to r_{ds} if the simple current source, M3 is replaced by a cascode current source.



Solution

The effective resistance of the cascoded PMOS transistors is represented by R_{D3} and it is given by

$$R_{D3} \cong g_{m3}r_{ds3}r_{ds4}$$

Referring to the small-signal model in the figure

$$v_1 = \left[g_{m2}v_x + \frac{(v_x - v_1)}{r_{ds2}} \right] R_{D3}$$

or, $$v_1 = \frac{(1 + g_{m2}r_{ds2})R_{D3}}{(R_{D3} + r_{ds2})} v_x \qquad (1)$$

Now

$$i_x = g_{m2}v_x + \frac{(v_x - v_1)}{r_{ds2}} + \frac{v_x}{r_{ds1}}$$

$$i_x = (g_{m2} + g_{ds2} + g_{ds1})v_x - g_{ds2}v_1$$

$$i_x \cong g_{m2}v_x - g_{ds2}v_1$$

Replacing v_1 from Eq. (1) and assuming $R_{D3} >> r_{ds2}$

$$i_x \cong v_x \frac{[g_{m2}(R_{D3} + r_{ds2}) - g_{m2}R_{D3}]}{R_{D3}}$$

or, $$R_{S2} = \frac{v_x}{i_x} \cong \frac{R_{D3}}{g_{m2}r_{ds2}}$$

or, $$R_{S2} = \frac{g_{m3}r_{ds3}r_{ds4}}{g_{m2}r_{ds2}} = \underline{\underline{r_{ds}}}$$

Problem 5.3-05

Show how by adding a dc current source from V_{DD} to the drain of M1 in Fig. 5.3-1 that the small-signal voltage gain can be increased. Derive an expression similar to that of Eq. (11) in terms of I_{D1} and I_{D4} where I_{D4} is the current of the added dc current source. If I_{D2} = 10 μA, what value for this current source would increase the voltage gain by a factor of 10. How is the output resistance affected?

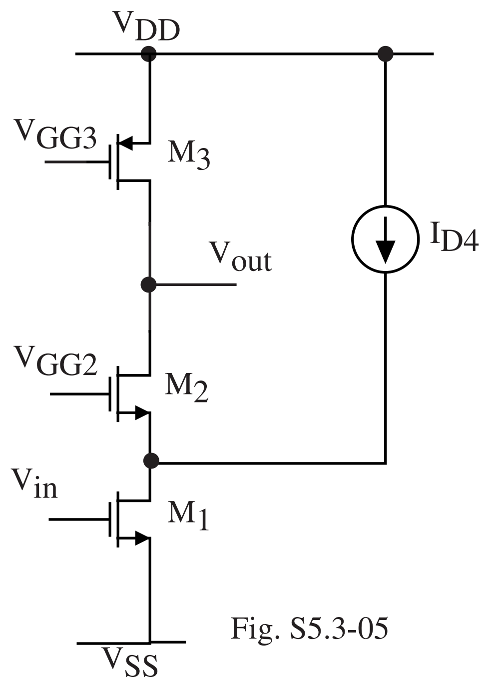


Fig. S5.3-05

Solution

Assuming all the transistors are in saturation

$$I_{D1} = I_{D2} + I_{D4}$$

$$A_v \cong -\frac{g_{m1}}{g_{ds3}}$$

or, $$A_v \cong -\sqrt{\frac{2K_N'\left(\frac{W}{L}\right)_1 (I_{D2}+I_{D4})}{I_{D2}^2\lambda_3^2}}$$

or, $$A_v \cong A_{vo}\sqrt{1+\frac{I_{D4}}{I_{D2}}}$$

where, $A_{vo} = -\sqrt{\dfrac{2K_N'\left(\frac{W}{L}\right)_1}{I_{D2}\lambda_3^2}}$ is the gain in absence of the current source I_{D4}

Thus, $$\frac{A_v}{A_{vo}} = \sqrt{1+\frac{I_{D4}}{I_{D2}}}$$

The small-signal voltage gain can be increased by making $I_{D4} >> I_{D2}$. In order to achieve

$$\frac{A_v}{A_{vo}} = 10 \qquad \rightarrow \qquad 10 = \sqrt{1+\frac{I_{D4}}{I_{D2}}}$$

or, $$I_{D4} = 99 I_{D2} = 990 \ \ \mu A$$

The output resistance can be given by

$$R_{out} \cong [g_{m2}r_{ds2}r_{ds1} \,\|\, r_{ds3}]$$

The value of r_{ds1} decreases due to increased current through M_1, thus decreasing the overall output resistance.

Problem 5.3-06

Assume that the dc current in each transistor in Fig. P5.3-6 is 100µA. If all transistor have a W/L of 10µm/1µm, find the small signal voltage gain, v_{out}/v_{in} and the small signal output resistance, R_{out}, if all transistors are in the saturated region.

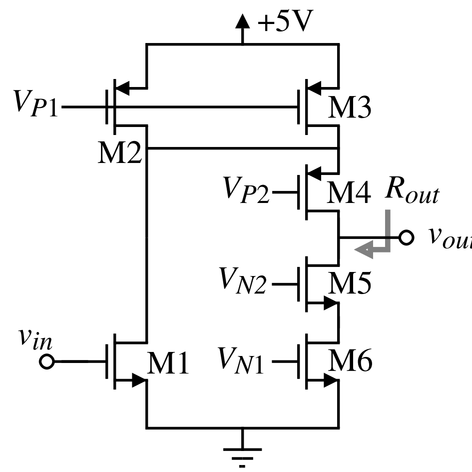


Fig. P5.3-6

Solution

This circuit is a folded cascode amplifier. The small signal analysis is best done by the schematic analysis approach. In words, v_{in} creates a current flowing into the drain of M1 of $g_{m1}v_{in}$. This current flows through M4 from drain to source back around to M1. The output voltage is simply this current times R_{out}. The details are:

$$v_{out} = -g_{m1}R_{out}v_{in}$$

$$R_{out} \approx [r_{ds6}(g_{m5}r_{ds5})]||[(r_{ds1}||r_{ds2}||r_{ds3})(g_{m4}r_{ds4})]$$

The various small signal parameters are:

$$g_{mN} = \sqrt{2\cdot 110\cdot 100\cdot 10} = 469\mu S, \quad g_{mP} = \sqrt{2\cdot 50\cdot 100\cdot 10} = 316.2\mu S$$

$$r_{dsN} = \frac{25V}{100\mu A} = 0.25M\Omega \quad \text{and} \quad r_{dsP} = \frac{20V}{100\mu A} = 0.2M\Omega$$

$$\therefore \; R_{out} \approx 29.31M\Omega||(0.0667M\Omega)(63.2) = 29.31M\Omega||4.216M\Omega = 3.686M\Omega$$

$$\boxed{R_{out} = 3.686M\Omega}$$

$$\boxed{\frac{v_{out}}{v_{in}} = -(469\mu S)(3.686M\Omega) = -1{,}729 \text{ V/V}}$$

Problem 5.3-07

Six versions of a cascode amplifier are shown below. Assume that $K'_N = 2K'_P$, $\lambda_P = 2\lambda_N$, all W/L ratios of all devices are equal, and that all bias currents in each device are equal. Identify which circuit or circuits have the following characteristics: (a.) highest small signal voltage gain, (b.) lowest small signal voltage gain, (c.) the highest output resistance, (d.) the lowest output resistance, (e.) the lowest power dissipation, (f.) the highest V_{out}(max), (g.) the lowest V_{out} (max), (h.) the highest V_{out} (min), (i.) the lowest V_{out} (min), and (j.) the highest -3dB frequency.

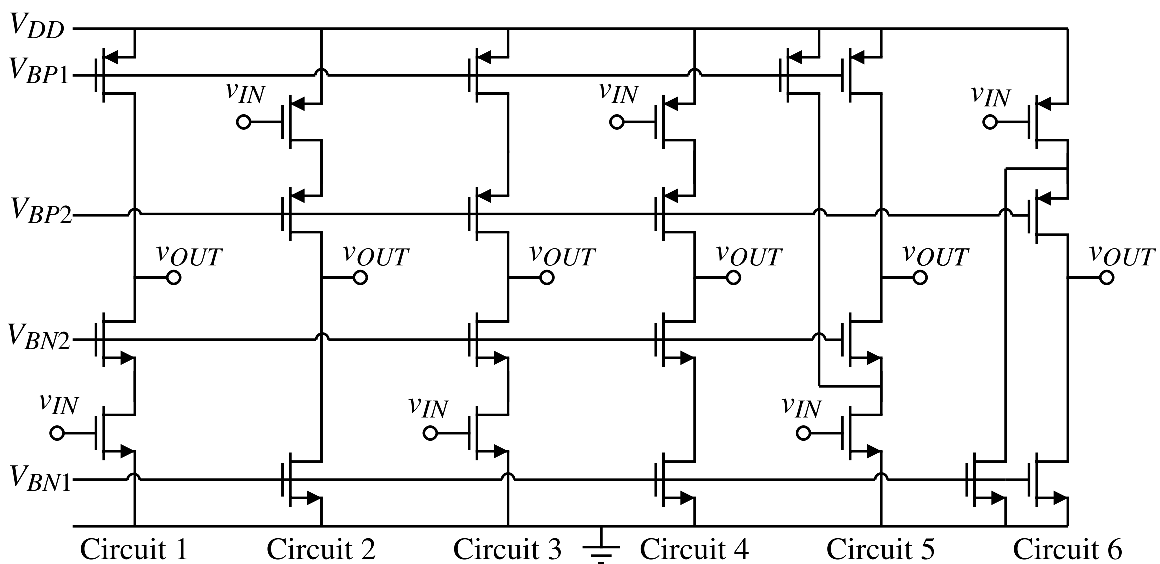


Figure P5.3-7

Solution

	Circuit 1	Circuit 2	Circuit 3	Circuit 4	Circuit 5	Circuit 6
g_m	g_{mN}	g_{mP}	g_{mN}	g_{mP}	$\sqrt{2}\, g_{mN}$	$\sqrt{2}\, g_{mP}$
R_{out}	$\approx r_{dsP}$	$\approx r_{dsN}$	R^*	R^*	$\approx r_{dsP}$	$\approx r_{dsN}$

$R^* = (g_{mP} \cdot r_{dsP}^2) || (g_{mN} \cdot r_{dsN}^2)$ Note that $g_{mN} = \sqrt{2}\, g_{mP}$ and $r_{dsN} = 2r_{dsP}$

e.) Circuit 3 has the highest gain.

f.) Circuit 1 has the lowest gain.

g.) Circuits 3 and 4 have the highest output resistance.

h.) Circuits 1 and 5 have the lowest output resistance.

i.) Circuits 1-4 have the lowest power dissipation.

j.) Circuits 1 and 5 have the highest V_{out}(max).

k.) Circuit 4 has the worst (lowest) V_{out}(max).

l.) Circuits 2 and 6 have the best (lowest) V_{out}(min).

m.) Circuit 3 has the worst (highest) V_{out}(min).

n.) Circuits 1 and 5 have the highest –3dB frequency because of lowest R_{out}.

Problem 5.3-08

All W/L ratios of each transistor in the amplifier shown in Fig. P5.3-8 are 10µm/1µm. Find the numerical value of the small signal voltage gain, v_{out}/v_{in}, and the output resistance, R_{out}.

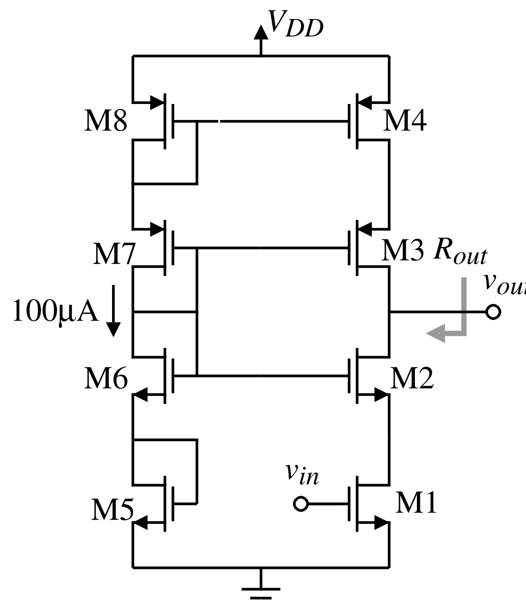


Figure P5.3-8

Solution

The output resistance can be given as

$$R_{out} \cong [g_{m2}r_{ds2}r_{ds1} \parallel g_{m3}r_{ds3}r_{ds4}]$$

Neglecting body effects

$$g_{m1} = g_{m2} = 469\ \mu S$$
$$g_{m3} = g_{m4} = 316\ \mu S$$

$$g_{ds1} = g_{ds2} = 4\ \mu S$$
$$g_{ds3} = g_{ds4} = 5\ \mu S$$

Thus, $R_{out} \cong [29.31M \parallel 12.64M]$

or, $R_{out} \approx \underline{\underline{8.838\ \text{M}\Omega}}$

The small-signal voltage gain is given as

$$\frac{v_{out}}{v_{in}} = -g_{m1}R_{out} = \underline{\underline{-41.42\ \text{V/V}}}$$

Problem 5.3-09

Use the Miller simplification described in Appendix A on the capacitor C_2 of Fig. 5.3-5(b) and derive an expression for the pole, p_1, assuming that the reactance of C_2 at the frequency of interest is greater than R_3. Compare your result with Eq. (5.3-32).

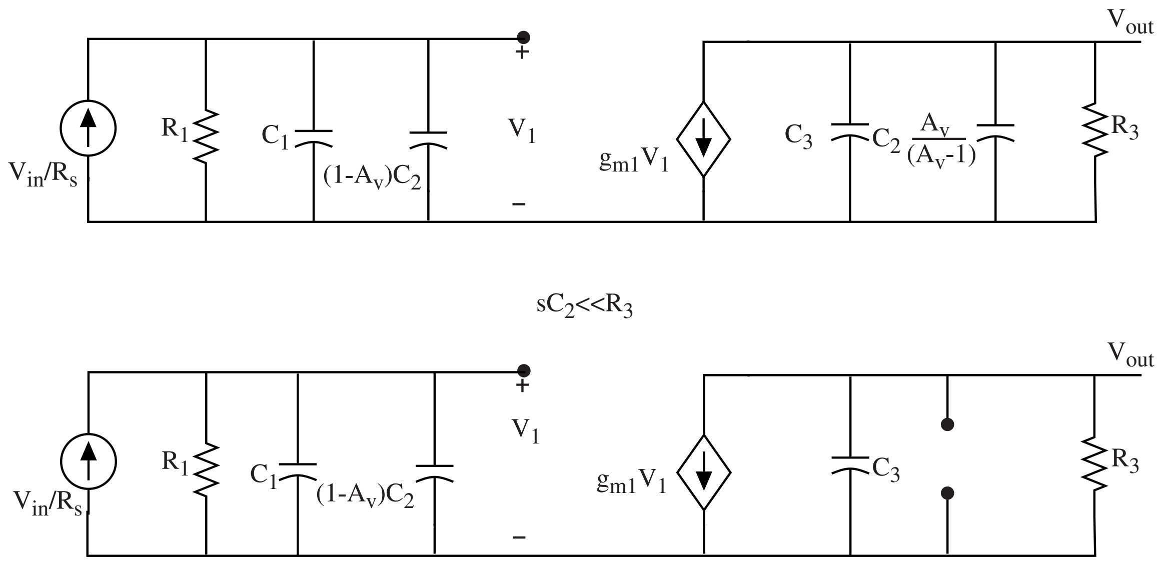


Fig. S5.3-09

Solution

Given that in the frequency of interest, the reactance of C_2 is greater than $1/R_3$

or, $\quad 2\pi f C_2 >> \dfrac{1}{R_3}$

Referring to the figure

$$V_1(s) = \frac{V_{in}(s)}{R_S\left[\dfrac{1}{R_1} + s\left(C_1 + (1+A_v)C_2\right)\right]} \qquad (1)$$

where, $A_v = g_{m1}R_3$

Also, $$V_o(s) = \frac{-g_{m1}V_1(s)}{\left(\dfrac{1}{R_3} + sC_3\right)} \cong \frac{-g_{m1}V_1(s)}{sC_3}$$

or, $$V_o(s) = \frac{-g_{m1}}{\left(\dfrac{1}{R_3} + sC_3\right)} \frac{V_{in}(s)}{R_S\left[\dfrac{1}{R_1} + s\left(C_1 + (1+A_v)C_2\right)\right]} \qquad (2)$$

The dominant pole in Eq. (2) can be expressed as

$$p_1 = \frac{-1}{R_1\left(A_vC_2 + C_1\right)} \cong \frac{-1}{R_1\left(A_vC_2\right)}$$

or, $$\boxed{p_1 = \frac{-1}{g_{m1}R_1R_3C_2}}$$

Problem 5.3-10

Consider the current-source load inverter of Fig. 5.1-5 and the simple cascode amplifier of Fig. 5.3-1. If the *W*/*L* ratio for M2 is 1 μm/1 μm and for M1 is 3 μm/1 μm of Fig. 5.1-5, and W_3/L_3 = 1 μm/1 μm, $W_2/L_2 = W_1/L_1$ = 3 μm/1 μm for Fig. 5.3-1, compare the minimum output-voltage swing, v_{OUT}(min) of both amplifiers if V_{GG2} = 0 V and V_{GG3} = 2.5 V when $V_{DD} = -V_{SS}$ = 5 V.

Solution

a) Current source load inverter

When $V_{in} = V_{DD}$, it can be assumed that M_1 operates in the triode region and M_2 is in saturation. Thus,

$$\beta_1(V_{DD} - V_{SS} - V_{T1})(V_{out}(\min) - V_{SS}) = 0.5\beta_2(V_{SG2} - |V_{T2}|)^2$$

or, $$V_{out}(\min) = \frac{0.5\beta_2(V_{SG2} - |V_{T2}|)^2}{\beta_1(V_{DD} - V_{SS} - V_{T1})} + V_{SS}$$

Assuming, $V_{SG2} = 5$ V

V_{out}(min) = $\underline{\underline{-4.85 \text{ V}}}$

b) Simple cascode amplifier

$$V_{out}(\min) = V_{SS} + V_{dsat1} + V_{dsat2}$$

or, $$V_{out}(\min) = V_{SS} + \sqrt{\frac{2I_{D1}}{K_N'(W/L)_1}} + \sqrt{\frac{2I_{D2}}{K_N'(W/L)_2}}$$

Now,

$$I_{D3} = \frac{\beta_3}{2}(V_{DD} - V_{GG3} - |V_{T3}|)^2 = 81 \ \mu A$$

Thus, V_{out}(min) = $\underline{\underline{-3.6 \text{ V}}}$

Problem 5.3-11

Use nodal analysis techniques on the cascode amplifier of Fig. 5.3-6(b) to find v_{out}/v_{in}. Verify the result with Eq. (5.3-37) of Sec. 5.3.

Solution

Nodal analysis of cascode amplifier

Applying KCL

$$g_{m1}v_{in} + g_{ds1}v_1 + g_{m2}v_1 + g_{mbs2}v_1 = g_{ds2}(v_{out} - v_1)$$

or, $$g_{m1}v_{in} + (g_{ds1} + g_{m2} + g_{mbs2} + g_{ds2})v_1 = g_{ds2}v_{out}$$

or, $$v_1 = \frac{(g_{ds2}v_{out} - g_{m1}v_{in})}{(g_{ds1} + g_{m2} + g_{mbs2} + g_{ds2})} \quad (1)$$

Again, applying KCL

$$g_{ds4}v_4 + g_{ds3}(v_4 - v_{out}) + g_{m3}v_4 + g_{mbs3}v_4 = 0$$

or, $$v_4 = \frac{g_{ds3}}{(g_{m3} + g_{ds3} + g_{ds4} + g_{mbs3})}v_{out} \quad (2)$$

Also,

$$(g_{m3} + g_{mbs3})v_4 + g_{ds3}(v_4 - v_{out}) + (g_{m2} + g_{mbs2})v_1 + g_{ds2}(v_1 - v_{out}) = 0$$

or, $$(g_{m3} + g_{mbs3} + g_{ds3})v_4 + (g_{m2} + g_{mbs2} + g_{ds2})v_1 = (g_{ds3} + g_{ds4})v_{out} \quad (3)$$

Using Eqs. (1) through (3) and neglecting body effect, it can be shown that

$$A_v = \frac{-g_{m1}g_{m2}g_{m3}}{(g_{m3}g_{ds1}g_{ds2} + g_{m2}g_{ds3}g_{ds4})}$$

or, $$A_v = \frac{-g_{m1}}{\left(\dfrac{g_{ds1}g_{ds2}}{g_{m2}} + \dfrac{g_{ds3}g_{ds4}}{g_{m3}}\right)}$$

or, $$A_v = \frac{-\sqrt{2K_1'(W/L)_1}}{I_D\left(\dfrac{\lambda_1\lambda_2}{\sqrt{2K_2'(W/L)_2}} + \dfrac{\lambda_3\lambda_4}{\sqrt{2K_3'(W/L)_3}}\right)} \quad \text{Eq. (5.3-37)}$$

Problem 5.3-12

Find the numerical value of the small signal voltage gain, v_{out}/v_{in}, for the circuit of Fig. P5.3-12. Assume that all devices are saturated and use the parameters of Table 3.1-2. Assume that the dc voltage drop across M7 keeps M1 in saturation.

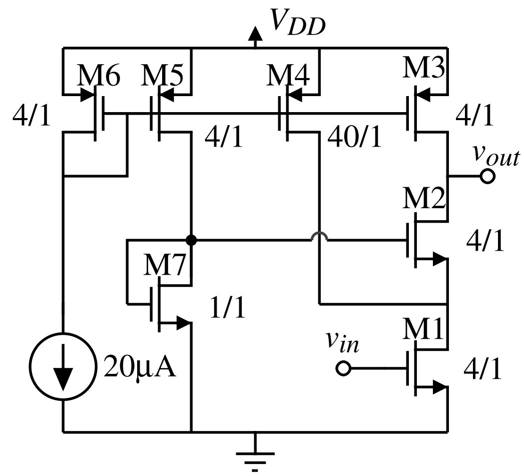


Fig. P5.3-12

Solution

$$I_{D3} = I_{D2} = 20\ \mu\text{A}$$

$$I_{D3} = 220\ \mu\text{A}$$

Now,

$$g_{m1} = 440\ \mu\text{S and } r_{ds1} = 113.64\ \text{k}\Omega$$

$$g_{m2} = 132.67\ \mu\text{S and } r_{ds2} = 1.25\ \text{k}\Omega$$

$$r_{ds3} = 1\ \text{M}\Omega$$

Thus,

$$R_{out} = \left[r_{ds3} \parallel g_{m2} r_{ds2} r_{ds1} \right]$$

or, $$R_{out} = [1M \parallel 18.8M] = 950\ \text{k}\Omega$$

So,

$$A_v = -g_{m1} R_{out} = \underline{\underline{\text{-418 V/V}}}$$

Problem 5.3-13

A cascoded differential amplifier is shown in Fig. P5.3-13.

(a) Assume all transistors are in saturation and find an algebraic expression for the small signal voltage gain, v_{out}/v_{in}.

(b) Sketch how would you implement V_{Bias}? (Use a minimum number of transistors.)

(c.) Suppose that $I_7+I_8 \neq I_9$. What would be the effect on this circuit and how would you solve it? Show a schematic of your solution. You should have roughly the same gain and the same output resistance.

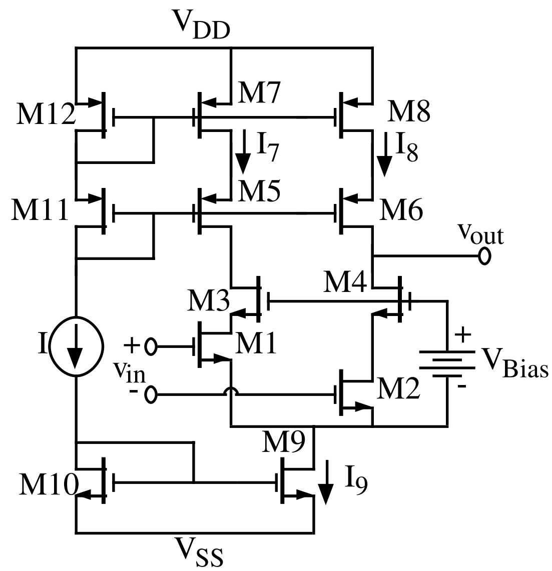


Fig. P5.3-13

Solution

a) The effective transconductance is given by

$$g_{m,eff} = \frac{g_{m1}}{2}$$

The output resistance of the cascoded output is given by

$$R_{out} = \left[\frac{1}{\dfrac{g_{ds2}g_{ds4}}{g_{m4}} + \dfrac{g_{ds6}g_{ds8}}{g_{m6}}} \right]$$

Thus, the small-signal voltage gain is given by

$$A_v = \left[\frac{0.5 g_{m1}}{\dfrac{g_{ds2}g_{ds4}}{g_{m4}} + \dfrac{g_{ds6}g_{ds8}}{g_{m6}}} \right]$$

b) The magnitude of V_{BIAS} should be at least $V_{GS} + V_{dsat}$. One way to implement V_{BIAS} is shown in Fig. 6.5-1(b) of the text.

c) If the currents were not equal, the voltages at the drains of M3-M5 and M4-M6 will near V_{DD} or near the sources of M1 and M2. Either, M5-M8 or M1-M4 will not be saturated. The best way to solve this problem is through the use of common mode feedback. This is illustrated in Fig. 5.2-15 of the text.

Problem 5.3-14

Design a cascode CMOS amplifier using Fig. 5.3-7 for the following specifications. V_{DD} = 5V, $P_{diss} \leq$ 0.5mW, $|A_v| \geq$ 100V/V, v_{OUT}(max) = 3.5V, v_{OUT}(min) = 1.5V, and slew rate of greater than 5V/µs for a 5pF capacitor load. Verify your design by simulation.

Solution

1.) The slew rate should be at least 5 V/µs driving a 5 pF load. So, the load current should be at least 25 µA.

Let,

$$I_{D3} = I_{D2} = I_{D1} = 25\ \mu\text{A}$$

2.) The maximum output voltage swing should be at least 3.5 V

Let, $V_{dsat3} = 1.5$ V

$$\left(\frac{W}{L}\right)_3 = \frac{2I_{D3}}{K_P^{'}V_{dsat3}^2} = 0.44$$

So, let us choose

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 1$$

3.) The small-signal voltage gain should be at least 100

$$A_v \cong -g_{m1}r_{ds3}$$

or, $$\left(\frac{W}{L}\right)_1 = \frac{(A_v\lambda_3)^2 I_{D1}}{2K_N^{'}} = 2.84$$

So, let us choose

$$\left(\frac{W}{L}\right)_1 = 3$$

$$V_{dsat1} = 0.39\ \text{V}$$

4.) The minimum output voltage swing should be greater than 1.5 V

$$V_{out}(\text{min}) = V_{dsat1} + V_{dsat2}$$

or, $$V_{dsat2} = V_{out}(\text{min}) - V_{dsat1} = 1.11\ \text{V}$$

or, $$\left(\frac{W}{L}\right)_2 = \frac{2I_{D2}}{K_N^{'}V_{dsat2}^2} = 0.37$$

So, let us choose

$$\left(\frac{W}{L}\right)_2 = 1$$

5.) The bias voltage V_{GG2} can be calculated as

$$V_{GG2} = V_{T1} + V_{dsat1} + V_{dsat2} = 1.76\ \text{V}$$

6.) The power dissipation is given by

$$P_{diss} = I_{D3}V_{DD} = 0.125\ \text{mW}$$

Problem 5.4-01

Assume that $i_o = A_i(i_p - i_n)$ of the current amplifier shown in Fig. P5.4-1. Find v_{out}/v_{in} and compare with Eq. (5.4-3).

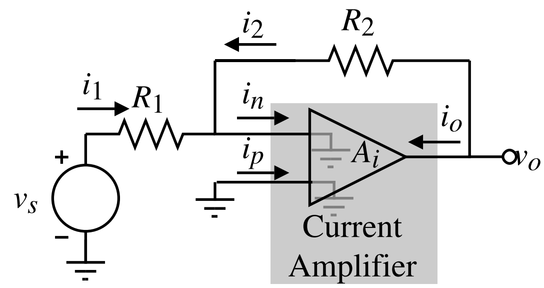


Figure P5.4-1

Solution

Referring to the figure, $i_p = 0$.

So, $i_o = A_i\left(i_p - i_n\right) = -A_i i_n$

Now, $v_{in} = i_1 R_1$

$v_o = -i_2 R_2$

or, $v_o = (i_1 - i_n)R_2 \quad \rightarrow \quad v_o = \left(\dfrac{v_{in}}{R_1} + \dfrac{i_o}{A_i}\right)R_2$

or, $v_o = \left(\dfrac{v_{in}}{R_1} + \dfrac{\left(-v_o/R_2\right)}{A_i}\right)R_2 \quad \rightarrow \quad \dfrac{v_o}{v_{in}} = \dfrac{R_2/R_1}{\left(1 + 1/A_i\right)}$ Eq. (5.4-3)

Problem 5.4-02

The simple current mirror of Fig. 5.4-3 is to be used as a current amplifier. If the W/L of M1 is 1µm/1µm, design the W/L ratio of M2 to give a gain of 10. If the value of I_1 is 100µA, find the input and output resistance assuming the current sources I_1 and I_2 are ideal. What is the actual value of the current gain when the input current is 50µA?

Solution

The current gain can be expressed as

$$A_i = \frac{(W/L)_2}{(W/L)_1}$$

For $A_i = 10$, $W_2 = 10$ µm and $L_2 = 1$ µm.

If $I_1 = 100$ µA, then $I_2 = 1000$ µA.

The input resistance is

$$R_{in} = \frac{1}{g_{m1}} = \underline{6.74\text{ k}\Omega}$$

The output resistance is

$$R_{out} = \frac{1}{\lambda_N I_{D2}} = \underline{\underline{25\text{ k}\Omega}}$$

When $I_1 = 50$ µA, then $I_2 = 500$ µA and the current gain (A_i) is still 10.

Problem 5.4-03

The capacitances of M1 and M2 in Fig. P.4-3 are C_{gs1}=C_{gs2}=20fF, C_{gd1}=C_{gd2} =5fF, and C_{bd1}=C_{bd2}=10fF. Find the low frequency current gain, i_{out}/i_{in}, the input resistance seen by i_{in}, the output resistance looking into the drain of M2, and the -3dB frequency in Hz.

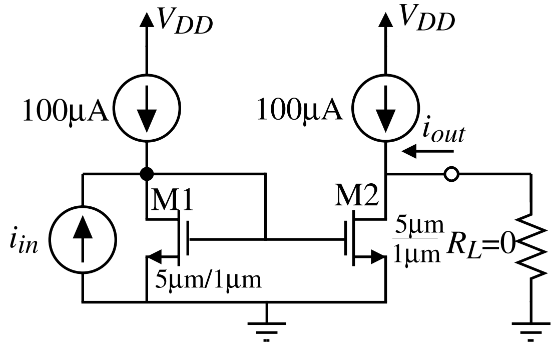
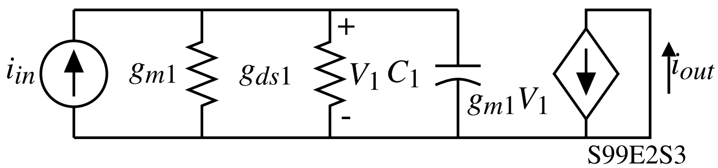


Fig. P5.4-3

Solution



(a.) Small-signal model is shown.

Note that

$$C_1 = C_{bd1} + C_{gs2} + C_{gd2} + C_{gs1} = 55\text{fF},$$

$$g_{m1} = g_{m2} = \sqrt{2K_N \frac{W_1}{L_1} I_1} = \sqrt{2\cdot 110\cdot 5\cdot 100} = 332\mu\text{S}$$

and

$$g_{ds1} = \lambda_N I_1 = 0.04\cdot 100\mu\text{A} = 4\mu\text{S}$$

The current gain is, $\quad i_{out} = g_{m2}\left(\dfrac{i_{in}}{g_{m1}+g_{ds1}+sC_1}\right)$

The low frequency current gain is

$$A_i(0) = \frac{g_{m2}}{g_{m1}+g_{ds1}} = \frac{332}{336} = 0.988 \Rightarrow \qquad \boxed{A_i(0) = 0.988}$$

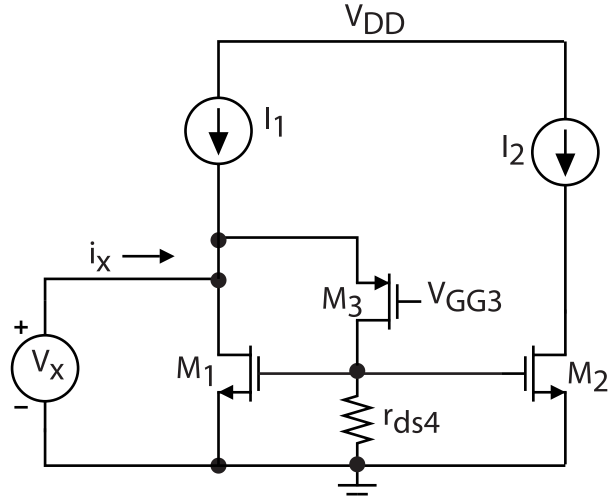
$$R_{in} = \frac{1}{g_{m1}+g_{ds1}} = \frac{1}{336\mu\text{S}} = 2.796\text{k}\Omega \qquad \Rightarrow \qquad \boxed{R_{in} = 2796\Omega}$$

$$R_{out} = 1/g_{ds2} = 1/g_{ds1} = 250\text{k}\Omega \qquad \Rightarrow \qquad \boxed{R_{out} = 250\text{k}\Omega}$$

$$\omega_{-3dB} = \frac{g_{m1}+g_{ds1}}{C_1} = \frac{332\mu\text{S}+4\mu\text{S}}{55\text{fF}} = 6.11\text{x}10^9 \qquad \Rightarrow \qquad \boxed{f_{-3dB} = 973\text{MHz}}$$

Problem 5.4-04

Derive an expression for the small-signal input resistance of the current amplifier of Fig. 5.4-5(a). Assume that the current sink, I_3, has a small signal resistance of r_{ds4} in your derivation.



Solution

Referring to the figure

$$v_{s3} = v_x$$

$$v_{g1} = v_{d3} \cong \frac{g_{m3}}{(g_{ds3} + g_{ds4})} v_x$$

$$i_x = i_{d1} + i_{d3}$$

or, $$i_x = g_{m1} v_{g1} + g_{m3} v_x$$

or, $$i_x = g_{m1} \frac{g_{m3}}{(g_{ds3} + g_{ds4})} v_x + g_{m3} v_x$$

or, $$\boxed{R_{in} = \frac{v_x}{i_x} \cong \frac{(g_{ds3} + g_{ds4})}{g_{m1} g_{m3}}}$$

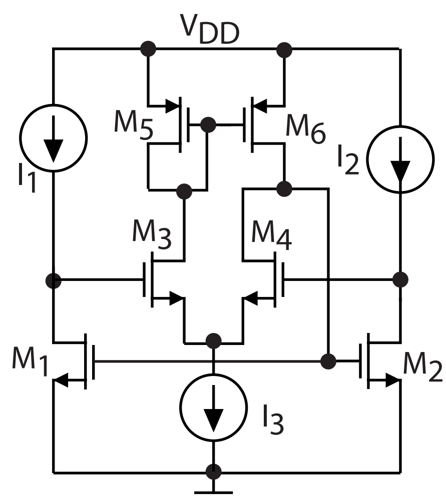
Problem 5.4-05

Show how to make the current accuracy of Fig. 5.4-5(a) better by modifying the circuit so that $V_{DS1} = V_{DS2}$.

Solution

Referring to the figure, M3-M6 form a differential amplifier. If it is assumed that the small-signal gain of this differential amplifier is large enough, then the bias voltages at the gates of M3 and M4 would almost be equal (because in presence of large gain, the differential input ports would act as null ports). Thus, the drain bias voltages of M1 and M2 would almost be identical causing very good mirroring.

It is also important to note that the bias voltage at the drain of M4 could be very large as gate bias voltages for M1 and M2. One can use a PMOS differential amplifier in place of the shown NMOS differential amplifier to overcome this problem.



Problem 5.4-06

Show how to use the improved high-swing current mirror of Sec. 4.4 to implement Fig. 5.4-7(a). Design the current amplifier so that the input resistance is 1kΩ and the dc bias current flowing into the input is 100µA (when no input current signal is applied) and the dc voltage at the input is 1.0V.

Solution

The high-swing cascode current mirror, constitut-ing the transistors M1 through M4, is shown in the figure. The overall figure shows a differential current amplifier. To design the high-swing cascode current mirror, it is desired that

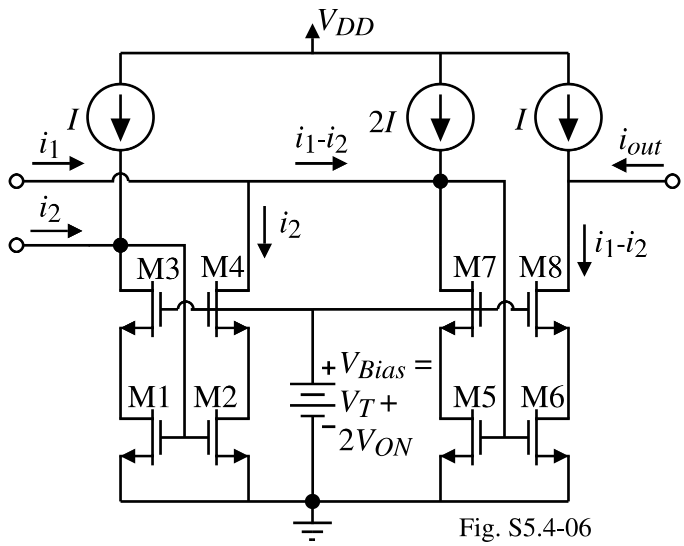


Fig. S5.4-06

$$R_{in} = 1\ \text{k}\Omega$$

or, $\quad g_{m1} = 1\ \mu\text{S}$

or, $\quad \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 45.5$

Let us assume

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 45.5$$

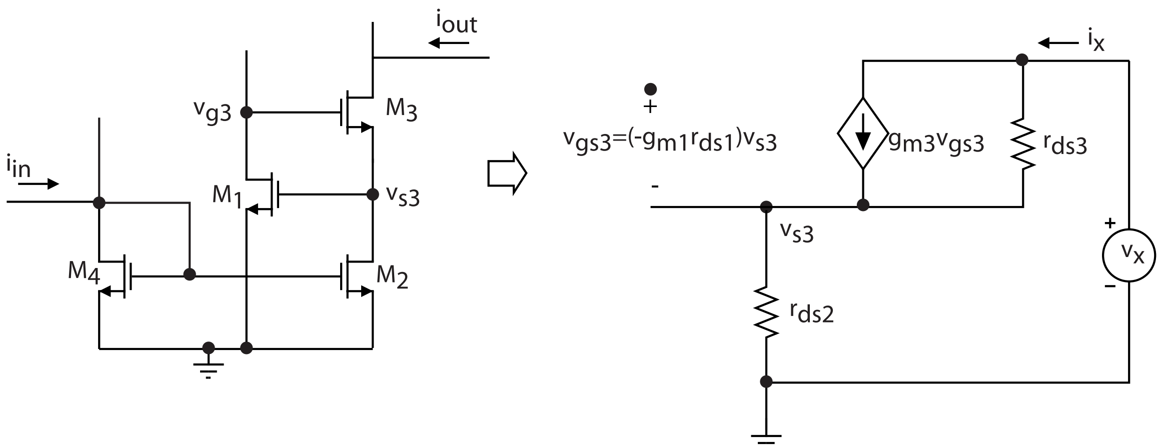
Then, ignoring bulk effects

$$V_{BIAS} = V_{T3} + V_{dsat3} + V_{dsat1} = 1.1\ \text{V}$$

Problem 5.4-07

Show how to use the regulated cascode mirror of Sec. 4.4 to implement a single-ended input current amplifier. Calculate an algebraic expression for the small signal input and output resistance of your current amplifier.

Solution



Referring to the figure, the current gain of the regulated cascode mirror can be expressed as

$$A_i = \frac{i_{out}}{i_{in}} \cong \frac{(W/L)_2}{(W/L)_4}$$

The input resistance is given by

$$R_{in} = \frac{1}{g_{m4}}$$

The output resistance can be calculated as follows:

$$v_{g3} = -(g_{m1}r_{ds1})v_{s3} \tag{1}$$

Now, $i_x = g_{m3}v_{gs3} + \dfrac{(v_x - v_{s3})}{r_{ds3}}$

or, $$i_x = -g_{m3}(g_{m1}r_{ds1})v_{s3} + \frac{(v_x - v_{s3})}{r_{ds3}} \tag{2}$$

Also, $$v_{s3} = i_x r_{ds2} \tag{3}$$

Using Eqs. (2) and (3), it can be shown that

$$v_x = i_x(g_{m1}r_{ds1}g_{m3}r_{ds3}r_{ds2})$$

or, $$\boxed{R_{out} = \frac{v_x}{i_x} = (g_{m1}r_{ds1}g_{m3}r_{ds3}r_{ds2})}$$

Problem 5.4-08

Find the exact expression for the small signal input resistance of the circuit shown when the output is short-circuited. Assume all transistors have identical W/L ratios, are in saturation and ignore the bulk effects. Simplify your expression by assuming that g_m=100g_{ds} and that all transistors are identical. Sketch a plot of i_{out} as a function of i_{in}.

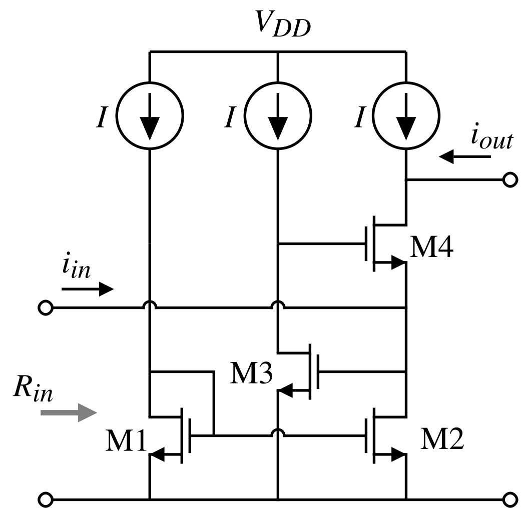
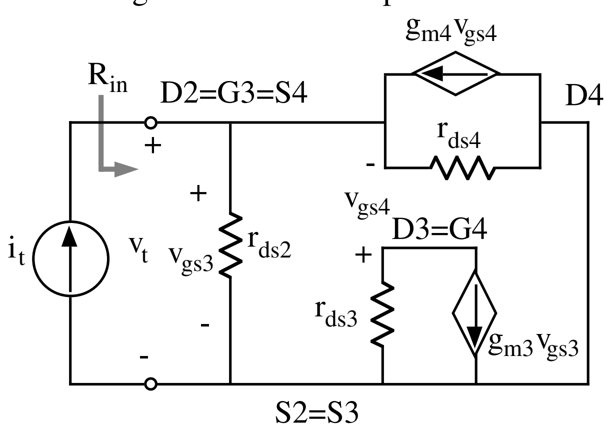


Figure P5.4-8

Solution

A small signal model for this problem is:



$$i_t = (g_{ds2}+g_{ds4})v_t - g_{m4}v_{gs4}$$

But, $v_{gs4} = -g_{m3}r_{ds3}v_{gs3} - v_t$

and

$v_{gs3} = v_t$

$\therefore \quad i_t = (g_{ds2}+g_{ds4})v_t + g_{m4}(1+g_{m3}r_{ds3})v_t$

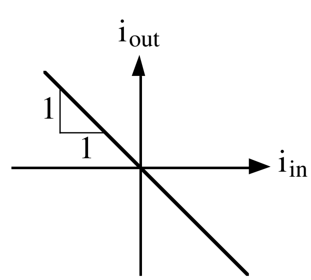
Thus, R_{in} is

$$\boxed{R_{in} = \frac{v_t}{i_t} = \frac{1}{g_{ds2}+g_{ds4}+g_{m4} + g_{m3}g_{m4}r_{ds3}} \approx \frac{1}{g_{m3}g_{m4}r_{ds3}}}$$

Sketching i_{out} as a function of i_{in}:

Note that $i_{D4} = I + i_{out}$ and $i_{D4} + i_{in} = i_{D2} = i_{D1} = I$

Therefore, $I + i_{out} = I - i_{in} \Rightarrow i_{out} = - i_{in}$



Problem 5.4-09

Find the exact small signal expression for R_{in} for the circuit in Fig. P5.4-9. Assume V_{DC} causes the current flow through M1 and M2 to be identical. Assume M1 and M2 are identical transistors and that the small signal r_{ds} of M5 can be ignored (do not neglect r_{ds1} and r_{ds2}).

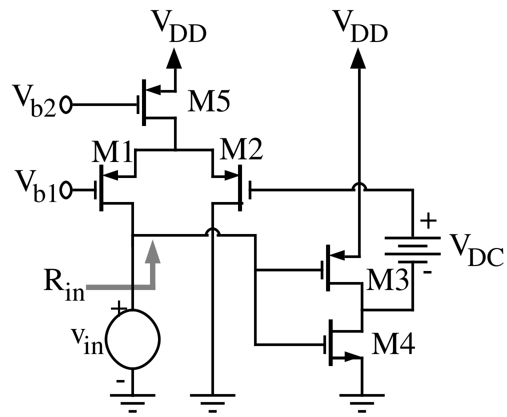


Fig. 5.4-9

Solution

The small-signal model is shown below.

We may write that,

$$v_{in} = v_{d1} = (i_{in} - g_{m1}v_{gs1})r_{ds1} + (i_{in} + g_{m2}v_{gs2})\, r_{ds2}$$

but $v_{gs1} = -\,v_{s1}$ and $v_{gs2} = v_{g2} - v_{s2}$

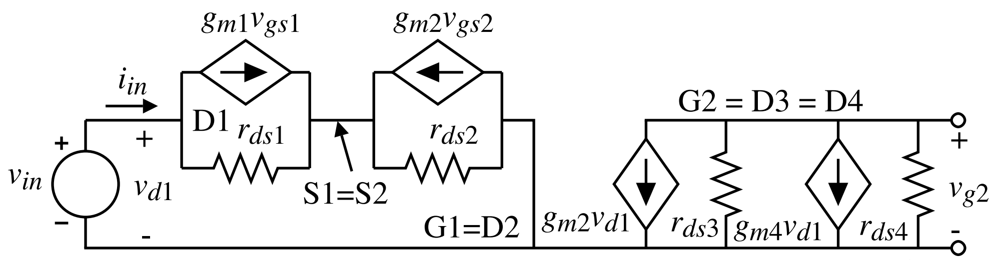


Fig. S5.4-9

$$\therefore \quad v_{in} = i_{in}\, r_{ds1} + g_{m1}v_{s1}r_{ds1} + i_{in}\, r_{ds2} + g_{m2}v_{g2}r_{ds2} - g_{m2}v_{s2}r_{ds2}$$

$$= i_{in}\, r_{ds1} + i_{in}\, r_{ds2} + g_{m2}v_{g2}r_{ds2} = i_{in}\,(r_{ds1} + r_{ds2}) - g_{m2}r_{ds2}\left(\frac{g_{m3} + g_{m4}}{g_{ds3} + g_{ds4}}\right)v_{in}$$

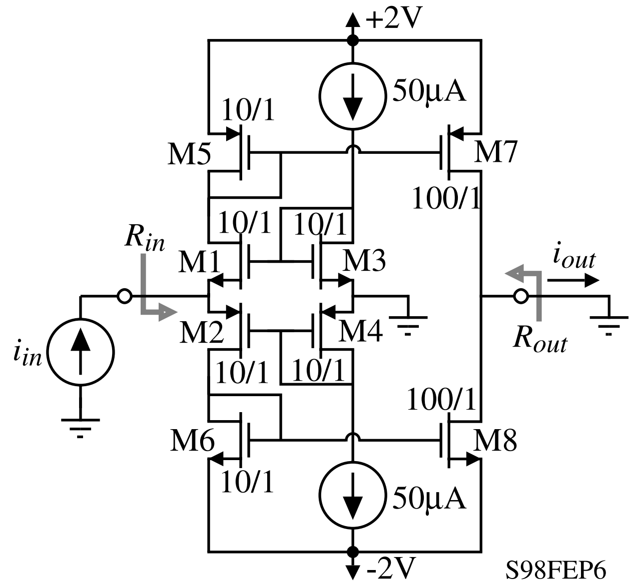
$$\therefore \quad v_{in} = \frac{(r_{ds1} + r_{ds2})i_{in}}{1 + \dfrac{g_{m2}r_{ds2}(g_{m3} + g_{m4})}{g_{ds3} + g_{ds4}}} \;\rightarrow\; R_{in} = \frac{v_{in}}{i_{in}} = \frac{(r_{ds1} + r_{ds2})}{1 + \dfrac{g_{m2}r_{ds2}(g_{m3} + g_{m4})}{g_{ds3} + g_{ds4}}}$$

or

$$\boxed{R_{in} = \frac{r_{ds1} + r_{ds2}}{1 + g_{m2}r_{ds2}(g_{m3} + g_{m4})r_{ds3} \| r_{ds4}}}$$

Problem 5.4-10

A CMOS current amplifier is shown. Find the small signal values of the current gain, $A_i = i_{out}/i_{in}$, input resistance, R_{in}, and output resistance, R_{out}. For R_{out}, assume that g_{ds2}/g_{m6} is equal to g_{ds1}/g_{m5}. Use the parameters of Table 3.1-3.



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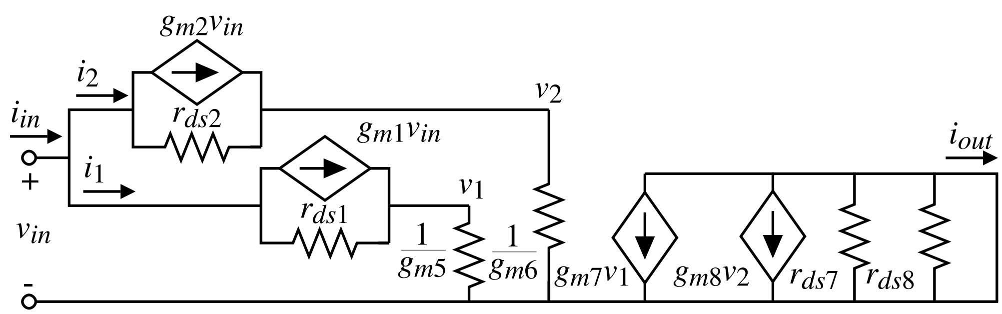
Solution

Since this is a new circuit, use the small signal model approach. The model for this problem is given below.

$$i_{out} = -(g_{m7}v_1 + g_{m8}v_2)$$

$$= -\frac{g_{m7}i_1}{g_{m5}} - \frac{g_{m8}i_2}{g_{m6}} = -\frac{g_{m7}}{g_{m5}}(i_1+i_2) = \frac{g_{m7}}{g_{m5}}i_{in} \rightarrow \boxed{A_i = \frac{i_{out}}{i_{in}} = -10}$$



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$$\boxed{R_{out} = \frac{1}{g_{ds7}+g_{ds8}} = \frac{1}{(500\mu\text{A})(0.04+0.05)} = \frac{1}{45\mu\text{S}} = 22.2\text{k}\Omega}$$

R_{in}:

$$i_{in} = g_{m1}v_{in} + g_{m2}v_{in} + g_{ds1}(v_{in}-v_1) + g_{ds2}(v_{in}-v_2)$$

$$= (g_{m1}+g_{m2}+g_{ds1}+g_{ds2})v_{in} - \frac{g_{ds1}i_1}{g_{m5}} - \frac{g_{ds2}i_2}{g_{m6}} = (g_{m1}+g_{m2}+g_{ds1}+g_{ds2})v_{in} - \frac{g_{ds1}}{g_{m5}}i_{in}$$

$$\therefore\ R_{in} = \frac{v_{in}}{i_{in}} = \frac{1+\frac{g_{ds1}}{g_{m5}}}{g_{m1}+g_{m2}+g_{ds1}+g_{ds2}}\ \ , g_{m1} = \sqrt{2K_N{\cdot}10{\cdot}50} = 331.7\mu\text{S},\ g_{ds1} = 2\mu\text{S}$$

$$g_{m2} = \sqrt{2K_P{\cdot}10{\cdot}50} = 223.6\mu\text{S},\ g_{ds1} = 2.5\mu\text{S, and } g_{m5} = g_{m2}$$

Thus, $$\boxed{R_{in} = \frac{1+0.0112}{331.7+223.6+2+2.5} = 1.8\text{k}\Omega}$$

Problem 5.4-11

Find the exact algebraic expression (ignoring bulk effects) for the following characteristics of the amplifier shown. Express your answers in terms of g_m's and r_{ds}'s in the form of the ratio of two polynomials.

(a.) The small signal voltage gain, $A_v = v_{out}/v_{in}$., and current gain, $A_i = i_{out}/i_{in}$.

(b.) The small signal input resistance, R_{in}.

∴ The small signal output resistance, R_{out}.

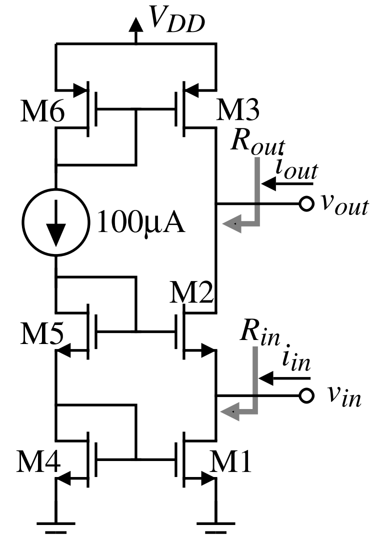


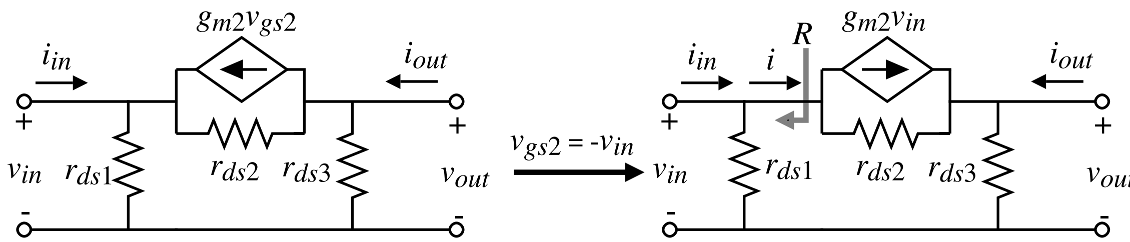
Figure P5.4-11

Solution

(a.) Small-signal model is shown below. Summing currents at the output node gives:

$$g_{m2}v_{in} + g_{ds2}(v_{in}-v_{out}) = g_{ds3}v_{out}$$

or $$\boxed{\frac{v_{out}}{v_{in}} = \frac{g_{m2}+g_{ds2}}{g_{ds2}+g_{ds3}} = \frac{r_{ds3}+g_{m2}r_{ds2}r_{ds3}}{r_{ds2}+r_{ds3}}}$$



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(b.) The input resistance is best done by finding R and putting it in parallel with r_{ds1}.

$$v_{in} = (i-g_{m2}v_{in})r_{ds2} + ir_{ds3} \quad \rightarrow \quad R = \frac{v_{in}}{i} = \frac{r_{ds2}+r_{ds3}}{1+g_{m2}r_{ds2}}$$

$$\therefore \quad R_{in} = r_{ds1}||R = r_{ds1}||\left(\frac{r_{ds2}+r_{ds3}}{1+g_{m2}r_{ds2}}\right) \rightarrow \quad \boxed{R_{in} = \frac{r_{ds1}(r_{ds2}+r_{ds3})}{r_{ds1}+r_{ds2}+r_{ds3}+g_{m2}r_{ds2}r_{ds1}}}$$

(c.) $$\boxed{R_{out} = r_{ds2}||r_{ds3} = \frac{r_{ds2}r_{ds3}}{r_{ds2}+r_{ds3}}}$$

Problem 5.4-12

Find the exact expression for the small signal input resistance of the circuit shown. Assume all transistors have identical W/L ratios, are in saturation and ignore the bulk effects. Simplify your expression by assuming that g_m=100g_{ds} and that all transistors are identical. Sketch a plot of i_{out} as a function of i_{in}.

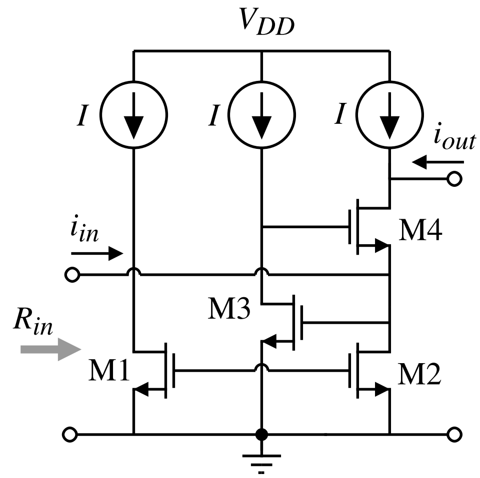
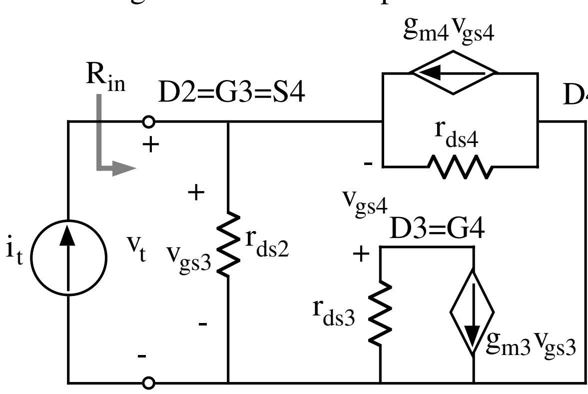


Figure P5.4-12

Solutions

A small signal model for this problem is:



$$i_t = (g_{ds2}+g_{ds4})v_t - g_{m4}v_{gs4}$$

But, $v_{gs4} = -g_{m3}r_{ds3}v_{gs3} - v_t$

and

$$v_{gs3} = v_t$$

$\therefore$ $i_t = (g_{ds2}+g_{ds4})v_t + g_{m4}(1+g_{m3}r_{ds3})v_t$

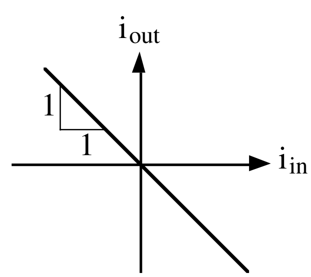
Thus, R_{in} is

$$\boxed{R_{in} = \frac{v_t}{i_t} = \frac{1}{g_{ds2}+g_{ds4}+g_{m4} + g_{m3}g_{m4}r_{ds3}} \approx \frac{1}{g_{m3}g_{m4}r_{ds3}}}$$

Sketching i_{out} as a function of i_{in}:

Note that $i_{D4} = I + i_{out}$ and $i_{D4} + i_{in} = i_{D2} = i_{D1} = I$

Therefore, $I + i_{out} = I - i_{in} \Rightarrow i_{out} = - i_{in}$



Problem 5.5-01

Use the values of Table 3.1-2 and design the *W*/*L* ratios of M1 and M2 of Fig. 5.5-1 so that a voltage swing of ±3 volts and a slew rate of 5 volts/μs is achieved if R_L = 10 kΩ and C_L = 1 nF. Assume that $V_{DD} = -V_{SS}$ = 5 volts and V_{GG2} = 2 volts.

Solution

$$I_{D2} = \frac{K_P'}{2}\left(\frac{W}{L}\right)_2 \left(V_{DD} - V_{GG2} - |V_{T2}|\right)^2$$

For positive swing of the output voltage, the slew rate should be at least +5 V/µs.

$$SR = \frac{I_{D2}}{C_L}$$

Thus, $I_{out} = I_{D2} = SR(C_L) = 5\ \text{mA}$

Now, $$\left(\frac{W}{L}\right)_2 = \frac{2I_{D2}}{K_P'\left(V_{DD} - V_{GG2} - |V_{T2}|\right)^2} \quad \rightarrow \quad \left(\frac{W}{L}\right)_2 \cong \underline{\underline{38/1}}$$

Also, for the output voltage to swing to +3 V, the load current into R_L will be 0.3 mA. Since I_{D2} is greater than 0.3 mA, the output voltage would be greater than +3 V.

For negative output voltage swing

$$I_{out} = SR(C_L) = 5\ \text{mA}$$

$$I_{D1} = -I_{out} + I_{D2} = 10\ \text{mA}$$

or, $$\left(\frac{W}{L}\right)_1 = \frac{2I_{D1}}{K_N'\left(V_{DD} - V_{SS} - V_{T1}\right)^2} \quad \rightarrow \quad \left(\frac{W}{L}\right)_1 = 2.1 \cong \underline{\underline{3/1}}$$

For $V_{out}(\min) = -3\ \text{V}$, $I_{out} = -0.3\ \text{mA}$. Since $I_{D1} > -I_{out} + I_{D2}$, the output will be able to swing down to –3 V.

Problem 5.5-02

Find the *W/L* of M1 for the source follower of Fig. 5.5-3a when $V_{DD} = -V_{SS} = 5$ V, V_{OUT} = 1 V, and $W_2/L_2 = 1$ that will source 1 mA of output current. Use the parameters of Table 3.1-2.

Solution

Given, $V_{out} = 1$ V and $V_{SS} = -5$ V

So, $V_{GS2} = 6$ V

$$I_{D2} = \frac{K_N'}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{T2})^2 \quad \rightarrow \quad I_{D2} = 1.55 \text{ mA}$$

Thus, $I_{D1} = I_{D2} + I_{out} = 2.55$ mA

Due to body effects, the threshold voltage of M_1 can be given by

$$V_{T1} = V_{T0} + \gamma_1\sqrt{V_{out} - V_{SS}} = 1.68 \text{ V}$$

Now, $\left(\frac{W}{L}\right)_1 = \frac{2I_{D1}}{K_N'(V_{DD} - V_{out} - V_{T1})^2} = \underline{\underline{8.6/1}}$

Problem 5.5-03

Find the small-signal voltage gain and output resistance of the source follower of Fig. 5.5-3b. Assume that $V_{DD} = -V_{SS} = 5$ V, $V_{OUT} = 1$ V, $I_D = 50$ μA, and the *W/L* ratios of both M1 and M2 are 20 μm/10 μm. Use the parameters of Table 3.1-2 where pertinent.

Solution

The small-signal voltage gain is given by

$$A_v = \frac{g_{m1}}{(g_{m1} + g_{ds1} + g_{ds2})}$$

$$V_{T1} = V_{T0} + \gamma_1\sqrt{V_{out} - V_{SS}} \quad \rightarrow \quad V_{T1} = 1.68 \text{ V}$$

$$g_{m1} = \sqrt{2K_N'\left(\frac{W}{L}\right)_1 I_{D1}} \quad \rightarrow \quad g_{m1} = 148 \text{ µS}$$

$$g_{ds1} + g_{ds2} = 4.5 \text{ µS}$$

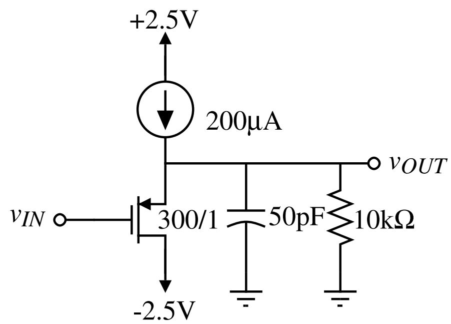
$\therefore$ $A_v = \underline{\underline{0.943 \text{ V/V}}}$

The output resistance is given by

$$R_{out} = \frac{1}{(g_{m1} + g_{ds1} + g_{ds2})} = \underline{\underline{6.37 \text{ k}\Omega}}$$

Problem 5.5-04

An output amplifier is shown. Assume that v_{IN} can vary from -2.5V to +2.5V. Let K_P' = 50μA/V^2, V_{TP} = -0.7V, and λ_P = 0.05V^{-1}. Ignore bulk effects.



a.) Find the maximum value of v_{OUT}, v_{OUT}(max).

b.) Find the minimum value of v_{OUT}, v_{OUT}(min).

c.) Find the positive slew rate, SR^+ when v_{OUT} = 0V in volts/microseconds.

d.) Find the negative slew rate, SR^- when v_{OUT} = 0V in volts/microseconds.

e.) Find the small signal output resistance (excluding the 10kΩ resistor) when v_{OUT} = 0V.

Solution

∴ When v_{IN} = +2.5V, the transistor is shut off and v_{OUT}(max) = 200μA·10kΩ = +2V

∴ When v_{IN} = -2.5V, the transistor is in saturation (drain = gate) and the minimum output voltage under steady-state is,

$$v_{OUT} = -10\text{k}\Omega(I_D\text{-}200\mu\text{A}) = -10\text{k}\Omega\left[\frac{50\cdot 300}{2}(v_{OUT}+2.5-0.7)^2 - 200\mu\text{A}\right]$$

$$v_{OUT} = -75(v_{OUT}+1.8)^2 + 2 \quad\rightarrow\quad v_{OUT}^2 + 3.6133v_{OUT} + 3.21333 = 0$$

$$\therefore \quad v_{OUT} = -\frac{3.61333}{2} \pm \frac{\sqrt{(3.61333)^2 - 4\cdot 3.21333}}{2} = -1.80667 \pm 0.22519$$

It can be shown that the correct choice is v_{OUT}(min) = -1.80667 + 0.22519 = -1.5815V

c.) The positive slew rate is $SR^+ = \dfrac{200\mu\text{A}}{50\text{pF}} = +4\text{V}/\mu\text{s} \quad\rightarrow\quad SR^+ = +4\text{V}/\mu\text{s}$

d.) The negative slew rate is found as follows. With v_{OUT} = 0V, the drain current is

$$I_D = 7.5\text{mA/V}^2(2.5-0.7)^2 = 24.3\text{mA}$$

Therefore, the sourcing current is 24.3mA-0.2mA = 24.1mA which gives a negative slew rate of $SR^- = \dfrac{24.1\text{mA}}{50\text{pF}} = -\,482\text{V}/\mu\text{s} \quad\rightarrow\quad SR^- = -\,482\text{V}/\mu\text{s}$

e.) The output resistance, R_{out}, is approximately equal to $1/g_m$. Therefore,

$$R_{out} \approx \frac{1}{g_m} = \sqrt{\frac{L}{2K_P I_D W}} = \frac{1}{\sqrt{2\cdot 50\cdot 200\cdot 300}} = 408.2\Omega \quad\rightarrow\quad R_{out} \approx 408\Omega$$

Problem 5.5-05

An output amplifier is shown. Assume that v_{IN} can vary from -2.5V to +2.5V. Ignore bulk effects. Use the parameters shown below.

a.) Find the maximum value of v_{OUT}, v_{OUT}(max).

b.) Find the minimum value of v_{OUT}, v_{OUT}(min).

c.) Find the positive slew rate, SR^+ when v_{OUT} = 0V in volts/microseconds.

d.) Find the negative slew rate, SR^- when v_{OUT} = 0V in volts/microseconds.

e.) Find the small signal output resistance when v_{OUT} = 0V.

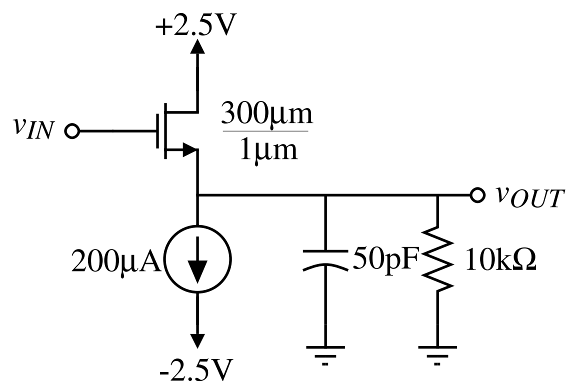


Figure P5.5-5

Solution

(a.) When v_{IN} = 2.5V, the transistor shuts off and $\boxed{v_{OUT}(\text{max}) = 200\mu\text{A}\cdot 10\text{k}\Omega = +2\text{V}}$

(b.) Assume v_{IN} = -2.5V. Therefore, the transistor is in saturation and the minimum output voltage under steady-state is,

$$v_{OUT} = -10\text{k}\Omega(I_D\text{-}200\mu\text{A}) = -10\text{k}\Omega\left(\frac{110\text{x}10^{-6}\cdot 300}{2}(v_{OUT}+2.5-0.7)^2-200\mu\text{A}\right)$$

or

$$v_{OUT} = -165(v_{OUT}+1.8)^2 + 2\text{V} \rightarrow \qquad v_{OUT}^2 + 3.6061\, v_{OUT} + 3.228 = 0$$

$$\therefore \quad v_{OUT} = -\frac{3.6061}{2} \pm \frac{\sqrt{(3.6061)^2 - 4\cdot 3.228}}{2} = -1.8030 \pm 0.1516$$

It can be shown that the correct choice is v_{OUT} = -1.8030 + 0.1516 = -1.6514V

Thus $\boxed{v_{OUT}(\text{min}) = -1.6514\text{V}}$

(c.) The positive slew rate is $\boxed{SR^+ = \frac{200\mu\text{A}}{50\text{pF}} = +4\text{V}/\mu\text{s}}$

(d.) The negative slew rate is found as follows. With v_{OUT} = 0V, the drain current is

$$I_D = \frac{110\text{x}10^{-6}\cdot 300}{2}(2.5-0.7)^2 = 53.46\text{mA}$$

Therefore, the sourcing current is 53.46mA - 0.2mA = 53.44mA which gives a negative slew rate of $\boxed{SR^- = -\frac{53.44\text{mA}}{50\text{pF}} = 1069\text{V}/\mu\text{s}}$

(e.) The output resistance, R_{out}, is approximately equal to $1/g_m$. Therefore,

$$\boxed{R_{out} = \frac{1}{g_m} = \sqrt{\frac{L}{2KI_DW}} = \frac{10^6}{\sqrt{2\cdot 110\cdot 300\cdot 200}} = 275.24\Omega}$$

Problem 5.5-06

For the circuit shown in Fig. P5.5-6, find the small signal voltage gain, v_{out}/v_{in} and the small signal output resistance, R_{out}. Assume that the dc value of v_{OUT} is 0V and that the dc current through M1 and M2 is 200µA.

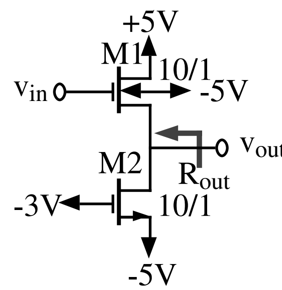


Fig. P5.5-6

Solution

(Unfortunately the gate-source voltage is given on the schematic which causes a conflict with the problem statement of 200µA of current. We will use the 200µA in the solution.)

The small-signal model for this problem is shown below.

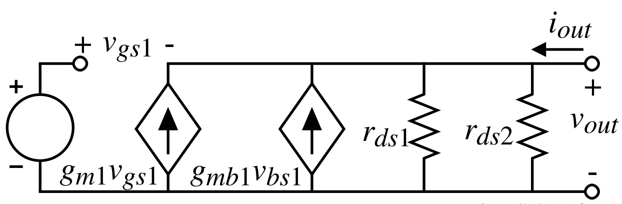


Fig. S5.5-6

$$g_{m1} = \sqrt{2\cdot 110\cdot 200\cdot 10}\ \mu\text{S} = 663.3\mu\text{S},\ g_{mb1} = \frac{663.3\mu\text{S}(0.4)}{2\sqrt{0.7+5}} = 55.57\mu\text{S},$$

$$g_{ds1} = g_{ds2} = 0.04\cdot 200\mu\text{A} = 8\mu\text{S}$$

Summing currents at the output,

$$v_{out}(g_{ds1} + g_{ds2}) = g_{m1}v_{gs1} + g_{mb1}v_{bs1} = g_{m1}v_{in} - g_{m1}v_{out} - g_{mb1}v_{out}$$

(e.) $$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{mb1} + g_{ds1} + g_{ds2}} = \frac{663.3}{663.3 + 55.57 + 8 + 8} = \underline{\underline{0.9026\text{ V/V}}}$$

$$R_{out} = \frac{v_{out}}{i_{out}} = \frac{1}{g_{m1} + g_{mb1} + g_{ds1} + g_{ds2}} = \frac{1}{663.3 + 55.57 + 8 + 8} = \underline{\underline{1361\Omega}}$$

Problem 5.5-07

Develop an expression for the efficiency of the source follower of Fig. 5.5-3b in terms of the maximum symmetrical peak-output voltage swing. Ignore the effects of the bulk-source voltage. What is the maximum possible efficiency?

Solution

Efficiency (η) is expressed as

$$\eta_{\max} = \frac{P_{RL}}{P_{supply}} = \frac{\left(\dfrac{V_{out}(peak)^2}{2R_L}\right)}{(V_{DD}-V_{SS})I_Q}$$

The maximum output voltage swing is

$$V_{out}(\max) \cong V_{DD} - V_{T1}$$

The minimum output voltage swing is

$$V_{out}(\min) \cong V_{SS}$$

Assuming symmetrical maximum positive and negative output swings

$$V_{out}(peak) \cong V_{DD} - V_{T1}$$

The quiescent current can be expressed as

$$I_Q = \frac{(V_{out}(\max) - V_{out}(\min))}{2R_L}$$

or, $$I_Q = \frac{(V_{DD} - V_{SS} - V_{T1})}{2R_L}$$

Thus,

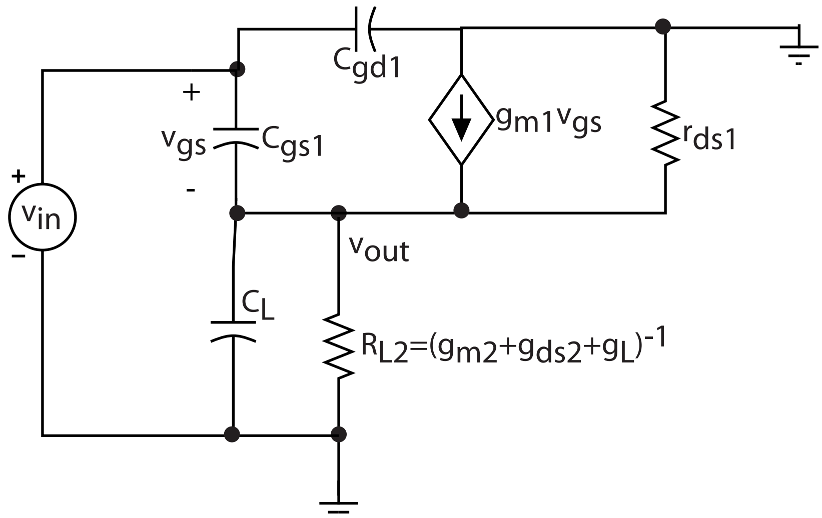
$$\eta_{\max} = \frac{\left(\dfrac{V_{out}(peak)^2}{2R_L}\right)}{(V_{DD}-V_{SS})I_Q} = \frac{(V_{DD}-V_{T1})^2}{(V_{DD}-V_{SS})(V_{DD}-V_{SS}-V_{T1})}$$

Assuming $V_{DD} = -V_{SS} = 5$ V gives $\eta_{\max} \approx \underline{\underline{20\%}}$

Problem 5.5-08

Find the pole and zero location of the source followers of Fig. 5.5-3a and Fig. 5.5-3b if $C_{gs1} = C_{gd2} = 5$fF and $C_{bs1} = C_{bd2} = 30$fF and $C_L = 1$ pF. Assume the device parameters of Table 3.1-2, $I_D = 100$ μA, $W_1/L_1 = W_2/L_2 = 10$ μm/10 μm, and $V_{SB} = 5$ volts.

Solution



a.) Referring to the figure

The location of the zero of the follower is given by

$$z = \frac{-g_{m1}}{C_{gs1}} = \underline{\underline{-14.9 \text{ GHz}}}$$

The location of the pole of the follower is given by

$$p = \frac{-(g_{m1} + g_{m2} + g_{ds1} + g_{ds2} + g_L)}{(C_{gs1} + C_{gs2} + C_{bd1} + C_{bd2} + C_L)} = \underline{\underline{-140.8 \text{ MHz}}}$$

b.) Referring to the figure

The location of the zero of the follower is given by

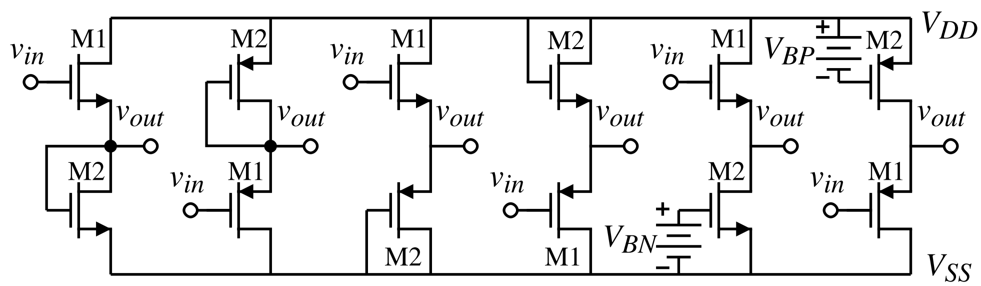
$$z = \frac{-g_{m1}}{C_{gs1}} = \underline{\underline{-14.9 \text{ GHz}}}$$

The location of the pole of the follower is given by

$$p = \frac{-(g_{m1} + g_{ds1} + g_{ds2} + g_L)}{(C_{gs1} + C_{gs2} + C_{bd1} + C_{bd2} + C_L)} = \underline{\underline{-71.1 \text{ MHz}}}$$

Problem 5.5-09

Six versions of a source follower are shown below. Assume that $K'_N = 2K'_P$, $\lambda_P = 2\lambda_N$, all W/L ratios of all devices are equal, and that all bias currents in each device are equal. Neglect bulk effects in this problem and assume no external load resistor. Identify which circuit or circuits have the following characteristics: (a.) highest small-signal voltage gain, (b.) lowest small-signal voltage gain, (c.) the highest output resistance, (d.) the lowest output resistance, (e.) the highest v_{out}(max) and (f.) the lowest v_{out}(max).



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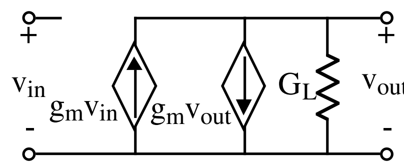
Solution

(a.) and (b.) - Voltage gain. Small signal model:



The voltage gain is found as: $\dfrac{v_{out}}{v_{in}} = \dfrac{g_m}{g_m+G_L}$

where G_L is the load conductance. Therefore we get:

Circuit	1	2	3	4	5	6
$\dfrac{v_{out}}{v_{in}}$	$\dfrac{g_{mN}}{g_{mN}+g_{mN}}$	$\dfrac{g_{mP}}{g_{mP}+g_{mP}}$	$\dfrac{g_{mN}}{g_{mN}+g_{mP}}$	$\dfrac{g_{mP}}{g_{mP}+g_{mN}}$	$\dfrac{g_{mN}}{g_{mN}+g_{dsN}+g_{dsP}}$	$\dfrac{g_{mP}}{g_{mP}+g_{dsN}+g_{dsP}}$

But $g_{mN} = \sqrt{2}\, g_{mP}$ and $g_{dsN} = 0.5g_{dsP}$, therefore

Circuit	1	2	3	4	5	6
$\dfrac{v_{out}}{v_{in}}$	$\dfrac{1}{2}$	$\dfrac{1}{2}$	0.5858	0.4142	$\dfrac{g_{mP}}{g_{mP}+(g_{dsP}+g_{dsN})/\sqrt{2}}$	$\dfrac{g_{mP}}{g_{mP}+g_{dsP}+g_{dsN}}$

$\boxed{\text{Thus, circuit 5 has the highest gain and circuit 4 the lowest gain}}$

(c.) and (d.) - Output resistance.

The denominators of the first table show the following:

$\boxed{\text{Ckt.6 has the highest output resistance and Ckt. 1 the lowest output resistance.}}$

(e.) Assuming no current has to be provided by the output, circuits 2, 4, and 6 can pull the output to V_{DD}. ∴ $\boxed{\text{Circuits 2, 4 and 6 have the highest output swing.}}$

(f.) Assuming no current has to be provided by the output, circuits 1, 3, and 5 can pull the output to ground. ∴ $\boxed{\text{Circuits 1, 3 and 5 have lowest output swing.}}$

Summary

(a.) Ckt. 5 has the highest voltage gain
(b.) Ckt. 4 has the lowest voltage gain
(c.) Ckt. 6 has the highest output resistance
(d.) Ckt. 1 has the lowest output resistance
(e.) Ckts. 2,4 and 6 have the highest output
(f.) Ckts. 1,3 and 5 have the lowest output

Problem 5.5-10

Show that a class B, push-pull amplifier has a maximum efficiency of 78.5% for a sinusoidal signal.

Solution

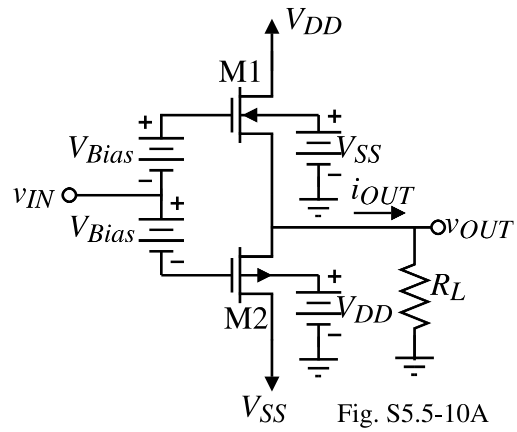


Fig. S5.5-10A

Referring to the figure, assuming there is no cross-over distortion, the efficiency can be given by

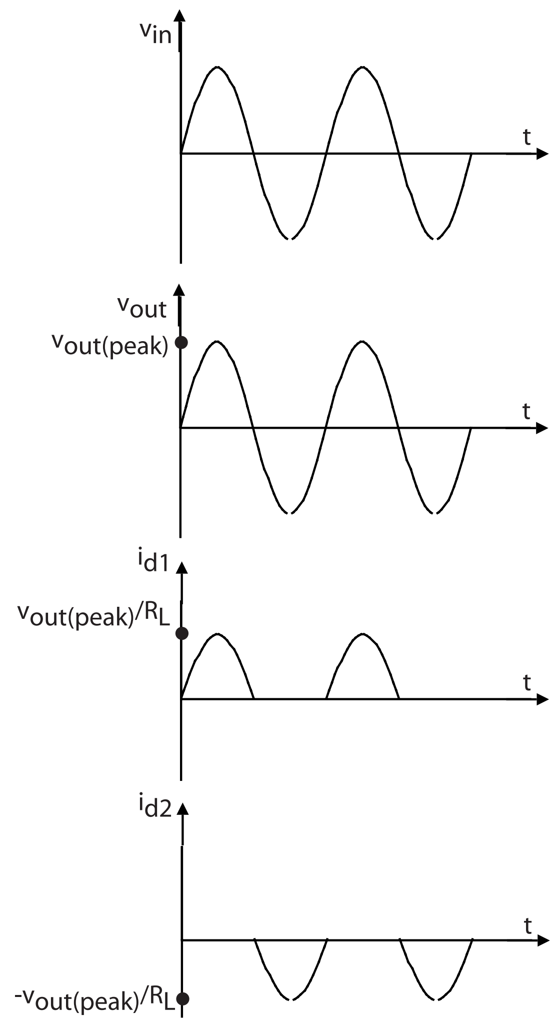
$$\eta = \frac{\dfrac{V_{out}(peak)^2}{2R_L}}{(V_{DD}-V_{SS})\left(\dfrac{V_{out}(peak)}{\pi R_L}\right)}$$

For maximum efficiency, it can be assumed that the output swing is symmetrical and the peak output voltage can be given by

$$V_{out}(peak) = V_{DD} = -V_{SS}$$

Thus, $$\eta = \frac{\dfrac{V_{DD}^2}{2R_L}}{(V_{DD}-V_{SS})\left(\dfrac{V_{DD}^2}{\pi R_L}\right)}$$

or, $$\eta = \frac{\pi}{4} = \underline{\underline{78.5\%}}$$



Problem 5.5-11

Assume the parameters of Table 3.1-2 are valid for the transistors of Fig. 5.5-5a. Design V_{Bias} so that M1 and M2 are working in class-B operation, i.e., M1 starts to turn on when M2 starts to turn off.

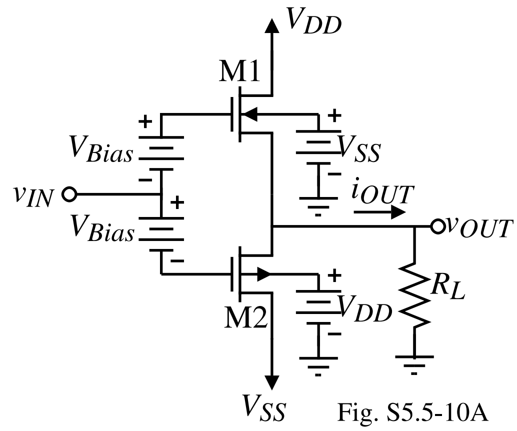


Fig. S5.5-10A

Solution

$$V_{GS1} = \left(V_{in} + V_{BIAS} - V_{out}\right)$$

$$V_{GS2} = \left(V_{in} - V_{BIAS} - V_{out}\right)$$

In Class B operation, when M_1 starts to turn on and M_2 starts to turn off, the drain currents can be written as

$$I_{D1} = I_{D2} + I_{out}$$

or, $$\frac{K_N'}{2}\left(\frac{W}{L}\right)_1 \left(V_{GS1} - V_{T1}\right)^2 = \frac{K_P'}{2}\left(\frac{W}{L}\right)_2 \left(V_{SG2} - |V_{T2}|\right)^2 + \frac{V_{out}}{R_L}$$

Assuming, when $V_{in} = 0$, $V_{out} = 0$, we get

$$\frac{K_N'}{2}\left(\frac{W}{L}\right)_1 \left(V_{BIAS} - V_{T1}\right)^2 = \frac{K_P'}{2}\left(\frac{W}{L}\right)_2 \left(V_{BIAS} - |V_{T2}|\right)^2$$

or, $$\left(\frac{V_{BIAS} - V_{T1}}{V_{BIAS} - |V_{T2}|}\right) = \sqrt{\frac{K_P'}{K_N'}\left(\frac{W}{L}\right)_2 \left(\frac{L}{W}\right)_1}$$

or, $$\boxed{V_{BIAS} = \frac{\left[V_{T1} - \sqrt{\frac{K_P'}{K_N'}\left(\frac{W}{L}\right)_2 \left(\frac{L}{W}\right)_1}\,|V_{T2}|\right]}{\left[1 - \sqrt{\frac{K_P'}{K_N'}\left(\frac{W}{L}\right)_2 \left(\frac{L}{W}\right)_1}\right]}}$$

Problem 5.5-12

Find an expression for the maximum and minimum output voltage swing for Fig. 5.5-5a.

Solution

To calculate the maximum output voltage swing, it can be assumed that the input is taken to V_{DD}. Thus,

$$V_{GS1} - V_{T1} = \left(V_{DD} + V_{BIAS} - V_{out}(\text{max}) - V_{T1}\right)$$

and, $$V_{DS1} = \left(V_{DD} - V_{out}(\text{max})\right)$$

So, $$V_{DS1} - \left(V_{GS1} - V_{T1}\right) = \left(V_{BIAS} - V_{T1}\right)$$

Thus, if $V_{BIAS} \geq V_{T1}$, $V_{DS1} \geq (V_{GS1} - V_{T1})$ and M_1 will be in saturation.

Now, $$I_{D1} = I_L$$

or, $$\frac{K_N'}{2}\left(\frac{W}{L}\right)_1 \left(V_{DD} + V_{BIAS} - V_{out}(\text{max}) - V_{T1}\right)^2 = \frac{V_{out}(\text{max})}{R_L}$$

or, $$V_{out}(\text{max}) = \left(V_{DD} + V_{BIAS} - V_{T1}\right) + Y$$

where, $$Y = \frac{1}{R_L K_N'(W/L)_1} - \sqrt{\frac{1}{\left(R_L K_N'(W/L)_1\right)^2} + \frac{2\left(V_{DD} + V_{BIAS} - V_{T1}\right)}{\left(R_L K_N'(W/L)_1\right)}}$$

To calculate the minimum output voltage swing

$$I_{D2} = -I_L$$

or, $$\frac{K_P'}{2}\left(\frac{W}{L}\right)_2 \left(V_{SS} - V_{BIAS} - V_{out}(\text{min}) + |V_{T2}|\right)^2 = -\frac{V_{out}(\text{min})}{R_L}$$

or, $$V_{out}(\text{min}) = \left(V_{SS} - V_{BIAS} + |V_{T2}|\right) - Z$$

where, $$Z = \frac{1}{R_L K_P'(W/L)_2} - \sqrt{\frac{1}{\left(R_L K_P'(W/L)_2\right)^2} - \frac{2\left(V_{SS} - V_{BIAS} + |V_{T2}|\right)}{\left(R_L K_P'(W/L)_2\right)}}$$

Problem 5.5-13

Repeat the previous problem for Fig. 5.5-8.

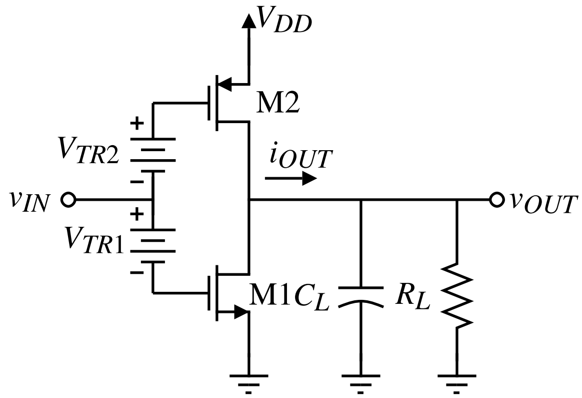


Figure 5.5-8 Push-pull inverting CMOS amplifier.

Solution

Assuming M_2 operate in triode region when $V_{in}=V_{SS}$, the maximum output voltage swing can be calculated as follows:

$$I_{D2}=I_{out}$$

or,

$$K_P'\left(\frac{W}{L}\right)_2\left(V_{SS}-V_{DD}+V_{TR2}+|V_{T2}|\right)\left(V_{out}(\max)-V_{DD}\right)=\frac{V_{out}(\max)}{R_L}$$

or, $$V_{out}(\max)=\frac{V_{DD}}{\left[1+\left(\dfrac{1}{K_P'\left(\frac{W}{L}\right)_2 R_L\left(V_{SS}-V_{DD}+V_{TR2}+|V_{T2}|\right)}\right)\right]}$$

Assuming M_1 operate in triode region when $V_{in}=V_{DD}$, the minimum output voltage swing can be calculated as follows:

$$I_{D1}=-I_{out}$$

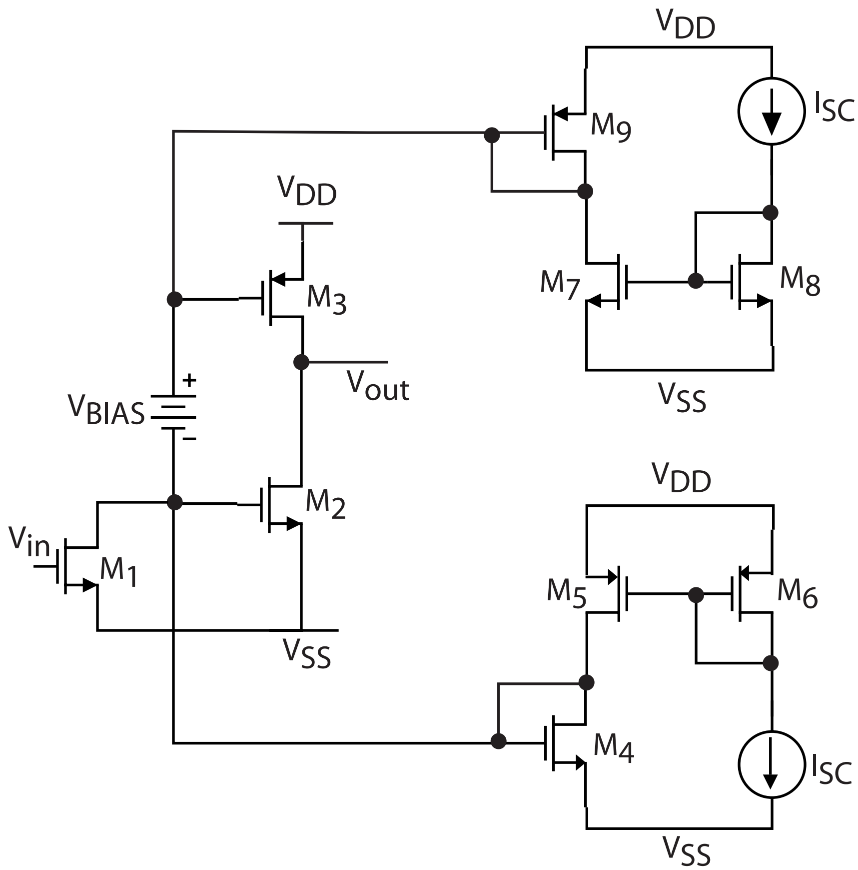
or, $$K_N'\left(\frac{W}{L}\right)_1\left(-V_{SS}+V_{DD}-V_{TR1}-V_{T1}\right)\left(V_{out}(\min)-V_{SS}\right)=\frac{-V_{out}(\min)}{R_L}$$

or, $$V_{out}(\min)=\frac{V_{SS}}{\left[1+\left(\dfrac{1}{K_N'\left(\frac{W}{L}\right)_1 R_L\left(-V_{SS}+V_{DD}-V_{TR1}-V_{T1}\right)}\right)\right]}$$

Problem 5.5-14

Given the push-pull inverting CMOS amplifier shown in Fig. 5.5-14, show how short-circuit protection can be added to this amplifier. Note that R_1 could be replaced with an active load if desired.

Solution

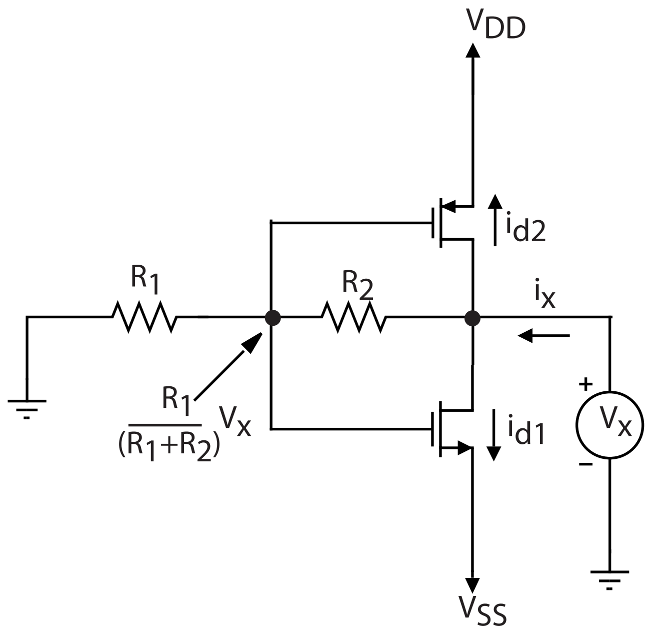


The current source I_{SC} in the figure represents the short circuit current whose value can be set as desired. The current through the transistors M2 and M3 need to be regulated for short circuit protection. The currents carried by M2 and M3 are mirrored into M4 and M9 respectively. When the current tends to increase in M2, the current in M4 would also increase. This would tend to increase the voltage at the drain of M5, but it will decrease the current in M5. Since the current carried by M4 and M5 are same, the gate bias of M4 as well as M2 cannot increase beyond a point where they both carry the maximum limit of the current as set by the short circuit current source. Similarly, the diode-connected transistor M9 would limit the gate bias of M3, thus limiting the output sinking current.

Problem 5.5-15

If $R_1 = R_2$ of Fig. 5.5-12, find an expression for the small-signal output resistance R_{out}. Repeat including the influence of R_L on the output resistance.

Solution



$$v_{g1} = v_{g2} = \frac{R_1}{(R_1 + R_2)} v_x$$

or, $v_{g1} = v_{g2} = 0.5 v_x$

$$i_{d1} = 0.5 g_{m1} v_x$$

and, $i_{d2} = 0.5 g_{m2} v_x$

Now, $i_x = i_{d1} + i_{d2}$

or, $i_x = 0.5(g_{m1} + g_{m2}) v_x$

So, the output resistance becomes

$$R_{out} = \frac{v_x}{i_x} = \frac{2}{(g_{m1} + g_{m2})}$$

In presence of load (R_L), the output resistance will become

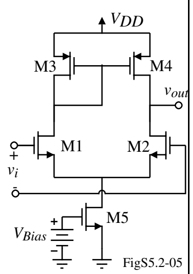
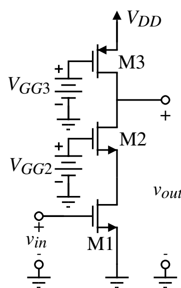
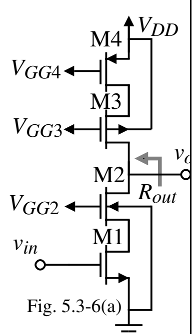
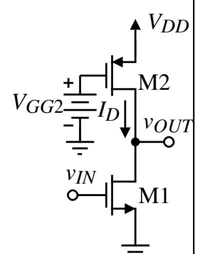
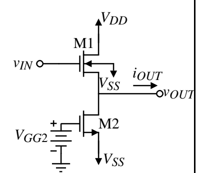
$$R_{out} = \left[\frac{2}{(g_{m1} + g_{m2})}\right] \| [R_L]$$

The presence of the load resistance (R_L) will tend to decrease the output resistance.

Problem 5.5-16

Develop a table that expresses the dependence of the small-signal voltage gain, output resistance, and the dominant pole as a function of dc drain current for the differential amplifier of Fig. 5.2-1, the cascode amplifier of Fig. 5.3-1, the high-output-resistance cascode of Fig. 5.3-6, the inverter of Fig. 5.5-1, and the source follower of Fig. 5.5-3b.

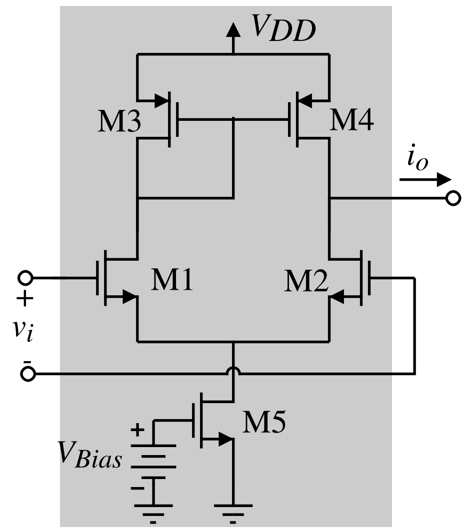
Solution

	Differential Amplifier	Cascode Amplifier	High-Gain Cascode Amp.	Inverting Amplifer	Source Follower
Circuit	 FigS5.2-05	 Figure 5.3-1	 Fig. 5.3-6(a)	 Figure 5.1-1	 Fig. 5.5-3(b)
A_v	$\frac{2}{\lambda_N+\lambda_P}\sqrt{\frac{K_N'W}{2I_DL}}$	$-\sqrt{\frac{2K_N'W_1}{L_1 I_D \lambda_P^2}}$	See Eq. (5.3-37) Gain $\propto I_D^{-1}$	$\frac{-2}{\lambda_N+\lambda_P}\sqrt{\frac{K_N'W}{2I_DL}}$	**Error!**
R_{out}	$\propto \frac{1}{I_D}$	$\propto \frac{1}{I_D}$	$\propto \frac{1}{I_D^{-1.5}}$	$\propto \frac{1}{I_D}$	$\propto \frac{1}{\sqrt{I_D}}$
$\lvert p_1\rvert$	$\propto I_D$	$\propto I_D$	$\propto I_D^{1.5}$	$\propto I_D$	$\propto I_D^{0.5}$

Problem 5.6-01

Propose an implementation of the VCCS of Fig. 5.6-2(b).

Solution

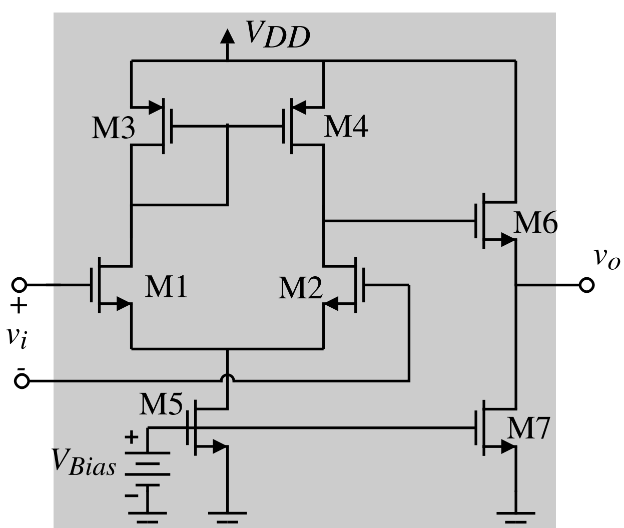


FigS5.6-01

Problem 5.6-02

Propose an implementation of the VCVS of Fig. 5.6-3(b).

Solution



FigS5.6-02

Problem 5.6-03

Propose an implementation of the CCCS of Fig. 5.6-4(b).

Solution

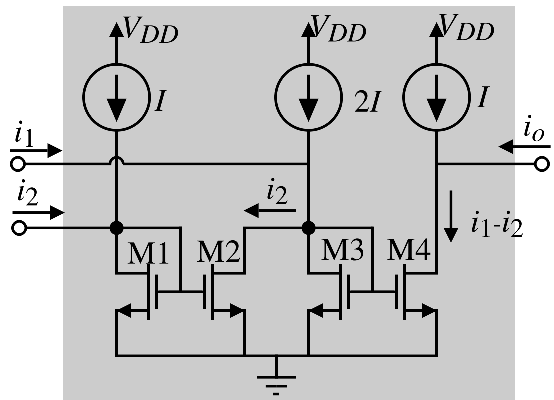


Fig. S5.6-03

Problem 5.6-04

Propose an implementation of the CCVS of Fig. 5.6-5(b).

Solution

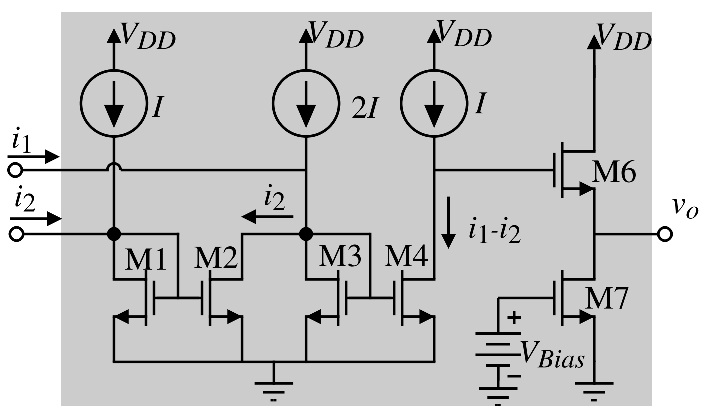


Fig. S5.6-04

CHAPTER 6 – HOMEWORK SOLUTIONS

Problem 6.1-01

Use the null port concept to find the voltage transfer function of the noninverting voltage amplifier shown in Fig. P6.1-1.

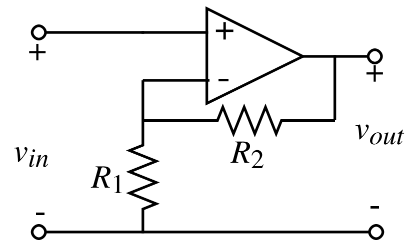


Figure P6.1-1

Solution

Let, v_1 and v_2 be the voltages at the non-inverting and inverting terminals respectively. Using the Null-port concept and assuming that the lower negative rail is at ground

$$v_1 = v_2 = v_{in}$$

Applying KCL

$$\frac{(v_{out} - v_2)}{R_2} = \frac{(v_2)}{R_1} \quad \rightarrow \quad \frac{(v_{out} - v_{in})}{R_2} = \frac{(v_{in})}{R_1}$$

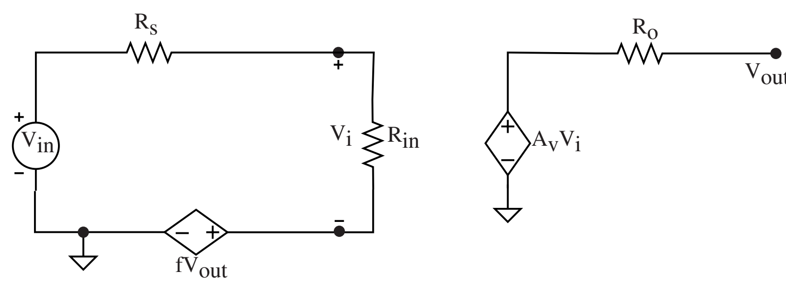
or, $$\boxed{\left(\frac{v_{out}}{v_{in}}\right) = \left(1 + \frac{R_2}{R_1}\right)}$$

Problem 6.1-02

Show that if the voltage gain of an op amp approaches infinity that the differential input becomes a null port. Assume that the output is returned to the input by means of negative feedback.

Solution

Referring to the figure, in the presence of negative series feedback, the differential input can be written as



$$v_{in} = v_S - fv_{out}$$

and, $$v_{out} = A_v v_{in}$$

So, $$v_{in} = v_S - fA_v v_{in}$$

or, $$v_{in} = \frac{v_S}{(1 + fA_v)}$$

For a finite value of the negative feedback factor (f), if the value of open-loop differential gain (A_v) tends to become infinite, then the value of the differential input voltage (v_{in}) would tend to become zero and become a null port.

Problem 6.1-03

Show that the controlled source of Fig. 6.1-5 designated as v_1/CMRR is in fact a suitable model for the common-mode behavior of the op amp.

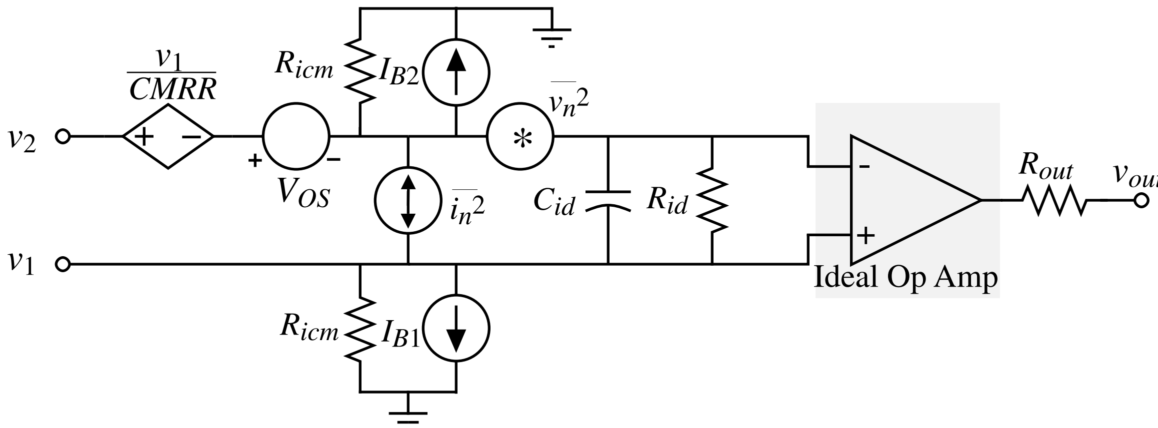


Figure 6.1-5 A model for a nonideal op amp showing some of the nonideal linear characteristics.

Solution

Referring to the figure, considering only the source representing the common-mode behavior, $v_1 / CMRR$, the following analysis is carried out

The common-mode input, v_{cm}, is given by

$$v_{cm} = v_1 = v_2$$

Thus, the differential input is

$$v_{id} = v_1 - v_2 + \frac{v_1}{CMRR}$$

or, $$v_{id} = \frac{v_1}{CMRR}$$

The output voltage is given by

$$v_{out} = A_{vd} v_{id}$$

and, the common-mode rejection ratio is given by

$$CMRR = \frac{A_{vd}}{A_{cm}}$$

where, A_{vd} and A_{cm} are the differential and common-mode gains respectively.

Thus,

$$v_{out} = A_{vd} v_{id} = (CMRR)(A_{cm})\left(\frac{v_1}{CMRR}\right)$$

or, $v_{out} = (A_{cm})v_1 \qquad \rightarrow \qquad v_{out} = (A_{cm})v_{cm}$

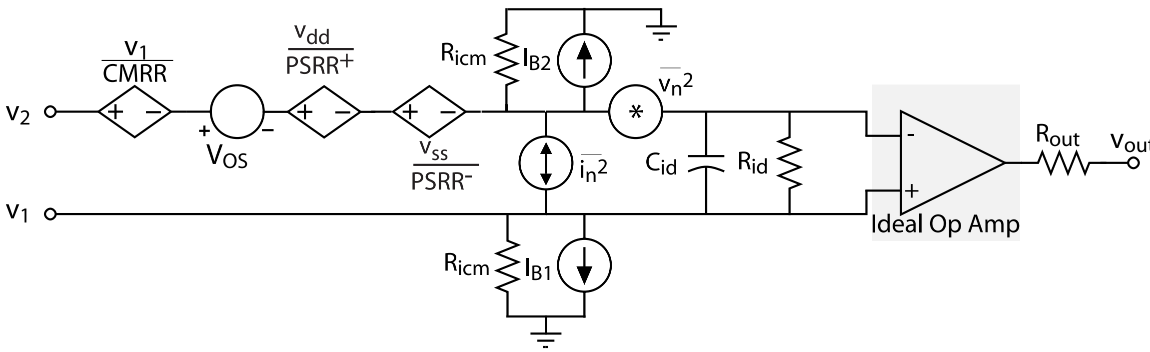
This expression proves that the source $v_1 / CMRR$ represents the common-mode behavior of the op amp.

Problem 6.1-04

Show how to incorporate the PSRR effects of the op amp into the model of the nonideal effects of the op amp given in Fig. 6.1-5.

Solution

Referring to the figure, the sources ($v_{dd} / PSRR^{+}$) and ($v_{ss} / PSRR^{-}$) would model the positive PSRR and negative PSRR respectively.



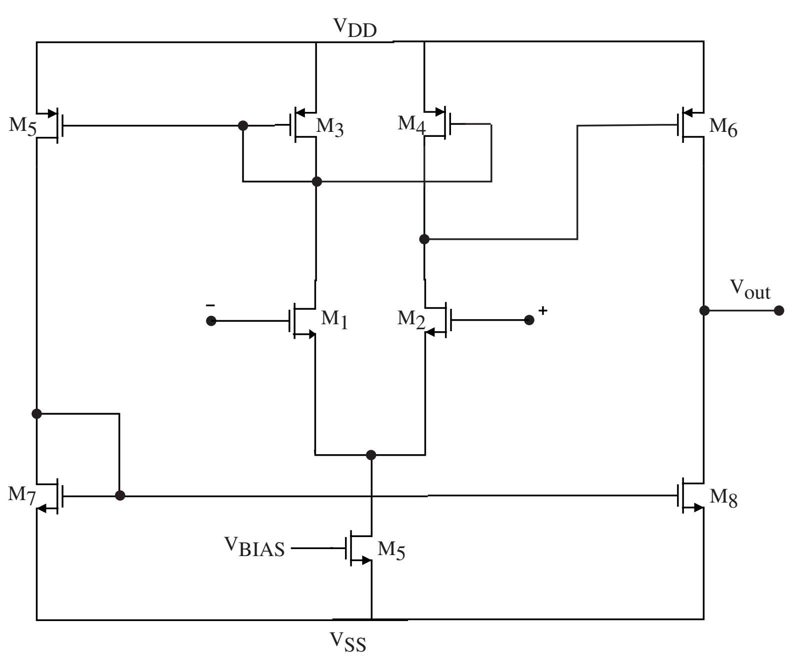
Problem 6.1-05

Replace the current mirror load of Fig. 6.1-8 with two separate current mirror and show how to recombine these currents in an output stage to get a push-pull output. How can you increase the gain of the configuration equivalent to a two-stage op amp?

Solution

Referring to the figure, if the aspect ratios of M3 through M6 are same and that of M7 and M8 are equal, then the small-signal gain of this configuration becomes equivalent to a two-stage op amp. The small-signal gain of this configuration is given by

$$A_v = \left(\frac{g_{m2}(g_{m6} + g_{m5})}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds8})} \right)$$



Problem 6.1-06

Replace the *I→I* stage of Fig. 6.1-9 with a current mirror load. How would you increase the gain of this configuration to make it equivalent to a two-stage op amp?

Solution

In the figure, the transistor M4 is a diode-connected transistor.

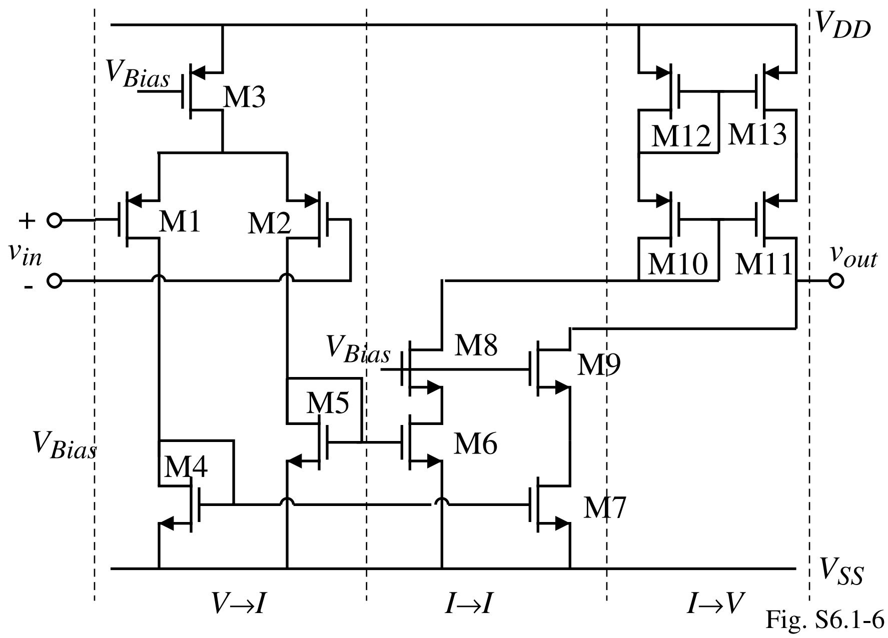


Fig. S6.1-6

The gain in the above circuit is already at the level of a two-stage op amp. The gain could easily be increased by making the W/L ratio of M7 to M4 and M6 to M5 greater than one.

Problem 6.2-01

Develop the expression for the dominant pole in Eq. (6.2-10) and the output pole in Eq. (6.2-11) from the transfer function of Eq. (6.2-9).

Solution

The transfer function is given by Equation (6.2-9). Assuming the dominant pole and the output pole are wide apart, the dominant pole, p_1, can be calculated as the root of the polynomial

$$\left[1 + s\{R_I(C_I + C_C) + R_{II}(C_{II} + C_C) + g_{mII}R_I R_{II}C_C\}\right] = 0$$

where, the effect due to the s^2 term is neglected assuming the dominant pole is a low frequency pole.

$$p_1 = \frac{-1}{\{R_I(C_I + C_C) + R_{II}(C_{II} + C_C) + g_{mII}R_I R_{II}C_C\}}$$

Considering the most dominant term

$$\boxed{p_1 \cong \frac{-1}{\{g_{mII}R_I R_{II}C_C\}}}$$

To compute the output pole (which is assumed to be at high frequency), the polynomial with the s and s^2 terms are considered.

$$\left[s\{R_I(C_I + C_C) + R_{II}(C_{II} + C_C) + g_{mII}R_I R_{II}C_C\} + s^2\{R_I R_{II}(C_I C_{II} + C_I C_C + C_C C_{II})\}\right] = 0$$

or, $$p_2 = \frac{-\{R_I(C_I + C_C) + R_{II}(C_{II} + C_C) + g_{mII}R_I R_{II}C_C\}}{\{R_I R_{II}(C_I C_{II} + C_I C_C + C_C C_{II})\}}$$

or, $$p_2 \cong \frac{-\{g_{mII}R_I R_{II}C_C\}}{\{R_I R_{II}(C_C C_{II})\}}$$

or, $$\boxed{p_2 \cong \frac{-\{g_{mII}\}}{\{C_{II}\}}}$$

Problem 6.2-02

Fig. 6.2-7 uses asymptotic plots to illustrate the difference between an uncompensated and compensated op amp. What is the approximate value of the real phase margin using the actual curves and not the asymptotic approximations?

Solution

Assume that the open-loop gain can be expressed as

$$L(j\omega) = \frac{-A_{v0}}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{GB}+1\right)} \text{ where } p_1 \text{ is the dominant pole}$$

The magnitude and phase shift of the open-loop gain can be expressed as,

$$|L(j\omega)| = \frac{A_{v0}}{\sqrt{\left(\frac{\omega}{p_1}\right)^2+1}\sqrt{\left(\frac{\omega}{GB}\right)^2+1}}$$

$$\text{Arg}[L(j\omega)] = \pm 180° - \tan^{-1}(\omega/p_1) - \tan^{-1}(\omega/GB)$$

At frequencies near GB, we can simplify these expression as,

$$|L(j\omega)| \approx \frac{\frac{GB}{\omega}}{\sqrt{\left(\frac{\omega}{GB}\right)^2+1}}$$

$$\text{Arg}[L(j\omega)] = \pm 180° - 90° - \tan^{-1}(\omega/GB) = 90° - \tan^{-1}(\omega/GB)$$

The unity gain frequency is found as,

$$\frac{\frac{GB}{\omega_o}}{\sqrt{\left(\frac{\omega_o}{GB}\right)^2+1}} = 1 \qquad \rightarrow \qquad (\omega_o/GB)^4 + (\omega_o/GB)^2 - 1 = 0$$

$$(\omega_o/GB)^2 = 0.5 \pm 0.5\sqrt{1+4} = 0.6180 \qquad \rightarrow \qquad \omega_o = 0.7862GB$$

The phase margin becomes,

$$\text{Arg}[L(j\omega_o)] = 90° - \tan^{-1}(\omega_o/GB) = 90° - \tan^{-1}(0.7862)$$

$$= 90° - 38.173° = 51.83°$$

$\therefore$ The actual phase margin is 51.83° compared to 45° estimated from the Bode plot.

Problem 6.2-03

Derive the relationship for *GB* given in Eq. (6.2-17) of Sec. 6.2.

Solution

The small signal voltage gains of the two stages can be given by

$$A_{v1} = g_{m1}R_I$$

$$A_{v2} = g_{m2}R_{II}$$

And, the overall small-signal voltage gain is given by

$$A_v = g_{m1}R_I g_{m2}R_{II}$$

Assuming the dominant pole is much smaller than the output pole, and the Gain-bandwidth frequency is smaller than the output pole, the overall transfer function of the op amp can be approximated by a single dominant pole, p_1 .

$$A_v(s) = \frac{A_v}{\left(1+\dfrac{s}{p_1}\right)}$$

where, $$p_1 \cong \frac{-1}{\{g_{mII}R_I R_{II} C_C\}}$$

or, $$A_v(j\omega) = \frac{A_v}{\left(1+\dfrac{j\omega}{p_1}\right)}$$

It can be seen that at $\omega \cong A_v p_1$, $|A_v(j\omega)| = 1$

So, the Gain-bandwidth frequency, ω_{GB} , is given by

$$\boxed{\omega_{GB} \cong A_v p_1 = \frac{g_{mI}}{C_C}}$$

Problem 6.2-04

For an op amp model with two poles and one RHP zero, prove that if the zero is 10 times larger than *GB,* then in order to achieve a 45° phase margin, the second pole must be placed at least 1.22 times higher than *GB.*

Solution

Given, $z = 10(GB)$

The transfer function is given by

$$A_v(s) = \frac{A_v\left(1 - \dfrac{s}{z}\right)}{\left(1 + \dfrac{s}{p_1}\right)\left(1 + \dfrac{s}{p_2}\right)}$$

The phase margin, PM, can be written as

$$PM = 180° - \left(\tan^{-1}\left(\frac{GB}{p_1}\right) + \tan^{-1}\left(\frac{GB}{p_2}\right) + \tan^{-1}\left(\frac{GB}{z}\right)\right)$$

or, $$45° = 180° - \left(90° + \tan^{-1}\left(\frac{GB}{p_2}\right) + 5.7°\right) \quad \rightarrow \quad \tan^{-1}\left(\frac{GB}{p_2}\right) = 39.3°$$

or, $$\boxed{p_2 = 1.22(GB)}$$

Problem 6.2-05

For an op amp model with three poles and no zero, prove that if the highest pole is 10 times *GB,* then in order to achieve 60° phase margin, the second pole must be placed at least 2.2 times *GB*.

Solution

The transfer function is given by

$$A_v(s) = \frac{A_v}{\left(1 + \dfrac{s}{p_1}\right)\left(1 + \dfrac{s}{p_2}\right)\left(1 + \dfrac{s}{p_3}\right)}$$

The phase margin, PM, can be written as

$$PM = 180° - \left(\tan^{-1}\left(\frac{GB}{p_1}\right) + \tan^{-1}\left(\frac{GB}{p_2}\right) + \tan^{-1}\left(\frac{GB}{p_3}\right)\right)$$

or, $$60° = 180° - \left(90° + \tan^{-1}\left(\frac{GB}{p_2}\right) + 5.7°\right) \quad \rightarrow \quad \tan^{-1}\left(\frac{GB}{p_2}\right) = 24.3°$$

or, $$\boxed{p_2 = 2.2(GB)}$$

Problem 6.2-06

Derive the relationships given in Eqs. (6.2-34) through (6.2-37) in Sec. 6.2.

Solution

The transfer function is given by Equations (6.2-32) through (6.2-36). Now, the denominator of Equation (6.2-32) cannot be factorized readily. So, the roots of this polynomial can be determined intuitively. The zero can be calculated as

$$\left\{1 - s\left(\frac{C_C}{g_{mII}} - R_z C_C\right)\right\} = 0$$

or, $$\boxed{z = \frac{-1}{C_C\left(R_Z - 1/g_{mII}\right)}}$$

The dominant pole, p_1, is given by

$$[1 + s\{R_I(C_I + C_C) + R_{II}(C_{II} + C_C) + g_{mII}R_I R_{II} C_C + R_Z C_C\}] = 0$$

where, the effect due to the s^2 and higher order terms are neglected assuming the dominant pole is a low frequency pole.

$$p_1 = \frac{-1}{\{R_I(C_I + C_C) + R_{II}(C_{II} + C_C) + g_{mII}R_I R_{II} C_C + R_Z C_C\}}$$

Considering the most dominant term

$$\boxed{p_1 \cong \frac{-1}{\{g_{mII}R_I R_{II} C_C\}}}$$

To compute the output pole (which is assumed to be at high frequency), the polynomial with the s and s^2 terms from Equations (6.2-34) and (6.2-35) are considered.

or, $$p_2 = \frac{-\{R_I(C_I + C_C) + R_{II}(C_{II} + C_C) + g_{mII}R_I R_{II} C_C + R_Z C_C\}}{\{R_I R_{II}(C_I C_{II} + C_I C_C + C_C C_{II}) + R_Z C_C(R_I C_I + R_{II} C_{II})\}}$$

or, $$p_2 \cong \frac{-\{g_{mII}R_I R_{II} C_C\}}{\{R_I R_{II}(C_C C_{II})\}}$$

or, $$\boxed{p_2 \cong \frac{-\{g_{mII}\}}{\{C_{II}\}}}$$

To compute the third pole, p_4, the polynomial with the s^2 and s^3 terms from Equations (6.2-35) and (6.2-36) are considered.

or, $$p_4 = \frac{-\{R_I R_{II}(C_I C_{II} + C_I C_C + C_C C_{II}) + R_Z C_C(R_I C_I + R_{II} C_{II})\}}{R_I R_{II} R_Z C_I C_{II} C_C}$$

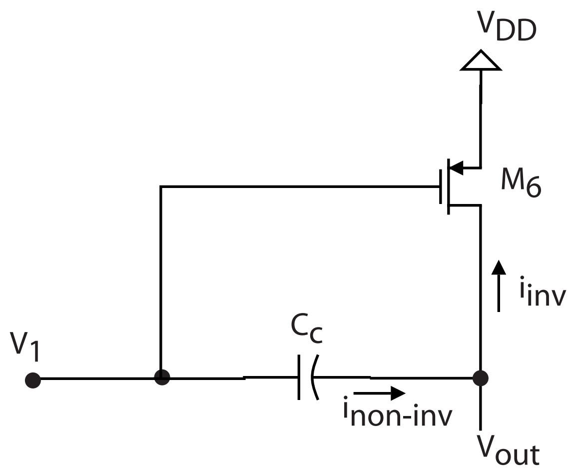
or, $$p_4 \cong \frac{-\{R_I R_{II} C_{II} C_C\}}{R_I R_{II} R_Z C_I C_{II} C_C}$$

or, $$\boxed{p_4 \cong \frac{-1}{R_Z C_I}}$$

Problem 6.2-07

Physically explain why the RHP zero occurs in the Miller compensation scheme illustrated in the op amp of Fig. 6.2-8. Why does the RHP zero have a stronger influence on a CMOS op amp than on a similar type BJT op amp?

Solution



Referring to the figure and considering the transistor M_6, there are two paths from the input (gate) to the output (drain): inverting and non-inverting.
The signal current in the inverting path is given by

$$i_{inv} = g_{m6}v_{g6}$$

The signal current in the non-inverting path is given by

$$i_{non-inv} = (v_{g6} - v_{out})sC_C$$

The zero is created when

$$i_{inv} = i_{non-inv} \text{ and } i_{out} = 0$$

or, $$g_{m6}v_{g6} = (v_{g6} - v_{out})sC_C$$

or, $$\frac{v_{out}}{v_{g6}} = \frac{(-g_{m6} + sC_C)}{sC_C}$$

Thus, the RHP zero is given by the numerator $(-g_{m6} + sC_C)$.

The RHP zero has a stronger (degrading) influence in MOS than in BJT as

$$g_{m,MOS} < g_{m,BJT}$$

and, the RHP zero is closer to the Gain-bandwidth frequency thus decreasing the phase margin.

Problem 6.2-08

A two-stage, Miller-compensated CMOS op amp has a RHP zero at $20GB$, a dominant pole due to the Miller compensation, a second pole at p_2 and a mirror pole at $-3GB$. (a) If GB is 1MHz, find the location of p_2 corresponding to a 45° phase margin. (b) Assume that in part (a) that $|p_2| = 2GB$ and a nulling resistor is used to cancel p_2. What is the new phase margin assuming that GB = 1MHz? (c) Using the conditions of (b), what is the phase margin if C_L is increased by a factor of 4?

Solution

a.) Since the magnitude of the op amp is unity at GB, then let ω = GB to evaluate the phase.

$$\text{Phase margin= PM} = 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{|p_3|}\right) - \tan^{-1}\left(\frac{GB}{|z_1|}\right)$$

But, $p_1 = GB/A_o$, $p_3 = -3GB$ and $z_1 = -20GB$ which gives

$$PM = 45° = 180° - \tan^{-1}(A_o) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}(0.33) - \tan^{-1}(0.05)$$

$$45° \approx 90° - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}(0.33) - \tan^{-1}(0.05) = 90° - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - 18.26° - 2.86°$$

$$\therefore \quad \tan^{-1}\left(\frac{GB}{|p_2|}\right) = 45° - 18.26° - 2.86° = 23.48° \rightarrow \frac{GB}{|p_2|} = \tan(23.84°) = 0.442$$

$$\boxed{p_2 = -2.26 \cdot GB = -14.2\text{x}10^6 \text{ rads/sec}}$$

b.) The only roots now are p_1 and p_3. Thus,

$$\boxed{PM = 180° - 90° - \tan^{-1}(0.33) = 90° - 18.3° = 71.7°}$$

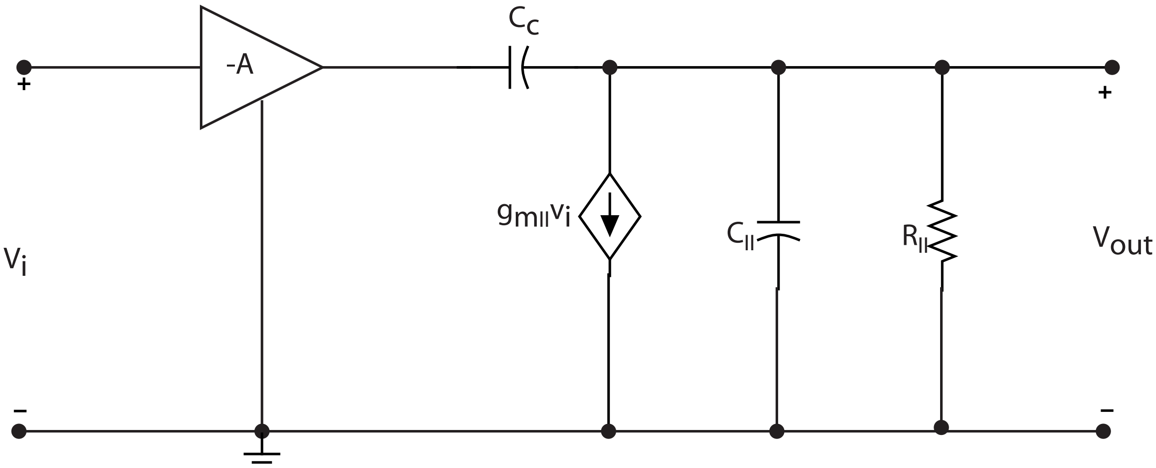
c.) In this case, z_1 is at -2GB and p_2 moves to -0.5GB. Thus the phase margin is now,

$$\boxed{PM = 90° - \tan^{-1}(2) + \tan^{-1}(0.5) - \tan^{-1}(0.33) = 90°-63.43°+26.57°-18.3° = 34.4°}$$

Problem 6.2-09

Derive Eq. (6.2-53).

Solution



Referring to the figure, applying KCL

$$\left(-Av_i(s) - v_{out}(s)\right)sC_C = g_{mII}v_i(s) + \left(sC_{II} + \frac{1}{R_{II}}\right)v_{out}(s)$$

or, $$\left(sAC_C + g_{mII}\right)v_i(s) = -\left(sC_{II} + \frac{1}{R_{II}} + sC_C\right)v_{out}(s)$$

or, $$\frac{v_{out}(s)}{v_i(s)} = -\frac{\left(sAC_C + g_{mII}\right)}{\left(sC_{II} + \frac{1}{R_{II}} + sC_C\right)}$$

or, $$\boxed{\frac{v_{out}(s)}{v_i(s)} = -\frac{AC_C}{\left(C_C + C_{II}\right)}\frac{\left(s + \frac{g_{mII}}{AC_C}\right)}{\left(s + \frac{1}{R_{II}\left(C_C + C_{II}\right)}\right)}}$$

Problem 6.2-10

For the two-stage op amp of Fig. 6.2-8, find W_1/L_1, W_6/L_6, and C_c if GB = 1 MHz, $|p_2|$ = 5 GB, z = 3 GB and $C_L = C_2$ = 20 pF. Use the parameter values of Table 3.1-2 and consider only the two-pole model of the op amp. The bias current in M5 is 40 μA and in M7 is 320 μA.

Solution

Given

$GB = 1$ MHz.

$p_2 = 5GB$

$z = 3GB$

$C_L = C_2 = 20$ pF

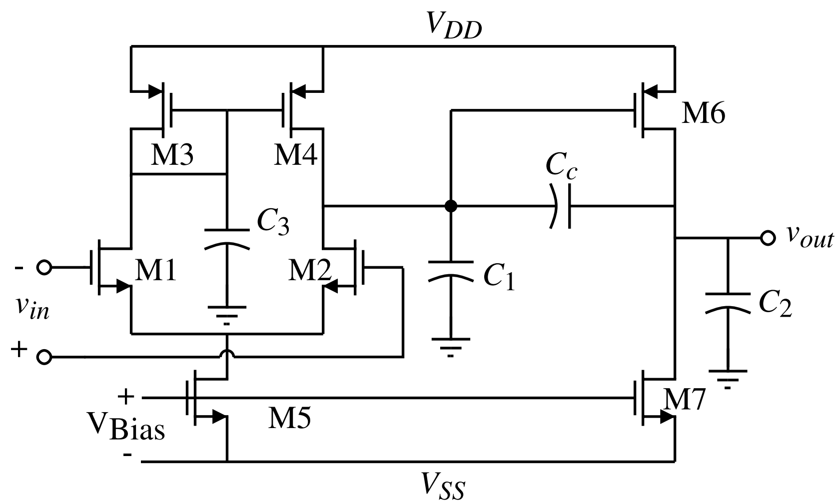


Figure 6.2-8 A two-stage op amp with various parasitic and circuit capacitances shown.

Now, $p_2 = \dfrac{g_{m6}}{C_2}$

or,

$g_{m6} = 628.3\mu\text{S}$

or,

$$\boxed{\left(\frac{W}{L}\right)_6 = \frac{g_{m6}^{\;2}}{2K_P^{'}I_{D6}} \cong 12.33}$$

RHP zero is given by

$$z = \frac{g_{m6}}{C_C}$$

or, $$\boxed{C_C = \frac{g_{m6}}{z} = 33.3\text{pF}}$$

Finally, Gain-bandwidth is given by

$$GB = \frac{g_{m1}}{C_C}$$

or, $g_{m1} = 209.4 \ \ \mu S$

or, $$\boxed{\left(\frac{W}{L}\right)_1 = \frac{g_{m1}^{\;2}}{2K_N^{'}I_{D1}} \cong 10}$$

Problem 6.2-11

In Fig. 6.2-13, assume that $R_I = 150$ kΩ, $R_{II} = 100$ kΩ, $g_{mII} = 500$ μS, $C_I = 1$ pF, $C_{II} = 5$ pF, and $C_c = 30$ pF. Find the value of R_z and the locations of all roots for (a) the case where the zero is moved to infinity and (b) the case where the zero cancels the next highest pole.

Solution

(a.) Zero at infinity.

$$R_z = \frac{1}{g_{mII}} = \frac{1}{500\mu\text{S}}$$

$$\boxed{R_z = \ 2\text{k}\Omega}$$

Check pole due to R_z.

$$p_4 = \frac{-1}{R_z C_I} = \frac{-1}{2\text{k}\Omega\cdot 1\text{pF}} = -500\text{x}10^6 \text{ rps or } 79.58 \text{ MHz}$$

The pole at p_2 is

$$p_2 \cong \frac{-g_{mII}C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \cong \frac{-g_{mII}}{C_{II}} = \frac{-500\mu\text{S}}{5\text{pF}} = 100\text{x}10^6 \text{ rps or } 15.9 \text{ MHz}$$

Therefore, p_2 is the next highest pole.

(b.) Zero at p_2.

$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)(1/g_{mII}) = \left(\frac{30+5}{30}\right)\frac{1}{500\mu\text{S}} = 2.33\text{k}\Omega$$

$$\boxed{R_z = \ 2.33\text{k}\Omega}$$

Problem 6.3-01

Express all of the relationships given in Eqs. (6.3-1) through (6.3-9) of Sec. 6.3 in terms of the large-signal model parameters and the dc values of drain current.

Solution

$$SR = \frac{I_5}{C_C} \tag{6.3-1}$$

$$A_{v1} = -\sqrt{\frac{2K_N'(W/L)_1}{I_1(\lambda_P+\lambda_N)^2}} \tag{6.3-2}$$

$$A_{v2} = -\sqrt{\frac{2K_P'(W/L)_6}{I_6(\lambda_P+\lambda_N)^2}} \tag{6.3-3}$$

$$GB = \frac{\sqrt{2K_N'(W/L)_1 I_1}}{C_C} \tag{6.3-4}$$

$$p_2 = -\frac{\sqrt{2K_p'(W/L)_6 I_6}}{C_L} \tag{6.3-5}$$

$$z_1 = \frac{\sqrt{2K_p'(W/L)_6 I_6}}{C_C} \tag{6.3-6}$$

Positive CMR

$$V_{in}(\max) = V_{DD} - \sqrt{\frac{I_5}{K_P'(W/L)_3}} - |V_{T03}|(\max) + V_{T1}(\min) \tag{6.3-7}$$

Negative CMR

$$V_{in}(\min) = V_{SS} + \sqrt{\frac{I_5}{K_N'(W/L)_1}} + \sqrt{\frac{2I_5}{K_N'(W/L)_5}} + V_{T1}(\max) \tag{6.3-8}$$

$$V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \tag{6.3-9}$$

Problem 6.3-02

Develop the relationship given in step 5 of Table 6.3-2.

Solution

Referring to the figure, p_3 is generated at the drain of M_3.

Resistance looking into the drain of M_3 is given by

$$R_{III} = \frac{1}{(g_{m3} + g_{ds3} + g_{ds1})} \cong \frac{1}{g_{m3}}$$

The total capacitance at the drain of M_3 is given by

$$C_{III} = (C_{gs3} + C_{gs4} + C_{bd3} + C_{bd1} + C_{gd1}) \cong 2C_{gs3}$$

Thus, the pole at the drain of M_3 is given by

$$p_3 = \frac{-1}{R_{III} C_{III}}$$

or, $$p_3 = \frac{-g_{m3}}{2C_{gs3}}$$

Now, if $\dfrac{g_{m3}}{2C_{gs3}} > 10GB$, then the contribution due to this pole on the phase margin is less than 5.7°, i.e., this pole can be neglected.

Problem 6.3-03

Show that the relationship between the W/L ratios of Fig. 6.3-1 which guarantees that $V_{SG4} = V_{SG6}$ is given by $S_6/S_4 = 2(S_7/S_5)$ where $S_i = W_i/L_i$.

Solution

Let us assume that

$$V_{SG4} = V_{SG6} \qquad (1)$$

or, $$V_{T4} + V_{dsat4} = V_{T6} + V_{dsat6} \qquad \rightarrow \qquad V_{T4} = V_{T6}$$

So, $$V_{dsat4} = V_{dsat6} \qquad \rightarrow \qquad \sqrt{\frac{2I_4}{K'_P (W/L)_4}} = \sqrt{\frac{2I_6}{K'_P (W/L)_6}}$$

or, $$\frac{(W/L)_6}{(W/L)_4} = \frac{I_6}{I_4} = \frac{I_7}{I_4} \qquad \rightarrow \qquad \frac{(W/L)_6}{(W/L)_4} = \frac{2I_7}{I_5}$$

Since, $V_{GS5} = V_{GS7}$, we have

$$\boxed{\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}}$$

Problem 6.3-04

Draw a schematic of the op amp similar to Fig. 6.3-1 but using p-channel input devices. Assuming that same bias currents flow in each circuit, list all characteristics of these two circuits that might be different and tell which is better or worse than the other and by what amount (if possible).

Solution

In working this problem we shall assume that $K_N' > K_P'$.

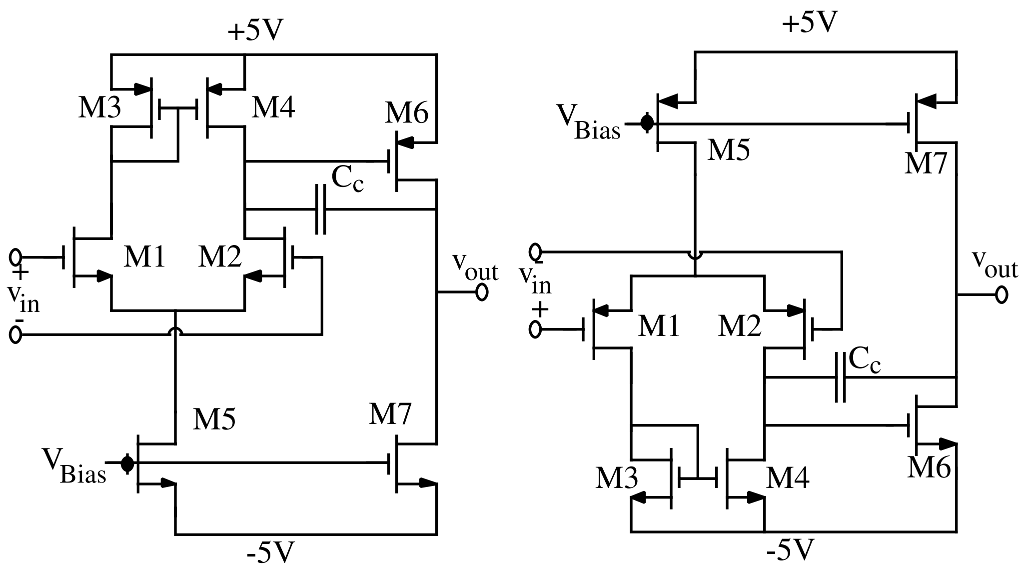


Fig. S6.3-04

Characteristic	Circuit 1	Circuit 2
Noise	Worse but not by much because the first stage gain is higher.	Better but degraded by the lower first stage gain
Phase margin	Poorer (g_{mI} larger but g_{mII} is smaller)	Better
Gainbandwidth	Larger ($GB = g_{mI}/C_c$)	Smaller
V_{icm}(max.)	Larger	Smaller
V_{icm}(min.)	Smaller	Larger
Sourcing output current	Large	Constrained
Sinking output current	Constrained	Large

Problem 6.3-05

Use the op amp designed in Ex. 6.3-1 and assume that the input transistors, M1 and M2 have their bulks connected to -2.5V. How will this influence the performance of the op amp designed in Ex. 6.3-1? Use the W/L values of Ex. 6.3-1 for this problem. Wherever the performance is changed, calculate the new value of performance and compare with the old.

Solution

Referring to the design in Example. 6.3-1, it can be shown that the threshold voltages of the input transistors M_1 and M_2 are increased due to body effect $(V_{BS} \neq 0)$

$$V_{BS1} = V_{BS2} = -V_{DS5}$$

Let us assume that $V_{DS5} = 1$ V. Then,

$$V_{T1} = V_{T2} = V_{T0} + \gamma_N \left(\sqrt{2\phi + V_{SB1}} - \sqrt{2\phi}\right)$$

or, $$V_{T1} = V_{T2} = 0.89 \text{ V}$$

Assuming that the bias currents in the various branches remain the same, the small-signal g_m and g_{ds} values will remain the same. Considering all the performance specifications of the op amp, only the ICMR will be effected.

The maximum input common-mode voltage can be given by

$$V_{in}(\max) = V_{DD} + V_{T1}(\min) - V_{T3}(\max) - \sqrt{\frac{2I_3}{K_P'(W/L)_3}}$$

or, $$V_{in}(\max) = 2.5 + 0.55 - (0.89 + 0.15) - 0.2 = 1.81 \text{ V}$$

The original value of $V_{in}(\max)$ was 2 V.

The minimum input common-mode voltage can be given by

$$V_{in}(\min) = V_{SS} + V_{T1}(\max) + \sqrt{\frac{2I_1}{K_N'(W/L)_1}} + \sqrt{\frac{2I_5}{K_N'(W/L)_5}}$$

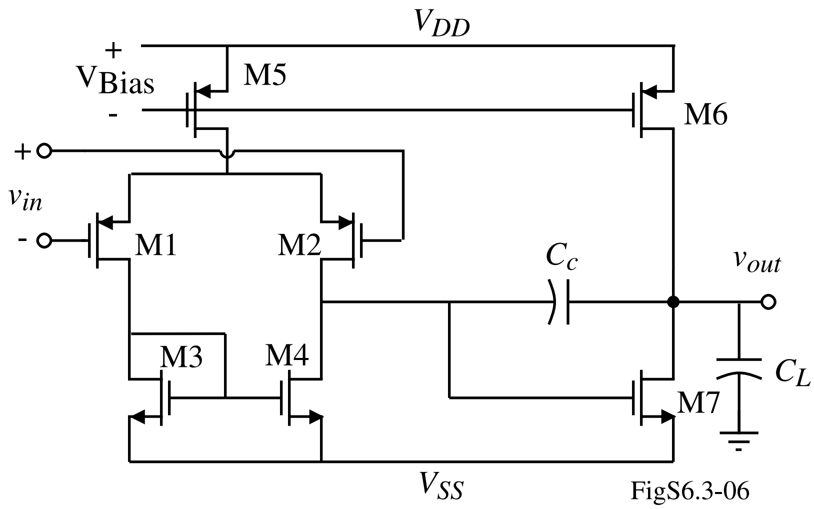
or, $$V_{in}(\min) = -2.5 + 0.89 + 0.15 + 0.3 + 0.35 = -0.81 \text{ V}$$

The original value of $V_{in}(\min)$ was -1 V.

The new value of ICMR is 2.62 V as compared to 3 V.

Problem 6.3-06

Repeat Ex. 6.3-1 for a p-channel input, two-stage op amp. Choose the same currents for the first-stage and second-stage as in Ex. 6.3-1.



FigS6.3-06

Solution

Following the steps of Ex. 6.3-1 we have the following:

C_c = 3pF, I_5 = 30µA,

$$(W/L)_3 = \frac{30 \text{ x } 10^{-6}}{(110\text{x}10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 6.82 \rightarrow W_3 = W_4 = \underline{\underline{7\mu\text{m}}}$$

Next, we find that g_{m1} = (5x10^6)(2π)(3x10^{-12}) = 94.25µS which gives

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}{}^2}{2K'_N I_1} = \frac{(94.25)^2}{2\cdot 50\cdot 15} = 5.92 \qquad \rightarrow W_1 = W_2 = \underline{\underline{6\mu\text{m}}}$$

Calculating V_{SD5}(sat) we get

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30\text{x}10^{-6}}{50\text{x}10^{-6}\cdot 3}} - .85 = 0.203\text{V}$$

$$\therefore \qquad (W/L)_5 = \frac{2(30 \text{ x } 10^{-6})}{(50 \text{ x } 10^{-6})(0.203)^2} = 29.1 \qquad \rightarrow \qquad W_5 = \underline{\underline{29\mu\text{m}}}$$

Next, we find $g_{m4} \approx$ 150µS which gives

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} = 7\cdot\frac{942.5}{150} = 43.4 \approx 43 \qquad \rightarrow \qquad W_6 = \underline{\underline{43\mu\text{m}}}$$

The output stage current is,

$$I_6 = \frac{(942.5 \text{ x } 10^{-6})^2}{(2)(110 \text{ x } 10^{-6})(43)} = 93\mu\text{A}$$

$$\therefore \qquad (W/L)_7 = (W/L)_5\left(\frac{93\mu\text{A}}{20\mu\text{A}}\right) = 29(93/30) = 89.9 \qquad \rightarrow W_7 = \underline{\underline{90\mu\text{m}}}$$

The gain and power dissipation are identical with that in Ex. 6.3-1.

Problem 6.3-07

For the p-channel input, CMOS op amp of Fig. P6.3-7, calculate the open-loop, low-frequency differential gain, the output resistance, the power consumption, the power-supply rejection ratio at DC, the input common-mode range, the output-voltage swing, the slew rate, the common-mode rejection ratio, and the unity-gain bandwidth for a load capacitance of 20 pF. Assume the model parameters of Table 3.1-2. Design the W/L ratios of M9 and M10 to give a resistance of $1/g_{m6}$ and use the simulation program SPICE to find the phase margin and the 1% settling time for no load and for a 20 pF load.

Solution

Bias current calculation:

$$V_{T8} + V_{ON8} + I_8.R_S = V_{dd} - V_{ss} \quad \text{or,} \quad V_{T8} + \sqrt{\frac{2.I_8}{3.K_p'}} = 5 - I_8.R_s. \tag{1}$$

Solving for I_8 quadratically gives, $I_8 = 36\mu A$, $I_5 = 36\mu A$, and $I_7 = 60\mu A$

Using the formula, $g_m = \sqrt{2.K' \frac{W}{L}.I}$ and $g_{ds} = \lambda I$ we get,

$$g_{m2} = 60\mu S \;,\; g_{ds2} = 0.9\mu S \;,\; g_{ds4} = 0.72\mu S \tag{2}$$

$$g_{m6} = 363\mu S \;,\; g_{ds6} = 3\mu S \;,\; g_{ds7} = 2.4\mu S \tag{3}$$

Small-signal open-loop gain:

The small-signal voltage gain can be expressed as,

$$A_{V1} = \frac{-g_{m2}}{(g_{ds2} + g_{ds4})} = -37 \quad \text{and} \quad A_{V2} = \frac{-g_{m6}}{(g_{ds6} + g_{ds7})} = -67$$

Thus, total open-loop gain is, $A_v = A_{v1} \cdot A_{v2} = 2489\text{V/V}$ (3)

Output resistance:

$$R_{out} = \frac{1}{(g_{ds6} + g_{ds7})} = 185K\Omega \tag{5}$$

Power dissipation:

$$P_{diss} = 5(36 + 36 + 60)\mu W = 660\mu W \tag{6}$$

ICMR:

$$V_{in,\max} = 2.5 - V_{T1} - V_{ON1} - V_{ON5} = 0.51V \tag{7}$$

$$V_{in,\min} = -2.5 - V_{T1} + V_{T3} + V_{ON3} = -2.21V \tag{8}$$

Output voltage swing:

$$V_{0,\max} = 2.5 - V_{ON7} = 1.81V \tag{9}$$

Slew Rate:

Slew rate under no load condition can be given as $SR = \frac{I_5}{C_C} = 6V/\mu s$

Problem 6.3-7 - Continued

In presence of a load capacitor of 20 pF, slew rate would be,

$$SR = \min\left[\frac{I_5}{C_c},\frac{I_7}{C_L}\right]$$

CMRR:

Under perfectly balanced condition where $I_1 = I_2$, if a small signal common-mode variation occurs at the two input terminals, the small signal currents $i_1 = i_2 = i_3 = i_4$ and the differential output current at node (7) is zero. So, ideally, common-mode gain would be zero and the value for CMRR would be infinity.

GBW:

Let us design M9 and M10 first. Both these transistors would operate in triode region and will carry zero dc current. Thus, $V_{ds9} = V_{ds10} \cong 0$. The equation of drain current in triode region is given as,

$$I_D \cong K' \frac{W}{L}(V_{GS} - V_T)V_{DS} \ .$$

The on resistance of the MOS transistor in triode region of operation would be,

$$R_{ON} = K' \frac{W}{L}(V_{GS} - V_T) \ .$$

It is intended to make the effective resistance of M9 and M10 equal to $\dfrac{1}{g_{m6}}$.

So,
$$K'_9\left(\frac{W_9}{L_9}\right)(V_{GS9}\text{-}V_{T9}) + K'_{10}\left(\frac{W_{10}}{L_{10}}\right)(V_{GS10}\text{-}V_{T10}) = g_{m6} \qquad (11)$$

$$V_{D4} = V_{D3} = -2.5 + V_{T3} + V_{ON3} = -1.51V$$

Thus,

$$V_{GS9} \cong 4V \quad \text{and} \quad V_{GS10} \cong -1V \ .$$

Putting the appropriate values in (11), we can solve for the aspect ratios of M9 and M10. One of the solutions could be,

$$K'_9\left(\frac{W_9}{L_9}\right) = \frac{1}{1} \quad \text{and} \quad K'_{10}\left(\frac{W_{10}}{L_{10}}\right) = \text{very small} \qquad (12)$$

The dominant pole could be calculated as,

$$p_1 = \frac{-(g_{ds4} + g_{ds2})}{2.\pi.A_{V1}.C_C} = -1.16KHz.$$

And the load pole would be,

$$p_2 = \frac{-g_{m6}}{2.\pi.C_L} = -2.8MHz. \quad \text{for a 20 pF load.}$$

It can be noted that in this problem, the product of the open-loop gain and the dominant pole is approximately equal to the load pole. Thus, the gain bandwidth is approximately equal to 2.8 MHz and the phase margin would be close to 45 degrees.

Problem 6.3-08

Design the values of W and L for each transistor of the CMOS op amp in Fig. P6.3-8 to achieve a differential voltage gain of 4000. Assume that K'_N = 110 μA/V^2, K'_P = 50 μA/V^2, $V_{TN} = -V_{TP}$ = 0.7 V, and $\lambda_N = \lambda_P$ = 0.01 V^{-1}. Also, assume that the minimum device dimension is 2 μm and choose the smallest devices possible. Design C_c and R_z to give GB = 1 MHz and to eliminate the influence of the RHP zero. How much load capacitance should this op amp be capable of driving without suffering a degradation in the phase margin? What is the slew rate of this op amp? Assume $V_{DD} = -V_{SS}$ = 2.5V and R_B = 100 kΩ.

Solution

Given

$$A_v = 4000 \text{ V/V} \qquad GB = 1 \text{ MHz} \qquad \text{and} \qquad z_1 = \infty$$

For $I_5 = 50\ \mu A$, let us assume $I_8 = 40\ \mu A$

Thus, $V_{GS8} = 1$ V

or, $$\left(\frac{W}{L}\right)_8 = \frac{2I_8}{K'_N(V_{GS8} - V_{T8})^2} \cong \frac{16}{2}\ \frac{\mu m}{\mu m}$$

or, $$\left(\frac{W}{L}\right)_5 = \frac{5}{4}\left(\frac{W}{L}\right)_8 = \frac{20}{2}\ \frac{\mu m}{\mu m}$$

and, $$\left(\frac{W}{L}\right)_7 = \frac{40}{2}\ \frac{\mu m}{\mu m}$$

Also, let us assume that $V_{SG3} = V_{SG4} = 1.5$ V

or, $$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{2I_3}{K'_P(V_{SG3} - |V_{T3}|)^2} = \frac{3}{2}\ \frac{\mu m}{\mu m}$$

The aspect ratio of M_6 can be calculated as

$$\left(\frac{W}{L}\right)_6 = 2\left(\frac{W}{L}\right)_7\left(\frac{L}{W}\right)_5\left(\frac{W}{L}\right)_4 \quad \rightarrow \quad \left(\frac{W}{L}\right)_6 = \frac{12}{2}\ \frac{\mu m}{\mu m}$$

or, $$g_{m6} = 245\ \mu S$$

In order to eliminate the RHP zero $\quad R_Z = \dfrac{1}{g_{m6}} \cong 4\ K\Omega$

Now,

$$A_v = \frac{2g_{m1}g_{m6}}{I_5 I_7(\lambda_P + \lambda_N)^2}$$

Problem 6.3-08 - Continued

or, $$g_{m1} = \frac{A_v I_5 I_7 (\lambda_P + \lambda_N)^2}{2 g_{m6}}$$

or, $$g_{m1} = 16 \ \mu S$$

or, $$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}{}^2}{K_N' I_5} \qquad \rightarrow \qquad \left(\frac{W}{L}\right)_1 = 0.00145$$

Let us assume a more realistic value as

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{2}{2} \ \frac{\mu m}{\mu m}$$

This will give

$$g_{m1} = 74.2 \ \mu S \ \text{ and } \ A_v = 9090 \ \text{V/V}$$

Now, $$C_C = \frac{g_{m1}}{GB} = 74.2 \ \text{pF}$$

The phase margin can be approximated as

$$PM = 180^\circ - \left[\tan^{-1}\left(\frac{GB}{p_1}\right) + \tan^{-1}\left(\frac{GB}{p_2}\right)\right]$$

Considering the worst-case phase margin to be 60 degrees

$$60^\circ = 180^\circ - \left[90^\circ + \tan^{-1}\left(\frac{GB}{p_2(\text{min})}\right)\right]$$

or, $$p_2(\text{min}) = 1.732 GB = 1.732 \ \text{MHz.}$$

or, $$C_L(\text{max}) = \frac{g_{m6}}{p_2(\text{min})} = 141.5 \ \text{pF}$$

Problem 6.3-09

Use the electrical model parameters of the previous problem to design W_3, L_3, W_4, L_4, W_5, L_5, C_c, and R_z of Fig. P6.3-8 if the dc currents are increased by a factor of two and if $W_1 = L_1 = W_2 = L_2 = 2\ \mu$m to obtain a low-frequency, differential-voltage gain of 5000 and a *GB* of 1 MHz. All devices should be in saturation under normal operating conditions and the effect of the RHP should be canceled. How much load capacitance should this op amp be able to drive before suffering a degradation in the phase margin? What is the slew rate of this op amp?

Solution

Given

$$W_1 = L_1 = W_2 = L_2 = 2\ \ \mu m$$

Referring to the solution of P6.3-8

$$g_{m1} = 104.8\ \ \mu S$$

or, $$C_C = \frac{g_{m1}}{GB} = 105\ \text{pF}$$

Also,

$$g_{m6} = \frac{A_v I_5 I_7 (\lambda_P + \lambda_N)^2}{2g_{m1}} = 190.8\ \ \mu S$$

or, $$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}^{\ 2}}{K_P' I_7} = \frac{7.2}{2}\ \frac{\mu m}{\mu m}$$

and, $$R_Z = \frac{1}{g_{m6}} \cong 5.24\ K\Omega$$

Now,

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 0.5\left(\frac{W}{L}\right)_6\left(\frac{L}{W}\right)_7\left(\frac{W}{L}\right)_5 \cong \frac{2}{2}\ \frac{\mu m}{\mu m}$$

Assuming $V_{GS5} = 1$ V

$$\left(\frac{W}{L}\right)_5 = \frac{2I_5}{K_N'(V_{GS5} - V_{T5})^2} \cong \frac{40}{2}\ \frac{\mu m}{\mu m}$$

Slew rate can be expressed as

$$SR = \frac{I_5}{C_C} \cong 1\ V/\mu s$$

Considering the worst-case phase margin to be 60 degrees

$$60° = 180° - \left[90° + \tan^{-1}\left(\frac{GB}{p_2(\text{min})}\right)\right]$$

or, $$p_2(\text{min}) = 1.732GB = 1.732\ \ \text{MHz.}$$

or, $$C_L(\text{max}) = \frac{g_{m6}}{p_2(\text{min})} = 110\ \text{pF}$$

Problem 6.3-10

For the op amp shown in Fig. P6.3-10, assume all transistors are operating in the saturation region and find (a.) the dc value of I_5, I_7 and I_8, (b.) the low frequency differential voltage gain, $A_{vd}(0)$, (c.) the GB in Hz, (d.) the positive and negative slew rates, (e.) the power dissipation, and (f.) the phase margin assuming that the open-loop unity gain is 1MHz.

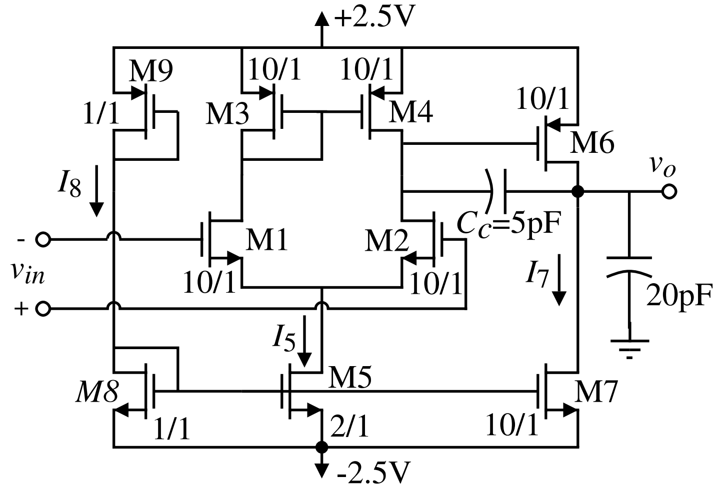


Figure P6.3-10

Solution

(a.)

$$5\text{V} = \sqrt{\frac{2\cdot I_8}{K_P\cdot 1}} + 0.7 + \sqrt{\frac{2\cdot I_8}{K_N\cdot 1}} + 0.7 \;\Rightarrow\; 3.6 = \sqrt{I_8}\left(\frac{1}{\sqrt{25}} + \frac{1}{\sqrt{55}}\right) \Rightarrow I_8 = 10.75\mu\text{A}$$

$\therefore$ $\boxed{I_8 = 10.75\mu\text{A},\;\; I_5 = 2I_8 = 21.5\mu\text{A},\;\; \text{and}\;\; I_7 = 10I_8 = 107.5\mu\text{A}}$

(b.) $A_v(0) = g_{m1}(r_{ds2}||r_{ds4})g_{m6}(r_{ds6}||r_{ds7})$

$g_{m1} = \sqrt{2\cdot K_N\cdot 10\cdot I_8} = 153.8\mu\text{S}$, $g_{m6} = \sqrt{2\cdot K_P\cdot 10\cdot I_7} = 327.9\mu\text{S}$,

$r_{ds2} = \frac{25}{10.75} = 2.33\text{M}\Omega$,

$r_{ds4} = \frac{20}{10.75} = 1.86\text{M}\Omega$, $r_{ds6} = \frac{20}{107.5} = 0.186\text{M}\Omega$, and $r_{ds7} = \frac{25}{107.5} = 0.233\text{M}\Omega$.

$\therefore$ $\boxed{A_v(0) = (153.8\mu\text{S})(1.034\text{M}\Omega)(327.9\mu\text{S})(0.1034\text{M}\Omega) = 5395\text{ V/V}}$

(c.) $\boxed{\text{GB} = \frac{g_{m1}}{C_c} = \frac{153.8\mu\text{S}}{5\text{pF}} = 30.76\text{Mradians/sec} = 4.90\text{MHz}}$

(d.) Due to C_c: $|SR| = \frac{I_5}{C_c} = \frac{21.5\mu\text{A}}{5\text{pF}} = 4.3\text{ V/}\mu\text{s}$

Due to C_L: $|\text{SR}| = \frac{I_7 - I_5}{C_L} = \frac{86\mu\text{A}}{20\text{pF}} = 4.3\text{V/}\mu\text{s}$ $\therefore$ $\boxed{|\text{SR}| = 4.3\text{V/}\mu\text{s}}$

(e.) $\boxed{\text{Power Dissipation} = 5(I_8+I_5+I_7) = 5(139.75\mu\text{A}) = 0.699\text{mW}}$

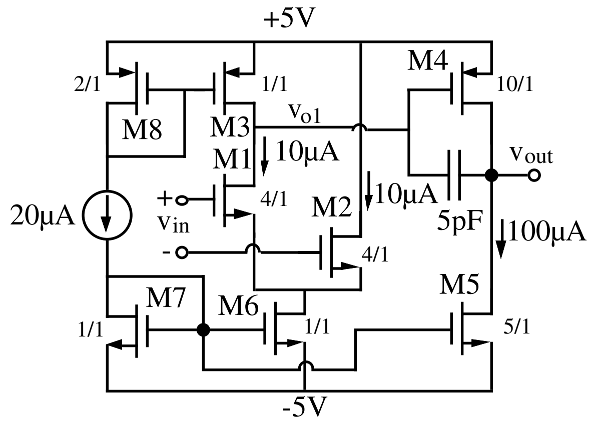
(f.) Phase margin $= 180° - \tan^{-1}\left(\frac{GB}{GB/A_v(0)}\right) - \tan^{-1}\left(\frac{GB}{p_2}\right) - \tan^{-1}\left(\frac{GB}{z}\right)$

$$p_2 = \frac{g_{m6}}{C_L} = 16.395\text{x}10^6 \text{ rads/sec} \quad \text{and } z = \frac{g_{m6}}{C_c} = 65.6\text{x}10^6 \text{ rads/sec}$$

$\therefore$ $\boxed{\text{Phase margin} = 90° - \tan^{-1}\left(\frac{6.28}{16.395}\right) - \tan^{-1}\left(\frac{6.28}{65.6}\right) = 63.6°}$

Problem 6.3-11

A simple CMOS op amp is shown. Use the following model parameters and find the numerical value of the small signal differential voltage gain, v_{out}/v_{in}, output resistance, R_{out}, the dominant pole, p_1, the unity-gainbandwidth, GB, the slew rate, SR, and the dc power dissipation. K_N'=24µA/V^2, K_P' = 8µA/V^2, V_{TN} = -V_{TP} = 0.75V, λ_N = 0.01V^{-1} and λ_P = 0.02V^{-1}.



Solution

Small signal differential voltage gain: By intuitive analysis methods,

$$\frac{v_{o1}}{v_{in}} = \frac{-0.5g_{m1}}{g_{ds1}+g_{ds3}} \quad \text{and} \quad \frac{v_{out}}{v_{o1}} = \frac{-g_{m4}}{g_{ds4}+g_{ds5}} \quad \rightarrow \quad \frac{v_{out}}{v_{in}} = \frac{0.5g_{m1}g_{m4}}{(g_{ds1}+g_{ds3})(g_{ds4}+g_{ds5})}$$

$$g_{m1} = \sqrt{\frac{2K_NW_1I_{D1}}{L_1}} = \sqrt{24\cdot 2\cdot 4\cdot 10}\ \text{x}10^{-6} = 43.82\mu\text{S}$$

$$g_{ds1} = \lambda_N I_{D1} = 0.01\cdot 10\mu\text{A} = 0.1\mu\text{S}, \quad g_{ds3} = \lambda_P I_{D3} = 0.02\cdot 10\mu\text{A} = 0.2\mu\text{S}$$

$$g_{m4} = \sqrt{\frac{2K_PW_4I_{D4}}{L_4}} = \sqrt{2\cdot 8\cdot 10\cdot 100}\ \text{x}10^{-6} = 126.5\mu\text{S}$$

$$g_{ds4} = \lambda_P I_{D4} = 0.02\cdot 100\mu\text{A} = 2\mu\text{S}, \quad g_{ds5} = \lambda_N I_{D5} = 0.01\cdot 100\mu\text{A} = 1\mu\text{S}$$

$$\therefore \boxed{\frac{v_{out}}{v_{in}} = \frac{0.5\cdot 43.82\cdot 126.5}{(0.1+0.2)(1+2)} = 3{,}079\text{V/V}}$$

Output resistance:

$$\boxed{R_{out} = \frac{1}{g_{ds4}+g_{ds5}} = \frac{10^6}{1+2} = 333\text{k}\Omega}$$

Dominant pole, p_1:

$$|p_1| = \frac{1}{R_1C_1} \quad \text{where } R_1 = \frac{1}{g_{ds1}+g_{ds3}} = \frac{10^6}{0.1+0.2} = 3.33\text{M}\Omega$$

$$\text{and } C_1 = C_c(1+|A_{v2}|) = 5\text{pF}\left(1 + \frac{g_{m4}}{g_{ds4}+g_{ds5}}\right) = 5\left(1+\frac{126.5}{3}\right) = 215.8\text{pF}$$

$$\therefore |p_1| = \frac{10^6}{3.33\cdot 2.15.8} = 1{,}391 \text{ rads/sec} \rightarrow \boxed{|p_1| = 1{,}391 \text{ rads/sec} = 221\text{Hz}}$$

$$\text{GB} = \frac{0.5\cdot g_{m1}}{C_c} = \frac{0.5\cdot 43.82\text{x}10^{-6}}{5\text{x}10^{-12}} = 4.382\text{Mrads/s} \quad \boxed{\text{GB=4.382 Mrads/sec=0.697MHz}}$$

$$\boxed{\text{SR} = \frac{I_{D6}}{C_c} = \frac{10\mu\text{A}}{5\text{pF}} = 2\text{V}/\mu\text{s}} \qquad \boxed{P_{diss} = 10\text{V}(140\mu\text{A}) = 1.4\text{mW}}$$

Problem 6.3-12

On a log-log plot with the vertical axis having a range of 10^{-3} to 10^{+3} and the horizontal axis having a range of 1 μA to 100 μA, plot the low-frequency gain $A_v(0)$, the unity-gain bandwidth GB, the power dissipation P_{diss}, the slew rate SR, the output resistance R_{out}, the magnitude of the dominant pole $|p_1|$, and the magnitude of the RHP zero z, all normalized to their respective values at $I_B = 1$ μA as a function of I_B from 1 μA to 100 μA for the standard two-stage CMOS op amp. Assume the current in M5 is $k_1 I_B$ and the output current (M6) is $k_2 I_B$.

Solution

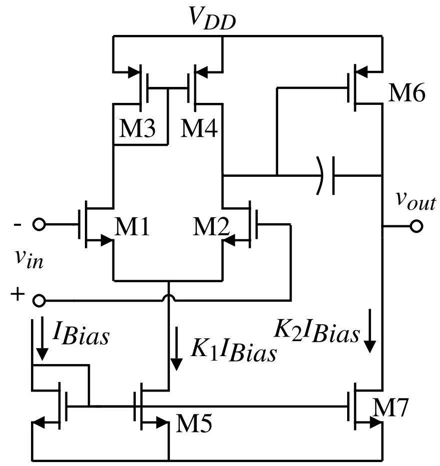


Fig. 6.3-04D

$$GB = \frac{g_{mI}}{C_c} \propto \sqrt{I_{Bias}}$$

$$P_{diss} = (V_{DD}+|V_{SS}|)(1+K_1+K_2)I_{Bias} \propto I_{bias}$$

$$SR = \frac{K_1 I_{Bias}}{C_c} \propto I_{Bias}$$

$$R_{out} = \frac{1}{2\lambda K_2 I_{Bias}} \propto \frac{1}{I_{Bias}}$$

$$|p_1| = \frac{1}{g_{mII}R_I R_{II} C_c} \propto \frac{I_{Bias}{}^2}{\sqrt{I_{Bias}}} \propto I_{Bias}{}^{1.5}$$

$$|z| = \frac{g_{mII}}{C_c} \propto \sqrt{I_{Bias}}$$

Illustration of the I_{bias} dependence $\rightarrow$

Plot is done for normalized bias current.

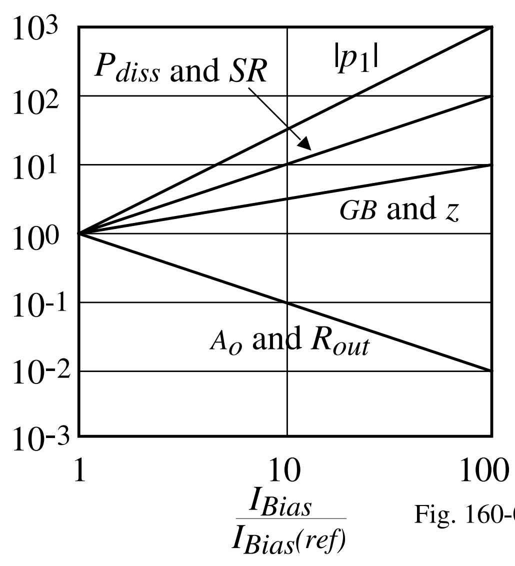


Fig. 160-05

Problem 6.3-13

Develop the expression similar to Eq. (6.3-32) for the W/L ratio of M6A in Fig. P6.3-13 that will cause the right-half plane zero to cancel the output pole. Repeat Ex. 6.3-2 using the circuit of Fig. P6.3-13 using the values of the transistors in Ex. 6.3-1.

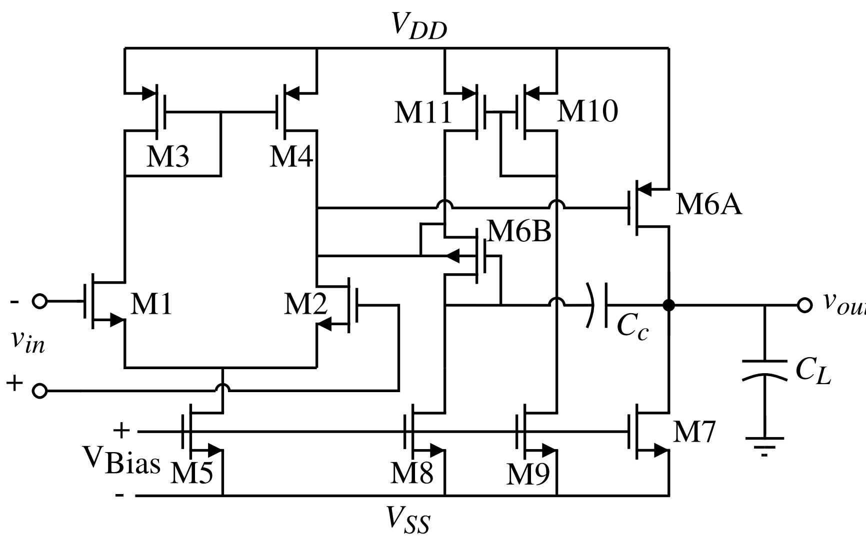


Figure P6.3-13 Nulling resistor implemented by a MOS diode.

Solution

$$R_Z = \frac{1}{g_{m6B}} = \frac{1}{\sqrt{2K_P'(W/L)_{6B}I_8}}$$

Now, $z_1 = p_2$

or, $\dfrac{-1}{C_C(R_Z - 1/g_{m6A})} = \dfrac{-g_{m6A}}{C_L} \quad\rightarrow\quad \dfrac{-1}{C_C(1/g_{m6B} - 1/g_{m6A})} = \dfrac{-g_{m6A}}{C_L}$

or, $$\left(\frac{W}{L}\right)_{6A} = \left(\frac{W}{L}\right)_{6A}\frac{I_8}{I_7}\left(\frac{C_C + C_L}{C_C}\right)^2 \qquad (1)$$

Referring to Example 6.3-1

$$\left(\frac{W}{L}\right)_{6A} = \left(\frac{W}{L}\right)_{6} = 94 \quad \text{and,} \quad I_8 = I_9 = I_{10} = I_{11} = 15 \ \mu A$$

From Equation (1)

$$\left(\frac{W}{L}\right)_{6B} = 31.7 \cong 32$$

or, $g_{m6B} = 218 \ \mu S$

$$g_{m6A} = 945 \ \mu S$$

$$R_Z = \frac{1}{g_{m6B}} = 4.59 \ K\Omega$$

$$z_1 = \frac{-1}{C_C(R_Z - 1/g_{m6A})} = -15 \text{ MHz.}$$

$$p_2 = \frac{-g_{m6A}}{C_L} = -15 \text{ MHz.}$$

Problem 6.3-14

Use the intuitive approach presented in Sec. 5.2 to calculate the small-signal differential voltage gain of the two-stage op amp of Fig. 6.3-1.

Solution

Referring to the figure, the small-signal currents in the first stage can be given by

$$i_{d4} = i_{d3} = i_{d1} = -g_{m1}\frac{v_{in}}{2}$$

and, $$i_{d2} = g_{m2}\frac{v_{in}}{2}$$

So, $$i_{out1} = i_{d4} - i_{d2} = -(g_{m1} + g_{m2})\frac{v_{in}}{2}$$

or, $$i_{out1} = -(g_{m1})v_{in}$$

The small-signal output conductance of the first stage is

$$g_{out1} = g_{ds2} + g_{ds4}$$

Thus, the small-signal gain of the first stage becomes

$$A_{v1} = \frac{-g_{m1}}{(g_{ds2} + g_{ds4})}$$

Considering the second gain stage, the gain can be given by

$$A_{v2} = \frac{-g_{m6}}{(g_{ds6} + g_{ds7})}$$

Thus, the overall small-signal voltage gain becomes

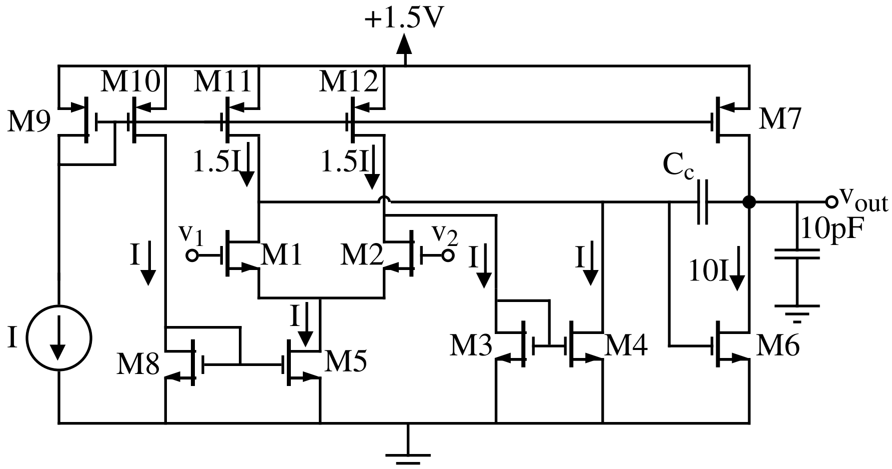
$$\boxed{A_v = A_{v1}A_{v2} = \frac{g_{m1}g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}}$$

Problem 6.3-15

A CMOS op amp capable of operating from 1.5V power supply is shown. All device lengths are 1µm and are to operate in the saturation region. Design all of the W values of every transistor of this op amp to meet the following specifications.

Slew rate = ±10V/µs	V_{out}(max) = 1.25V	V_{out}(min) = 0.75V
V_{ic}(min) = 1V	V_{ic}(max) = 2V	GB = 10MHz
Phase margin = 60° when the output pole = 2GB and the RHP zero = 10GB. Keep the mirror pole ≥ 10GB (C_{ox} = 0.5fF/µm²).		

Your design should meet or exceed these specifications. Ignore bulk effects in this problem and summarize your W values to the nearest micron, the value of C_c(pF), and I(µA) in the following table. Use the following model parameters: K_N'=24µA/V², K_P' = 8µA/V², V_{TN} = - V_{TP} = 0.75V, λ_N = 0.01V⁻¹ and λ_P = 0.02V⁻¹.



Solution

1.) p_2=2GB ⇒ $g_{m6}/C_L=2g_{m1}/C_c$ and z=10GB ⇒ $g_{m6}=10g_{m1}$. ∴ $\boxed{C_c = C_L/5 = 2\text{pF}}$

2.) $I = C_c\cdot SR = (2\text{x}10^{-11})\cdot 10^7 = 20\mu A$ ∴ $\boxed{I = 20\mu A}$

3.) $GB = g_{m1}/C_c \Rightarrow g_{m1} = 20\pi\text{x}10^6\cdot 2\text{x}10^{-12} = 40\pi\text{x}10^{-6} = 125.67\mu S$

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{2K_N(I/2)} = \frac{(125.67\text{x}10^{-6})^2}{2\cdot 24\text{x}10^{-6}\cdot 10\text{x}10^{-6}} = 32.9 \Rightarrow \boxed{W1 = W_2 = 33\mu m}$$

4.) $V_{ic}(\min) = V_{DS5}(\text{sat.})+V_{GS1}(10\mu A) = 1V \rightarrow V_{DS5}(\text{sat.}) = 1-\sqrt{\frac{2\cdot 10}{24\cdot 33}} -0.75 = 0.0908$

$$V_{DS5}(\text{sat}) = 0.0908 = \sqrt{\frac{2\cdot I}{K_N S_5}} \rightarrow W_5 = \frac{2\cdot 20}{24\cdot(0.0908)^2} = 201.9\mu m \quad \boxed{W_5 = 202\mu m}$$

5.) $V_{ic}(\max) = V_{DD}-V_{SD11}(\text{sat})+V_{TN} = 1.5-V_{SD11}(\text{sat})+0.75 = 2V \rightarrow V_{SD11}(\text{sat}) = 0.25V$

$$V_{SD11}(\text{sat}) \le \sqrt{\frac{2\cdot 1.5I}{K_P\cdot S_{11}}} \rightarrow S_{11} = W_{11} \ge \frac{2\cdot 30}{(0.25)^2\cdot 8} = 120 \rightarrow$$

$\underline{\underline{W_{11}=W_{12}\ge 120\mu m}}$

Problem 6.3-15 - Continued

6.) Choose $S_3(S_4)$ by satisfying $V_{ic}(max)$ specification then check mirror pole.

$$V_{ic}(max) \geq V_{GS3}(20\mu A) + V_{TN} \rightarrow V_{GS3}(20\mu A) = 1.25V \geq \sqrt{\frac{2\cdot I}{K_N\cdot S_3}} + 0.75V$$

$$S_3 = S_4 = \frac{2\cdot 20}{(0.5)^2\cdot 24} = 6.67 \Rightarrow \boxed{W_3 = W_4 = 7\mu m}$$

7.) Check mirror pole ($p_3 = g_{m3}/C_{Mirror}$).

$$p_3 = \frac{g_{m3}}{C_{Mirror}} = \frac{g_{m3}}{2\cdot 0.667\cdot W_3\cdot L_3\cdot C_{ox}} = \frac{\sqrt{2\cdot 24\cdot 6.67\cdot 20}\text{x}10^{-6}}{2\cdot 0.667\cdot 6.67\cdot 0.5\text{x}10^{-15}} = 17.98\text{x}10^9$$

which is much greater than 10GB ($0.0628\text{x}10^9$). Therefore, W_3 and W_4 are OK.

8.) $g_{m6} = 10g_{m1} = 1256.7\mu S$

a.) $g_{m6} = \sqrt{2K_N S_6 10I} \Rightarrow W_6 = 164.5\mu m$

b.) $V_{out}(min) = 0.5 \Rightarrow V_{DS6}(sat) = 0.5 = \sqrt{\frac{2\cdot 10I}{K_N S_6}} \Rightarrow W_6 = 66.67\mu m$

Therefore, use $\boxed{W_6 = 165\mu m}$

Note: For proper mirroring, $S_4 = \frac{I_4}{I_6} S_6 = 8.25\mu m$ which is close enough to 7μm.

9.) Use the $V_{out}(max)$ specification to design W_7.

$$V_{out}(max) = 0.25V \geq V_{DS7}(sat) = \sqrt{\frac{2\cdot 200\mu A}{8\text{x}10^{-6}\cdot S_7}}$$

$$\therefore \ S_7 \geq \frac{400\mu A}{8\text{x}10^{-6}(0.25)^2} \Rightarrow \boxed{W_7 = 800\mu m}$$

10.) Now to achieve the proper currents from the current source I gives,

$$S_9 = S_{10} = \frac{S_7}{10} = 80 \rightarrow \boxed{W_9 = W_{10} = 80\mu m}$$

and

$S_{11} = S_{12} = \frac{1.5\cdot S_7}{10} = 120 \rightarrow W_{11} = W_{12} = 120\mu m$. We saw in step 5 that W_{11} and W_{12} had to be greater than 120μm to satisfy $V_{ic}(max)$. $\therefore$ $\boxed{W_{11}=W_{12}=120\mu m}$

11.) $P_{diss} = 15I\cdot 1.5V = 300\mu A\cdot 1.5V = 450\mu W$

C_c	I	W1=W2	W3=W4	W5=W8	W6	W7	W9=W10	W11=W12	P_{diss}
2pF	20μA	33μm	7μm	202μm	165μm	800μm	80μm	120μm	450μW

Problem 6.3-16

A CMOS circuit used as an output buffer for an OTA is shown. Find the value of the small signal output resistance, R_{out}, and from this value estimate the -3dB bandwidth if a 50pF capacitor is attached to the output. What is the maximum and minimum output voltage if a 1kΩ resistor is attached to the output? What is the quiescent power dissipation of this circuit? Use the following model parameters: K_N'=24µA/V^2, K_P' = 8µA/V^2, V_{TN} = - V_{TP} = 0.75V, λ_N = 0.01V^{-1} and λ_P = 0.02V^{-1}.

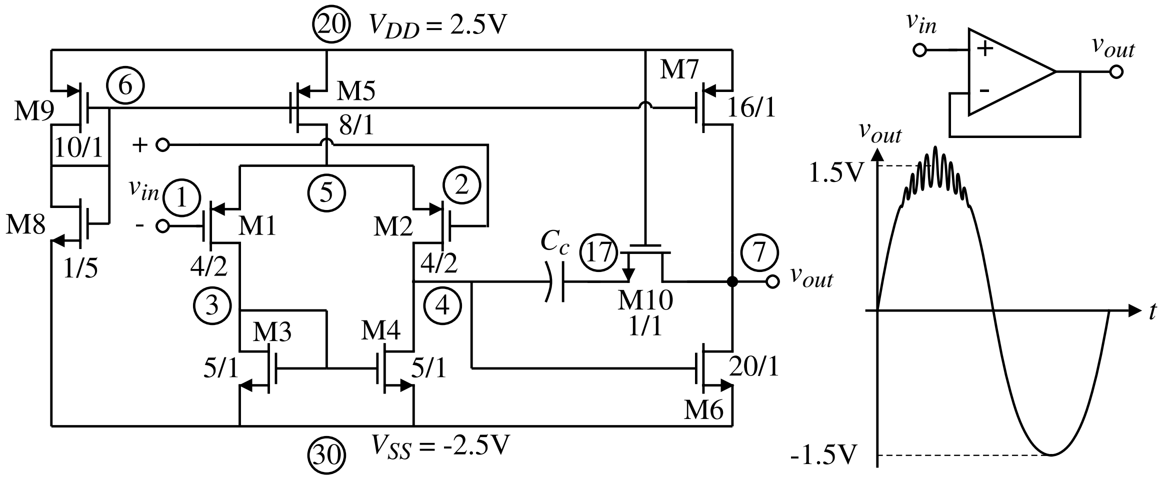


Figure P6.3-16

Solution

Considering the Miller compensation path, the value of the nulling resistor implemented by M_{10} is given by

$$R_Z = \frac{1}{K_N'(W/L)_{10}(V_{DD} - V_{S10} - V_{T10})} \quad (1)$$

The zero created at the output is given by

$$z_1 = \frac{-1}{C_C(R_Z - 1/g_{m6})} \quad (2)$$

a.) When the output swings high, the voltage at the source of M_{10} goes low assuming the compensation capacitor tends to get short-circuited. Thus, $(V_{DD} - V_{S10} - V_{T10})$ increases causing a decrease in the value of R_Z. Also, as the voltage at the gate of M_6 goes down, the current in M_6 decreases causing a decrease in value of g_{m6}. Referring to Equation (2), a decrease in both R_Z and g_{m6} would tend to place the zero in the right half plane and it would degrade the phase margin causing the op amp to oscillate.

b.) When the output swings low, the voltage at the gate of M_6 and the source of M_{10} goes up. This decreases $(V_{DD} - V_{S10} - V_{T10})$ causing an increase in R_Z. Also, as the voltage at the gate of M_6 increases, the current through M_6 increases causing and increase in g_{m6}. Thus, from Equation (2), an increase in R_Z and g_{m6} would create a LHP zero which would make the op amp more stable.

Problem 6.4-01

Sketch the asymptotic frequency response of PSRR+ and PSRR- of the two-stage op amp designed in Example 6.3-1.

Solution

Referring to Example 6.3-1, for the positive PSRR, the poles and zeros are

$$p_1 = \frac{(GB)g_{ds6}}{A_v(0)G_{II}} = 361 \text{ Hz.}$$

$$z_1 = GB = 5 \text{ MHz.}$$

$$z_2 = p_2 = 15 \text{ MHz.}$$

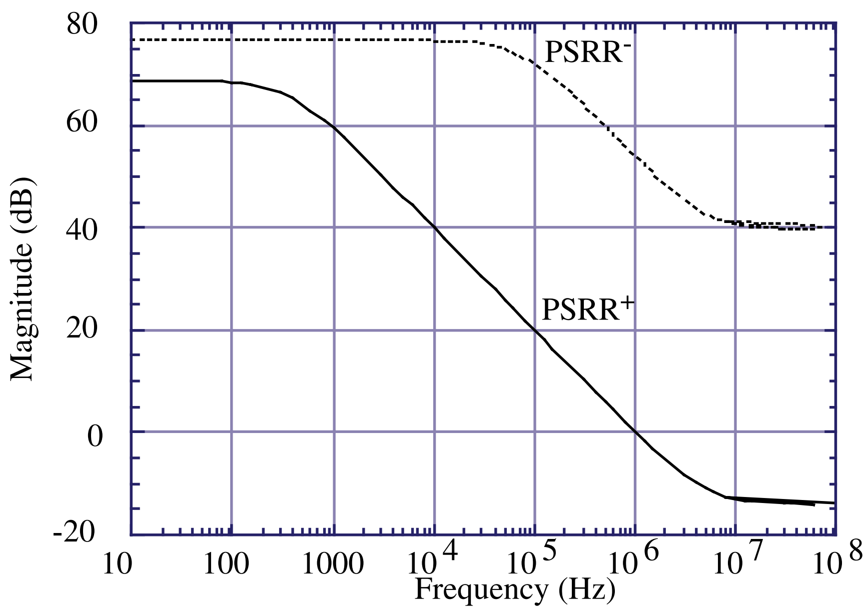
For the negative PSRR, the poles and zeros are

$$p_1 = \frac{(GB)G_I}{g_{m1}} = 71.6 \text{ KHz.}$$

$$z_1 = GB = 5 \text{ MHz.}$$

$$z_2 = p_2 = 15 \text{ MHz.}$$

The magnitude of the positive and negative PSRR is shown below.



Problem 6.4-02

Find the low frequency PSRR and all roots of the positive and negative power supply rejection ratio performance for the two-stage op amp of Fig. P6.3-9.

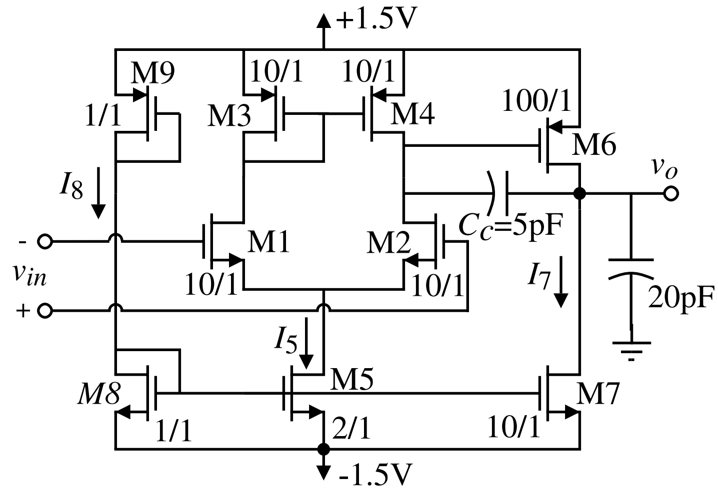


Figure P6.3-10

Solution

Referring to the figure

$$V_{DD} - V_{SS} = V_{T8} + V_{T9} + \sqrt{\frac{2I_8}{K_N'(W/L)_8}} + \sqrt{\frac{2I_8}{K_P'(W/L)_9}}$$

or, $I_8 = 60\ \mu A$

Now,

$g_{m1} = 363.3\ \mu S$, $g_{ds2} = 2.4\ \mu S$, $g_{ds4} = 3\ \mu S$, $g_{m6} = 774.6\ \mu S$, $g_{ds6} = 30\ \mu S$

and $g_{ds7} = 24\ \mu S$

$\therefore$ $A_{v1} = 67.3$ and $A_{v2} = 14.3$

For the positive PSRR, the low frequency PSRR is

$$PSRR^+ = \frac{A_v(0)G_{II}}{g_{ds6}} = 1737$$

and poles and zeros are

$p_1 = \dfrac{(GB)g_{ds6}}{A_v(0)G_{II}} = 6.66$ KHz, $z_1 = GB = 11.6$ MHz. and $z_2 = p_2 = 6.2$ MHz.

For the negative PSRR, the low frequency PSRR is given by

$$PSRR^- = \frac{A_v(0)G_{II}}{g_{ds7}} = 2171$$

and the poles and zeros are

$p_1 = \dfrac{(GB)G_I}{g_{m1}} = 172.4$ KHz, $z_1 = GB = 11.6$ MHz and $z_2 = p_2 = 6.2$ MHz.

Problem 6.4-03

Repeat the analysis of the positive PSRR of Fig. 6.4-2 if the Miller compensation circuitry of Fig. 6.2-15(a) is used. Compare the low frequency magnitude and roots with those of the positive PSRR for Fig. 6.4-2.

Solution

TBD

Problem 6.4-04

In Fig. P6.4-4, find v_{out}/v_{ground} and identify the low-frequency gain and the roots. This represents the case where a noisy ac ground can influence the noise performance of the two-stage op amp.

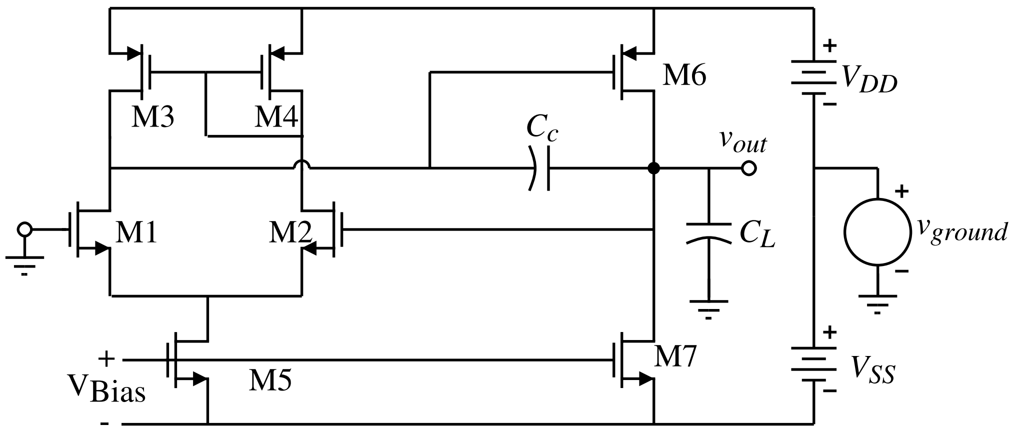


Figure P6.4-4

Solution

Let, $v_{dd} = -v_{ss} = \dfrac{v_{ground}}{2}$ and, v_5 be the small-signal ac voltage at the drain of M_5.

Applying nodal analysis

$$\left(g_{m2}(v_{out} - v_5) + g_{m5}v_{ss} + g_{ds2}(v_{dd} - v_5) - g_{m1}v_5 + g_{ds1}(v_1 - v_5)\right)r_{ds5} = v_5$$

or, $$v_5 = \frac{(g_{m2}v_{out} + g_{ds2}v_{dd} + g_{m5}v_{ss})}{(g_{m1} + g_{m2})} \qquad (1)$$

Now,

$$\left(g_{m2}(v_{out} - v_5) + g_{ds2}(v_{dd} - v_5) + g_{m1}v_5 + g_{ds3}(v_{dd} - v_1)\right) = \left(g_{ds1}(v_1 - v_5) + sC_C(v_1 - v_{out})\right)$$

or, $$(g_{m2} + sC_C)v_{out} + (g_{ds2} + g_{ds3})v_{dd} = (g_{ds1} + g_{ds3} + sC_C)v_1 \qquad (2)$$

Also,

$$\left(sC_C(v_1 - v_{out}) + g_{m7}v_{ss}\right) = \left(g_{ds6}(v_{out} - v_{dd}) + g_{ds7}(v_{out} - v_{ss}) + sC_Lv_{out} + g_{m6}(v_1 - v_{dd})\right)$$

Using $v_{dd} = -v_{ss}$, we get

$$(g_{m6} - g_{m7} + g_{ds6} - g_{ds7})v_{dd} = \left(g_{ds6} + g_{ds7} + s(C_C + C_L)\right)v_{out} + (g_{m6} - sC_C)v_1 (3)$$

Using Equations (2) and (3) gives the low frequency PSRR as

$$\frac{v_{out}}{v_{ground}} = \left[\frac{2g_{mI}g_{mII}}{G_I(g_{ds6} - g_{ds7} - g_{m7})}\right]^{-1}$$

The zero is

$$z_1 \cong -\frac{G_I(g_{ds6} - g_{ds7} - g_{m7})}{C_C(G_I + g_{m6} - g_{m7} + g_{ds6} - g_{ds7})}$$

The two poles are same as given by the zeros of Equation (6.4-14) in the text.

Problem 6.4-05

Repeat the analysis of Fig. 6.4-2 and Fig. 6.4-4 for the p-channel input, two-stage op amp shown in Fig. P6.4-5.

Solution

TBD

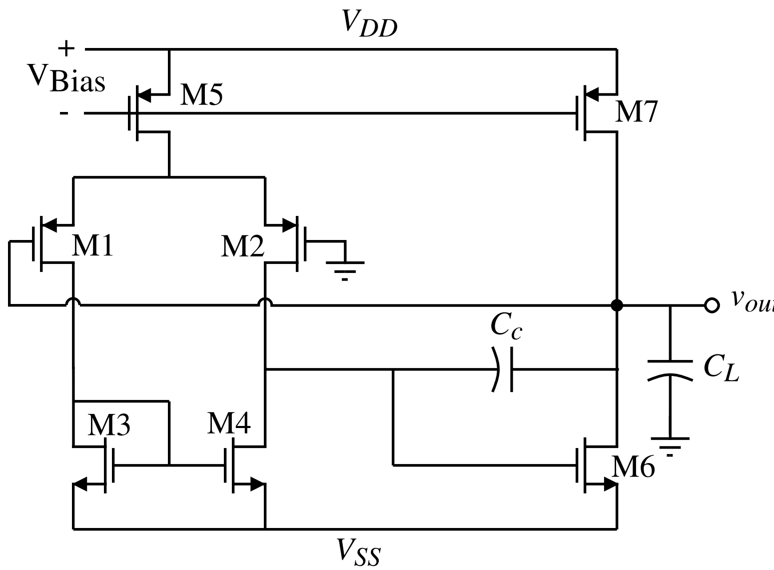


Figure P6.4-5

Problem 6.5-01

Assume that in Fig. 6.5-1(a) that the currents in M1 and M2 are 50µA and the W/L values of the NMOS transistors are 10 and of the PMOS transistors are 5. What is the value of V_{Bias} that will cause the drain-source voltage of M1 and M2 to be equal to V_{ds}(sat)? Design the value of R. to keep the source-drain voltage of M3 and M4 equal to V_{sd}(sat). Find an expression for the small-signal voltage gain of v_{o1}/v_{in} for Fig. 6.5-1(a).

Solution

$$V_{BIAS} = V_{T,MC1} + V_{dsat,MC1} + V_{dsat,M1}$$

or, $$V_{BIAS} = V_{T,MC1} + \sqrt{\frac{2I_1}{K_N'\left(\frac{W}{L}\right)_{C1}}} + \sqrt{\frac{2I_1}{K_N'\left(\frac{W}{L}\right)_1}}$$

Ignoring bulk effects

$$V_{BIAS} = \underline{\underline{1.3\text{V}}}$$

Now,

$$V_{G,C3} = V_{T,C3} + V_{dsat,C3} + V_{dsat3}$$

$$V_{G3} = V_{T3} + V_{dsat3}$$

And, $$IR = V_{G,C3} - V_{G3} = V_{dsat,C3}$$

or, $$R = \sqrt{\frac{2}{IK_P'\left(\frac{W}{L}\right)_{C3}}} = \underline{\underline{12.65\text{k}\Omega}}$$

The output impedance is given by

$$R_{out} = [g_{m,C4}r_{ds,C4}r_{ds4}] \| [g_{m,C2}r_{ds,C2}r_{ds2}]$$

$$R_{out} = 19.38 \quad M\Omega$$

The small-signal voltage gain is given by

$$A_v = -g_{m,C2}R_{out} = \underline{\underline{-6248 \text{ V/V}}}$$

Problem 6.5-02

If the W/L values of M1, M2, MC1 and MC2 in Fig. 6.5-1(b) are 10 and the currents in M1 and M2 are 50μA, find the W/L values of MB1 through MB5 that will cause the drain-source voltage of M1 and M2 to be equal to V_{ds}(sat). Assume that MB3 = MB4 and the current through MB5 is 5μA. What will be the current flowing through M5?

Solution

Let, $I_{B5} = 5 \ \mu A$

$$V_{T,B5} + V_{dsat,B5} = V_{T,C1} + V_{dsat,C1} + V_{dsat1}$$

or, $$V_{T,B5} + \sqrt{\frac{2I_{B5}}{K'_N (W/L)_{B5}}} = V_{T,C1} + \sqrt{\frac{2I_1}{K'_N (W/L)_{C1}}} + \sqrt{\frac{2I_1}{K'_N (W/L)_1}}$$

Ignoring bulk effects, and assuming $I_1 = 50 \ \mu A$

$$\boxed{\left(\frac{W}{L}\right)_{B5} = \frac{1}{4}}$$

The aspect ratios of the transistors MB1 through MB4 can be chosen (assumed) to be 1.

The total current through M5 is 110 μA.

Problem 6.5-03

In Fig. 6.5-1(a), find the small-signal impedance to ac ground looking into the sources of MC2 and MC4 assuming there is no capacitance attached to the output. Assume the capacitance to ground at these nodes is 0.2pF. What is the value of the poles at the sources of MC3 and MC4? Repeat if a capacitor of 10pF is attached to the output.

Solution

Let, C_1 and C_L be the capacitances at the source of MC2 (and MC4) and the output respectively. The impedance looking between the drain of M4 and Vdd (ac ground), Z_4, be

$$Z_4 = \frac{1}{(g_{ds4} + sC_1)}$$

The impedance looking between the drain of MC4 and Vdd (ac ground), Z_{C4}, be

$$Z_{C4} = \frac{1}{\left[\frac{(g_{ds4} + sC_1)g_{ds,C4}}{g_{m,C4}} + sC_L\right]}$$

Thus, the impedance looking between the source of MC2 and Vdd (ac ground), $Z_{S,C2}$, can be expressed as

$$Z_{S,C2} = \left[\frac{r_{ds,C2} + Z_{C4}}{1 + g_{m,C2}r_{ds,C2}}\right] \| \left[\frac{1}{sC_1}\right]$$

or, $$Z_{S,C2} \cong \left[\frac{Z_{C4}}{g_{m,C2}r_{ds,C2}}\right] \| \left[\frac{1}{sC_1}\right]$$

Problem 6.5-03 - Continued

or, $$Z_{S,C2} = \left[\frac{1}{\dfrac{g_{m,C2}(g_{ds4}+sC_1)g_{ds,C4}}{g_{m,C4}g_{ds,C2}} + s\dfrac{g_{m,C2}}{g_{ds,C2}}C_L + sC_1} \right]$$

or, $$Z_{S,C2} = \left[\frac{1}{\dfrac{g_{m,C2}g_{ds4}g_{ds,C4}}{g_{m,C4}g_{ds,C2}} + s\left(\dfrac{g_{m,C2}}{g_{ds,C2}}C_L + \left(1+\dfrac{g_{m,C2}g_{ds,C4}}{g_{m,C4}g_{ds,C2}}\right)C_1\right)} \right]$$

Similarly, the impedance looking from the source of MC4 to ac ground, $Z_{S,C4}$, can be expressed as

$$Z_{S,C4} = \left[\frac{1}{\dfrac{g_{m,C4}g_{ds2}g_{ds,C2}}{g_{m,C2}g_{ds,C4}} + s\left(\dfrac{g_{m,C4}}{g_{ds,C4}}C_L + \left(1+\dfrac{g_{m,C4}g_{ds,C2}}{g_{m,C2}g_{ds,C4}}\right)C_1\right)} \right]$$

Referring to problem 6.5-3, we have

$$g_{m,C4} = g_{m4} = 158.1 \ \mu S$$

$$g_{m,C2} = g_{m2} = 331.7 \ \mu S$$

$$g_{ds,C4} = g_{ds4} = 2.5 \ \mu S$$

$$g_{ds,C2} = g_{ds2} = 2 \ \mu S$$

When $C_L = 0$

$$Z_{S,C2} = \left[\frac{1}{6.6\times10^{-6} + s(0.72\times10^{-12})} \right] \ \Omega$$

$$Z_{S,C4} = \left[\frac{1}{0.76\times10^{-6} + s(0.27\times10^{-12})} \right] \ \Omega$$

When $C_L = 10$ pF

$$Z_{S,C2} = \left[\frac{1}{6.6\times10^{-6} + s(1659\times10^{-12})} \right] \ \Omega$$

$$Z_{S,C4} = \left[\frac{1}{0.76\times10^{-6} + s(632.7\times10^{-12})} \right] \ \Omega$$

Problem 6.5-04

Repeat Example 6.5-1 to find new values of W_1 and W_2 which will give a voltage gain of 10,000.

Solution

From Example 6.5-1

$$R_{out} = 25 \quad M\Omega$$

Thus, for $A_v = 10{,}000$

$$g_{m1} = \frac{A_v}{R_{out}} = 400 \quad \mu S$$

or, $$\boxed{\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m1}^2}{2K'_N I_1} = \frac{14.5}{1}}$$

Problem 6.5-05

Find the differential-voltage gain of Fig. 6.5-1(a) where the output is taken at the drains of MC2 and MC4, $W_1/L_1 = W_2/L_2 = 10$ μm/1 μm, $W_{C1}/L_{C1} = W_{C2}/L_{C2} = W_{C3}/L_{C3} = W_{C4}/L_{C4} = 1$ μm/1 μm, $W_3/L_3 = W_4/L_4 = 1$ μm/1 μm, and $I_5 = 100$ μA. Use the model parameters of Table 3.1-2 . Ignore the bulk effects.

Solution

$$I_5 = 100 \quad \mu A$$

$$g_{m1} = g_{m2} = 331.67 \quad \mu S$$

$$g_{m,C2} = 104.8 \quad \mu S$$

$$g_{m,C4} = 70.7 \quad \mu S$$

$$r_{ds,C4} = r_{ds4} = 400 \quad K\Omega$$

$$r_{ds,C2} = r_{ds2} = 500 \quad K\Omega$$

The output impedance is given by

$$R_{out} = [g_{m,C2} r_{ds,C2} r_{ds2}] \| [g_{m,C4} r_{ds,C4} r_{ds4}]$$

or, $$R_{out} = [26.2M] \| [11.3M] = 7.9M\Omega$$

So, $$\boxed{A_v = -g_{m2} R_{out} = -2620 V/V}$$

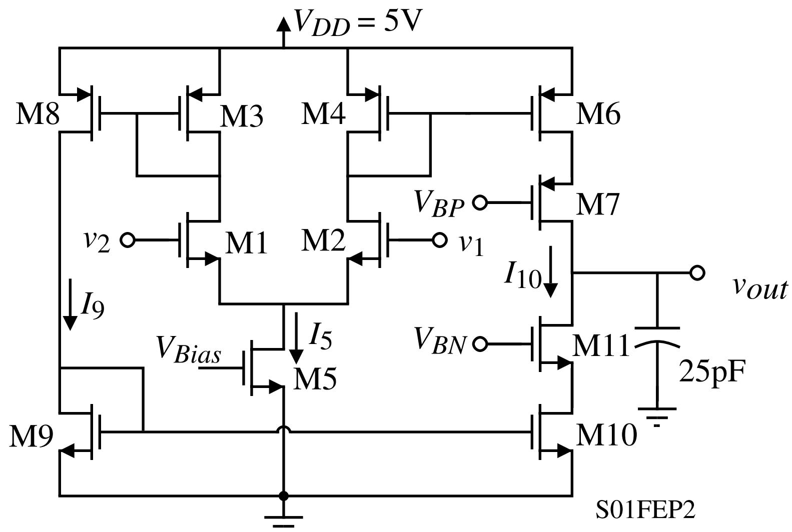
Problem 6.5-06

A CMOS op amp that uses a 5V power supply is shown. All transistor lengths are 1μm and operate in the saturation region. Design all of the W values of every transistor of this op amp to meet the following specifications. Use the following model parameters: K_N'=110μA/V^2, K_P'=50μA/V^2, V_{TN}=0.7V, V_{TP}=-0.7V, λ_N=0.04V^{-1} and λ_P=0.05V^{-1}.

Slew rate = ±10V/μs	V_{out}(max) = 4V	V_{out}(min) = 1V
V_{ic}(min) = 1.5V	V_{ic}(max) = 4V	GB = 10MHz

Your design should meet or exceed these specifications. Ignore bulk effects and summarize your W values to the nearest micron, the bias current, I_5(μA), the power dissipation, the differential voltage gain, A_{vd}, and V_{BP} and V_{BN} in the following table. Assume that V_{bias} is whatever value necessary to give I_5.

W1=W2	W3=W4=W6 =W7=W8	W9=W10 =W11	W5	I_5(μA)	A_{vd}	V_{BP}	V_{BN}	P_{diss}
89.75	40	18.2	13.75	250μA	17,338V/V	3.3V	1.7V	2.5mW



Solution

Since $W3 = W4 = W6 = W7 = W8$ and $W9 = W10 = W11$, then I_5 is the current available to charge the 25pF load capacitor. Therefore,

$$I_5 = C\frac{dv_{OUT}}{dt} = 25\text{pF}(10\text{V/μs}) = \underline{\underline{250\mu\text{A}}}$$

Note that normally, $I_{10} = I_9 = 125$μA. However, for the following calculations we will use I_6 or I_{10} equal to 250μA for the following v_{OUT}(max/min) calculations.

$$v_{OUT}(\max) = 4\text{V} \quad\Rightarrow\quad 0.5 = \sqrt{\frac{2I_5}{K_P'(W6/L6)}} = \sqrt{\frac{2I_5}{K_P'(W6/L6)}}$$

$\underline{\underline{W6 = W7 = 40 = W3 = W4 = W8}}$

Problem 6.5-07

Verify Eqs. (6.5-4) through (6.5-8) of Sec. 6.5 for the two-stage op amp of Fig. 6.5-3 having a cascode second stage. If the second stage bias current is 50 μA and $W_6/L_6 = W_{C6}/L_{C6} = W_{C7}/L_{C7} = W_7/L_7 = 1\ \mu\text{m}/1\ \mu\text{m}$, what is the output resistance of this amplifier using the parameters of Table 3.1-2?

Solution

From intuitive analysis, it can be shown that

$$A_{v1} = -\frac{g_{m1}}{(g_{ds2} + g_{ds4})}$$

For the second gain stage, the output resistance of the cascode stage can be given by

$$R_{II} = [g_{m,C6} r_{ds,C6} r_{ds6}] \,||\, [g_{m,C7} r_{ds,C7} r_{ds7}]$$

or, $A_{v2} = -g_{m6} R_{II}$

Thus, $A_v = A_{v1} A_{v2} = \dfrac{g_{m1} g_{m6}}{(g_{ds2} + g_{ds4})\{[g_{m,C6} r_{ds,C6} r_{ds6}] \,||\, [g_{m,C7} r_{ds,C7} r_{ds7}]\}}$

For, $I_7 = 50\ \mu A$

$$\boxed{R_{II} = [11.3M] \,||\, [26.2M] = 7.9\text{M}\Omega}$$

Problem 6.5-08

Verify Eqs. (6.5-9) through (6.5-11) of Sec. 6.5 assuming that M3 = M4 = M6 = M8 and M9 = M10 = M11 = M12 and give an expression for the overall differential-voltage gain of Fig. 6.5-4.

Solution

Solving the circuit intuitively

The effective transconductance of the first stage

$$g_{mI} = \frac{g_{m1}}{2}$$

The effective conductance of the first stage

$$g_I = g_{m3}$$

The effective transconductance of the second stage

$$g_{mII} = \left(g_{m6} + g_{m11}\right)$$

The effective conductance of the second stage

$$g_{II} = \frac{g_{ds6}g_{ds7}}{g_{m7}} + \frac{g_{ds11}g_{ds12}}{g_{m12}}$$

Now,

$$A_{v1} = -\frac{g_{m1}}{2g_{m3}}$$

$$A_{v2} = -\frac{\left(g_{m6} + g_{m11}\right)}{\left[\dfrac{g_{ds6}g_{ds7}}{g_{m7}} + \dfrac{g_{ds11}g_{ds12}}{g_{m12}}\right]}$$

or, $$A_v = \frac{g_{m1}\left(g_{m6} + g_{m11}\right)}{2g_{m3}\left[\dfrac{g_{ds6}g_{ds7}}{g_{m7}} + \dfrac{g_{ds11}g_{ds12}}{g_{m12}}\right]}$$

Problem 6.5-09

An internally-compensated, cascode op amp is shown in Fig. P6.5.-9. (a) Derive an expression for the common-mode input range. (b) Find W_1/L_1, W_2/L_2, W_3/L_3, and W_4/L_4 when I_{BIAS} is 80 μA and the input CMR is –3.5 V to 3.5 V. Use K'_N = 25 μA/V^2, K'_p = 11 μA/V^2 and $|V_T|$ = 0.8 to 1.0 V.

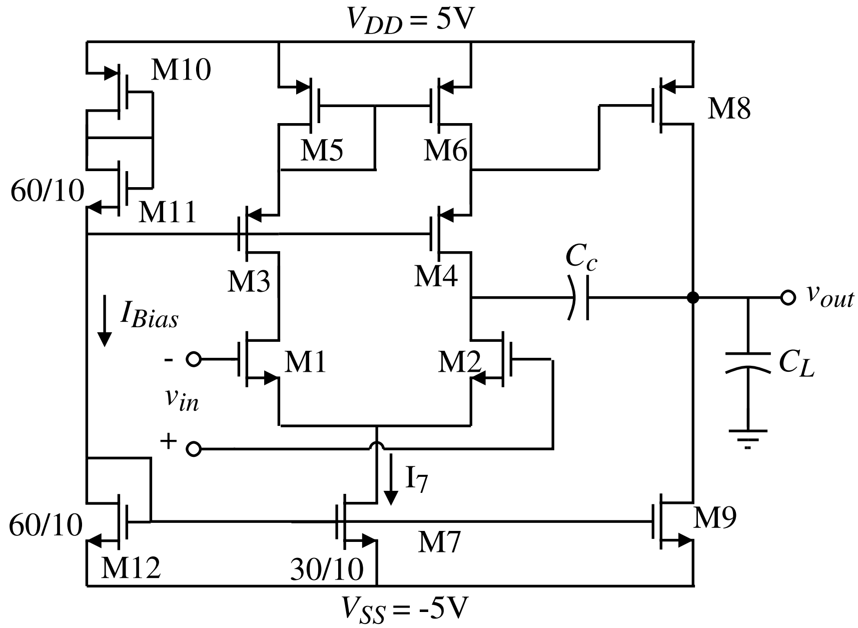


Figure P6.5-9

Solution

The minimum input common-mode voltage can be given by

$$V_{in}(\min) = V_{SS} + V_{T1}(\max) - V_{dsat1} - V_{dsat7}$$

$$V_{in}(\min) = V_{SS} + V_{T1}(\max) - \sqrt{\frac{I_7}{K_N'(W/L)_1}} - \sqrt{\frac{2I_7}{K_N'(W/L)_7}} \quad (1)$$

The maximum input common-mode voltage can be given by

$$V_{in}(\max) = V_{DD} + V_{T1}(\min) - |V_{T5}(\max)| - V_{dsat3} - V_{dsat5}$$

$$V_{in}(\max) = V_{DD} + V_{T1}(\min) - |V_{T5}(\max)| - \sqrt{\frac{I_7}{K_P'(W/L)_3}} - \sqrt{\frac{I_7}{K_P'(W/L)_5}} \quad (2)$$

The input common-mode range is given by

$$\boxed{ICMR = V_{in}(\max) - V_{in}(\min)}$$

which can be derived from Equations (1) and (2).

Given $I_7 = 40\ \ \mu A$, $V_{in}(\min) = -2.5$ V and $(W/L)_7 = 3$, from Equation (1)

$$\boxed{\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{64\ \mu m}{10\ \mu m}}$$

Also, for $I_7 = 40\ \ \mu A$, $V_{in}(\max) = 3.5$ V and assuming $(W/L)_5 = 6$, from Equation (2)

$$\boxed{\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{135\ \mu m}{10\ \mu m}}$$

Problem 6.5-10

Develop an expression for the small-signal differential-voltage gain and output resistance of the cascode op amp of Fig. P6.5-9.

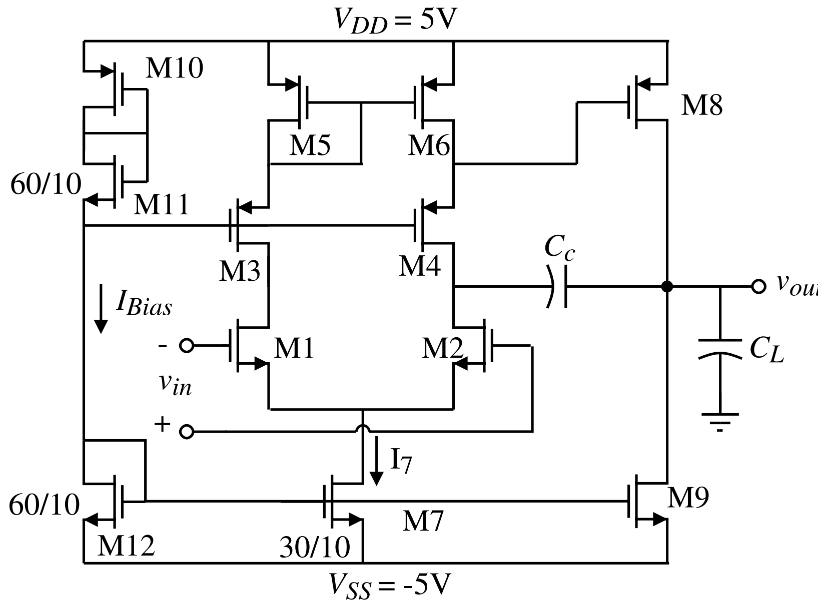


Figure P6.5-9

Solution

The output resistance of the first gain stage is

$$R_{out1} \cong r_{ds6}$$

So,

$$A_{v1} = -g_{m1}R_{out1} = -g_{m1}r_{ds6}$$

The output resistance of the second gain stage is

$$R_{out2} = \frac{1}{(g_{ds8} + g_{ds9})}$$

So,

$$A_{v2} = -g_{m8}R_{out2} = -\frac{g_{m8}}{(g_{ds8} + g_{ds9})}$$

The overall small-signal gain is

$$A_v = A_{v1}A_{v2}$$

or,
$$A_v = \frac{g_{m1}g_{m8}}{g_{ds6}(g_{ds8} + g_{ds9})}$$

or,
$$\boxed{A_v = \sqrt{\frac{8K'_N K'_P (W/L)_1 (W/L)_8}{I_7 I_9 (\lambda_P + \lambda_N)^2 \lambda_P^2}}}$$

The small-signal output resistance is given by

$$\boxed{R_{out} = R_{out2} = \frac{1}{(g_{ds8} + g_{ds9})}}$$

Problem 6.5-11

Verify the upper input common mode range of Ex. 6.5-2, step 6.) for the actual value of $S_3 = S_4$ of 40.

Solution

The maximum input common-mode voltage is given by

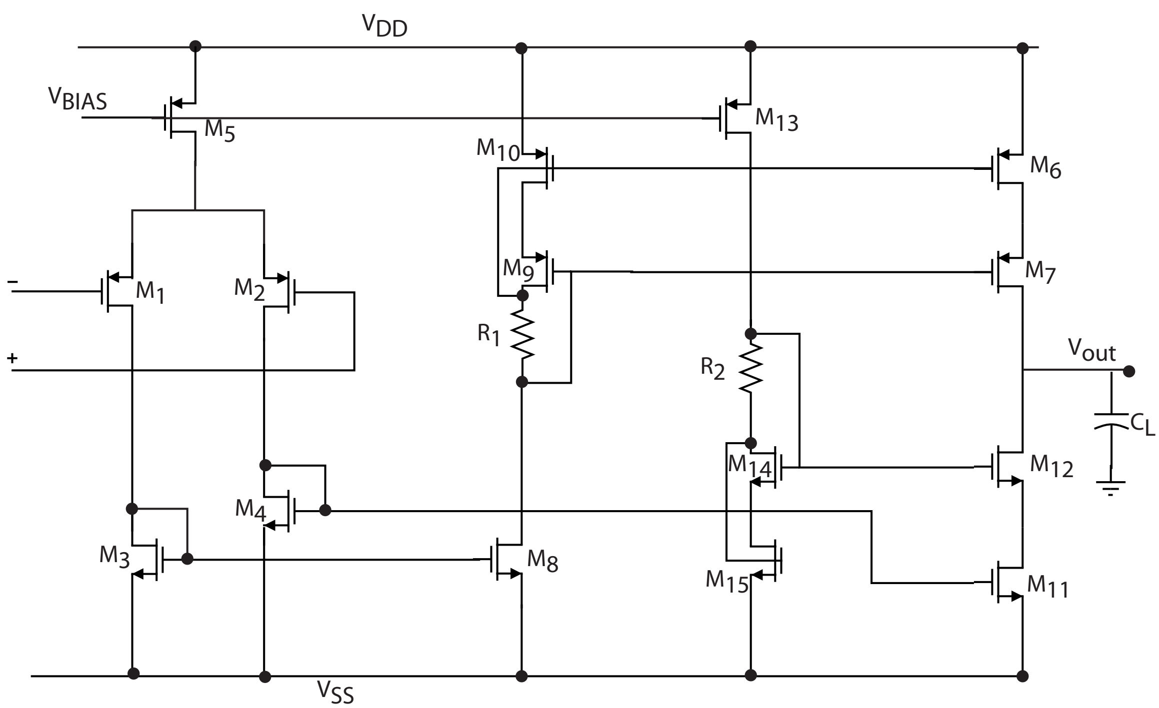
$$V_{in}(\max) = V_{DD} + V_{T1}(\min) - |V_{T3}(\max)| - V_{dsat3}$$

or, $$V_{in}(\max) = V_{DD} + V_{T1}(\min) - |V_{T3}(\max)| - \sqrt{\frac{2I_3}{K'_P(W/L)_3}}$$

or, $\boxed{V_{in}(\max) = 1.98V}$

Problem 6.5-12

Repeat Example 6.5-2 if the differential input pair are PMOS transistors (i.e. all NMOS transistors become PMOS and all PMOS transistors become NMOS and the power supplies are reversed).



Solution

To satisfy the slew rate

$$I_6 = I_7 = I_{12} = I_{11} = 250\ \mu A \qquad \text{and let } I_5 = 100\ \mu A$$

The maximum output voltage is 1.5 V

$$V_{dsat6} = V_{dsat7} = 0.5\ \text{V} \quad \rightarrow \quad \boxed{S_6 = S_7 = S_9 = S_{10} = 40}$$

Similarly, considering the minimum output voltage as –1.5 V

Problem 6.5-12 - Continued

$$V_{dsat11} = V_{dsat12} = 0.5 \text{ V} \quad \rightarrow \quad \boxed{S_{11} = S_{12} = S_{14} = S_{15} = 18.2}$$

The value of R1 and R2 can be calculated as

$$R_1 = \frac{V_{dsat7}}{I_8} = 2 \ K\Omega \qquad \text{and,} \qquad R_2 = \frac{V_{dsat12}}{I_{15}} = 2 \ K\Omega$$

Now,

$$g_{m1} = \frac{2g_{m3}A_v}{kR_{II}(g_{m6}+g_{m8})} \qquad \text{and,} \qquad k = \frac{S_6}{S_4} = 2.5 \ \text{ and } R_{II} \cong 11 \ M\Omega$$

Thus, $g_{m1} = 107.9 \ \mu S$ Also, $g_{m1} = \dfrac{2g_{m3}GB}{k(g_{m6}+g_{m8})} = 149 \ \mu S$

So, let us choose $g_{m1} = 149 \ \mu S$. $\rightarrow$ $\boxed{S_1 = S_2 = 4.4}$

But for this value of $S_1 = S_2 = 4.4$, from the expression of maximum input common-mode voltage, we will get $V_{dsat5} = 0.025$ V which is too small. So let us choose

$$S_1 = S_2 = 20$$

This, from the expression of $V_{in}(\text{max})$, will give $S_5 = 27.7$

Or, $\boxed{S_{13} = 1.25S_5 = 34.6}$ and, $\boxed{S_8 = 2.5S_3 = 40}$

Problem 6.5-13

A CMOS op amp that uses a 5V power supply is shown. All transistor lengths are 1μm and operate in the saturation region. Design all of the W values of every transistor of this op amp to meet the following specifications: Slew rate = ±10V/μs, $V_{out}(max)$ = 4V, $V_{out}(min)$ = 1V, $V_{ic}(min)$ = 1.5V, $V_{ic}(max)$ = 4V and GB = 10MHz.

Your design should meet or exceed these specifications. Ignore bulk effects and summarize your W values to the nearest micron, the bias current, I_5(μA), the power dissipation, the differential voltage gain, A_{vd}, and V_{BP} and V_{BN} in the table shown.

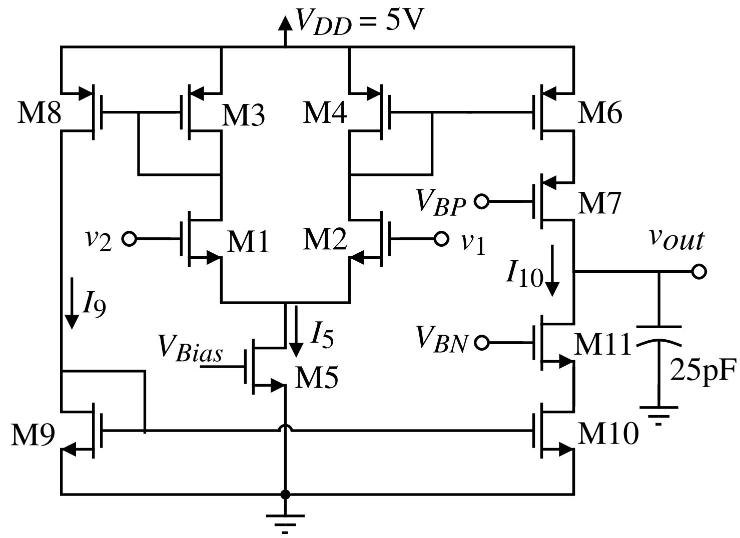


Figure P6.5-13

Solution

1.) $I_5 = C_L \cdot SR$ = 250μA

2.) $g_{m1} = GB \cdot C_L$ = $20\pi \text{x} 10^6 \cdot 25\text{pF}$ = 1,570.8μS $\Rightarrow \dfrac{W_1}{L_1} = \dfrac{(1.570\text{x}10^{-3})^2}{2 \cdot 110 \cdot 125\text{x}10^{-6}} = 90$

3.) $W3=W4=W6=W7=W8 = \dfrac{2I_D}{K'(V_{DS}(\text{sat}))^2} = \dfrac{2 \cdot 250}{50 \cdot 0.25} = 40$ (assumed I_D of 250μA worst case)

4.) $W9=W10=W11 = \dfrac{2I_D}{K'(V_{DS}(\text{sat}))^2} = \dfrac{2 \cdot 250}{110 \cdot 0.25} = 18$ (assumed I_D of 250μA worst case)

5.) $V_{icm}(\text{min}) = V_{DS5}(\text{sat}) + V_{GS1} \rightarrow V_{DS5}(\text{sat}) = 1.5 - (0.159+0.7) = 0.6411\text{V}$

$$\therefore W5 = \frac{2I_D}{K'(V_{DS}(\text{sat}))^2} = \frac{2 \cdot 250}{110 \cdot 0.6411^2} = 11$$

6.) $A_{vd} = g_{m1}R_{out}$ $\quad g_{mN}$ = 704μS, r_{dsN} = 0.2MΩ, g_{mP} = 707μS, r_{dsN} = 0.16MΩ

$$R_{out} \approx g_{mN} \cdot r_{dsN}^2 \| g_{mP} \cdot r_{dsP}^2 = 28.14\text{M}\Omega \| 18.1\text{M}\Omega = 11\text{M}\Omega$$

$$\therefore \quad A_{vd} = 1.57\text{mS} \cdot 11\text{M}\Omega = 17{,}329\text{V/V}$$

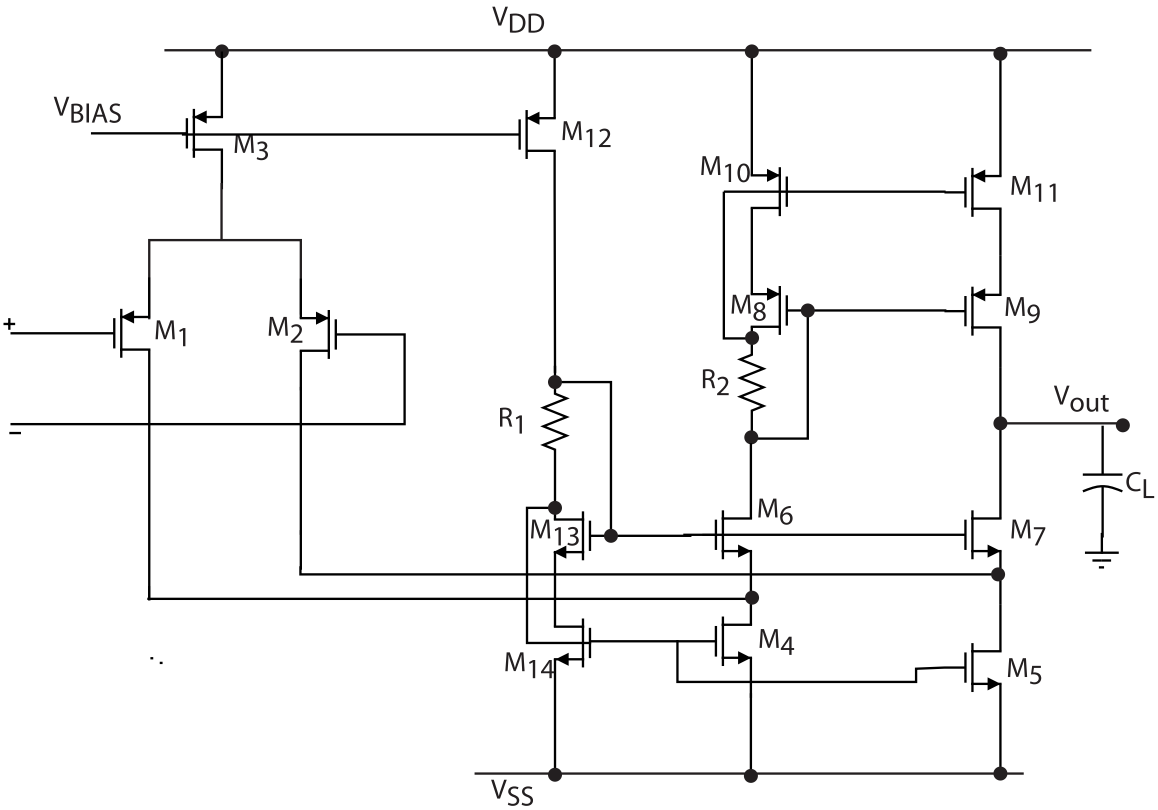
7.) $V_{BP} = 5 - V_{DSP}(\text{sat}) + V_{GSP}(\text{sat}) = 5-0.5+0.5+0.7 = 3.3\text{V}$
$V_{BN} = V_{DSP}(\text{sat}) + V_{GSP}(\text{sat}) = 0.5+0.5+0.7 = 1.7\text{V}$

8.) P_{diss} = 5(250μA + 250μA) = 2.5mW

W1=W2	W3=W4=W6 =W7=W8	W9=W10 =W11	W5	I_5(μA)	A_{vd}	V_{BP}	V_{BN}	P_{diss}
90	40	18	11	250μA	17,324V/V	3.3V	1.7V	2.5mW

Problem 6.5-14

Repeat Example 6.5-3 if the differential input pair are PMOS transistors (i.e. all NMOS transistors become PMOS and all PMOS transistors become NMOS and the power supplies are reversed).



Solution

$I_3 = 100\ \mu A$ and, $I_4 = I_5 = 125\ \mu A$

Given, $V_{out}(\max) = 2$ V $\rightarrow$ $V_{dsat9} = V_{dsat11} = 0.25$ V

Considering worst-case peak sourcing current of 125 μA

$\boxed{S_8 = S_9 = S_{10} = S_{11} = 80}$

Given, $V_{out}(\min) = -2$ V $\rightarrow$ $V_{dsat7} = V_{dsat5} = 0.25$ V

Considering worst-case peak sinking current of 125 μA

$I_5 = 125\ \mu A$ and $I_7 = 25\ \mu A$

$\boxed{S_6 = S_7 = S_{13} = 7.3}$

And, $\boxed{S_4 = S_5 = S_{14} = 36.4}$

$R_1 = \dfrac{V_{dsat7}}{I_{14}} = 2\ K\Omega$ and $R_2 = \dfrac{V_{dsat9}}{I_{10}} = 2\ K\Omega$

From gain-bandwidth

$$\boxed{S_1 = S_2 = \frac{(GB)^2 C_L^2}{K_P' I_3} = 79}$$

Problem 6.5-14 - Continued

Considering $V_{in}(\max) = 1$ V

$$V_{dsat3} = 0.43 \text{ V} \quad \rightarrow \quad \boxed{S_3 = 21.6}$$

The minimum input common-mode voltage is

$$V_{in}(\min) = V_{SS} - |V_{T1}(\min)| + V_{dsat4} = -2.8 \text{ V}$$

Finally, $\boxed{S_{12} = 1.25 S_3 = 27}$

The small-signal gain is

$$A_v = \frac{(2+k)}{(2+2k)} g_{mI} R_{II}$$

$$k = \frac{R_9 (g_{ds2} + g_{ds4})}{(g_{m7} r_{ds7})}$$

where, $R_9 = 55 \; M\Omega$

$g_{mI} = 628.3 \; \mu S$, $g_{m7} = 347 \; \mu S$, $g_{ds7} = 3 \; \mu S$, $g_{ds4} = 5 \; \mu S$, $g_{ds2} = 2.5 \; \mu S$

So, $k = 3.96$

$R_{II} = 12 \; M\Omega$

or, $A_v = 4364$ V/V

Problem 6.5-15

This problem deals with the op amp shown in Fig. P6.5-15. All device lengths are 1μm, the slew rate is ±10V/μs, the GB is 10MHz, the maximum output voltage is +2V, the minimum output voltage is -2V, and the input common mode range is from -1V to +2V. Design all W values of all transistors in this op amp. Your design must meet or exceed the specifications. When calculating the maximum or minimum output voltages, divide the voltage drop across series transistors equally. Ignore bulk effects in this problem. When you have completed your design, find the value of the small signal differential voltage gain, $A_{vd} = v_{out}/v_{id}$, where $v_{id} = v_1 - v_2$ and the small signal output resistance, R_{out}.

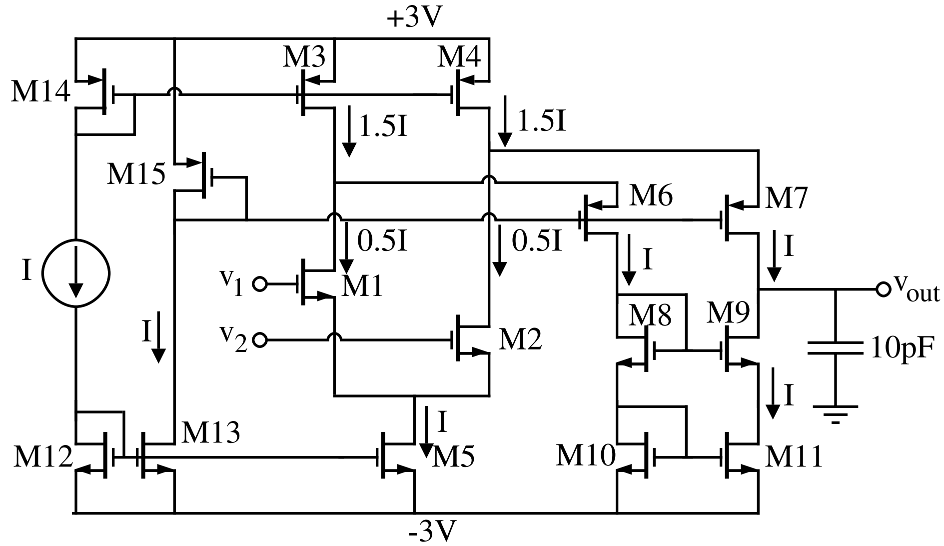


Figure P6.5-15

Solution

1.) The slew rate will specify *I*. ∴ $I = C\cdot SR = 10^{-11}\cdot 10^{7} = 10^{-4} = 100\mu\text{A}$.

2.) Use *GB* to define W_1 and W_2.

$$GB = \frac{g_{m1}}{C} \quad\rightarrow\quad g_{m1} = GB\cdot C = 2\pi\text{x}10^{7}\cdot 10^{-11} = 628\mu\text{S}$$

$$\therefore\ W_1 = \frac{g_{m1}{}^2}{2K_N(0.5I)} = \frac{(628)^2}{2\cdot 110\cdot 50} = 35.85 \quad\Rightarrow\quad \underline{\underline{W_1 = W_2 = 36\mu\text{m}}}$$

3.) Design W_{15} to give V_T+2V_{ON} bias for M6 and M7. V_{ON} = 0.5V will meet the desired maximum output voltage specification. Therefore,

$$V_{SG15} = V_{ON15} + |V_T| = 2(0.5\text{V}) + |V_T| \quad\rightarrow V_{ON15} = 1\text{V} = \sqrt{\frac{2I}{K_P W_{15}}}$$

$$\therefore\ W_{15} = \frac{2I}{K_P V_{ON15}{}^2} = \frac{2\cdot 100}{50\cdot 1^2} = 4\mu\text{m} \quad\Rightarrow\quad \underline{\underline{W_{15} = 4\mu\text{m}}}$$

4.) Design W_3, W_4, W_6 and W_7 to have a saturation voltage of 0.5V with 1.5I current.

$$W_3 = W_4 = W_6 = W_7 = \frac{2(1.5I)}{K_P V_{ON}{}^2} = \frac{2\cdot 150}{50\cdot 0.5^2} = 24\mu\text{m} \quad\Rightarrow \underline{\underline{W_3 = W_4 = W_6 = W_7 = 24\mu\text{m}}}$$

Problem 6.5-15 – Continued

5.) Next design W_8, W_9, W_{10} and W_{11} to meet the minimum output voltage specification. Note that we have not taken advantage of smallest minimum output voltage because a normal cascode current mirror is used which has a minimum voltage across it of $V_T + 2V_{ON}$. Therefore, setting $V_T + 2V_{ON} = 1\text{V}$ gives $V_{ON} = 0.15\text{V}$. Using worst case current, we choose $1.5I$. Therefore,

$$W_8 = W_9 = W_{10} = W_{11} = \frac{2(1.5I)}{K_N V_{ON}^2} = \frac{2\cdot 150}{110\cdot 0.15^2} = 121\mu\text{m} \Rightarrow \underline{\underline{W_8 = W_9 = W_{10} = W_{11} = 121\mu\text{m}}}$$

6.) Check the maximum ICM voltage.

$$V_{ic}(\max) = V_{DD} + V_{SD3}(\text{sat}) + V_{TN} = 3\text{V} - 0.5 + 0.7 = 3.2\text{V} \text{ which exceeds spec.}$$

7.) Use the minimum ICM voltage to design W_5.

$$V_{ic}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = -3 + V_{DS5}(\text{sat}) + \left(\sqrt{\frac{2\cdot 50}{110\cdot 36}} + 0.7\right) = -1\text{V}$$

$$\therefore \quad V_{DS5}(\text{sat}) = 1.141 \rightarrow W_5 = \frac{2I}{K_N\, V_{DS5}(\text{sat})^2} = 1.39\mu\text{m} = 1.4\mu\text{m}$$

Also, let $W_{12} = W_{13} = W_5 \quad \Rightarrow \quad \underline{\underline{W_{12} = W_{13} = W_5 = 1.4\mu\text{m}}}$

8.) W_{14} is designed as

$$W_{14} = W_3 \frac{I_{14}}{I_3} = 24\mu\text{m}\,\frac{I}{1.5I} = 16\mu\text{m} \quad \Rightarrow \quad \underline{\underline{W_{14} = 16\mu\text{m}}}$$

Now, calculate the op amp small-signal performance.

$$R_{out} \approx r_{ds11} g_{m9} r_{ds9} \| g_{m7} r_{ds7} (r_{ds2} \| r_{ds4})$$

$$g_{m9} = \sqrt{2K_N \cdot I \cdot W_9} = 1632\mu\text{S}, \quad r_{ds9} = r_{ds11} = \frac{25\text{V}}{100\mu\text{A}} = 0.25\text{M}\Omega,$$

$$g_{m7} = \sqrt{2K_P \cdot I \cdot W_7} = 490\mu\text{S}, \quad r_{ds7} = \frac{20\text{V}}{100\mu\text{A}} = 0.2\text{M}\Omega, \quad r_{d2} = \frac{25\text{V}}{50\mu\text{A}} = 0.5\text{M}\Omega$$

$$r_{ds4} = \frac{20\text{V}}{150\mu\text{A}} = 0.1333\text{M}\Omega \quad \therefore \quad \underline{\underline{R_{out} \approx 102\text{M}\Omega \| 10.31\text{M}\Omega = 9.3682\text{M}\Omega}}$$

$$A_{vd} = \left(\frac{2+\text{k}}{2+2\text{k}}\right) g_{m1} R_{out}, \quad \text{k} = \frac{102\text{M}\Omega}{(r_{ds2}\| r_{ds4}) g_{m7} r_{ds7}} = 9.888, \quad g_{m1} = \sqrt{K_N \cdot I \cdot W_1} = 629\mu\text{S}$$

$$\therefore \quad A_{vd} = (0.5459)(629\mu\text{S})(9.3682\text{M}\Omega) = 3{,}217\text{V/V} \quad \Rightarrow \quad \underline{\underline{A_{vd} = 3{,}217\text{V/V}}}$$

Problem 6.5-16

The small signal resistances looking into the sources of M6 and M7 of Fig. P6.5-15 will be different based on what we learned for the cascode amplifier of Chapter 5. Assume that the capacitance from each of these nodes (sources of M6 and M7) are identical and determine the influence of these poles on the small-signal differential frequency response.

Solution

The resistance looking from the output to Vss is

$$R_{D9} \cong g_{m9} r_{ds9} r_{ds11}$$

The resistance looking at the source of M7 is

$$R_B = \frac{(r_{ds7} + R_{D9})}{(1 + g_{m7} r_{ds7})}$$

or, $$R_B \cong \frac{(g_{m9} r_{ds9} r_{ds11})}{(g_{m7} r_{ds7})} \quad (1)$$

The resistance looking from the drain of M8 to V_{ss} is $R_{D8} = \dfrac{1}{g_{m8}} + \dfrac{1}{g_{m10}}$

The resistance looking at the source of M6 is

$$R_A = \frac{(r_{ds6} + R_{D8})}{(1 + g_{m6} r_{ds6})} \quad \rightarrow \quad R_B \cong \frac{1}{g_{m6}} \quad (2)$$

The poles at the sources of M6 and M7 are

$$p_A = -\frac{1}{R_A C} \cong -\frac{g_{m6}}{C} \quad \text{and} \quad p_B = -\frac{1}{R_B C} \cong -\frac{1}{r_{ds} C}$$

Both of these poles will appear as output poles in the overall voltage transfer function.

Problem 6.6-01

How large could the offset voltage in Fig. 6.6-1 be before this method of measuring the open-loop response would be useless if the open-loop gain is 5000 V/V and the power supplies are ±2.5V?

Solution

Given, $V_{DD} - V_{SS} = 5$ V, and $A_v = 5000$ V/V

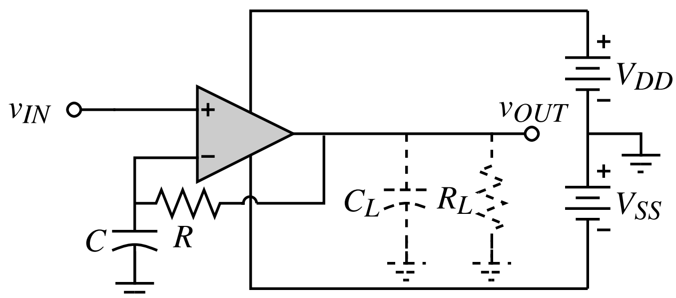
Therefore, the offset voltage should be less than

$$V_{os} < \frac{(V_{DD} - V_{SS})}{A_v}$$

or, $V_{os} < 1$ mV

Problem 6.6-02

Develop the closed-loop frequency response for op amp circuit shown which is used to measure the open-loop frequency reasponse. Sketch the closed-loop frequency response of the magnitude of V_{out}/V_{in} if the low frequency gain is 4000 V/V, the GB = 1MHz, R = 10MΩ, and C = 10µF. (Ignore R_L and C_L)



S01E2P2

Solution

The open-loop transfer function of the op amp is,

$$A_v(s) = \frac{GB}{s + (GB/A_v(0))} = \frac{2\pi \text{x} 10^6}{s + 500\pi}$$

The closed-loop transfer function of the op amp can be expressed as,

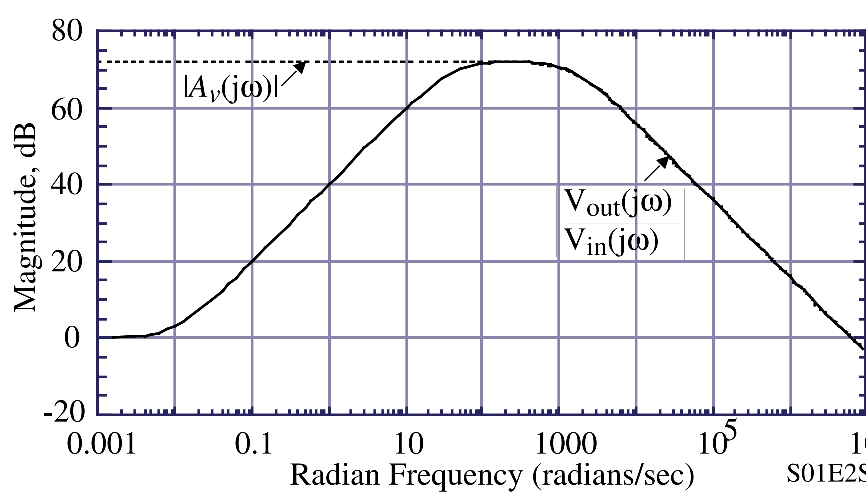
$$v_{OUT} = A_v(s)\left[\left(\frac{-1/sC}{R+(1/sC)}\right)v_{OUT} + v_{IN}\right] = A_v(s)\left[\left(\frac{-1/RC}{s+(1/RC)}\right)v_{OUT} + v_{IN}\right]$$

$$\therefore \quad \frac{v_{OUT}}{v_{IN}} = \frac{-[s+(1/RC)]A_v(s)}{s+(1/RC)+A_v(s)/RC} = \frac{-[s+(1/RC)]}{\frac{s+(1/RC)}{A_v(s)}+1/RC} = \frac{-(s+0.01)}{\frac{s+0.01}{A_v(s)}+0.01}$$

Substituting, $A_v(s)$ gives,

$$\frac{v_{OUT}}{v_{IN}} = \frac{-2\pi \text{x} 10^6 s - 2\pi \text{x} 10^4}{(s+0.01)(s+500\pi)+2\pi \text{x} 10^4} = \frac{-2\pi \text{x} 10^6 s - 2\pi \text{x} 10^4}{s^2+500\pi s+2\pi \text{x} 10^4} = \frac{-2\pi \text{x} 10^6(s+0.01)}{(s+41.07)(s+1529.72)}$$

The magnitude of the closed-loop frequency response is plotted below.



S01E2S2

Problem 6.6-03

Show how to modify Fig. 6.6-6 in order to measure the open-loop frequency response of the op amp under test and describe the procedure to be followed.

Solution

From the figure, let us change the v_{SET} associated with the top op amp. Change in this voltage would cause a change in v_I at the input of the DUT.

Let, for v_{SET1}

$$v_{I1} = \frac{v_{out1}}{A_V}$$

And, for v_{SET2}

$$v_{I2} = \frac{v_{out2}}{A_V}$$

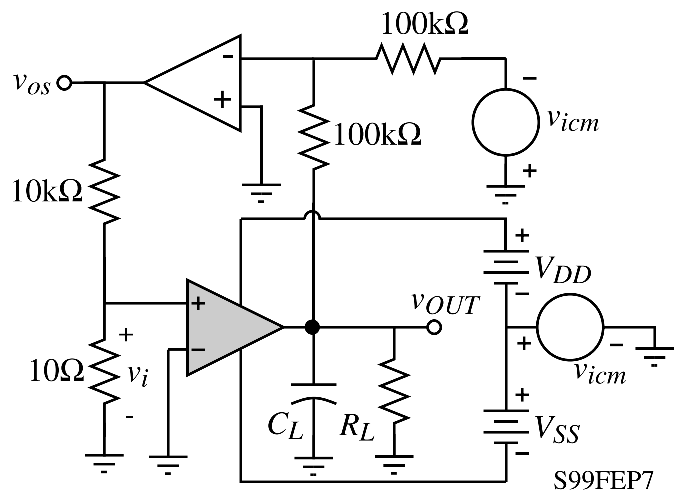
or, $$A_V = \frac{(v_{out1} - v_{out2})}{(v_{I1} - v_{I2})} = 1000\,\frac{(v_{out1} - v_{out2})}{(v_{os1} - v_{os2})} = 1000\,\frac{\Delta v_{out}}{\Delta v_{os}}$$

Thus, by measuring the values of Δv_{out} and Δv_{os} while changing v_{SET} can help in finding the value of the open-loop gain.

Problem 6.6-04

A circuit is shown which is used to measure the *CMRR* and *PSRR* of an op amp. Prove that the *CMRR* can be given as

$$CMRR = \frac{1000\ v_{icm}}{v_{os}}$$



Solution

The definition of the common-mode rejection ratio is

$$CMRR = \left|\frac{A_{vd}}{A_{cm}}\right| = \frac{\dfrac{v_{out}}{v_{id}}}{\dfrac{v_{out}}{v_{icm}}}$$

However, in the above circuit the value of v_{out} is the same so that we get

$$CMRR = \frac{v_{icm}}{v_{id}}$$

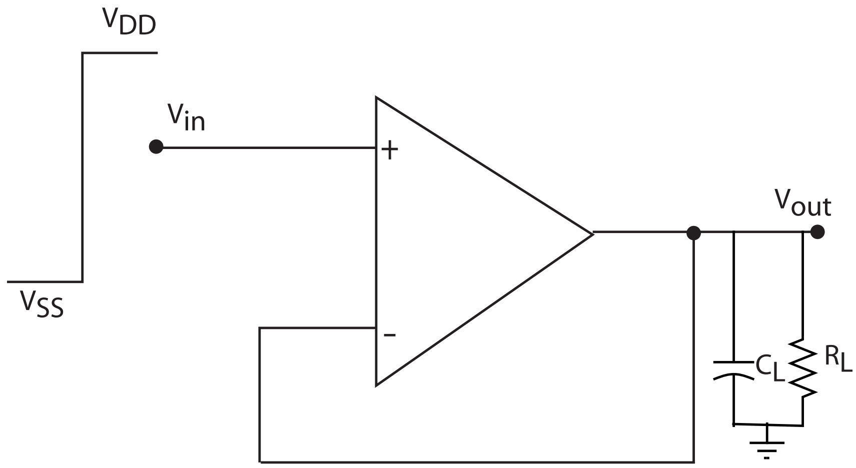
But $v_{id} = v_i$ and $v_{os} \approx 1000 v_i = 1000 v_{id}$ $\Rightarrow$ $v_{id} = \dfrac{v_{os}}{1000}$

Substituting in the previous expression gives, $$CMRR = \frac{v_{icm}}{\dfrac{v_{os}}{1000}} = \frac{1000\ v_{icm}}{v_{os}}$$

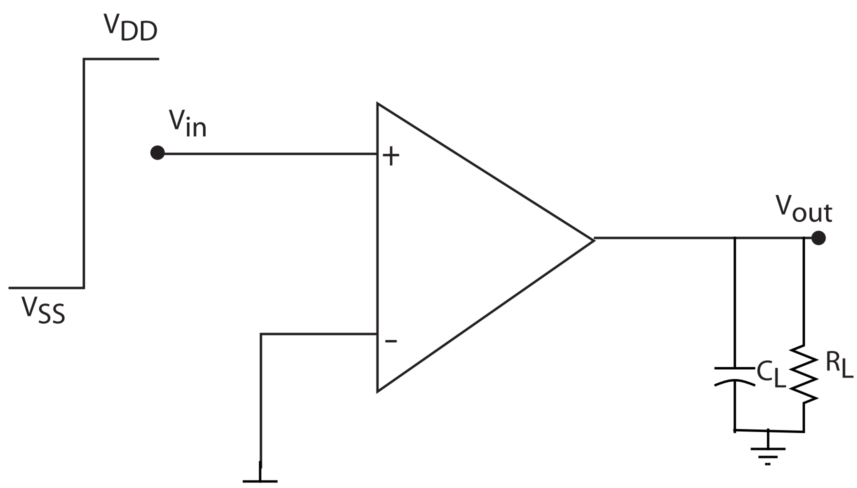
Problem 6.6-05

Sketch a circuit configuration suitable for simulating the following op amp characteristics: (a) slew rate, (b) transient response, (c) input CMR, (d) output voltage swing. Repeat for the measurement of the above op amp characteristics. What changes are made and why?

Solution



Slew rate, Transient response, and ICMR measurements



Output voltage swing measurement

The measurement of ICMR, Slew rate, and large-signal transient response can be measured using the buffer configuration as shown in the figure. The input applied is a rail-to-rail step signal, which can be used to measure the maximum and minimum input swing, the slew rate, rise and settling time. The same configuration can be used to measure the performance in simulation. This buffer configuration can also be used to measure the small-signal transient performance. The applied input should be a small signal applied over the nominal input common-mode bias voltage, and it can be used to measure the overshoot.

The maximum and minimum output voltage swing can be measured using the open-loop configuration of the op amp as shown in the figure. The input applied is a rail-to-rail step signal, which will overdrive the output to its maximum and minimum swing voltage levels.

Problem 6.6-06

Using two identical op amps, show how to use SPICE in order to obtain a voltage which is proportional to CMRR rather than the inverse relationship given in Sec. 6.6.

Solution

TBD

Problem 6.6-07

Repeat the above problem for PSRR.

Solution

TBD

Problem 6.6-08

Use SPICE to simulate the op amp of Example 6.5-2. The differential-frequency response, power dissipation, phase margin, common-mode input range, output-voltage range, slew rate, and settling time are to be simulated with a load capacitance of 20 pF. Use the model parameters of Table 3.1-2.

Solution

TBD

Problem 6.6-09

Use SPICE to simulate the op amp of Example 6.5-3. The differential frequency response, power dissipation, phase margin, input common-mode range, output-voltage range, slew rate, and settling time are to be simulated with a load capacitance of 20pF. Use the model parameters of Table 3.1-2.

Solution

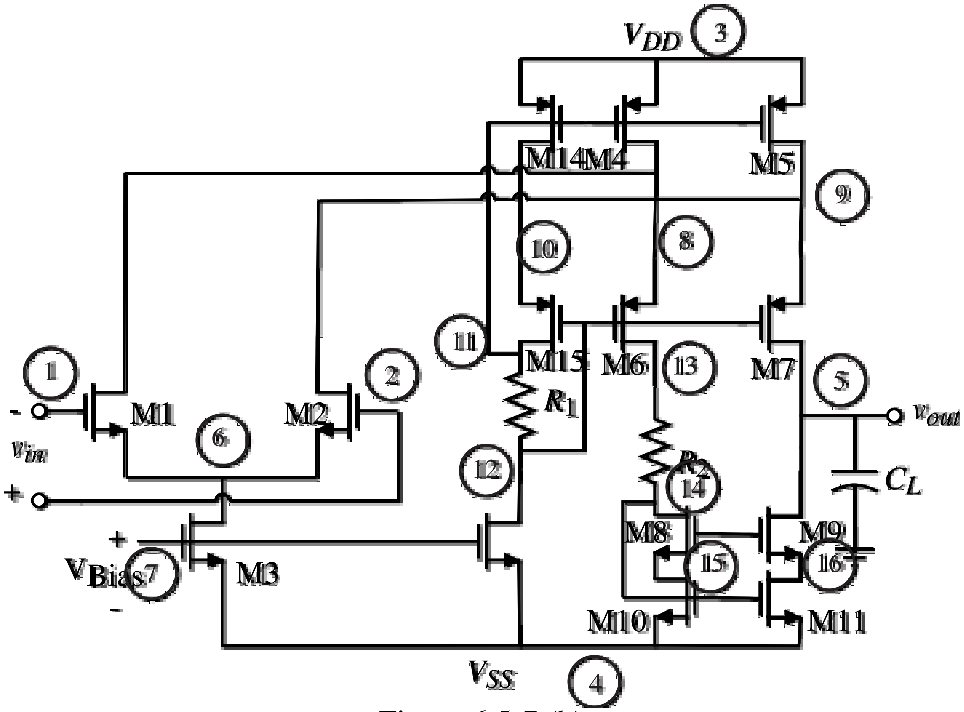


Figure 6.5-7 (b)

The following is the SPICE source file for figure 6.5-7.

```
* Problem 6.6-9 SPICE simulation
*

*Voltage gain and phase margin
*VDD 3 0 DC 2.5
*VSS 0 4 DC 2.5
*VIN 30 0 DC 0 AC 1.0
*EIN+ 1 0 30 0 1
*EIN- 2 0 30 0 -1

*Output voltage swing
*VDD 3 0 DC 2.5
*VSS 0 4 DC 2.5
*VIN+ 40 0 DC 0 AC 1.0
*VIN- 2 0 0
*Reg1 40 1 10K
*Reg2 5 1 100K
```

Problem 6.6-09 - Continued

```
*ICMR
*VDD 3 0 DC 2.5
*VSS 0 4 DC 2.5
*VIN+ 1 0 DC 0 AC 1.0

*PSRR+
*VDD 3 0 DC 2.5 AC 1.0
*VSS 0 4 DC 2.5
*PSRR-
VDD 3 0 DC 2.5
VSS 0 4 DC 2.5 AC 1.0
VIN+ 1 0 DC 0

*Slew Rate
*VDD 3 0 DC 2.5
*VSS 0 4 DC 2.5
*VIN+ 1 0 PWL(0 -1 10N -1 20N 1 2U 1 2.0001U -1 4U -1 4.0001U 1 6U 1 6.0001u
+ -1 8U -1 8.0001U 1 10U 1)

*General
*X1 1 2 3 4 5 OPAMP

*Unity gain configuration
X1 1 5 3 4 5 OPAMP

.SUBCKT OPAMP 1 2 3 4 5
M1 8 1 6 4 NPN W=35.9u L=1u
M2 9 2 6 4 NPN W=35.9u L=1u
M3 6 7 4 4 NPN W=20u L=1u
M4 8 11 3 3 PNP W=80u L=1u
M5 9 11 3 3 PNP W=80u L=1u
M6 13 12 8 8 PNP W=80u L=1u
M7 5 12 9 9 PNP W=80u L=1u
M8 14 13 15 4 NPN W=36.36u L=1u
M9 5 13 16 4 NPN W=36.36u L=1u
M10 15 14 4 4 NPN W=36.36u L=1u
M11 16 14 4 4 NPN W=36.36u L=1u
M12 12 7 4 4 NPN W=25u L=1u
M13 11 12 10 10 PNP W=80u L=1u
M14 10 11 3 3 PNP W=80u L=1u
R1 11 12 2K
R2 13 14 2K
VBIAS 0 7 1.29
.MODEL NPN NMOS VTO=0.70 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.MODEL PNP PMOS VTO=-0.7 KP=50U GAMMA=0.57 LAMBDA=0.05 PHI=0.8
.ENDS

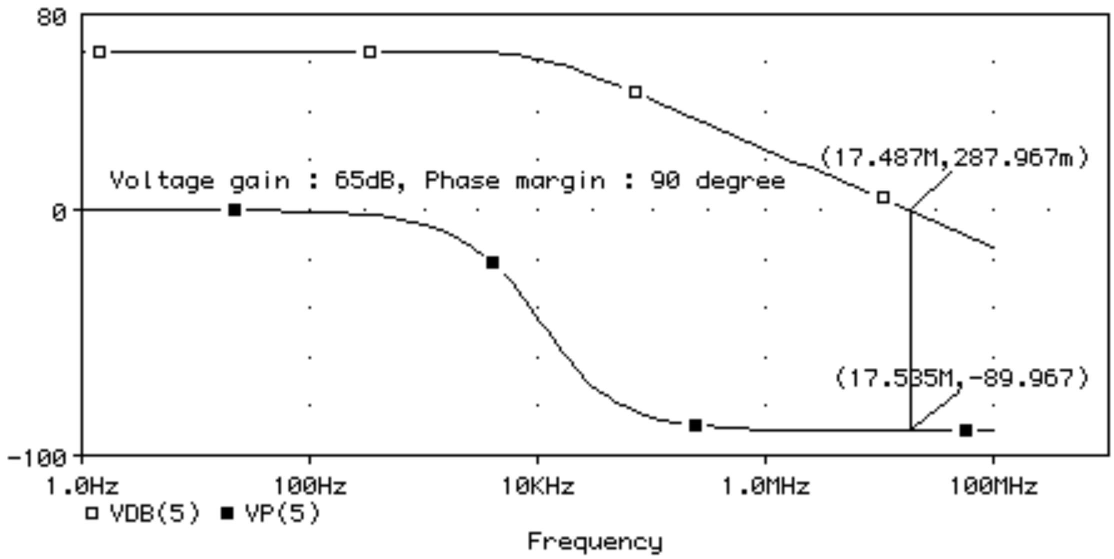
*Load cap
CL 5 0 20PF

.OP
.OPTION GMIN=1e-6
```

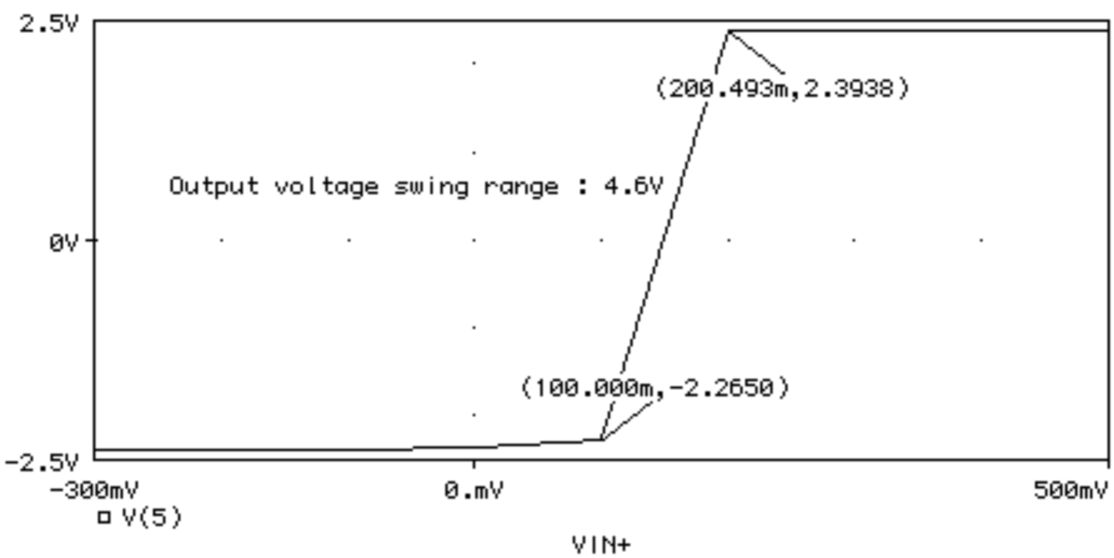
Problem 6.6-09 - Continued

```
.DC VIN+ -2.5 2.5 0.1
.PRINT DC V(5)
.TRAN 0.05u 10u
.PRINT TRAN V(5) V(1)
.AC DEC 10 1 100MEG
.PRINT AC VDB(5) VP(5)
.PROBE
.END
```

The simulation results are shown.

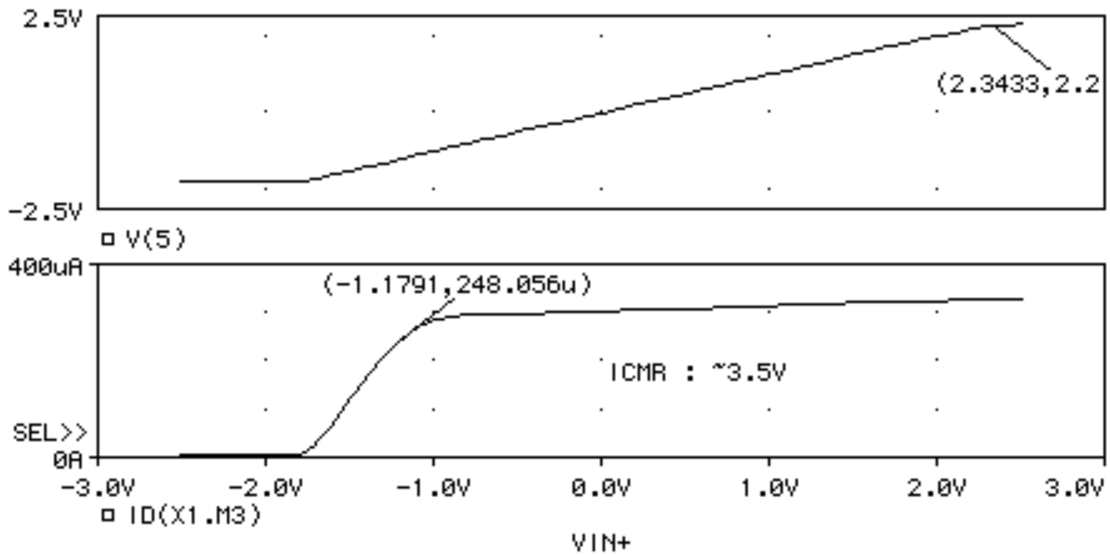


Result 1. Voltage gain and phase margin

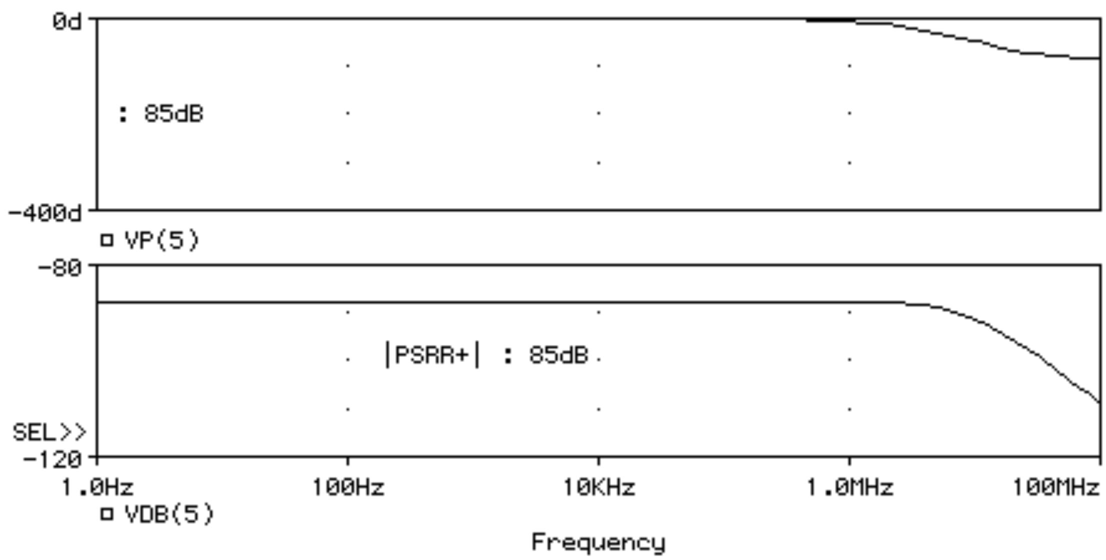


Result 2. Output voltage swing range

Problem 6.6-09 - Continued

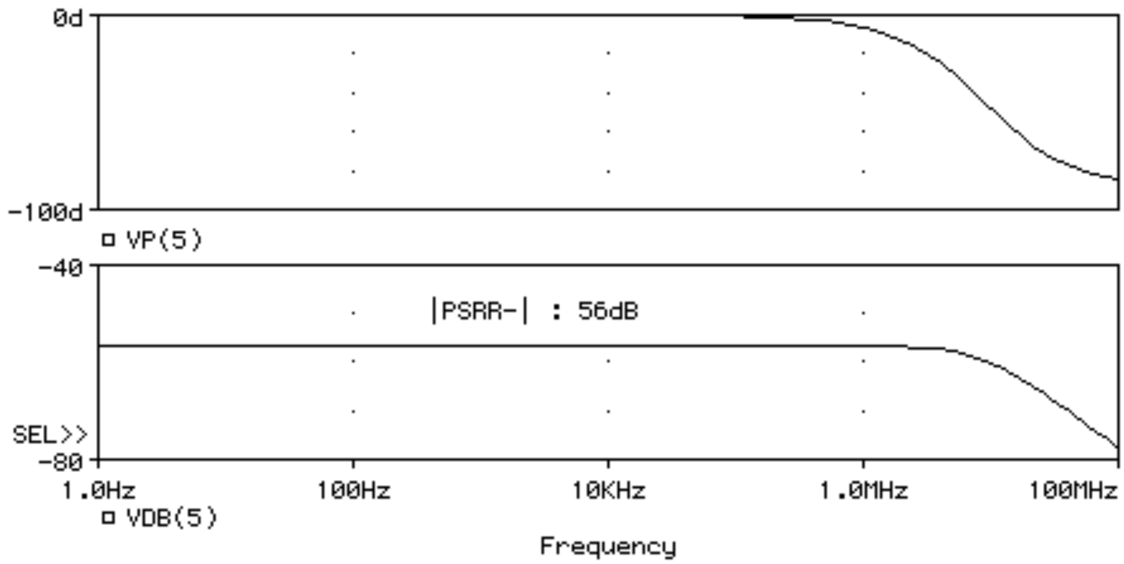


Result 3. Input common-mode range

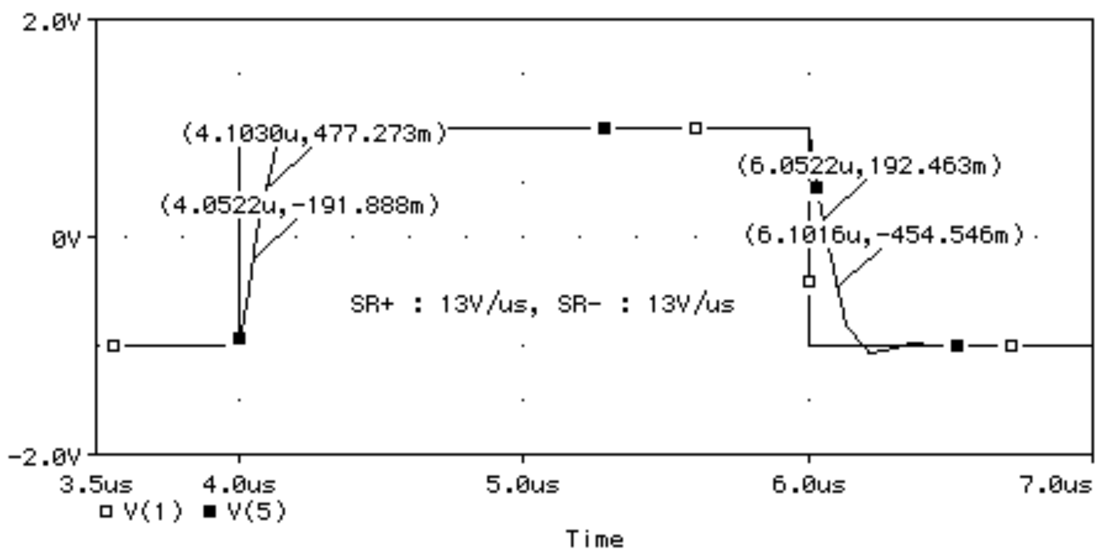


Result 4. Positive power supply rejection ratio

Problem 6.6-09 - Continued

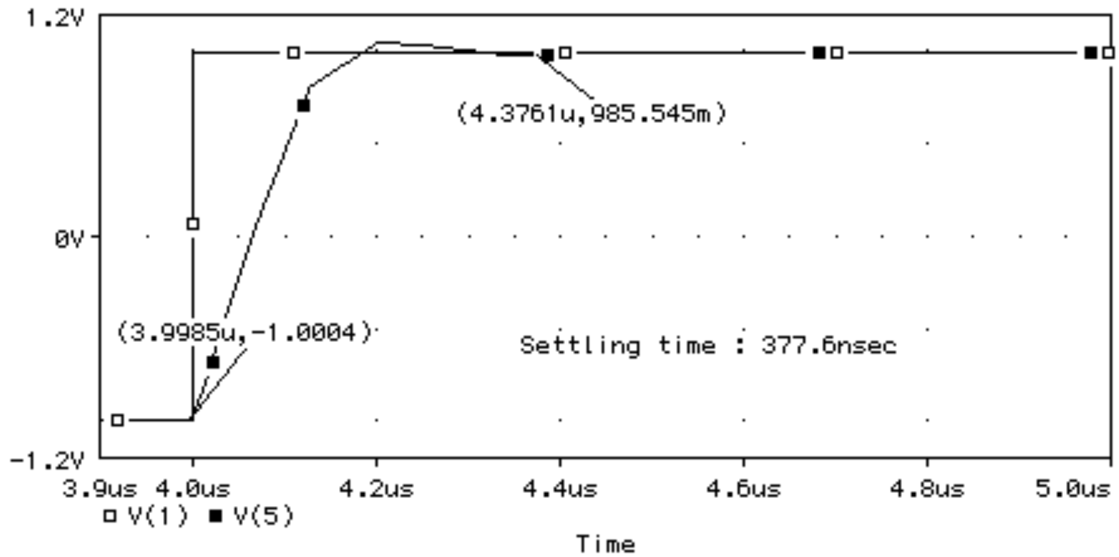


Result 5. Negative power supply rejection ratio



Result 6. Slew rate

Problem 6.6-09 - Continued



Result 7. Settling time

From the output file of the SPICE simulation, total power dissipation is 6mW. The following is a part of the output file.

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.0000	(3)	2.5000	(4)	-2.5000	(5)	-1.0004
(X1.6)	-2.0477	(X1.7)	-1.2900	(X1.8)	1.5876	(X1.9)	1.5874
(X1.10)	1.7094	(X1.11)	1.3594	(X1.12)	.5508	(X1.13)	-.9291
(X1.14)	-1.4451	(X1.15)	-2.0731	(X1.16)	-2.0706		

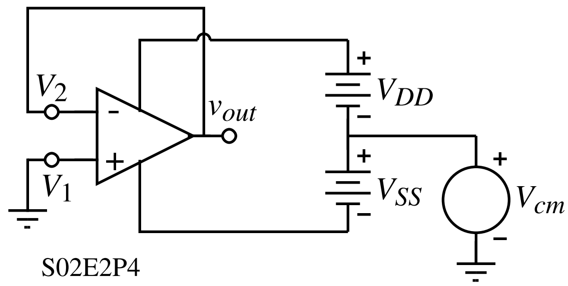
VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VDD	-1.218E-03
VSS	-1.218E-03
VIN+	0.000E+00
X1.VBIAS	0.000E+00

TOTAL POWER DISSIPATION 6.09E-03 WATTS

Problem 6.6-10

A possible scheme for simulating the *CMRR* of an op amp is shown. Find the value of V_{out}/V_{in} and show that it is approximately equal to 1/*CMRR*. What problems might result in the actual implementation of this circuit to measure *CMRR*?

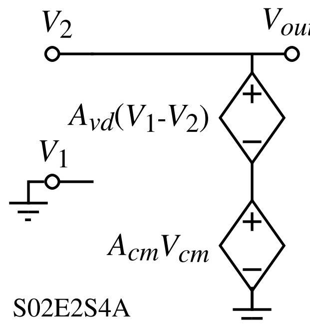


S02E2P4

Solution

The model for this circuit is shown. We can write that

$$V_{out} = A_{vd}(V_1\text{-}V_2) + A_{cm}V_{cm}$$
$$= \text{-}A_{vd}V_{out} + A_{cm}V_{cm}$$



S02E2S4A

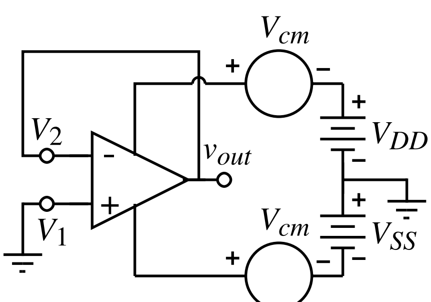
Thus,

$$V_{out}(1+A_{vd}) = A_{cm}V_{cm}$$

or

$$\frac{V_{out}}{V_{cm}} = \frac{A_{cm}}{1+A_{vd}} \approx \frac{A_{cm}}{A_{vd}} = \frac{1}{CMRR}$$

The potential problem with this method is that $PSRR^+$ is not equal to $PSRR^-$. This can be seen by moving the V_{cm} through the power supplies so it appears as power supply ripple as shown below. This method depends on the fact that the positive and negative power supply ripple will cancel each other.



S02E2S4B

Problem 6.6-11

Explain why the positive overshoot of the simulated positive step response of the op amp shown in Fig. 6.6-20(b) is smaller than the negative overshoot for the negative step response. Use the op amp values given in Ex. 6.3-1 and the information given in Tables 6.6-1 and 6.6-3.

Solution

Consider the following circuit and waveform:

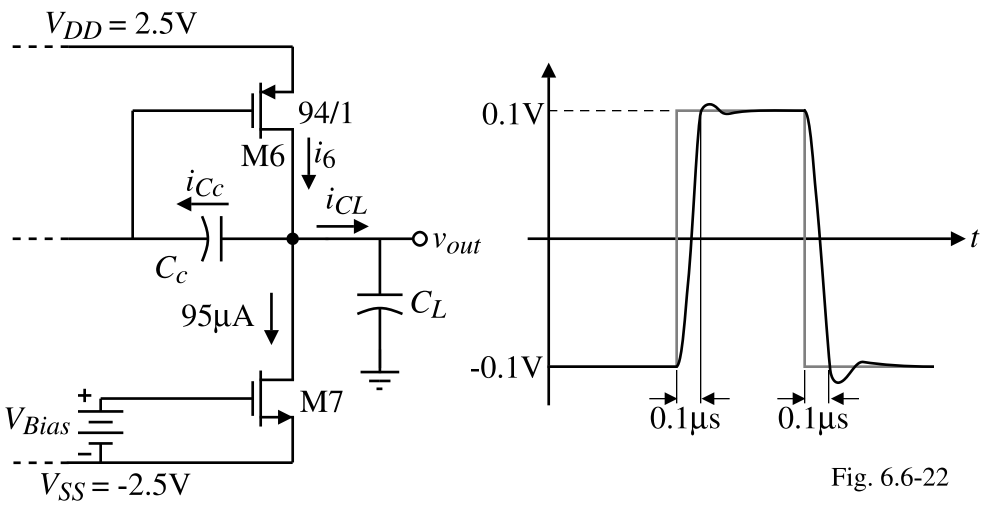


Fig. 6.6-22

During the rise time, $i_{CL} = C_L(dv_{out}/dt) = 10\text{pF}(0.2\text{V}/0.1\mu\text{s}) = 20\mu\text{A}$ and $i_{Cc} = 3\text{pf}(2\text{V}/\mu\text{s}) = 6\mu\text{A}$

$\therefore\ i_6 = 95\mu\text{A} + 20\mu\text{A} + 6\mu\text{A} = 121\mu\text{A} \Rightarrow g_{m6} = 1066\mu\text{S}$ (nominal was 942.5µS)

During the fall time, $i_{CL} = C_L(-dv_{out}/dt) = 10\text{pF}(-0.2\text{V}/0.1\mu\text{s}) = -20\mu\text{A}$

and $i_{Cc} = -3\text{pf}(2\text{V}/\mu\text{s}) = -6\mu\text{A}$

$\therefore\ i_6 = 95\mu\text{A} - 20\mu\text{A} - 6\mu\text{A} = 69\mu\text{A} \Rightarrow g_{m6} = 805\mu\text{S}$

The dominant pole is $p_1 \approx (R_I g_{m6} R_{II} C_c)^{-1}$ where $R_I = 0.694\text{M}\Omega$, $R_{II} = 122.5\text{k}\Omega$ and $C_c = 3\text{pF}$.

$\therefore\ p_1(95\mu\text{A}) = 4{,}160$ rads/sec, $p_1(121\mu\text{A}) = 3{,}678$ rads/sec, and $p_1(69\mu\text{A}) = 4{,}870$ rads/sec.

Thus, the phase margin is less during the fall time than the rise time.

Problem 6.7-01

Develop a macromodel for the op amp of Fig. 6.1-2 which models the low frequency gain $A_v(0)$, the unity-gain bandwidth *GB,* the output resistance R_{out}, and the output-voltage swing limits V_{OH} and V_{OL}. Your macromodel should be compatible with SPICE and should contain only resistors, capacitors, controlled sources, independent sources, and diodes.

Solution

TBD

Problem 6.7-02

Develop a macromodel for the op amp of Fig. 6.1-2 that models the low-frequency gain $A_v(0)$, the unity-gain bandwidth *GB,* the output resistance R_{out}, and the slew rate *SR*. Your macromodel should be compatible with SPICE and should contain only resistors, capacitors, controlled sources, independent sources, and diodes.

Solution

TBD

Problem 6.7-03

Develop a macromodel for the op amp shown in Fig. P6.7-3 that has the following properties:

a.) $$A_{vd}(s) = \frac{A_{vd}(0)\left(\frac{s}{z_1} - 1\right)}{\left(\frac{s}{p_1} + 1\right)\left(\frac{s}{p_2} + 1\right)}$$

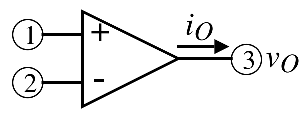


Figure P6.7-3

where $A_{vd}(0) = 10^4$,$z_1 = 10^6$ rads/sec., $p_1 = 10^2$ rads/sec, and $p_2 = 10^7$ rads/sec.

b.) $R_{id} = 1\text{M}\Omega$.

c.) $R_o = 100\Omega$.

d.) CMRR(0) = 80dB.

Show a schematic diagram of your macromodel and identify the elements that define the model parameters $A_{vd}(0)$, z_1, p_1, p_2, R_{id}, R_o, and CMRR(0). Your macromodel should have a minimum number of nodes.

Solution

The following macromodel is used to solve this problem.

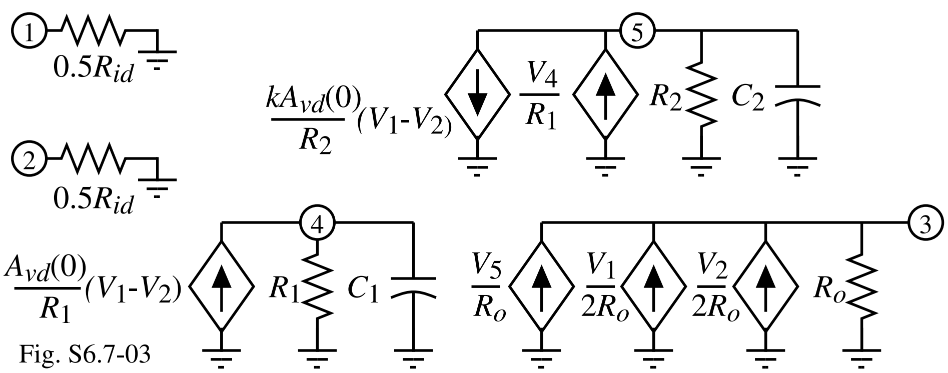


Fig. S6.7-03

Verifying the macromodel by solving for V_3 gives,

$$V_3 = V_5 + 0.5(V_1+V_2) = \left(\frac{R_2}{sR_2C_2+1}\right)\left[\frac{V_4}{R_2} - \frac{kA_{vd}(0)}{R_2}(V_1\text{-}V_2)\right] + V_{icm}$$

$$= \left(\frac{A_{vd}(0)}{sR_2C_2+1}\right)\left[\frac{V_{id}}{sR_1C_1+1} - kV_{id}\right] + V_{icm} = \frac{A_{vd}(0)}{(sR_1C_1+1)(sR_2C_2+1)}(1\text{-}ksR_1C_1\text{-}k)V_{id} + V_{icm}$$

Choose $R_1 = 10\text{k}\Omega \rightarrow C_1 = 1\mu\text{F}$, $R_2 = 1\Omega \rightarrow C_1 = 0.1\mu\text{F}$, $R_o = 100\Omega$, and $R_{id} = 1\text{M}\Omega$ and solve for k. (note that the polarity of k was defined in the above macromodel to make k positive).

$$1\text{-}ksR_1C_1\text{-}k = 0 \;\rightarrow\; z = \frac{1}{R_1C_1}\left(\frac{1}{k} - 1\right) \;\rightarrow\; 10^6 = 10^2\left(\frac{1}{k} - 1\right) \;\rightarrow\; k \approx 10^{-4}$$

With these choices, the transconductance values of all controlled sources are unity except for the ones connected to the output node, node 3.

Problem 6.7-04

Develop a macromodel suitable for SPICE of a differential, current amplifier of Fig. P6.7-4 having the following specifications:

$$i_{OUT} = A_i(s)[i_1 - i_2]$$

where

$$A_i(s) = \frac{\mathbf{GB}}{s+\boldsymbol{\omega_a}} = \frac{10^6}{s+100}$$

$$\mathbf{R_{in1}} = \mathbf{R_{in2}} = 10\Omega$$

$$\mathbf{R_{out}} = 100\text{k}\Omega$$

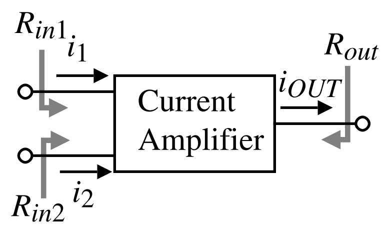


Figure P6.7-4

and

$$\mathbf{Max|di_{OUT}/dt|} = 10\text{A}/\mu\text{s}.$$

Your macromodel *may use only passive components, dependent and independent sources, and diodes* (i.e., no switches). Give a schematic for your macromodel and relate each component to the parameters of the macromodel. (The parameters are in bold.) Minimize the number of nodes where possible.

Solution

A realization is shown below along with the pertinent relationships.

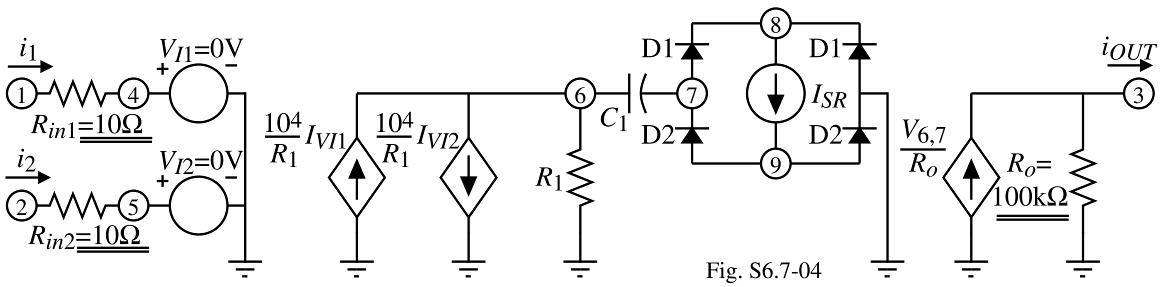


Fig. S6.7-04

$$i_{C1} = \frac{dv_{6,7}}{dt} C_1 \rightarrow I_{SR} = 10^7\ C_1 \qquad \text{Choose } C_1 = 0.1\mu\text{F} \Rightarrow \qquad \underline{\underline{I_{SR} = 1\text{A}}}$$

$$\text{Therefore, } \frac{1}{R_1C_1} = 100 \qquad \rightarrow \qquad R_1 = \frac{1}{100\cdot C_1} = \frac{10^7}{10^2} = 100\text{k}\Omega \rightarrow \underline{\underline{R_1 = 100\text{k}\Omega}}$$

Note that the voltage rate limit becomes a current rate limit because $i_{OUT} = v_{6,7}$

CHAPTER 7 – HOMEWORK SOLUTIONS

Problem 7.1-01

Assume that V_{DD} = -V_{SS} and I_{17} and I_{20} in Fig. 7.1-2 are 100µA. Design W_{18}/L_{18} and W_{19}/L_{19} to get V_{SG18} = V_{GS19} = 1.5V. Design W_{21}/L_{21} and W_{22}/L_{22} so that the quiescent current in M21 and M22 is also 100µA.

Solution

Assuming $V_{DD} = -V_{SS} = 2.5$ V, and $V_o = 0$ V

Due to bulk effects,

$$V_T = V_{T0} + \gamma\left(\sqrt{2\phi + V_{SB}} - \sqrt{2\phi}\right)$$

Thus, $V_{T19} = 0.89$ V, and $|V_{T18}| = 0.95$ V

Now,

$$V_{SG18} = |V_{T18}| + \sqrt{\frac{2I_{18}}{K'_P(W/L)_{18}}}$$

or, $\left(\frac{W}{L}\right)_{18} = 13.5$

And, $V_{SG19} = V_{T19} + \sqrt{\frac{2I_{19}}{K'_N(W/L)_{19}}}$

or, $\left(\frac{W}{L}\right)_{19} = 4.9$

Since $V_o = 0$ V, $V_{T21} = 1.08$ V, and $|V_{T22}| = 1.23$ V

$$V_{SG21} = V_{T21} + \sqrt{\frac{2I_{21}}{K'_N(W/L)_{21}}}$$

or, $\boxed{\left(\frac{W}{L}\right)_{21} = 10.3}$

And, $V_{SG22} = |V_{T22}| + \sqrt{\frac{2I_{22}}{K'_P(W/L)_{22}}}$

or, $\boxed{\left(\frac{W}{L}\right)_{22} = 55}$

Problem 7.1-02

Calculate the value of V_A and V_B in Fig. 7.1-2 and therefore the value of V_C.

Solution

The first trip point V_A is defined as the input for which M_5 trips (or turns on). If it is assumed that the small-signal gain of the inverters ($M_1 - M_3$ and $M_2 - M_4$) is large, then it can be assumed that M_5 will trip when $M_1 - M_3$ are in saturation.

Thus,

$$V_A = V_{GS1} = V_{T1} + \sqrt{\frac{\beta_3}{\beta_1}}\left(V_{SG3} - |V_{T3}|\right) \qquad \rightarrow \qquad \underline{\underline{V_A = 0.9\text{ V}}}$$

Similarly, it can be assumed that M_6 will trip when $M_2 - M_4$ are in saturation.

Thus,

$$V_B = V_{GS2} = V_{T2} + \sqrt{\frac{\beta_4}{\beta_2}}\left(V_{SG4} - |V_{T4}|\right)$$

or, $\underline{\underline{V_A = 1.0\text{ V}}}$

So, $V_C = V_B - V_A = \underline{\underline{0.1\text{V}}}$

Problem 7.1-03

Assume that $K'_N = 47\ \mu A/V^2$, $K'_P = 17\ \mu A/V^2$, $V_{TN} = 0.7$ V, $V_{TP} = -0.9$ V, $\gamma_N = 0.85$ $V^{1/2}$, $\gamma_P = 0.25$ $V^{1/2}$, $2|\phi_F| = 0.62$ V, $\lambda_N = 0.05$ V^{-1}, and $\lambda_P = 0.04$ V^{-1}. Use SPICE to simulate Fig. 7.1-2 and obtain the simulated equivalent of Fig. 7.1-3.

Solution

TBD

Problem 7.1-04

Use SPICE to plot the total harmonic distortion (THD) of the output stage of Fig. 7.1-5 as a function of the RMS output voltage at 1 kHz for an input-stage bias current of 20 μA. Use the SPICE model parameters given in the previous problem.

Solution

TBD

Problem 7.1-05

An MOS output stage is shown in Fig. P7.1-5. Draw a small-signal model and calculate the ac voltage gain at low frequency. Assume that bulk effects can be neglected.

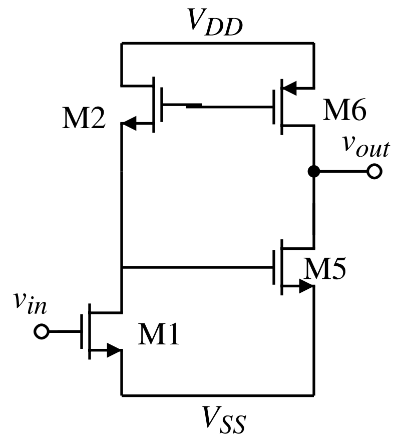


Figure P7.1-5

Solution

Referring to the figure

$$v_{gs2} = v_{out}\ \text{, and } v_{gs1} = v_{in}$$

Applying nodal analysis

$$(g_{ds2} + g_{ds1})v_{gs4} + g_{m1}v_{in} + g_{m2}v_{out} = 0 \qquad (1)$$

And, $$g_{m4}v_{gs4} + (g_{m3} + g_{ds4})v_{out} = 0 \qquad (2)$$

From Equations (1) and (2)

$$\boxed{\frac{v_{out}}{v_{in}} = \frac{-g_{m1}g_{m4}}{(g_{m2}g_{m4} - (g_{m3} + g_{ds4})(g_{ds1} + g_{ds2}))}}$$

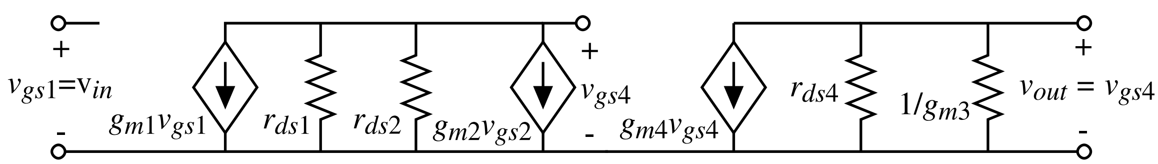


Fig. S7.1-05A

Problem 7.1-06

Find the value of the small-signal output resistance of Fig. 7.1-9 if the *W* values of M1 and M2 are increased from 10µm to 10µm. Use the model parameters of Table 3.1-2. What is the -3dB frequency of this buffer if C_L = 10pF?

Solution

The loop-gain of the negative feedback loop is given by

$$LG = -\frac{g_{m2}(g_{m6} + g_{m8})}{2g_{m4}(g_{ds6} + g_{ds7})}$$

or, $$LG = -164$$

The output resistance can be expressed as

$$R_{out} = \frac{(g_{ds6} + g_{ds7})^{-1}}{1 - LG}$$

or, $$R_{out} = 67.3\ \Omega$$

The –3 dB frequency point is

$$f_{-3dB} = \frac{1}{2\pi R_{out}C_L}$$

or, $f_{\text{-3dB}}$ = 236 MHz

Problem 7.1-07

A CMOS circuit used as an output buffer for an OTA is shown. Find the value of the small signal output resistance, R_{out}, and from this value estimate the -3dB bandwidth if a 50pF capacitor is attached to the output. What is the maximum and minimum output voltage if a 1kΩ resistor is attached to the output? What is the quiescent power dissipation of this circuit? Use the following model parameters: K_N'=110μA/V^2, K_P' = 50μA/V^2, V_{TN} = $-V_{TP}$ = 0.7V, λ_N = 0.04V^{-1} and λ_P = 0.05V^{-1}.

Solution

Use feedback concepts to calculate the output resistance, R_{out}.

$$R_{out} = \frac{R_o}{1\text{-}LG}$$

where R_o is the output resistance with the feedback open and LG is the loop gain.

$$R_o = \frac{1}{g_{ds6}+g_{ds7}} = \frac{1}{(\lambda_N+\lambda_P)I_6} = \frac{10^6}{0.09\cdot 500} = 22.22\text{k}\Omega$$

The loop gain is,

$$LG = \frac{v_{out}'}{v_{out}} = -\frac{1}{2}\left[\frac{g_{m2}g_{m6}}{g_{m4}} + \frac{g_{m1}g_{m9}}{g_{m7}}\right]R_o$$

$g_{m1} = g_{m2} = \sqrt{2\cdot 110\cdot 50\cdot 10} = 331.67\mu\text{S}$, $g_{m3} = g_{m4} = \sqrt{2\cdot 50\cdot 50\cdot 10} = 223.6\mu\text{S}$,

$g_{m6} = \sqrt{2\cdot 50\cdot 100\cdot 500} = 2236\mu\text{S}$ and $g_{m7} = \sqrt{2\cdot 110\cdot 500\cdot 100} = 3316.7\mu\text{S}$

$$\therefore \quad LG = \frac{v_{out}'}{v_{out}} = -\frac{1}{2}\left[\frac{-331.67\cdot 2236}{223.6} + \frac{-331.67\cdot 3316.7}{331.67}\right] = -73.68\text{V/V}$$

$$R_{out} = \frac{R_o}{1\text{-}LG} = \frac{22.22\text{k}\Omega}{1+73.68} = \underline{\underline{294.5\Omega}}$$

$$f_{\text{-3dB}} = \frac{1}{2\pi\cdot R_{out}\cdot 50\text{pF}} = \frac{1}{2\pi\cdot 294.5\cdot 50\text{pF}} = \underline{\underline{10.81\text{MHz}}}$$

To get the maximum swing, we must check two limits. First, the saturation voltages of M6 and M7.

$$V_{ds6}(\text{sat}) = \sqrt{\frac{2\cdot 1000}{50\cdot 100}} = 0.6325\text{V} \quad \text{and} \quad V_{ds7}(\text{sat}) = \sqrt{\frac{2\cdot 1000}{110\cdot 100}} = 0.4264\text{V}$$

Second, the maximum current available to the 1kΩ resistor is ±1mA which means that the output swing can only be ±1V. Therefore, maximum/minimum output = ±1V.

$P_{diss} = 6\text{V}(650\mu\text{A}) = \underline{\underline{3.9\text{mW}}}$

Problem 7.1-08

What type of BJT is available with a bulk CMOS p-well technology? A bulk CMOS n-well technology?

Solution

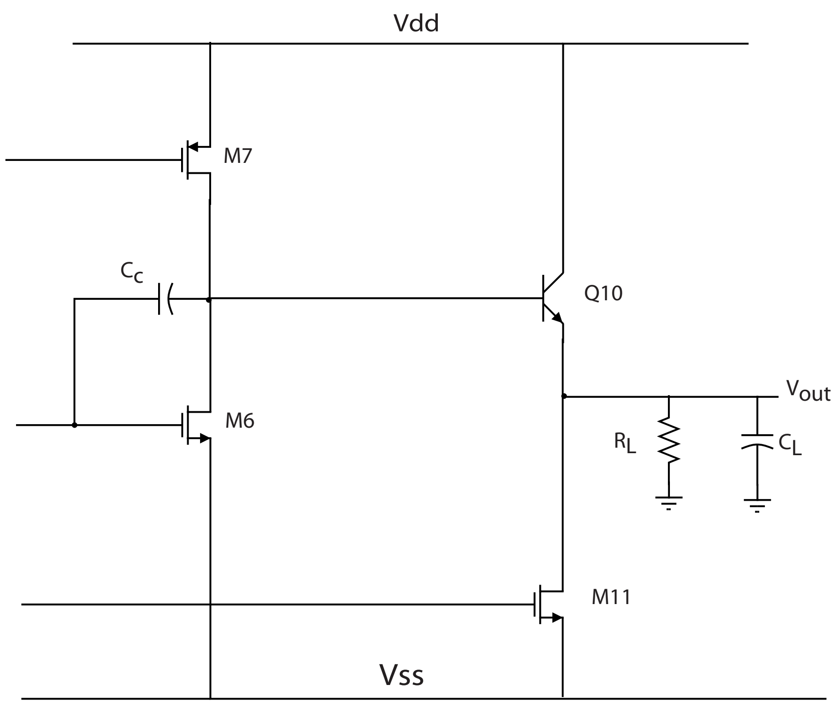
In a bulk CMOS p-well technology, n-p-n BJTs (both substrate and lateral) are available.

In a bulk CMOS n-well technology, p-n-p BJTs (both substrate and lateral) are available.

Problem 7.1-09

Assume that Q10 of Fig. 7.1-11 is connected directly to the drains of M6 and M7 and that M8 and M9 are not present. Give an expression for the small-signal output resistance and compare this with Eq. (9). If the current in Q10-M11 is 500μA, the current in M6 and M7 is 100μA, and β_F = 100, use the parameters of Table 3.1-2 assuming 1μm channel lengths and calculate this resistance at room temperature.

Solution



The output resistance is

$$R_{out} \cong \frac{1}{g_{m10}} + \frac{1}{(1+\beta_F)(g_{ds6}+g_{ds7})}$$

From Equation (7.1-9)

$$R_{out} \cong \frac{1}{g_{m10}} + \frac{1}{(1+\beta_F)g_{m9}}$$

Here,

$g_{m10} = 19.23$ μS and $g_{ds6} + g_{ds7} = 9$ μS

Thus, R_{out} = 1152 Ω

Problem 7.1-10

Find the dominant roots of the MOS follower and the BJT follower for the buffered, class-A op amp of Ex. 7.1-2. Use the capacitances of Table 3.2-1. Compare these root locations with the fact that GB = 5MHz? Assume the capacitances of the BJT are C_π = 10pf and C_μ = 1pF.

Solution

The model of just the output buffer of Ex. 7.1-2 is shown.

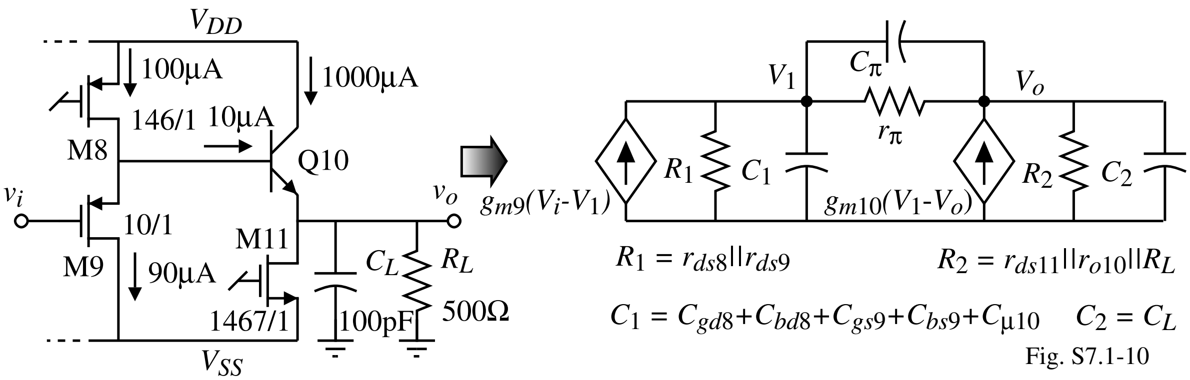


Fig. S7.1-10

The nodal equations can be written as,

$$g_{m9}V_i = (g_{m9} + G_1 + g_{\pi10} + sC_{\pi10} + sC_1)V_1 - (g_{\pi10} + sC_{\pi10})V_o$$

$$0 = -(g_{m10} + g_{\pi10} + sC_{\pi10})V_1 + (g_{m10} + G_2 + g_{\pi10} + sC_{\pi10} + sC_2)V_o$$

Solving for V_o/V_i gives,

$$\frac{V_o}{V_i} = \frac{g_{m9}(g_{m10}+ g_{\pi10}+ sC_{\pi10})}{(g_{\pi10} + sC_{\pi10})(g_{m9}+ G_1 + G_2 + sC_1 + sC_2) + (g_{m10}+ G_2+ sC_2)(g_{m9}+ G_1 + sC_1)}$$

$$\frac{V_o}{V_i} = \frac{g_{m9}(g_{m10}+ g_{\pi10}+ sC_{\pi10})}{a_0 + sa_1 + s^2a_2}$$

where

$$a_0 = g_{m9}g_{\pi10} + g_{\pi10}G_1 + \boldsymbol{g_{\pi10}G_2} + \boldsymbol{g_{m9}g_{m10}} + \boldsymbol{g_{m10}G_1} + \boldsymbol{g_{m9}G_2} + G_1G_2$$

$$a_1 = g_{m9}C_{\pi10}+G_1C_{\pi10}+\boldsymbol{G_2C_{\pi10}}+g_{\pi10}C_1+\boldsymbol{g_{\pi10}C_2}+\boldsymbol{g_{m10}C_1}+G_2C_1+\boldsymbol{g_{m9}C_2}+G_1C_2$$

$$a_2 = C_{\pi10}C_1 + \boldsymbol{C_{\pi10}C_2} + C_1C_2$$

The numerical value of the small signal parameters are:

$g_{m10} = \dfrac{1\text{mA}}{25.9\text{mV}}$ = 38.6mS, G_2 = 2mS, $g_{\pi10}$ = 386µS, $g_{m9} = \sqrt{2\cdot50\cdot10\cdot90}$ = 300µS, $G_1 = g_{ds8} + g_{ds9}$ = 0.05·100µA + 0.05·90µA = 9.5µS

C_2 = 100pF, $C_{\pi10}$ = 10pF, $C_1 = C_{gs9} + C_{bs9} + C_{bd8} + C_{gd8} + C_{\mu10}$

$$C_{gs9} = C_{ov} +0.667C_{ox}W_9L_9 = (220\text{x}10^{-12})(10\text{x}10^{-6})$$

$$+0.667(24.7\text{x}10^{-4})(10\text{x}10^{-12}) = 18.7\text{fF}$$

Problem 7.1-10 – Continued

$$C_{bs9} = 560\text{x}10^{-6}(30\text{x}10^{-12})+350\text{x}10^{-12}(26\text{x}10^{-6}) = 25.9\text{fF}$$

(Assumed area=3µmx10µm = 30µm and perimeter is 3µm+10µm+3µm+10µm = 26µm)

$$C_{bd8} = 560\text{x}10^{-6}(438\text{x}10^{-12})+350\text{x}10^{-12}(298\text{x}10^{-6}) = 349\text{fF}$$

$$C_{gd8} = C_{ov} = (220\text{x}10^{-12})(146\text{x}10^{-6}) = 32.1\text{fF}$$

$\therefore\ C_1$ = 18.7fF + 25.9fF + 349fF + 32.1fF + 1000fF = 1.43pF

(We have ignored any reverse bias influence on pn junction capacitors.)

The dominant terms of a_0 , a_1, and a_2 based on these values are shown in boldface above.

$$\therefore \frac{V_o}{V_i} \approx \frac{g_{m9}(g_{m10}+ g_{\pi10}+ sC_{\pi10})}{g_{m9}g_{m10}+ g_{\pi10}G_2+s(G_2C_{\pi10}+g_{\pi10}C_2+g_{m10}C_1+g_{m9}C_2)+s^2C_2C_{\pi10}}$$

$$\frac{V_o}{V_i} = \frac{g_{m9}g_{m10}}{g_{m9}g_{m10}+ g_{\pi10}G_2}\left[\frac{1+\dfrac{sC_{\pi10}}{g_{m10}}}{1+s\left(\dfrac{G_2C_{\pi10}+g_{\pi10}C_2+g_{m10}C_1+g_{m9}C_2}{g_{m9}g_{m10}+ g_{\pi10}G_2}\right)+s^2\dfrac{C_2C_{\pi10}}{g_{m9}g_{m10}+ g_{\pi10}G_2}}\right]$$

Assuming negative real axis roots widely spaced gives,

$$p_1 = -\frac{1}{\text{a}} = \frac{-(g_{m9}g_{m10}+ g_{\pi10}G_2)}{G_2C_{\pi10}+g_{\pi10}C_2+g_{m10}C_1+g_{m9}C_2} = -\frac{1.235\text{x}10^{-5}}{1.465\ \text{x}10^{-13}} = \underline{\underline{-84.3\ \text{x}10^6\ \text{rads/sec.}}}$$

$$= -13.4\text{MHz}$$

$$p_2 = -\frac{\text{a}}{\text{b}} = \frac{-(G_2C_{\pi10}+g_{\pi10}C_2+g_{m10}C_1+g_{m9}C_2)}{C_2C_{\pi10}} = -\frac{1.465\ \text{x}10^{-13}}{100\text{x}10^{-12}\cdot 10\text{x}10^{-12}}$$

$$= \underline{\underline{-146.5\ \text{x}10^6\ \text{rads/sec.}}} \rightarrow -23.32\text{MHz}$$

$$z_1 = -\frac{g_{m10}}{C_{\pi10}} = -\frac{38.6\text{x}10^{-3}}{10\ \text{x}10^{-12}} = \underline{\underline{-3.86\ \text{x}10^9\ \text{rads/sec.}}} \rightarrow -614\text{MHz}$$

We see that neither p_1 or p_2 is greater than 10*GB* if *GB* = 5MHz so they will deteriorate the phase margin of the amplifier of Ex. 7.1-2.

Problem 7.1-11

Given the op amp in Fig. P7.1-11, find the quiescent currents flowing in the op amp, the small-signal voltage gain, ignoring any loading produced by the output stage and the small-signal output resistance. Assume K'_N = 25 μA/V^2 and K'_P = 10 μA/V^2 and λ = 0.04 V^{-1} for both types of MOSFETs. Assume the the BJT has a current gain of β_F = 100.

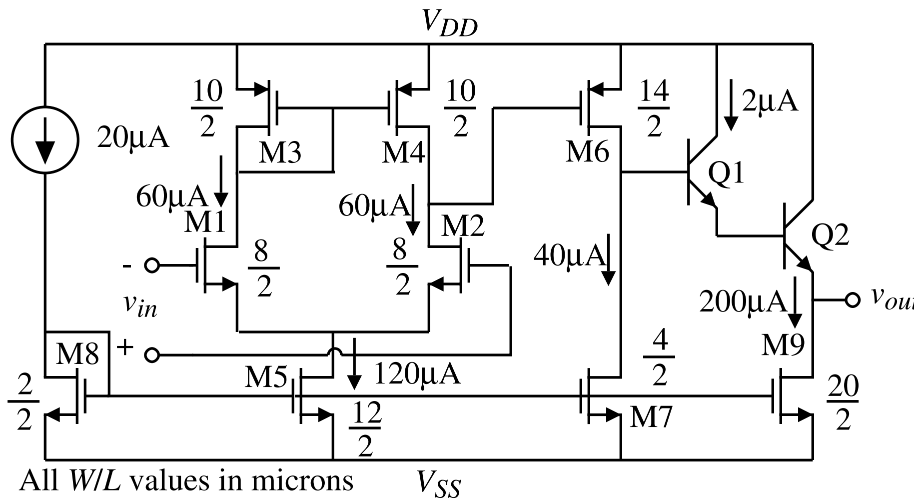


Figure P7.1-11 - Solution

Solution

The quiescent currents flowing in the op amp are shown on the above schematic.

The small-signal model parameters for the MOSFETs are:

$$g_{m1} = g_{m2} = \sqrt{2\cdot25\cdot4\cdot60} = 109.5\mu\text{S} \qquad \text{and } g_{m6} = \sqrt{2\cdot10\cdot7\cdot40} = 74.8\mu\text{S}$$

$$r_{ds2} = r_{ds4} = \frac{25\text{x}10^6}{60} = 0.4167\text{M}\Omega,\ r_{ds6} = r_{ds7} = \frac{25\text{x}10^6}{40} = 0.625\text{M}\Omega$$

and $r_{ds9} = \dfrac{25\text{x}10^6}{200} = 0.125\text{M}\Omega$ For the two BJT's, $g_{m1} = \dfrac{2\text{x}10^{-6}}{26\text{x}10^{-3}} = 7.7\mu\text{S}$,

$$r_{\pi1} = \frac{101}{7.7\mu\text{S}} = 1.308\text{M}\Omega,\quad g_{m2} = \frac{200\text{x}10^{-6}}{26\text{x}10^{-3}} = 7.7\text{mS} \quad \text{and } r_{\pi2} = \frac{101}{7.7\text{mS}} = 13.08\text{k}\Omega$$

The small-signal voltage gain is $A_v = g_{m1}R_I\, g_{m6}R_{II}\, A_{buff}$ where

$$R_I = 0.4167\text{M}\Omega||0.4167\text{M}\Omega\ 0.2083\text{M}\Omega \text{ and } R_{II} = 0.625\text{M}\Omega||0.615\text{M}\Omega = 0.3125\text{M}\Omega.$$

$$A_{buff} = \frac{(1+\beta_F)^2 r_{ds9}}{r_{\pi1}+(1+\beta_F)[r_{\pi2}+(1+\beta_F)r_{ds9}]} = \frac{101^2 0.125\text{M}\Omega}{1.3\text{M}\Omega+101[13.08\text{k}\Omega+101\cdot0.125\text{M}\Omega]} = 0.998$$

$$\therefore \qquad A_v = 109.5\mu\text{S}\cdot0.2083\text{M}\Omega\cdot74.8\mu\text{S}\cdot0.3125\text{M}\Omega\cdot0.998 = \underline{\underline{532.2\text{V/V}}}$$

$$R_{out} = r_{ds9}||\left[\frac{(r_{\pi1}+R_{II})/(1+\beta_F)+r_{\pi2}}{1+\beta_F}\right] = 0.125\text{M}\Omega||\left[\frac{(0.3125\text{M}\Omega+1.208\text{M}\Omega)/101+13.08\text{k}\Omega}{101}\right]$$

$$= 0.125\text{M}\Omega||288 = \underline{\underline{287.4\Omega}}$$

Problem 7.2-1

Find the GB of a two-stage op amp using Miller compensation using a nulling resistor that has 60° phase margin where the second pole is -10x10^6 rads/sec and two higher poles both at -100x10^6 rads/sec. Assume that the RHP zero is used to cancel the second pole and that the load capacitance stays constant. If the input transconductance is 500µA/V, what is the value of C_c?

Solution

The resulting higher-order poles are two at -100x10^6 radians/sec. The resulting phase margin expression is,

$$\text{PM} = 180° - \tan^{-1}(A_v(0)) - 2\tan^{-1}\left(\frac{GB}{10^7}\right) = 90° - 2\tan^{-1}\left(\frac{GB}{10^7}\right) = 60°$$

$$\therefore\ 30° = 2\tan^{-1}\left(\frac{GB}{10^7}\right) \rightarrow \left(\frac{GB}{10^7}\right) = \tan(15°) = 0.2679$$

$$GB = 2.679\text{x}10^7 = \frac{g_{m1}}{C_c} \rightarrow C_c = \frac{500\text{x}10^{-6}}{26.79\text{x}10^7} = \underline{\underline{18.66\text{pF}}}$$

Problem 7.2-02

For an op amp where the second pole is smaller than any larger poles by a factor of 10, we can set the second pole at $2.2GB$ to get 60° phase margin. Use the pole locations determined in Example 7.2-2 and find the constant multiplying GB if p_6 for 60° phase margin.

Solution

Referring to Example (7.2-2)

$$p_6 = -0.966 \text{ Grad/sec}$$
$$p_A = -1.346 \text{ Grad/sec}$$
$$p_B = -1.346 \text{ Grad/sec}$$
$$p_8 = -3.149 \text{ Grad/sec}$$
$$p_9 = -3.149 \text{ Grad/sec}$$
$$p_{10} = -3.5 \text{ Grad/sec}$$

For a phase margin of 60°, the contributions due to all the poles on the phase margin can be given as

$$\tan^{-1}\left(\frac{GB}{p_6}\right) + 2\tan^{-1}\left(\frac{GB}{p_A}\right) + 2\tan^{-1}\left(\frac{GB}{p_8}\right) + \tan^{-1}\left(\frac{GB}{p_{10}}\right) = 30°$$

Solving for the value of gain-bandwidth, we get

$$GB \cong 0.23p_6 = 35 \text{ MHz.}$$

Problem 7.2-03

What will be the phase margin of Ex. 7.2-2 if C_L = 10pF?

Solution

The value of the output resistance from Example (7.2-2) is

$$R_{out} = 19.4 \quad M\Omega$$

Thus, the dominant pole is

$$p_1 = \frac{-1}{R_{out}C_L} = 8.2 \quad \text{KHz.}$$

The gain-bandwidth is given by

$$GB = A_v(0)\,p_1 = (7464)(8.2K) = 61 \quad \text{MHz.}$$

Considering the location of the various poles from Example (7.2-2), the phase margin becomes

$$PM = 180^\circ - \left[90^\circ - \left\{\tan^{-1}\left(\frac{GB}{p_6}\right) + 2\tan^{-1}\left(\frac{GB}{p_A}\right) + 2\tan^{-1}\left(\frac{GB}{p_8}\right) + \tan^{-1}\left(\frac{GB}{p_{10}}\right)\right\}\right]$$

or, $$PM = 180^\circ - \left[90^\circ - \{21.7^\circ + 32^\circ + 14^\circ + 6.2^\circ\}\right]$$

or, $$\boxed{PM = 16^\circ}$$

Problem 7.2-04

Use the technique of Ex. 7.2-2 to extend the *GB* of the cascode op amp of Ex. 6.5-2 as much as possible that will maintain 60° phase margin. What is the minimum value of C_L for the maximum *GB*?

Solution

Assuming all channel lengths to be 1 μm, the total capacitance at the source of M7 is

$$C_7 = C_{gs7} + C_{bd7} + C_{gd6} + C_{bd6} \quad \rightarrow \quad C_7 = 75 + 51 + 9 + 51 = 186 \text{ fF}$$

$$g_{m7} = 707 \ \mu S$$

Thus, the pole at the source of M7 is

$$p_{S7} = -\frac{g_{m7}}{C_7} = -605 \text{ MHz.}$$

The total capacitance at the source of M12 is

$$C_{12} = C_{gs12} + C_{bd12} + C_{gd11} + C_{bd11} \quad \rightarrow \quad C_{12} = 34 + 29 + 4 + 29 = 96 \text{ fF}$$

$$g_{m12} = 707 \ \mu S$$

Thus, the pole at the source of M12 is

$$p_{S12} = -\frac{g_{m12}}{C_{12}} = -1170 \text{ MHz.}$$

The total capacitance at the drain of M4 is

$$C_4 = C_{gs4} + C_{gs6} + C_{bd4} + C_{gd2} + C_{bd2} \quad \rightarrow \quad C_4 = 43 + 75 + 21 + 3 + 19 = 161 \text{ fF}$$

$$g_{m4} = 283 \ \mu S$$

Thus, the pole at the drain of M4 is

$$p_{D4} = -\frac{g_{m4}}{C_4} = -280 \text{ MHz.}$$

The total capacitance at the drain of M8 is

$$C_8 = C_{gd8} + C_{bd8} + C_{gs10} + C_{gs12} \quad \rightarrow \quad C_8 = 9 + 51 + 34 + 34 = 128 \text{ fF}$$

$$R_2 + \frac{1}{g_{m10}} = 3.4 \ K\Omega$$

Thus, the pole at the drain of M8 is

$$p_{D8} = -\frac{1}{\left(R_2 + \frac{1}{g_{m10}}\right) C_8} = -366 \text{ MHz.}$$

For a phase margin of 60°, we have

$$PM = 180^\circ - \left[90^\circ - \left\{ \tan^{-1}\left(\frac{GB}{p_{S7}}\right) + \tan^{-1}\left(\frac{GB}{p_{S12}}\right) + \tan^{-1}\left(\frac{GB}{p_{D4}}\right) + \tan^{-1}\left(\frac{GB}{p_{D8}}\right) \right\} \right]$$

Solving the above equation

$$GB \cong 65 \text{ MHz} \quad \text{and} \quad A_v = 6925 \text{ V/V}$$

Thus, $p_1 = 9.39$ KHz, and $C_L \geq \underline{\underline{1.54 \text{ pF}}}$

Problem 7.2-05

For the voltage amplifier using a current mirror shown in Fig. 7.2-11, design the currents in M1, M2, M5 and M6 and the W/L ratios to give an output resistance which is at least 1MΩ and an input resistance which is less than 1kΩ. (This would allow a voltage gain of -10 to be achieved using R_1 = 10kΩ and R_2 = 1MΩ.

Solution

$$R_{out} = \frac{1}{(g_{ds6} + g_{ds2})}$$

Let, $I_2 = I_6 = 10\ \mu A$

or, $R_{out} = \dfrac{1}{(g_{ds6} + g_{ds2})} = 1.1\ M\Omega$

Given, $R_1 = 10\ K\Omega$, $R_2 = 1000\ K\Omega$, and $A_v = -10$

And, $A_v = -\dfrac{R_2 A_0}{R_1(1 + A_0)}$

Thus, $A_0 = \dfrac{I_2}{I_1} = \dfrac{1}{9}$

or, $I_2 = I_6 = 10\ \mu A$ and $I_1 = I_5 = 90\ \mu A$

$$R_{in} = \frac{1}{g_{m1}} = 1\ K\Omega$$

or, $\boxed{\left(\dfrac{W}{L}\right)_1 = 50.5}$, and $\boxed{\left(\dfrac{W}{L}\right)_2 = 5.6}$

and, $\boxed{\left(\dfrac{W}{L}\right)_5 = 50.5}$, and $\boxed{\left(\dfrac{W}{L}\right)_6 = 5.6}$

Problem 7.2-06

In Ex. 7.2-3, calculate the value of the input pole of the current amplifier and compare with the magnitude of the output pole.

Solution

Assuming all channel lengths to be 1 μm .

In this problem, $A_0 = 0.1$, $S_2 = 20$, $S_1 = 200$, $I_2 = 100 \ \mu A$, and $I_1 = 1000 \ \mu A$

$$g_{m1} = 6.63 \ mS$$

Thus, $R_{in} = R_3 + \dfrac{1}{g_{m1}} = 451 \ \Omega$

The input capacitance is

$$C_{in} = C_{gd5} + C_{bd5} + C_{gs3} + C_{gs4} + C_{gd3} + C_{gd4}$$

or, $C_{in} = 44 + 253 + 375 + 38 + 44 + 4.4 = 758$ fF

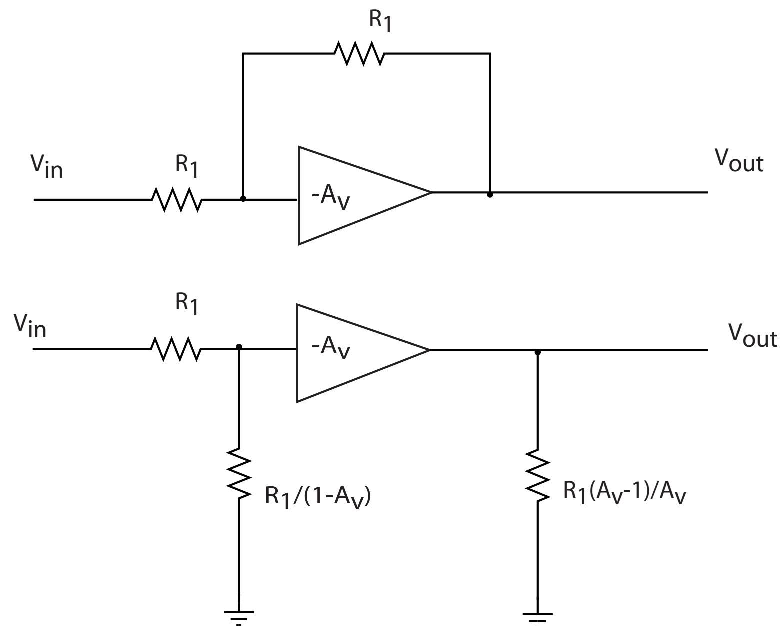
The input pole is given by

$p_{in} = -\dfrac{1}{R_{in}C_{in}} = -466$ MHz which is compared to 50 MHz for the output pole.

Problem 7.2-07

Add a second input to the voltage amplifier of Fig. 7.2-12 using another R_1 resistor connected from this input to the input of the current amplifier. Using the configuration of Fig. P7.2-7, calculate the input resistance, output resistance, and -3dB frequency of this circuit. Assume the values for Fig. 7.2-12 as developed in Ex. 7.2-3 but let the two R_1 resistors each be 1000Ω.

Solution



Referring to the figure, the Miller resistance, R_1 , between the input and the output can be broken as shown.

Here, $R_1 = 1\ K\Omega$, $R_2 = 110\ K\Omega$, and $R_3 = 0.3\ K\Omega$

The input resistance can be written as

$$R_{in} = R_1 + \left[\frac{R_1}{1-A_v}\right] \| \left[\left(R_3 + \frac{1}{g_{m1}}\right)\right] \quad \rightarrow \quad R_{in} = 1K + \left[\frac{1K}{1+10}\right] \| \left[\left(300 + \frac{1}{6.63m}\right)\right]$$

or, R_{in} = 1076 Ω

The output resistance can be written as

$$R_{out} = \frac{1}{g_{m12}} \| \frac{R_1(A_v - 1)}{A_v} \quad \rightarrow \quad R_{out} = 636\ \Omega$$

The –3 dB frequency, the pole created at the drains of M4 and M6, is given by

$$f_{-3dB} = \frac{1}{2\pi R_2 C_o}$$

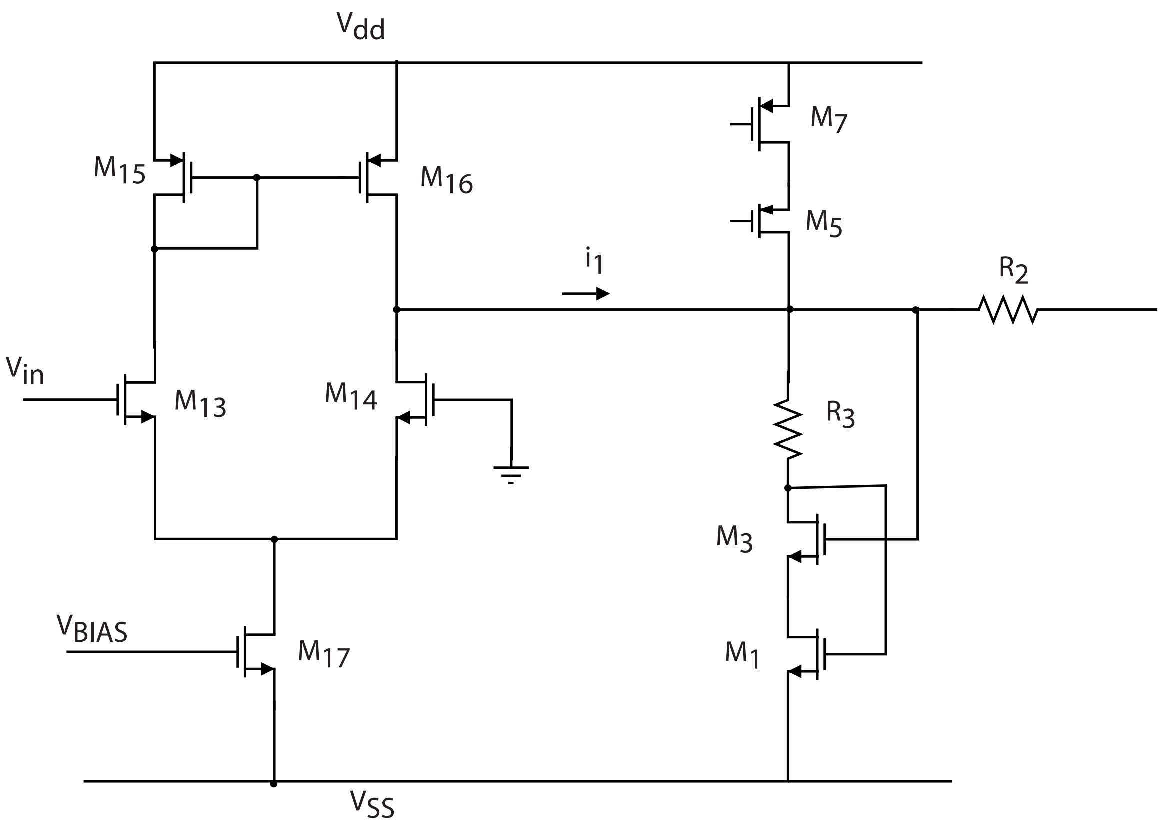
where, $R_2 = 110\ K\Omega$, and $C_o = 105$ pF.

So, $f_{\text{-3dB}}$ = 13.87 MHz.

Problem 7.2-08

Replace R_1 in Fig. 7.2-12 with a differential amplifier using a current mirror load. Design the differential transconductance, g_m, so that it is equal to $1/R_1$.

Solution



Referring to the figure, the output current of the input transconductor, i_1 , is given by

$$i_1 = g_{m13} v_{in}$$

Comparing with the expression $i_1 = \dfrac{v_{in}}{R_1}$, we get

$$R_1 = \frac{1}{g_{m13}}$$

Problem 7.3-01

Compare the differential output op amps of Fig. 7.3-3, 7.3-5, 7.3-6, 7.3-7, 7.3-8 and 7.3-10 from the viewpoint of (a.) noise, (b.) *PSRR*, (c.) *ICMR* [V_{ic}(max) and V_{ic}(min)], (d.) *OCMR* [V_o)max) and V_o(min)], (e.) *SR* assuming all input differential currents are identical, and (f.) power dissipation if all current of the input differential amplifiers are identical and power supplies are equal.

Solution

Assume that all differential amplifiers have the same bias current of I_{SS}.

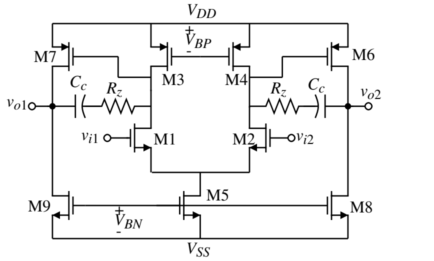


Figure 7.3-3 Two-stage, Miller, differential-in, differential-out op amp.

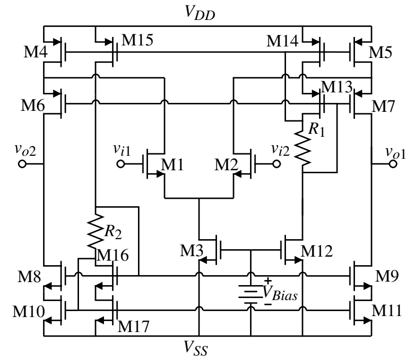


Figure 7.3-5 Differential output, folded-cascode op amp.

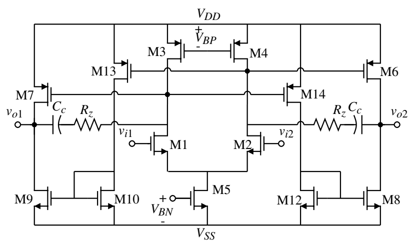


Figure 7.3-6 Two-stage, Miller, differential-in, differential-out op amp with a push-pull output stage.

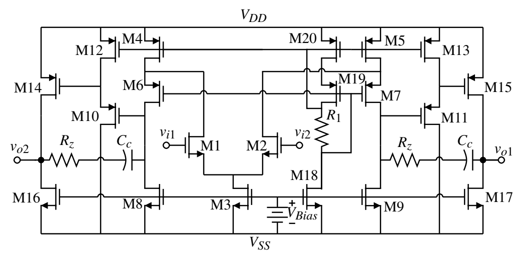


Figure 7.3-7 Two-stage, differential output, folded-cascode op amp.

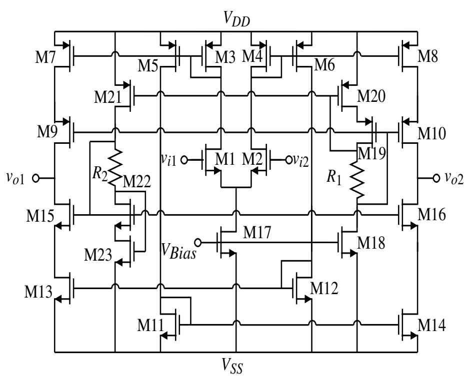


Figure 7.3-8 Unfolded cascode op amp with differential-outputs.

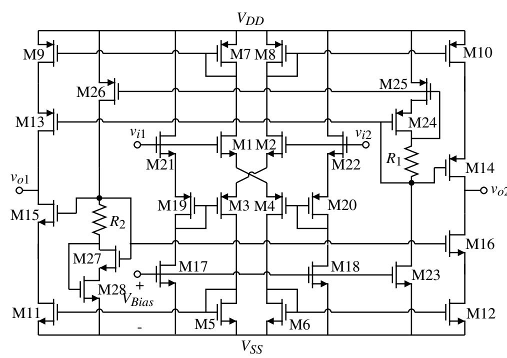


Figure 7.3-10 Class AB, differential output op amp using a cross-coupled differential input stage.

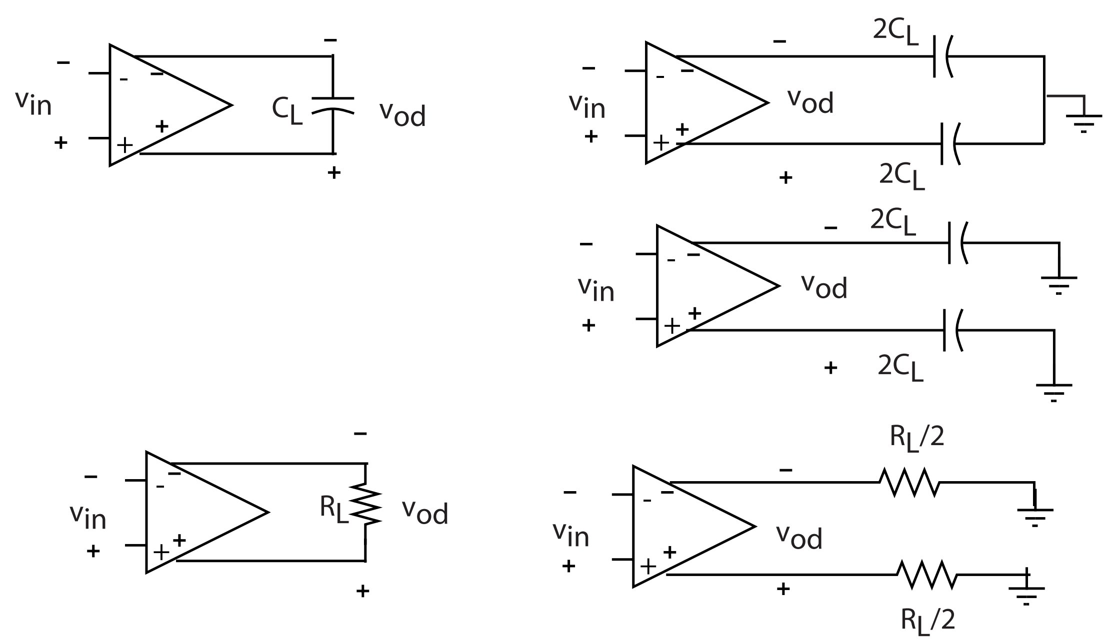
Problem 7.3-01 – Continued

	Fig. 7.3-3	Fig. 7.3-5	Fig. 7.3-6	Fig. 7.3-7	Fig. 7.3-8	Fig. 7.3-10
Noise	Good	Poor	Good	Poor	Okay	Poor
PSRR	Poor	Good	Poor	Good	Good	Good
ICMR V_{ic}(max) V_{ic}(min)	V_{DD}-V_{ON} V_{SS}+ $2V_{ON}$+V_T	V_{DD}+V_T V_{SS}+ $2V_{ON}$+V_T	V_{DD}-V_{ON} V_{SS}+ $2V_{ON}$+V_T	V_{DD}+V_T V_{SS}+ $2V_{ON}$+V_T	V_{DD}-V_{ON} V_{SS}+ $2V_{ON}$+V_T	V_{DD}-V_{ON} V_{SS}+ $3V_{ON}$+$2V_T$
OCMR V_o(max) V_o(min)	V_{DD}-V_{ON} V_{SS}+V_{ON}	V_{DD}-$2V_{ON}$ V_{SS}+$2V_{ON}$	V_{DD}-V_{ON} V_{SS}+V_{ON}	V_{DD}-V_{ON} V_{SS}+V_{ON}	V_{DD}-$2V_{ON}$ V_{SS}+$2V_{ON}$	V_{DD}-$2V_{ON}$ V_{SS}+$2V_{ON}$
SR	I_{SS}/C_c	I_{SS}/C_L	I_{SS}/C_c	I_{SS}/C_L	I_{SS}/C_L	I_{SS}/C_L

Problem 7.3-02

Prove that the load seen by the differential outputs of the op amps in Fig. 7.3-4 are identical. What would be the single-ended equivalent loads if C_L was replaced with a resistor, R_L?

Solution



Referring to the figure, when a capacitive load of C_L is driven differentially, the load capacitor can be broken into two capacitors in series, each with a magnitude of $2C_L$. The mid point of the connection of these two capacitors is ac ground as the output signal swings differentially. In case of a resistive load R_L, it can be broken into two resistive loads in series, each resistor being $R_L / 2$.

Problem 7.3-03

Two differential output op amps are shown in Fig. P7.3-3. (a.) Show how to compensate these op amps. (b.) If all dc currents through all transistors is 50μA and all W/L values are 10μm/1μm, use the parameters of Table 3.1-2 and find the differential-in, differential-out small-signal voltage gain.

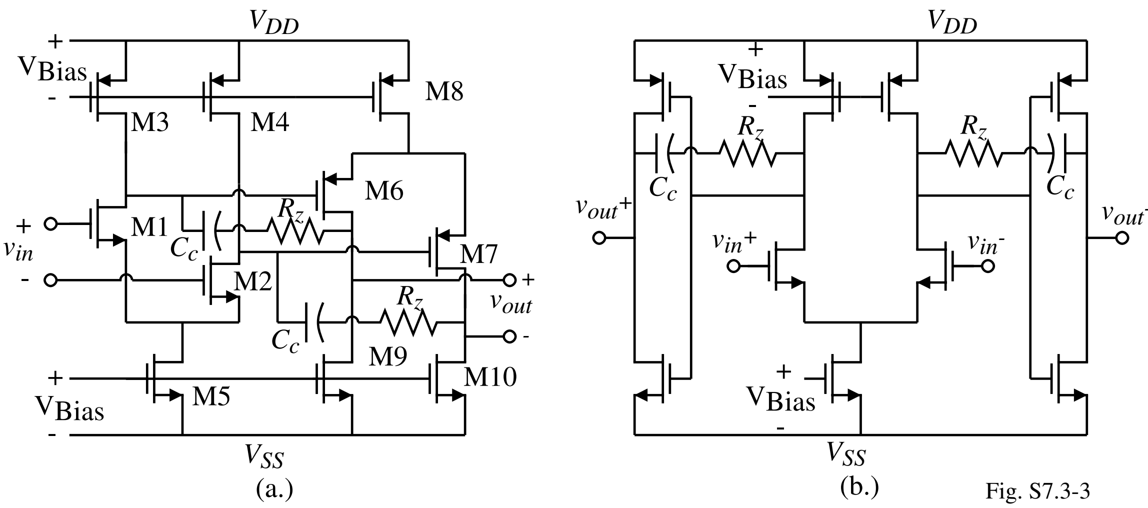


Fig. S7.3-3

Solution

a) The compensation of both the op amps are shown in the figure.

b) The small-signal voltage gain of Figure P7.3-3(a) is given by

$$A_v = \frac{g_{m1} g_{m6}}{(g_{ds1}+g_{ds3})(g_{ds6}+g_{ds9})}$$

or, $$A_v = \frac{(332\mu)(224\mu)}{(4.5\mu)(4.5\mu)}$$

or, A_v = 3673 V/V

The small-signal voltage gain of Figure P7.3-3(b) is given by

$$A_v = \frac{g_{m1}(g_{m6}+g_{m9})}{(g_{ds1}+g_{ds3})(g_{ds6}+g_{ds9})}$$

or, $$A_v = \frac{(332\mu)(556\mu)}{(4.5\mu)(4.5\mu)}$$

or, A_v = 9117 V/V

Problem 7.3-04

Comparatively evaluate the performance of the two differential output op amps of Fig. P7.3-3 with the differential output op amps of Fig. 7.3-3, 7.3-5, 7.3-6, 7.3-7, 7.3-8 and 7.3-10. Include the differential-in, differential-out voltage gain, the noise, and the *PSRR*.

Solution

TBD

Problem 7.3-05

Fig. P7.3-5 shows a differential-in, differential-out op amp. Develop an expression for the small-signal, differential-in, differential-out voltage gain and the small-signal output resistance.

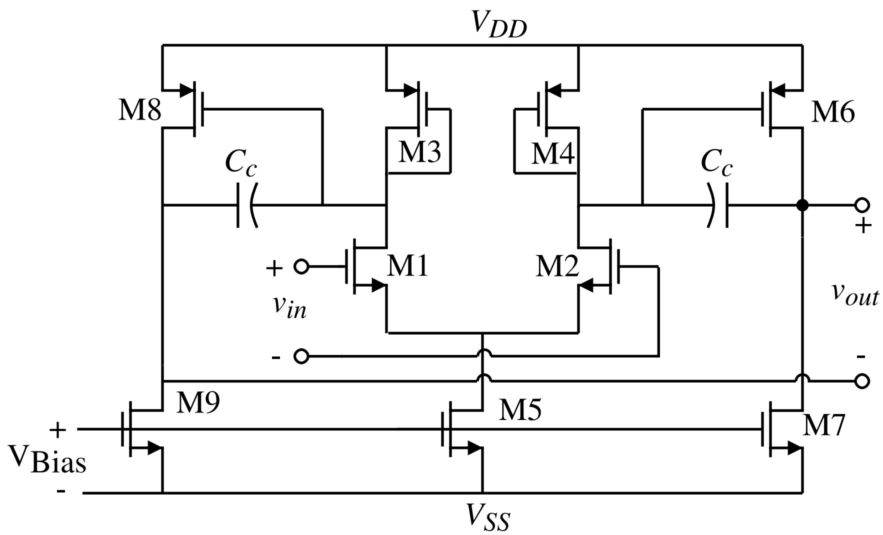


Figure P7.3-5

Solution

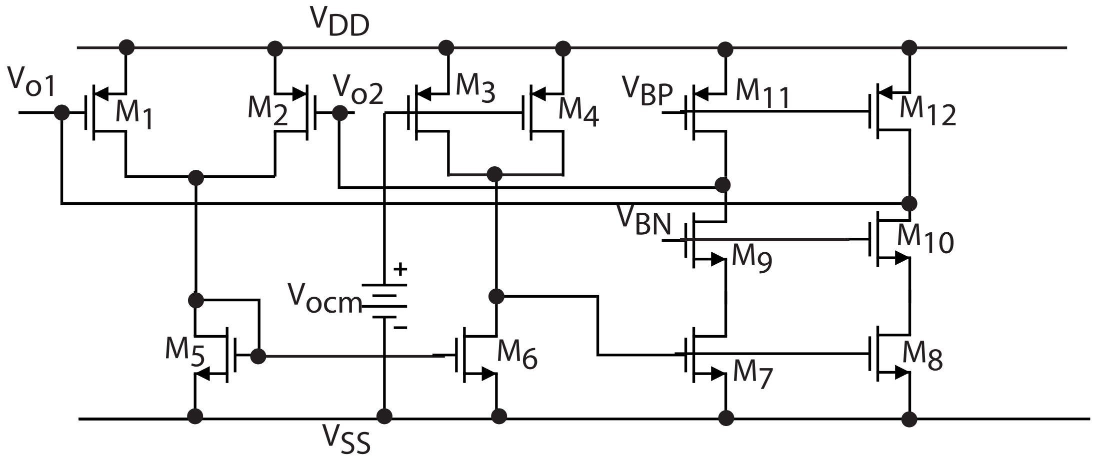
The small-signal differential voltage gain can be found by simply connecting the sources of M1 and M2 to ac ground and solving for the single-ended output assuming the full input is applied single-ended.

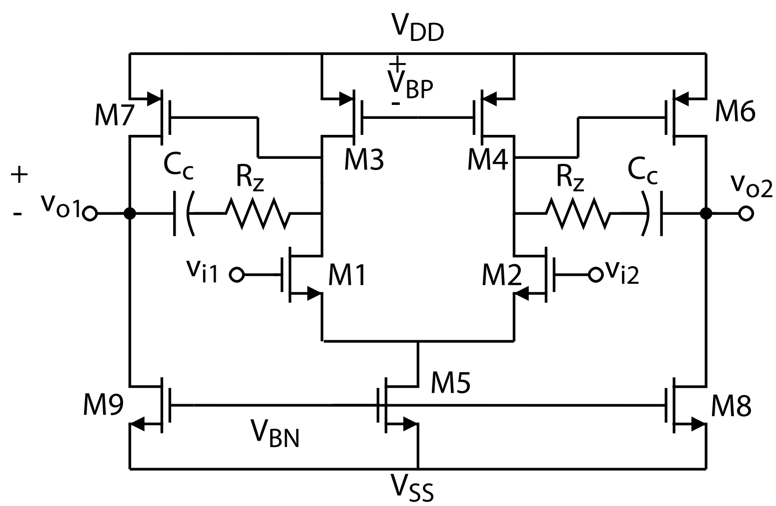
$$\therefore \qquad A_{vdd} = \frac{g_{m1}}{g_{m3}}\left(\frac{g_{m8}}{g_{ds8}+g_{ds9}}\right) \qquad\qquad R_{out} = \left(\frac{1}{g_{ds8}+g_{ds9}} + \frac{1}{g_{ds6}+g_{ds7}}\right)$$

Problem 7.3-06

Use the common-mode output stabilization circuit of Fig. 7.3-13 to stabilize the differential output op amp of Fig. 7.3-3 to ground assuming that the power supplies are split around ground ($V_{DD} = |V_{SS}|$). Design a correction circuit that will function properly.

Solution





Referring to the figure of the common-mode stabilizing circuit, the common-mode voltage at the output nodes v_{o1} and v_{o2} will be held close to the common-mode voltage V_{ocm} due to negative feedback. If these two output nodes swing differential, the drain of M5 will not change and thus, the common-mode feedback circuit is non-functional. When the common-mode voltage at these two output nodes tend to change in the same direction, the negative feedback loop of M1-M5-M6-M7-M9 and M2-M5-M6-M8-M10 will reduce the variations at v_{o1} and v_{o2}, respectively.

Problem 7.3-07

(a.) If all transistors in Fig. 7.3-12 have a dc current of 50µA and a *W/L* of 10µm/1µm, find the gain of the common mode feedback loop. (b.) If the output of this amplifier is cascoded, then repeat part (a.).

Solution

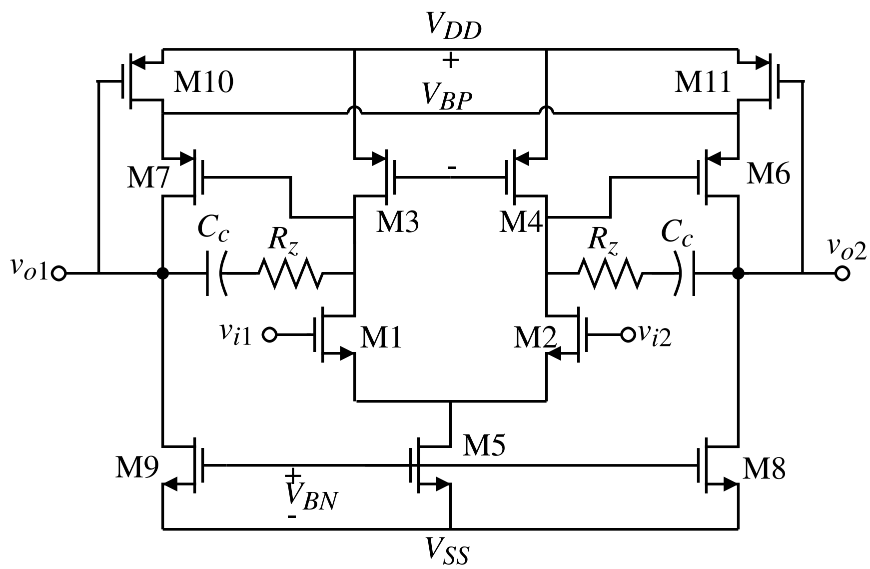


Figure 7.3-12 Two-stage, Miller, differential-in, differential-out op amp with common-mode stabilization.

The loop gain of the common-mode feedback loop is,

$$\text{CMFB Loop gain} \approx -\frac{g_{m10}}{g_{ds9}} = -g_{m10}r_{ds9} \quad \text{or} \quad -\frac{g_{m11}}{g_{ds8}} = -g_{m11}r_{ds8}$$

With I_D = 50µA and W/L = 10µm/1µm, $g_{m10} = \sqrt{\frac{2K_P'WI_D}{L}} = \sqrt{2\cdot 50\cdot 10\cdot 50)}$
= 223.6µS,

$$r_{dsN} = \frac{1}{\lambda_N I_D} = \frac{25}{50\mu\text{A}} = 0.5\text{M}\Omega \qquad \text{and} \qquad r_{dsP} = \frac{1}{\lambda_P I_D} = \frac{20}{50\mu\text{A}} = 0.4\text{M}\Omega$$

$$\therefore \qquad \boxed{\text{CMFB Loop gain} \approx -g_{m10}r_{ds9} = -223.6(0.5) = -111.8\text{V/V}}$$

If the output is cascoded, the gain becomes,

$$\text{CMFB Loop gain with cascoding} \approx -\frac{g_{m10}}{g_{ds9}}\; g_m(\text{cascode})r_{ds}(\text{cascode})$$

$$= -g_{m10}\{[r_{ds9}\, g_m(\text{cascode})r_{ds}(\text{cascode})]||[g_{m7}r_{ds7}\,(r_{ds10}||r_{ds10}]\}$$

$$g_{mP} = \sqrt{\frac{2K_N'WI_D}{L}} = \sqrt{2\cdot 110\cdot 10\cdot 50)} = 331.67\mu\text{S}$$

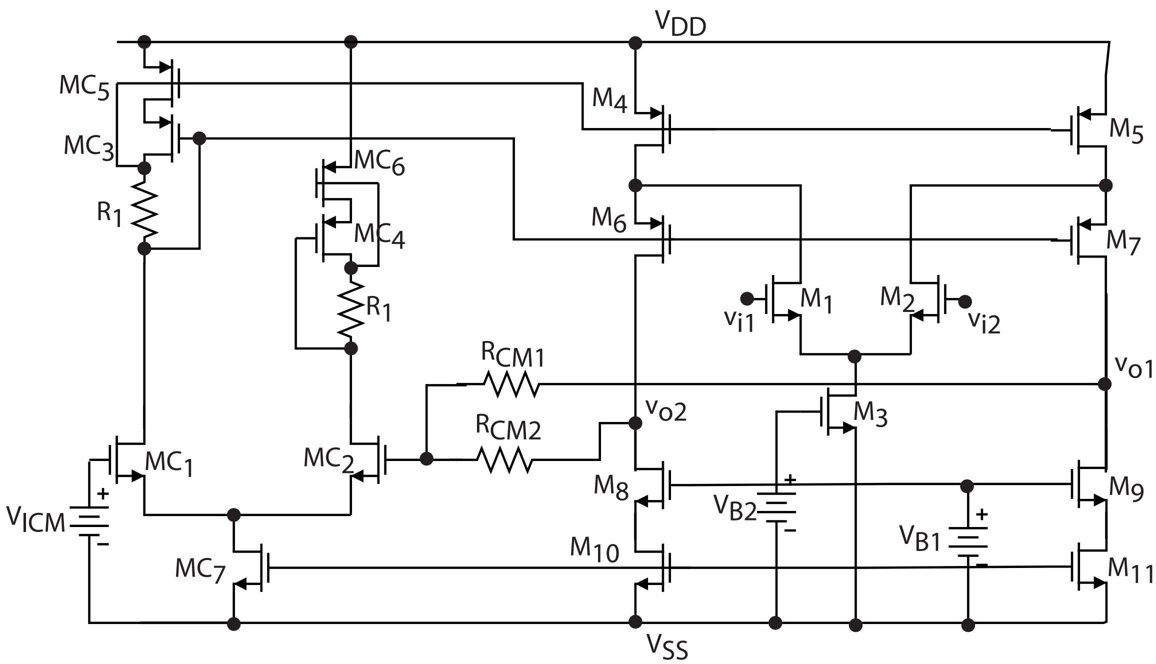
$$= -(223.6)[(0.5\cdot 331.67\cdot 0.5)||(223.6)(0.4)(0.2)] = 223.6(14.7) = -3{,}290 \text{ V/V}$$

$$\therefore \qquad \boxed{\text{CMFB Loop gain with cascoding} \approx -3.290\text{V/V}}$$

Problem 7.3-08

Show how to use the common feedback circuit of Fig. 5.2-15 to stabilize the common mode output voltage of Fig. 7.3-5. What would be the approximate gain of the common mode feedback loop (in terms of g_m and r_{ds}) and how would you compensate the common mode feedback loop?

Solution



Referring to the figure, the loop gain of the common-mode feedback loop can be given by

$$\boxed{|LG| = \frac{g_{m,C2}g_{m4}}{2g_{m,C5}\left\{\dfrac{g_{ds4}g_{ds6}}{g_{m4}} + \dfrac{g_{ds8}g_{ds10}}{g_{m10}}\right\}}}$$

The compensation of the common-mode feedback loop can be done using the output load capacitor (single-ended load capacitors to ac ground). The dominant pole of this loop would be caused at the output nodes by the large output resistance given by

$$R_{out} = \frac{1}{\left\{\dfrac{g_{ds4}g_{ds6}}{g_{m4}} + \dfrac{g_{ds8}g_{ds10}}{g_{m10}}\right\}}$$

Considering the differential output load capacitance to be C_L , the dominant pole of the common-mode feedback loop can be expressed as

$$p_1 = \frac{1}{R_{out}(2C_L)}$$

The other poles, at the source and drain of MC3, and the source of M6, can be assumed to be large as these nodes are low impedance nodes.

Problem 7.4-01

Calculate the gain, GB, SR and P_{diss} for the folded cascode op amp of Fig. 6.5-7b if V_{DD} = $-V_{SS}$ = 1.5V, the current in the differential amplifier pair is 50nA each and the current in the sources, M4 and M5, is 150nA. Assume the transistors are all 10µm/1µm, the load capacitor is 2pF and that n_1 is 2.5 for NMOS and 1.5 for PMOS.

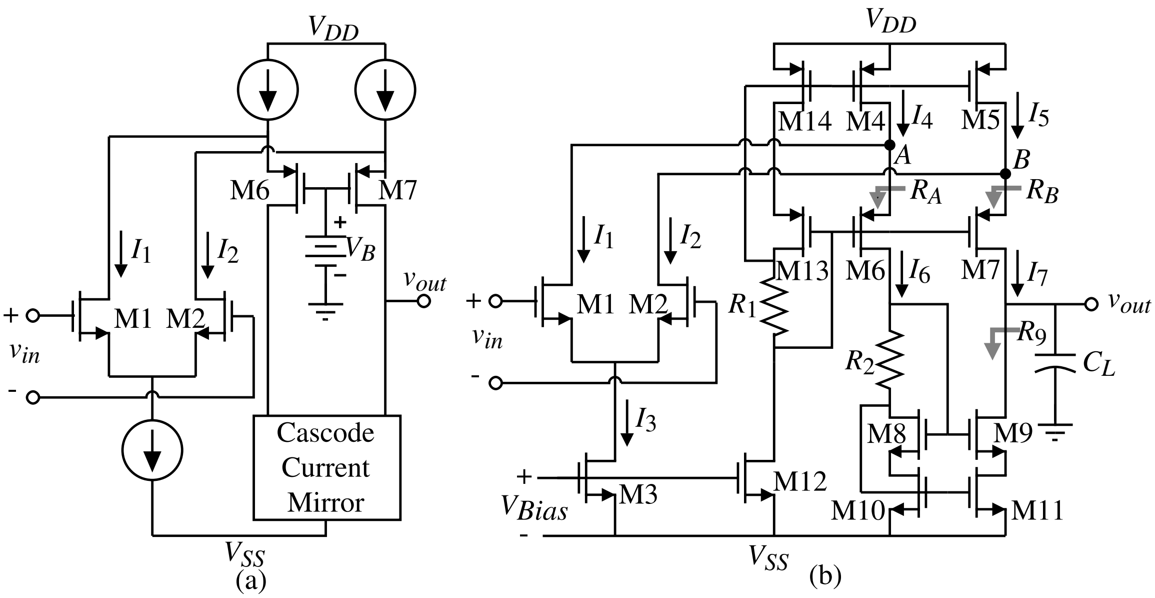


Figure 6.5-7 (a) Simplified version of an N-channel input, folded cascode op amp. (b) Practical version (a).

Solution

$$g_{m1} = g_{m2} = \frac{I_D}{n_1(kT/q)} = \frac{50\text{nA}}{2.5\cdot 25.9\text{mV}} = 0.772\mu\text{S} \quad \text{and } r_{ds1} = r_{ds2} = \frac{1}{I_D\lambda_N} = 500\text{M}\Omega$$

$$g_{m4} = g_{m5} = \frac{I_D}{n_1(kT/q)} = \frac{150\text{nA}}{1.5\cdot 25.9\text{mV}} = 3.861\mu\text{S} \quad \text{and } r_{ds4} = r_{ds5} = \frac{1}{I_D\lambda_N} = 133\text{M}\Omega$$

$$g_{m6} = g_{m7} = \frac{I_D}{n_1(kT/q)} = \frac{100\text{nA}}{1.5\cdot 25.9\text{mV}} = 2.574\mu\text{S} \quad \text{and } r_{ds6} = r_{ds5} = \frac{1}{I_D\lambda_N} = 200\text{M}\Omega$$

$$g_{m8} = g_{m9} = g_{m10} = g_{m11} = \frac{I_D}{n_1(kT/q)} = \frac{100\text{nA}}{2.5\cdot 25.9\text{mV}} = 1.544\mu\text{S}$$

and $r_{ds8} = r_{ds9} = r_{ds10} = r_{ds11} = \dfrac{1}{I_D\lambda_N} = 250\text{M}\Omega$

Gain: $A_v(0) = g_{m1}R_{out}$,

$$R_{out} \approx r_{ds11}g_{m9}r_{ds9}||[g_{m7}r_{ds7}(r_{ds5}||r_{ds2})] = 96.5\text{G}\Omega||34.23\text{G}\Omega = 25.269\text{G}\Omega$$

$\therefore \quad A_v(0) = 0.772\mu\text{S}\cdot 25.269\text{G}\Omega = \underline{\underline{19{,}508\ \text{V/V}}}$

$GB = g_{m1}/C_L = 386\text{krads/sec} = \underline{\underline{61.43\text{kHz}}}$ (this assumes all other poles are greater than GB which is the case if C_L makes R_B approximately the same as R_A at $\omega = GB$.)

$SR = 100\text{nA}/2\text{pF} = \underline{\underline{0.05\text{V}/\mu\text{s}}}$ $\qquad P_{diss} = 3\text{V}\cdot(3\cdot 150\text{nA}) = \underline{\underline{1.35\mu\text{W}}}$

Problem 7.4-02

Calculate the gain, GB, SR and P_{diss} for the op amp of Fig. 7.4-3 where I_5 = 100nA, all transistor widths (M1-M11) are 10µm and lengths 1µm, and $V_{DD} = -V_{SS}$ = 1.5V. If the saturation voltage is 0.1V, design the W/L values of M12-M15 that achieves maximum and minimum output swing assuming the transistors M12 and M15 have 50nA. Assume that I_{DO} = 2nA, n_p = 1.5, n_n = 2.5 and V_t = 25mV.

Solution

(Solution incomplete)

The small-signal gain can be expressed as

$$A_v = \frac{g_{m1}}{2g_{m3}}\left[\left(\frac{g_{m8}}{g_{m9}}\right)g_{m7} + g_{m6}\right]R_{out}$$

or, $A_v = g_{m1}R_{out}$

The output resistance is given by

$$R_{out} = \left[\frac{g_{m10}}{g_{ds10}g_{ds6}}\right] \| \left[\frac{g_{m11}}{g_{ds11}g_{ds7}}\right]$$

or, $R_{out} = 96\ G\Omega$

Thus,

$$A_v = g_{m1}R_{out} = 73{,}846\ \text{V/V}$$

Assuming $C_c = 1\ \text{pF}$

The dominant pole is

$$p_1 = -\frac{1}{R_{out}C_c} = 1.66\ \text{Hz.}$$

Thus, the gain-bandwidth becomes

$$GB = A_v(0)p_1 = 122.5\ \text{KHz.}$$

The power dissipation is 0.9 μW.

$$V_{SG10} = V_{dsat6} + V_{dsat10} + n_p V_t \ln\left(\frac{I_{10}}{(W/L)_{10} I_{D0}}\right) = 0.236\ \text{V}$$

$$V_{GS11} = V_{dsat7} + V_{dsat11} + n_n V_t \ln\left(\frac{I_{11}}{(W/L)_{11} I_{D0}}\right) = 0.26\ \text{V}$$

Problem 7.4-03

Derive Eq. (17). If A = 2, at what value of v_{in}/nV_t will $i_{out} = 5I_5$ or $5I_b$ if b=1 ?

Solution

Start with the following relationships:

$$i_1 + i_2 = I_5 + A(i_2 - i_1) \qquad \text{Eq. (15)}$$

and $$\frac{i_2}{i_1} = \exp\left(\frac{v_{in}}{nV_t}\right) \qquad \text{Eq. (16)}$$

Defining $i_{out} = b(i_2 - i_1)$ solve for i_2 and I_1.

$$i_1 + i_1 \exp\left(\frac{v_{in}}{nV_t}\right) = I_5 + Ai_1 \exp\left(\frac{v_{in}}{nV_t}\right) - Ai_1$$

or $$i_1[(1+A) + (1-A) \exp\left(\frac{v_{in}}{nV_t}\right)] = I_5 \qquad \rightarrow \qquad i_1 = \frac{I_5}{(1+A) + (1-A) \exp\left(\frac{v_{in}}{nV_t}\right)}$$

Similarly for i_2,

$$i_1 = \frac{I_5 \exp\left(\frac{v_{in}}{nV_t}\right)}{(1+A) + (1-A) \exp\left(\frac{v_{in}}{nV_t}\right)}$$

$$\therefore \qquad i_{out} = b(i_2 - I_1) = i_{out} = (i_2 - I_1) = \frac{I_5 \left(\exp\left(\frac{v_{in}}{nV_t}\right) - 1\right)}{(1+A) + (1-A) \exp\left(\frac{v_{in}}{nV_t}\right)} \qquad \text{Eq.}$$

(17)

Setting $i_{out} = 5I_5$ and solving for $\frac{v_{in}}{nV_t}$ gives,

$$5[3 - \exp\left(\frac{v_{in}}{nV_t}\right)] = \exp\left(\frac{v_{in}}{nV_t}\right) - 1 \qquad \rightarrow \qquad 16 = 6 \exp\left(\frac{v_{in}}{nV_t}\right) \qquad \rightarrow \qquad \exp\left(\frac{v_{in}}{nV_t}\right) = 2.667$$

$$\therefore \qquad \frac{v_{in}}{nV_t} = \ln(2.667) = \underline{\underline{0.9808}}$$

Problem 7.4-04

Design the current boosting mirror of Fig. 7.4-6a to achieve 100µA output when M2 is saturated. Assume that i_1 = 10µA and W_1/L_1 = 10. Find W_2/L_2 and the value of V_{DS2} where i_2 = 10µA.

Solution

Given, S_1 =10, I_1 = 10 µA, and I_1 = 100 µA when M2 is saturated. Thus,

$$\boxed{S_2 = 100}$$

And, $V_{dsat1} = V_{dsat2} = 0.135$ V

Now, in the active region of operation for M2

$$I_D = K_N^{'} S_2 \left[V_{dsat2} V_{ds} - \frac{V_{ds}^2}{2} \right]$$

or, $$10\mu = (100\mu)100\left[0.135V_{ds} - \frac{V_{ds}^2}{2}\right]$$

or, $$\boxed{V_{ds} \cong 7mV}$$

Problem 7.4-05

In the op amp of Fig. 7.4-7, the current boosting idea illustrated in Fig. 7.4-6 suffers from the problem that as the gate of M15 or M16 is increased to achieve current boosting, the gate-source drop of these transistors increases and prevents the v_{DS} of the boosting transistor (M11 and M12) from reaching saturation. Show how to solve this problem and confirm your solution with simulation.

Solution

TBD

Problem 7.5-01

For the transistor amplifier in Fig. P7.5-1, what is the equivalent input-noise voltage due to thermal noise? Assume the transistor has a dc drain current of 20 μA, W/L = 150 μm/10 μm, K'_N = 25 μA/V^2, and R_D is 100 Kilohms.

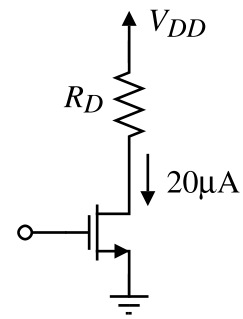


Figure P7.5-1

Solution

$$g_m = 122 \quad \mu S$$

and, $A_v \cong -g_m R_D = -12.2$

The equivalent input thermal noise is

$$e_{eq}^2 = \frac{8KT}{3g_m} + \frac{4KTR_D}{A_v^2}$$

or, $e_{eq}^2 = 102.1\times10^{-18} \quad V^2/Hz$

or, $V_{eq}(rms) \approx \underline{\underline{10\text{nV}/\sqrt{\text{Hz}}}}$

Problem 7.5-02

Repeat Ex. 7.5-1 with $W_1 = W_2$ = 500µm and $L_1 = L_2$ = 0.5µm to decrease the noise by a factor of 10.

Solution

$S_1 = 500/0.5$, $S_3 = 100/20$

Flicker noise

$$B_N = 7.36\times10^{-22} \ (Vm)^2 \qquad \text{and} \qquad B_P = 2.02\times10^{-22} \ (Vm)^2$$

$$e_{n1}^2 = \frac{B_P}{fW_1L_1} = \frac{8.08\times10^{-13}}{f} \ V^2/Hz$$

So, $$e_{eq}^2 = 2e_{n1}^2\left[1+\left(\frac{K'_N B_N}{K'_P B_P}\right)\left(\frac{L_1}{L_3}\right)^2\right] \quad \rightarrow \quad e_{eq}^2 = \frac{1.624\times10^{-12}}{f} \ V^2/Hz$$

Thermal noise

$$e_{n1}^2 = \frac{8KT}{3g_{m1}} = 0.49\times10^{-17} \ V^2/Hz$$

$$e_{eq}^2 = 2e_{n1}^2\left[1+\sqrt{\frac{K'_N W_3 L_1}{K'_P W_1 L_3}}\right] \quad \rightarrow \quad e_{eq}^2 = 1.08\times10^{-17} \ V^2/Hz$$

The corner frequency, $f_c = 150.4$ KHz

Considering a 100 KHz. Bandwidth

$$V_{eq}^2(rms) = 1.624\times10^{-12}\ln\left(10^5\right) + 1.08\times10^{-17}\left(10^5\right) \quad \rightarrow \quad V_{eq}(rms) = 4.45 \quad \mu V$$

Problem 7.5-03

Interchange all n-channel and p-channel transistors in Fig. 7.5-1 and using the W/L values designed in Example 7.5-1, find the input equivalent 1/*f* noise, the input equivalent thermal noise, the noise corner frequency and the *rms* noise in a 1Hz to 100kHz bandwidth.

Solution

The flicker noise is

$$B_N = 7.36\times10^{-22}\ (Vm)^2 \quad \text{and} \quad B_P = 2.02\times10^{-22}\ (Vm)^2$$

$$e_{n1}^2 = \frac{B_N}{fW_1L_1} = \frac{7.36\times10^{-12}}{f}\ V^2/Hz$$

So,
$$e_{eq}^2 = 2e_{n1}^2\left[1+\left(\frac{K'_PB_P}{K'_NB_N}\right)\left(\frac{L_1}{L_3}\right)^2\right] \rightarrow \quad e_{eq}^2 = \frac{14.72\times10^{-12}}{f}\ V^2/Hz$$

The thermal noise is

$$e_{n1}^2 = \frac{8KT}{3g_{m1}} = 1.05\times10^{-17}\ V^2/Hz$$

$$e_{eq}^2 = 2e_{n1}^2\left[1+\sqrt{\frac{K'_PW_3L_1}{K'_NW_1L_3}}\right] \rightarrow \quad e_{eq}^2 = \underline{2.42\text{x}10\text{-}17\ \text{V}^2/\text{Hz}}$$

The corner frequency is f_c = 608 KHz.

Considering a 100 KHz. Bandwidth

$$V_{eq}^2\ (rms) = 14.72\text{x}10^{-12}\ ln(10^5) + 2.42\text{x}10^{-17}\ ln(10^5) \rightarrow V_{eq}(rms) = \underline{13.1\ \text{nV}/\sqrt{\text{Hz}}}$$

Problem 7.5-04

Find the input equivalent *rms* noise voltage of the op amp designed in Ex. 6.3-1 of a bandwidth of 1Hz to 100kHz.

Solution

The input referred noise is given by

$$e_{eq}^2 = \left[2e_{n1}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 2e_{n3}^2 + \left(\frac{1}{A_{v1}}\right)^2 e_{n6}^2\right]$$

Flicker noise

$$e_{eq}^2 = \left[2e_{n1}^2 + \left(\frac{K'_P B_P}{K'_N B_N}\right)\left(\frac{L_1}{L_3}\right)^2 2e_{n3}^2 + \left(\frac{1}{A_{v1}}\right)^2 e_{n6}^2\right]$$

$$e_{n1}^2 = \frac{2.45\times10^{-10}}{f}\ V^2/Hz$$

$$e_{n3}^2 = \frac{1.35\times10^{-11}}{f}\ V^2/Hz$$

$$e_{n6}^2 = \frac{2.15\times10^{-12}}{f}\ V^2/Hz$$

$$A_{v1} = -68.5$$

Thus, $$e_{eq}^2 = \frac{4.9\times10^{-10}}{f}\ V^2/Hz$$

Thermal noise

$$e_{n1}^2 = 1.11\times10^{-16}\ V^2/Hz$$

$$e_{n3}^2 = 7.395\times10^{-17}\ V^2/Hz$$

$$e_{n6}^2 = 1.17\times10^{-17}\ V^2/Hz$$

or, $$e_{eq}^2 = 5.58\times10^{-16}\ V^2/Hz$$

The corner frequency is

$$f_c = 884\ \text{KHz}$$

Considering a 100 KHz bandwidth

$$V_{eq}^2(rms) = 4.9\times10^{-10}\ln\left(10^5\right) + 5.58\times10^{-16}\left(10^5\right) \quad \rightarrow V_{eq}(rms) = \underline{\underline{75.5\ \mu V/\sqrt{Hz}}}$$

<u>Problem 7.5-05</u>

Find the equivalent rms noise voltage of the op amp designed in Example 6.5-2 over a bandwidth of 1Hz to 100kHz. Use the values for *KF* of Example 7.5-1.

<u>Solution</u>

The circuit for this amplifier is shown.

The *W/L* ratios in microns are:

$S_1 = S_2 = 12/1$

$S_3 = S_4 = 16/1$

$S_5 = 7/1$

$S_5 = 8.75/1$

$S_6 = S_7 = S_8 = S_{14} = S_{15} = 40/1$

$S_9 = S_{10} = S_{11} = S_{12} = 18.2/1$

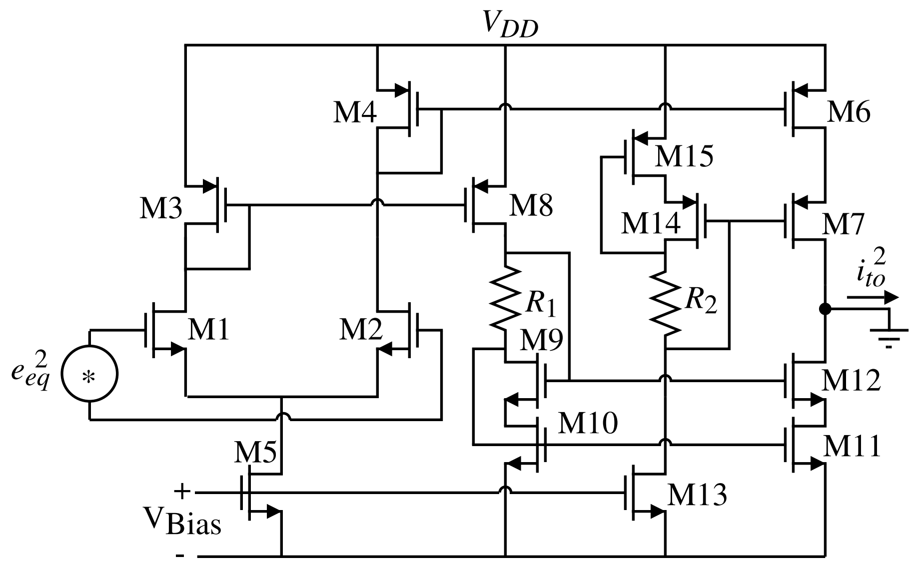


Fig. S7.5-05

Find the short circuit noise current at the output, i_{to}^2, due to each noise-contributing transistor in the circuit (we will not includeM7, M9, M12 and M14 because they are cascodes and their effective g_m is small. The result is,

$$i_{to}^2 = 2g_{m1}^2 e_{n1}^2\left(\frac{g_{m8}^2}{g_{m3}^2}\right) + 2g_{m8}^2 e_{n3}^2 + 2g_{m8}^2 e_{n8}^2 + + 2g_{m11}^2 e_{n10}^2$$

where we have assumed that g_{m1}=g_{m2}, g_{m3}=g_{m4}, g_{m6}=g_{m8}, and g_{m10}=g_{m11} and e_{n1}=e_{n2}, e_{n3}=e_{n4}, e_{n6}=e_{n8}, and e_{n10}=e_{n11}. Dividing i_{to}^2 by the transconductance gain gives

$$e_{eq}^2 = \frac{i_{to}^2}{g_{m1}^2 g_{m8}^2/g_{m3}^2} = 2e_{n1}^2 + 2\left(\frac{g_{m3}^2}{g_{m1}^2}\right)e_{n3}^2 + 2\left(\frac{g_{m3}^2}{g_{m1}^2}\right)e_{n8}^2 + 2\left(\frac{g_{m3}^2 g_{m11}^2}{g_{m1}^2 g_{m8}^2}\right)e_{n10}^2$$

The values of the various parameters are:

g_{m1} = 251µS, g_{m3} = 282.5µS, g_{m8} = 707µS, and g_{m11} = 707µS.

$$\therefore \qquad e_{eq}^2 = 2e_{n1}^2\left[1 + 1.266\left(\frac{e_{n3}^2}{e_{n1}^2} + \frac{e_{n8}^2}{e_{n1}^2} + \frac{e_{n10}^2}{e_{n1}^2}\right)\right]$$

Problem 7.5-05 – Continued

1/f Noise:

Using the results of Ex. 7.5-1 we get $B_N = 7.36\text{x}10^{-22}(\text{V}\cdot\text{m})^2$ and $B_p = 2.02\text{x}10^{-22}(\text{V}\cdot\text{m})^2$

$$e_{n1}^2 = \frac{B_N}{fW_1L_1} = \frac{7.36\text{x}10^{-22}}{f\cdot 12\text{x}10^{-12}} = \frac{6.133\text{x}10^{-11}}{f}\ V^2/\text{Hz}$$

$$\frac{e_{n3}^2}{e_{n1}^2} = \frac{B_P\cdot f\cdot W_1L_1}{B_N\cdot f\cdot W_3L_3} = \frac{B_P\cdot W_1L_1}{B_N\cdot W_3L_3} = \frac{2.02\cdot 12}{7.36\cdot 16} = 0.2058$$

$$\frac{e_{n8}^2}{e_{n1}^2} = \frac{B_P\cdot f\cdot W_1L_1}{B_N\cdot f\cdot W_8L_3} = \frac{B_P\cdot W_1L_1}{B_N\cdot W_3L_3} = \frac{2.02\cdot 12}{7.36\cdot 40} = 0.0823$$

$$\frac{e_{n10}^2}{e_{n1}^2} = \frac{B_N\cdot f\cdot W_1L_1}{B_N\cdot f\cdot W_{10}L_{10}} = \frac{B_P\cdot W_1L_1}{B_N\cdot W_3L_3} = \frac{12}{18.2} = 0.6593$$

$$\therefore \qquad e_{eq}^2 = 2\frac{6.133\text{x}10^{-11}}{f}[1+1.266(0.2058+0.0823+0.6593)] = 2\ \frac{6.133\text{x}10^{-11}}{f}2.1995$$

$$e_{eq}^2 = \frac{2.1995\text{x}10^{-10}}{f}\ V^2/\text{Hz}$$

Thermal noise:

$$e_{n1}^2 = \frac{8kT}{3g_{m1}} = \frac{8\cdot 1.38\text{x}10^{-23}\cdot 300}{3\cdot 251\text{x}10^{-6}} = 4.398\text{x}10^{-17}\ V^2/\text{Hz}$$

$$\frac{e_{n3}^2}{e_{n1}^2} = \frac{g_{m1}}{g_{m3}} = \frac{251}{282.4} = 0.8888 \quad \text{and} \quad \frac{e_{n8}^2}{e_{n1}^2} = \frac{e_{n10}^2}{e_{n1}^2} = \frac{g_{m1}}{g_{m8}} = \frac{251}{707} = 0.0.355$$

The corner frequency is $f_c = 2.698\text{x}10^{-10}/2.66\text{x}10^{-16} = 1.01\text{x}10^6$ Hz. Therefore in a 1Hz to 100kHz band, the noise is 1/*f*. Solving for the *rms* value gives,

$$V_{eq}^2\ (\text{rms}) = \int_1^{100,000}\frac{2.698\text{x}10^{-10}}{f}df = 2.698\text{x}10^{-10}[\ln(100,000) - \ln(1)]$$

$$= 3.1062\text{x}10^{-9}\ \text{V}^2(\text{rms})$$

$$\therefore \qquad V_{eq}(\text{rms}) = \underline{\underline{55.73\mu\text{V(rms)}}}$$

Problem 7.6-01

If the W and L of all transistor in Fig. 7.6-3 are 100µm and 1µm, respectively, find the lowest supply voltage that gives a zero value of *ICMR* if the dc current in M5 is 100µA.

Solution

$$I_5 = 100 \ \mu A\text{, and } \left(\frac{W}{L}\right) = 100$$

$$V_{IC}(\max) = V_{DD} + V_{T1}(\min) - V_{dsat3}$$

and, $$V_{IC}(\min) = V_{dsat1} + V_{T1}(\max) + V_{dsat5}$$

The input common-mode range is

$$ICMR = V_{IC}(\max) - V_{IC}(\min)$$

For ICMR=0

$$V_{DD} = V_{dsat1} + V_{dsat5} + V_{dsat3} + V_{T1}(\max) - V_{T1}(\min)$$

or, $$V_{DD} = \sqrt{\frac{2I_1}{K_N^{'}S_1}} + \sqrt{\frac{2I_5}{K_N^{'}S_5}} + \sqrt{\frac{2I_3}{K_P^{'}S_3}} + V_{T1}(\max) - V_{T1}(\min) \quad \rightarrow \quad V_{DD} = \underline{\underline{0.671\ \text{V}}}$$

Problem 7.6-02

Repeat Problem 1 if M1 and M2 are natural MOSFETs with a V_T = 0.1V and the other MOSFET parameters are given in Table 3.1-2.

Solution

$$V_{T1} = 0.1 \text{ V, } I_5 = 100 \ \mu A\text{, and } \left(\frac{W}{L}\right) = 100$$

Let, the variation in the threshold voltage be $\pm$ 20%

or, $$\Delta V_{T1} = \pm 0.02 \text{ V}$$

$$V_{IC}(\max) = V_{DD} + V_{T1}(\min) - V_{dsat3}$$

and, $$V_{IC}(\min) = V_{dsat1} + V_{T1}(\max) + V_{dsat5}$$

The input common-mode range is

$$ICMR = V_{IC}(\max) - V_{IC}(\min)$$

For ICMR=0

$$V_{DD} = V_{dsat1} + V_{dsat5} + V_{dsat3} + V_{T1}(\max) - V_{T1}(\min)$$

or, $$V_{DD} = \sqrt{\frac{2I_1}{K_N^{'}S_1}} + \sqrt{\frac{2I_5}{K_N^{'}S_5}} + \sqrt{\frac{2I_3}{K_P^{'}S_3}} + V_{T1}(\max) - V_{T1}(\min) \quad \rightarrow \quad V_{DD} = \underline{\underline{0.411\ \text{V}}}$$

Problem 7.6-03

Repeat Problem 1 if M1 and M2 are depletion MOSFETs with a V_T = -1V and the other MOSFET parameters are given in Table 3.1-2.

Solution

$$V_{T1} = -1 \text{ V},\ I_5 = 100\ \mu A, \text{ and } \left(\frac{W}{L}\right) = 100$$

Let, the variation in the threshold voltage be $\pm$ 20%

or, $\Delta V_{T1} = \text{m}0.2$ V

$$V_{IC}(\max) = V_{DD} + V_{T1}(\min) - V_{dsat3}$$

and, $V_{IC}(\min) = V_{dsat1} + V_{T1}(\max) + V_{dsat5}$

The input common-mode range is

$$ICMR = V_{IC}(\max) - V_{IC}(\min)$$

For ICMR=0

$$V_{DD} = V_{dsat1} + V_{dsat5} + V_{dsat3} + V_{T1}(\max) - V_{T1}(\min)$$

or, $V_{DD} = \sqrt{\dfrac{2I_1}{K_N^{'}S_1}} + \sqrt{\dfrac{2I_5}{K_N^{'}S_5}} + \sqrt{\dfrac{2I_3}{K_P^{'}S_3}} + V_{T1}(\max) - V_{T1}(\min) \rightarrow V_{DD} = \underline{\underline{0.711 \text{ V}}}$

Problem 7.6-04

Find the values of *Vonn* and *Vonp* of Fig. 7.6-4 if the *W* and *L* values of all transistors are 10µm and 1µm, respectively and the bias currents in MN5 and MP5 are 100µA each.

Solution

$$Vonn = V_{dsat,N5} + V_{TN1}(\max) + V_{dsat,N1}$$

or, $Vonn = 0.426 + 0.85 + 0.302 \qquad \rightarrow \qquad V_{onn} = \underline{\underline{1.578 \text{ V}}}$

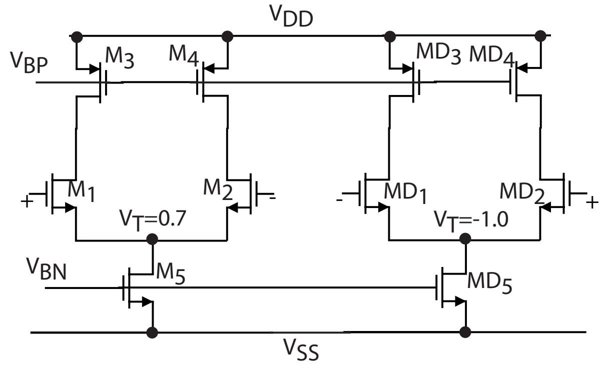
Let us assume that $V_{DD} = 2.5$ V

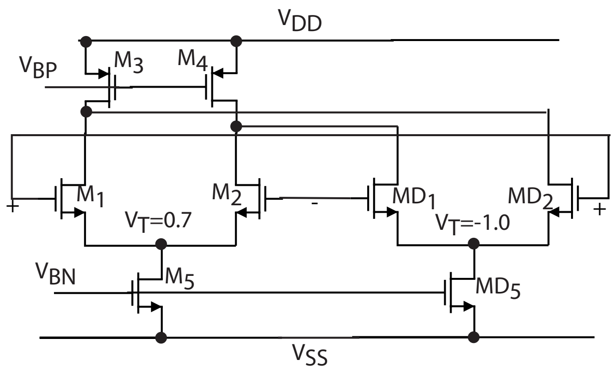
$$Vonp = V_{DD} - V_{dsat,P1} - V_{dsat,P5} - \left|V_{T,P1}(\max)\right| \rightarrow V_{onp} = \underline{\underline{0.57 \text{ V}}}$$

Problem 7.6-05

Two n-channel source-coupled pairs, one using regular transistors and the other with depletion transistors having a V_T = -1Vare connected with their gates common and the sources taken to individual current sinks. The transistors are modeled by Table 3.1-2 except the threshold is -1V for the depeletion transistors. Design the combined source-coupled pairs to achieve rail-to-rail for a 0V to 2V power supply. Try to keep the equivalent input transconductance constant over the *ICMR*. Show how to recombine the drain currents from each source-coupled pair in order to drive a second-stage single-ended.

Solution





Considering the differential amplifier consisting of M1-M5, the range of the input common mode can be given by

$$V_{IC}(\max) = V_{DD} + V_{T1} - V_{dsat3} \quad \text{and} \quad V_{IC}(\min) = V_{SS} + V_{T1} + V_{dsat1} + V_{dsat5} \qquad (1)$$

Now, considering the differential amplifier consisting of MD1-MD5, the range of the input common mode can be given by

$$V_{IC}(\max) = V_{DD} + V_{T,D1} - V_{dsat,D3} \text{ and } V_{IC}(\min) = V_{SS} + V_{T,D1} + V_{dsat,D1} + V_{dsat,D5} \quad (2)$$

Let us assume that the saturation voltage (V_{dsat}) of each of the transistors is equal to 0.1 V, and let $V_{DD} = 2$ V

Then, from Equation (1), for the transistors M1-M5

$$V_{IC}(\max) = 2.6 \text{ V} \qquad \text{and} \qquad V_{IC}(\min) = 0.9 \text{ V}$$

From Equation (2), for the transistors MD1-MD5

$$V_{ic}(\max) = \underline{\underline{0.9 \text{ V}}} \qquad \text{and} \qquad V_{ic}(\min) = \underline{\underline{-0.8 \text{ V}}}$$

Since, the common-mode input range of both stages overlap, they can be joined as shown in the figure and will provide a constant g_m across the rail-to-rail input range of 0-2 V.

Problem 7.6-06

Show how to create current mirrors by appropriately modifying the circuits in Sec. 4.4 that will have excellent matching and a V_{MIN}(in) = V_{ON} and V_{MIN}(out) = V_{ON}.

Solution

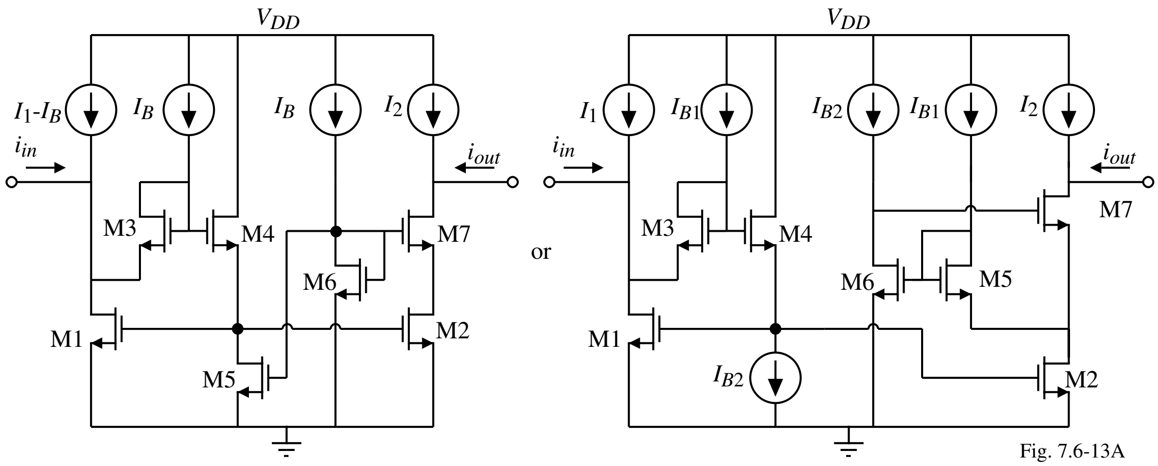


Fig. 7.6-13A

Problem 7.6-07

Show how to modify Fig. 7.6-16 to compensate for the temperature range to the left of where the two characteristics cross.

Solution

TBD

Problem 7.6-08

For the op amp of Ex. 7.6-1, find the output and higher order poles and increase the GB as much as possible and still maintain 60° phase margin. Assume that L1+L2+L3 = 2μm in order to calculate the bulk-source/drain depletion capacitors (assume zero voltage bias). What is the new value of GB and the value of C_c?

Solution

Referring to the Figure 7.6-17 and Example 7.6-1, the dominant pole is caused at the drain of M9. The second pole (p_2) is caused at the output by the load capacitor. The magnitude of this pole is given by

$$p_2 = \frac{-g_{m14}}{C_L} = -20 \text{ MHz.}$$

To increase the gain bandwidth, let us design the nulling resistor (R_Z) in such a way that the LHP zero created by this resistor will cancel the load pole. The value of $C_c = 2$ pF.

Thus, $R_Z = \dfrac{1}{g_{m14}} + \dfrac{1}{2\pi C_c p_2} = 4.77 \;K\Omega$

We can see that the pole at the source of M6 is

$$p_6 = -1.2 \text{ GHz.}$$

The third pole (p_3) at the output is caused by the nulling resistor and is given by

$$p_3 \cong \frac{-1}{2\pi R_Z C_{gs14}} = -101 \text{ MHz.}$$

In order to maintain a phase margin of $60°$, the gain bandwidth can be calculated as

$$\tan^{-1}\left(\frac{GB}{p_3}\right) = 30° \qquad \rightarrow \qquad GB = 58 \text{ MHz.}$$

or, $\quad g_{m1} = (GB)C_c = 729 \;\mu S \qquad \rightarrow \qquad \left(\dfrac{W}{L}\right)_1 = \left(\dfrac{W}{L}\right)_2 = 241.6$

Considering the minimum input common-mode range

$$V_{dsat5} = 0.22 \text{ V} \qquad \rightarrow \qquad \left(\frac{W}{L}\right)_5 = 7.5$$

Considering the maximum input common-mode range

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 19.2$$

Rest of the transistor sizes are the same as calculated in Example 7.6-1. But, the small-signal voltage gain is 18,000 V/V

Problem 7.6-09

Replace M8 and M9 of Fig. 7.6-17 with a high swing cascode current mirror of Fig. 4.3-7 and repeat Ex. 7.6-1.

Solution

Referring to the figure and Example 7.6-1

$$V_{GS8} = 1.5\text{ V} \quad \rightarrow \quad V_{dsat8} = 0.8\text{ V} \quad \rightarrow \quad \left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_9 = 0.57 \cong 1$$

Let us assume $V_{BIAS} = 2$ V. Then,

$$V_{dsat17} = 0.5\text{ V} \quad \rightarrow \quad \left(\frac{W}{L}\right)_{17} + \left(\frac{W}{L}\right)_{18} = 1.45$$

The output resistance seen at the drain of M7 is

$$R_{out1} = \frac{1}{\left\{\dfrac{g_{ds18}g_{ds9}}{g_{m18}} + \dfrac{g_{ds7}\left(g_{ds4}+g_{ds2}\right)}{g_{m7}}\right\}} = 50\ \ M\Omega$$

Thus, the overall small-signal gain becomes 2.8×10^5 V/V.

The gain bandwidth is 10 MHz. The load pole is at 20 MHz. Referring to the figure, the extra pole that would affect the phase margin the most is created at the source of M18. The resistance seen at the source of M18 can be given by

$$R_{S18} = \left[\frac{\left\{r_{ds18} + \dfrac{g_{m7}}{g_{ds7}\left(g_{ds4}+g_{ds2}\right)}\right\}}{\left(1+g_{m18}r_{ds18}\right)}\right] \| \left[r_{ds9}\right] \quad \rightarrow \quad R_{S18} = [844K] \| [1.25M] = 504\ \ K\Omega$$

The pole at the source of M18 is

$$p_{18} = \frac{-1}{R_{S18}\left(C_{gs18}+C_{bd18}+C_{gd9}+C_{bd9}\right)} \quad \rightarrow \quad p_{18} = \frac{-1}{(504K)\left(9\times 10^{-15}\right)} = -35\text{ MHz}$$

It can be seen that this pole p_{18} would degrade the phase margin by $16°$. Thus to maintain a $60°$ phase margin with a gain bandwidth of 10 MHz, let us use nulling resistor compensation to cancel this pole. The value of R_z can be given by

$$R_Z = \frac{1}{g_{m14}} + \frac{1}{2\pi C_c p_{18}} = 3.07\ \ K\Omega$$

The pole due to the introduction of R_z is

$$p_4 = \frac{-1}{R_Z C_{gs14}} = -157\text{ MHz}$$

This pole is large enough to affect the phase margin. Though the pole at the source of M18 has been eliminated using the nulling resistor compensation technique, the pole at the source of M7 could be dominant enough to degrade the phase margin.

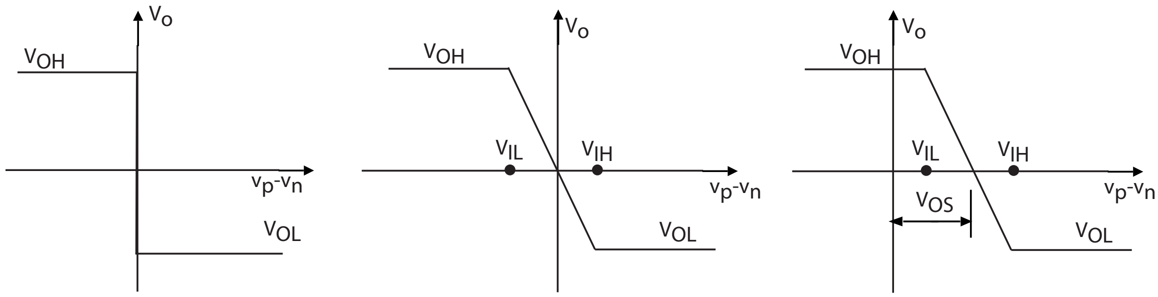
CHAPTER 8 – HOMEWORK SOLUTIONS

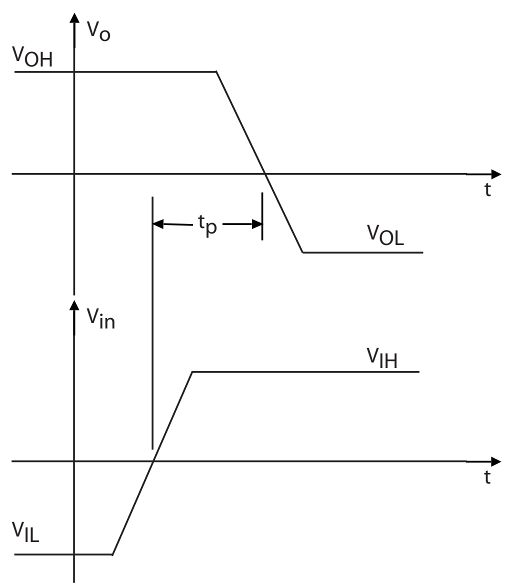
Problem 8.1-01

Give the equivalent figures for Figs. 8.1-2, 8.1-4, 8.1-6 and 8.1-9 for an inverting comparator.

Solution

The figures for the inverting comparator are shown below.





Problem 8.1-02

Use the macromodel techniques of Sec. 6.6 to model a comparator having a dc gain of 10,000 V/V, and offset voltage of 10mV, V_{OH} = 1V, V_{OL} = 0V, a dominant pole at -1000 radians/sec. and a slew rate of 1V/µs. Verify your macromodel by using it to simulate Ex. 8.1-1.

Solution

TBD

Problem 8.1-03

Draw the first-order time response of an inverting comparator with a 20 μs propagation delay. The input is described by the following equation

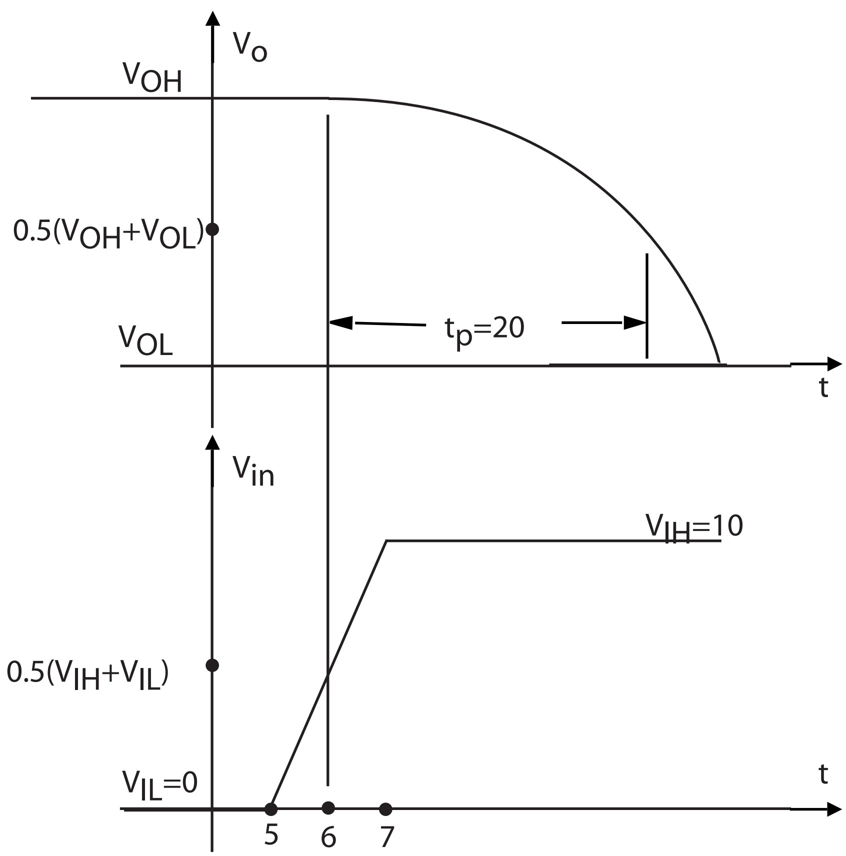
$v_{in} = 0$ for t < 5 μs

$v_{in} = 5(t - 5\ \mu s)$ for 5 μs < t < 7 μs

$v_{in} = 10$ for t > 7 μs

Solution

The input and the output response of the inverting comparator are shown in the figure.



Problem 8.1-04

Repeat Ex. 8.1-1 if the pole of the comparator is -10^5 radians/sec rather than -10^3 radians/sec.

Solution

The pole location is

$$\omega_c = -100 \text{ Krad/s}$$

$$k = \frac{V_{in}}{V_{in}(\min)} = \frac{10m}{0.1m} = 100$$

The propagation delay is given by

$$t_p = \frac{1}{\omega_c}\ln\left(\frac{2k}{2k-1}\right)$$

or, $$t_p = 50.1 \text{ ns} \tag{1}$$

Considering the maximum slew rate, the propagation delay can be expressed as

$$t_p' = \frac{V_{OH} - V_{OL}}{2SR}$$

or, $$t_p' = 500 \text{ ns} \tag{2}$$

From Equations (1) and (2), the propagation delay is

$$t_p = \underline{\underline{500 \text{ ns}}}$$

Problem 8.1-05

What value of V_{in} in Ex. 8.1-1 will give a slewing response?

Solution

The comparator will start to slew when the propagation delay of the comparator is dominated by its maximum slew rate (and not by the comparator's small-signal propagation delay).

$$\frac{V_{OH} - V_{OL}}{2SR} > \frac{1}{\omega_c}\ln\left(\frac{2k}{2k-1}\right)$$

or, $$\ln\left(\frac{2k}{2k-1}\right) < \frac{\omega_c(V_{OH} - V_{OL})}{2SR}$$

Solving for k, we get

$$k > 1000.5$$

or, $$V_{in} > \underline{\underline{100.05 \text{ mV}}}$$

<u>Problem 8.2-01</u>

Repeat Ex. 8.2-1 for the two-stage comparator of Fig. 8.2-5.

<u>Solution</u>

The output swing levels are

$$V_{OH} = V_{DD} - \left(V_{DD} - V_{G6}(\min) - |V_{TP}|\right)\left[1 - \sqrt{1 - \frac{2I_7}{\beta_6\left(V_{DD} - V_{G6}(\min) - |V_{TP}|\right)^2}}\right]$$

or, $$V_{OH} = 2.5 - (2.5 - 0 - 0.7)\left[1 - \sqrt{1 - \frac{2(234)}{(50)(38)(2.5 - 0 - 0.7)^2}}\right]$$

or, $V_{OH} = \underline{\underline{2.43\text{ V}}}$

$V_{OL} = -V_{SS} = \underline{\underline{-2.5\text{ V}}}$

The minimum input resolution is

$$V_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_v}$$

and, $$A_v = \frac{g_{m1}g_{m2}}{I_1 I_6(\lambda_P + \lambda_N)^2} = 3300$$

or, $V_{in}(\min) = \underline{\underline{1.5\text{ mV}}}$

The pole locations are

$$p_1 = \frac{g_{ds2} + g_{ds4}}{C_I} = \underline{\underline{1.074\text{ MHz}}}$$

$$p_2 = \frac{g_{ds6} + g_{ds7}}{C_{II}} = \underline{\underline{0.67\text{ MHz}}}$$

Problem 8.2-02

If the poles of a two-stage comparator are both equal to -10^7 radians/sec., find the maximum slope and the time it occurs if the magnitude of the input step is $10V_{in}$(min) and V_{OH} - V_{OL} = 1V. What must be the SR of this comparator to avoid slewing?

Solution

The response to a step response to the above comparator can be written as,

$$v_{out}' = 1 - e^{-tn} - t_n e^{-tn} \qquad \text{where } v_{out}' = \frac{v_{out}}{A_v(0)V_{in}} \text{ and } t_n = tp_1$$

To find the maximum slope, differentiate twice and set to zero.

$$\frac{dv_{out}'}{dt_n} = e^{-tn} + t_n e^{-tn} - e^{-tn} = t_n e^{-tn}$$

$$\frac{d^2v_{out}'}{dt_n^2} = -t_n e^{-tn} + e^{-tn} = 0 \quad \Rightarrow \quad (1-t_n)e^{-tn} = 0 \quad \Rightarrow \quad t_n(\text{max}) = tp_1 = 1$$

$\therefore$ $t_n(\text{max}) = 1\text{sec}$ and $t(\text{max}) = \dfrac{t_n}{|p_1|} = \dfrac{1}{10^7} = \underline{\underline{0.1\mu s}}$

$$\frac{dv_{out}'(\text{max})}{dt_n} = e^{-1} = 0.3679 \text{ V/sec} \quad \text{or} \quad \frac{dv_{out}'(\text{max})}{dt_n} = 3.679\text{V}/\mu\text{s}$$

$$\frac{dv_{out}'(\text{max})}{dt} = 10(V_{OH}\text{-}V_{OL})\cdot\frac{dv_{out}'(\text{max})}{dt_n} = \underline{\underline{36.79\text{V}/\mu\text{s}}}$$

$\therefore$ Therefore, the slew rate of the comparator should be greater than 36.79V/µs to avoid slewing.

Problem 8.2-03

Repeat Ex. 8.2-3 if p_1 = -5x10^6 radians/sec. and p_2 = 10x10^6 radians/sec.

Solution

Given $p_1 = -5$ Mrad/s, and $p_2 = -10$ Mrad/s

So, $m = \dfrac{p_2}{p_1} = 2$

When $V_{in} = 10m$

$$k = \frac{V_{in}}{V_{in}(\text{min})} = 15.576 \qquad \text{and,} \qquad t_p = \frac{1}{p_1\sqrt{mk}} = 35.8 \text{ ns}$$

When $V_{in} = 100m$ (assuming no slewing)

$$k = \frac{V_{in}}{V_{in}(\text{min})} = 155.76 \qquad \text{and,} \qquad t_p = \frac{1}{p_1\sqrt{mk}} = 11.3 \text{ ns}$$

When $V_{in} = 1$ (assuming no slewing)

$$k = \frac{V_{in}}{V_{in}(\text{min})} = 1557.6 \qquad \text{and,} \qquad t_p = \frac{1}{p_1\sqrt{mk}} = 3.58 \text{ ns}$$

Problem 8.2-04

For Fig. 8.2-5, find all of the possible initial states listed in Table 8.2-1 of the first stage output voltage and the comparator output voltage.

Solution

Condition: $V_{G1} > V_{G2}, I_1 < I_{SS}, I_2 > 0$

$2.1315 < V_{o1} < 2.5$, and $V_{o2} = -2.5$

Condition: $V_{G1} >> V_{G2}, I_1 = I_{SS}, I_2 = 0$

$V_{o1} = 2.5$, and $V_{o2} = -2.5$

Condition: $V_{G1} < V_{G2}, I_1 > 0, I_2 < I_{SS}$

$V_{S2} < V_{o1} < V_{S2} + 0.3$, and $V_{o2} = 2.5 - \dfrac{0.123}{(2.5 - V_{o1} - 0.7)}$

Condition: $V_{G1} << V_{G2}, I_1 = 0, I_2 = I_{SS}$

$V_{o1} = -2.5$, and $V_{o2} = 2.47$

Condition: $V_{G2} > V_{G1}, I_1 > 0, I_2 < I_{SS}$

$V_{S2} < V_{o1} < V_{S2} + 0.3$, and $V_{o2} = 2.5 - \dfrac{0.123}{(2.5 - V_{o1} - 0.7)}$

Condition: $V_{G2} >> V_{G1}, I_1 = 0, I_2 = I_{SS}$

$V_{o1} = -2.5$, and $V_{o2} = 2.47$

Condition: $V_{G2} < V_{G1}, I_1 < I_{SS}, I_2 > 0$

$2.1315 < V_{o1} < 2.5$, and $V_{o2} = -2.5$

Condition: $V_{G2} << V_{G1}, I_1 = I_{SS}, I_2 = 0$

$V_{o1} = 2.5$, and $V_{o2} = -2.5$

Problem 8.2-05

Calculate the trip voltage for the comparator shown in Fig. 8.2-4. Use the parameters given in Table 3.1-2. Also, $(W/L)_2 = 100$ and $(W/L)_1 = 10$. $V_{BIAS} = 1$V, $V_{SS} = 0$V, and $V_{DD} =$ 4 V.

Solution

Given, $V_{BIAS} = 1$, $V_{DD} = 4$, $V_{SS} = 0$, $S_7 = 100$, and $S_7 = 10$

The trip point is given by

$$V_{TRP} = V_{DD} - |V_{T6}| - \sqrt{\frac{K'_N S_7}{K'_P S_6}}(V_{BIAS} - V_{SS} - V_{T7})$$

or, $V_{TRP} = 1.89$ V

Problem 8.2-06

Using Problem 8.2-5, compute the worst-case variations of the trip voltage assuming a ±10% variation on V_T, K', V_{DD}, and V_{BIAS}.

Solution

The trip point is given by

$$V_{TRP} = V_{DD} - |V_{T6}| - \sqrt{\frac{K'_N S_7}{K'_P S_6}}\left(V_{BIAS} - V_{SS} - V_{T7}\right)$$

The maximum trip point can be given by

$$V_{TRP}(\max) = 1.1V_{DD} - 0.9|V_{T6}| - \sqrt{\frac{0.9K'_N S_7}{1.1K'_P S_6}}\left(0.9V_{BIAS} - V_{SS} - 1.1V_{T7}\right)$$

or, $V_{TRP}(\max)$ = 3.22 V

The minimum trip point can be given by

$$V_{TRP}(\min) = 0.9V_{DD} - 1.1|V_{T6}| - \sqrt{\frac{1.1K'_N S_7}{0.9K'_P S_6}}\left(1.1V_{BIAS} - V_{SS} - 0.9V_{T7}\right)$$

or, $V_{TRP}(\min)$ = 0.39 V

Problem 8.2-07

Sketch the output response of the circuit in Problem 5, given a step input that goes from 4 to 1 volts. Assume a 10 pF capacitive load. Also assume the input has been at 4 volts for a very long time. What is the delay time from the step input to when the output changes logical (CMOS) states?

Solution

Let us assume $V_{OH} = 5$ V and $V_{OL} = 0$ V

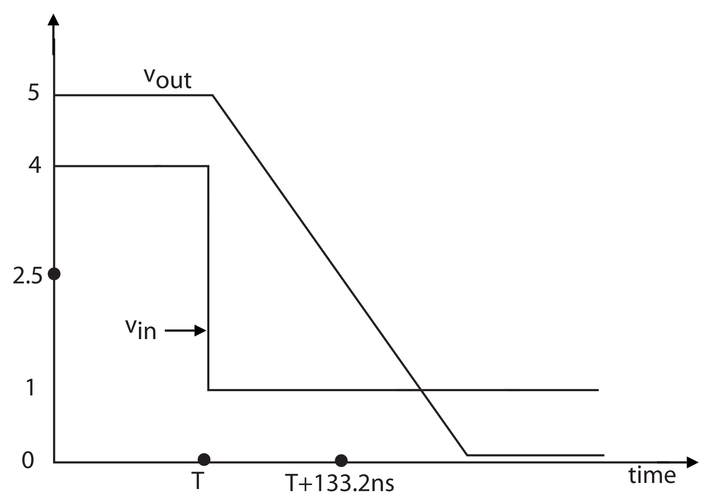
The trip point of the second stage is 3.965 V.

When the input makes a transition from 4 V to 1,

$$t_{ro1} = (0.2p)\frac{(3.965-0)}{30\mu} = 26.4$$

nsand $t_{f,out} = (10p)\dfrac{(2.5)}{234\mu} = 106.8$

ns



Thus, the total propagation delay is 133.2 ns. This is also the time it takes to change the output logical states.

Problem 8.2-08

Repeat Ex. 8.2-5 with v_{G2} constant and the waveform of Fig. 8.2-6 applied to v_{G1}.

Solution

Output fall time, t_r:

The initial states are $v_{o1} \approx$ -2.5V and $v_{out} \approx$ 2.5V. The reasoning for v_{o1} is interesting and should be understood. When V_{G1} = -2.5V and V_{G2} = 0V, the current in M1 is zero. This means the current is also zero in M4. Therefore, v_{o1} goes very negative and as M2 acts like a switch with $V_{DS} \approx 0$. Since the only current for M3 comes through M2 and from C_I, the voltage across M3 eventually collapses and I_3 becomes zero which causes $v_{o1} \approx$ -2.5V.

From Example 8.2-5, the trip point of the second stage is 1.465V, therefore the rise time of the first stage is,

$$t_{r1} = 0.2\text{pF}\left(\frac{1.465+2.5}{30\mu\text{A}}\right) = 26.4\text{ns}$$

The fall time of the second stage is found in Example 8.2-5 and is t_{f2} = 53.4ns. The total output fall time is

$$\therefore \quad t_r = t_{r1} + t_{f2} = \underline{\underline{79.8\text{ns}}}$$

Output rise time, t_r:

The initial states for this analysis are $v_{o1} \approx$ 2.5V and $v_{out} \approx$ -2.5V.

The input stage fall time is,

$$t_{f1} = 0.2\text{pF}\left(\frac{2.5-1.465}{30\mu\text{A}}\right) = 6.9\text{ns}$$

The output stage rise time is found by determining the best guess for V_{G6}. Since V_{G6} is going from 1.465 to –2.5V, let us approximate V_{G6} as

$$V_{G6} \approx 0.5(1.465\text{-}2.5) = -0.5175 \qquad \Rightarrow \qquad V_{SG6} = 2.5\text{-}(-0.5175) = 3.0175\text{V}$$

$$\therefore \quad I_6 = \frac{1}{2}K_P'\left(\frac{W_6}{L_6}\right)(V_{SG6}\text{-}|V_{TP}|)^2 = 0.5\cdot 50\text{x}10^{-6}\cdot 38(3.0175\text{-}0.7)^2 = 5102\mu\text{A}$$

$$t_{r2} = 5\text{pF}\left(\frac{2.5}{5102\mu\text{A}\text{-}234\mu\text{A}}\right) = 2.6\text{ns}$$

The total output rise time is,

$$\therefore \quad t_r = t_{f1} + t_{r2} = \underline{\underline{9.5\text{ns}}}$$

The propagation time delay of the comparator is,

$$t_p = t_r + t_r = \underline{\underline{44.7\text{ns}}}$$

Problem 8.2-09

Repeat Ex. 8.3-5 using the two-stage op amp designed in Ex. 6.3-1 if the compensation capacitor is removed.

Solution

Let us assume the initial states as

$$V_{G2} = -2.5 \text{ V}$$

$$V_{o1} = 2.5 \text{ V}$$

$$V_{out} = -2.5 \text{ V}$$

and, $C_I = 0.2$ pF

For the rising edge of the input, $V_{G2} = 2.5$ V

$$V_{TRP2} = V_{DD} - \left(|V_{T6}| + \sqrt{\frac{2I_7}{K_P^{'}S_6}}\right) \quad \rightarrow \quad V_{TRP2} = 1.6 \text{ V}$$

Thus, $\boxed{t_{fo1} = (0.2p)\dfrac{(0.9V)}{(30\mu)} = 6 \text{ ns}}$

The minimum value of V_{G6} is

$$V_{G6} \cong -V_{GS2} = -1 \text{ V}$$

Average value of V_{G6} is

$$V_{G6} = \frac{-1+1.6}{2} = 0.3 \text{ V}$$

Thus, $I_6 = \dfrac{K_P^{'}S_6}{2}\left(V_{SG6} - |V_{T6}|\right)^2 \quad \rightarrow \quad I_6 = 5.2875$ mA

So, $\boxed{t_{r,out} = (5p)\dfrac{(1.6-(-2.5))}{(5287.5\mu)} = 2.36 \text{ ns}}$

Thus, total propagation delay for the rising input is $\boxed{t_{p1} = 8.36 \text{ ns}}$

For the falling edge of the input, $V_{G2} = -2.5$ V

$$\boxed{t_{ro1} = (0.2p)\frac{(1.6-(-2.5))}{(30\mu)} = 27.3 \text{ ns}}$$

and, $\boxed{t_{f,out} = (5p)\dfrac{(2.5)}{(95\mu)} = 131.6 \text{ ns}}$

Thus, total propagation delay for the falling input is $\boxed{t_{p2} = 158.9 \text{ ns}}$

The average propagation delay is 83.63 ns.

Problem 8.2-10

Repeat Ex. 8.2-6 if the propagation time is t_p = 25ns.

Solution

Given, $t_p = 25$ ns

Let, $m = 1, k = 10$

or, $|p_1| = |p_2| = \dfrac{1}{t_p\sqrt{mk}} = 12.65$ Mrad/s

$$I_6 = I_7 = \frac{p_2 C_{II}}{(\lambda_P + \lambda_N)} = 752 \ \mu A$$

or, $\boxed{\left(\dfrac{W}{L}\right)_6 = \dfrac{2I_6}{K_P'(V_{dsat6})^2} = 120}$

and, $\boxed{\left(\dfrac{W}{L}\right)_7 = \dfrac{2I_7}{K_N'(V_{dsat7})^2} = 55}$

Now, $A_{v2} = 44.4$, and for $A_v = 4000$, we have $A_{v1} = 90.11$

In order to satisfy the propagation delay from the first stage, let us assume

$$I_1 = 40 \ \mu A$$

The corresponding propagation delay of the first stage becomes

$$t_{p1} = \frac{C_I(V_{OH} - V_{OL})}{2I_2} = 10 \ \text{ns}$$

Now, $g_{m1} = A_{v1}(\lambda_P + \lambda_N)I_1$

or, $g_{m1} = 324.4 \ \mu S$

or, $\boxed{\left(\dfrac{W}{L}\right)_1 = \left(\dfrac{W}{L}\right)_2 = 12}$

Also, $V_{IC}(\text{min}) = -1.25$ V, and $V_{GS1} = 0.946$ V.

Thus, $V_{dsat5} = 0.304$ V

or, $\boxed{\left(\dfrac{W}{L}\right)_5 = 16}$

Assuming a V_{SG3} = 1.2V gives,

$$\boxed{\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{40}{50(1.2\text{-}0.7)^2} \approx 4}$$

Problem 8.2-11

Design a comparator given the following requirements: $P_{\text{diss}} < 2$ mW, $V_{DD} = 3$ V, $V_{SS} = 0$ V $C_{\text{load}} = 3$ pF, $t_{\text{prop}} < 1$ μs, input CMR = 1.5 – 2.5 V, $A_{v0} > 2200$, and output voltage swing within 1.5 volts of either rail. Use Tables 3.1-2 and 3.3-1 with the following exceptions: $\lambda = 0.04$ for a 5 μm device length.

Solution

The ICMR is given as 1.5-2.5 V. Let us assume that

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 3 \text{ and } I_5 = 30 \ \ \mu A$$

Considering the minimum input common-mode range

$$V_{IC}(\text{min}) = V_{SS} + V_{T1}(\text{max}) + V_{dsat1} + V_{dsat5}$$

or, $\quad V_{dsat5} = 0.35$ V $\quad \rightarrow \quad \left(\frac{W}{L}\right)_1 = 4.5$

Considering the maximum input common-mode range

$$V_{IC}(\text{max}) = V_{DD} + V_{T1}(\text{min}) - V_{T3}(\text{max}) - V_{dsat3}$$

or, $\quad V_{dsat5} = 0.2$ V $\quad \rightarrow \quad \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 15$

Let us assume $\left(\frac{W}{L}\right)_7 = 31.5$ and $I_7 = 210 \ \ \mu A$

From proper mirroring of the bias currents, we get

$$\left(\frac{W}{L}\right)_6 = 210$$

The value of $C_{gs6} \cong 348$ fF. Thus, let us assume $C_I = 0.5$ pF.

The small-signal gain for this comparator is 8189 V/V.

The total power dissipation is 0.81 mW.

The trip point of the second stage is

$$V_{TRP2} = 2.1 \text{ V}$$

For the rising edge of the input, referring to the procedure in Example 8.2-5, the propagation delay can be calculated as

$t_{fo1} = 15$ ns, $t_{r,out} = 2.4$ ns, and the total propagation delay $t_{p1} = 17.4$ ns

For the falling edge of the input, the propagation delay can be found as

$t_{ro1} = 35$ ns, $t_{f,out} = 21.4$ ns, and the total propagation delay $t_{p2} = 56.4$ ns

The average propagation delay is 36.9 ns, which is well below 1000 ns.

Problem 8.3-01

Assume that the dc current in M5 of Fig. 8.3-1 is 100µA. If $W_6/L_6 = 5(W_4/L_4)$ and $W_{10}/L_{10} = 5(W_3/L_3)$, what is the propagation time delay of this comparator if C_L = 10pF and $V_{DD} = -V_{SS}$ = 2V?

Solution

The quiescent bias currents are

$$I_6 = I_7 = 250 \ \ \mu A$$

Under large-signal swing conditions, the maximum sourcing and sinking currents are

$$I_6(\max) = 500 \ \ \mu A$$

$$I_7(\max) = 500 \ \ \mu A$$

Thus, the propagation delay can be given by

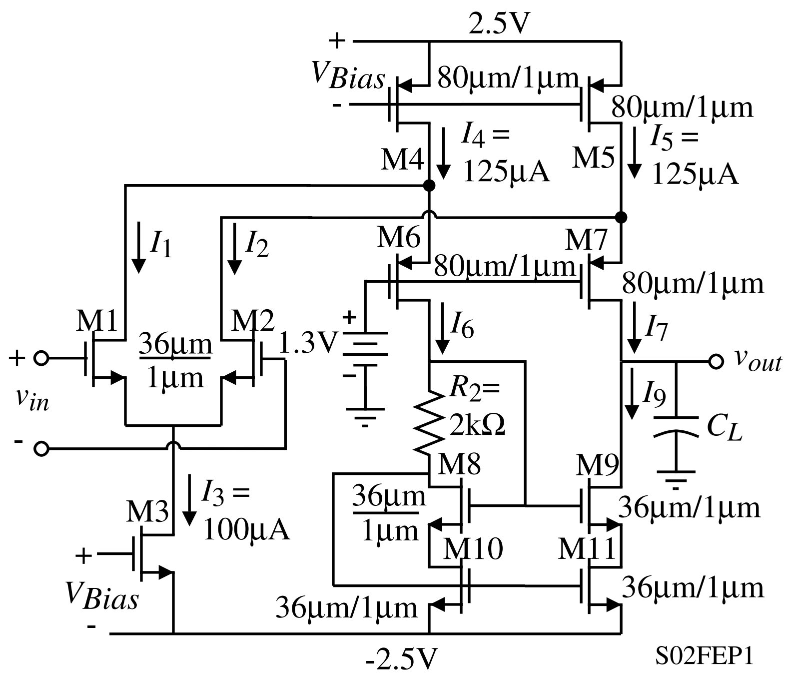
$$t_p = C_L \frac{0.5(V_{DD} - V_{SS})}{I_L}$$

or, $$t_p = (10p)\frac{0.5(2)}{(500\mu)}$$

or, $t_p = \underline{\underline{20 \text{ ns}}}$

Problem 8.3-02

If the folded-cascode op amp shown having a small-signal voltage gain of 7464V/V is used as a comparator, find the dominant pole if C_L = 5pF. If the input step is 10mV, determine whether the response is linear or slewing and find the propagation delay time. Assume the parameters of the NMOS transistors are K_N'=110V/µA^2, V_{TN} = 0.7V, λ_N=0.04V^{-1} and for the PMOS transistors are K_P'=110V/µA^2, V_{TP} = 0.7V, λ_P=0.04V^{-1}.



Solution

V_{OH} and V_{OL} can be found from many approaches. The easiest is simply to assume that V_{OH} and V_{OL} are 2.5V and –2.5V, respectively. However, no matter what the input, the values of V_{OH} and V_{OL} will be in the following range,

$$(V_{DD}\text{-}2V_{ON}) < V_{OH} < V_{DD} \quad \text{and} \quad V_{DD} < V_{OH} < (V_{SS}+2V_{ON})$$

The reasoning is as follows, suppose V_{in} >0. This gives I_1>I_2 which gives I_6<I_7 which gives I_9<I_7. V_{out} will increase until I_7 equals I_9. The only way this can happen is for M5 and M7 to leave saturation. The same reasoning holds for V_{in} <0.

Therefore assuming that V_{OH} and V_{OL} are 2.5V and –2.5V, respectively, we get

$$V_{in}(\text{min}) = \frac{5\text{V}}{7464} = 0.67\text{mV} \quad \rightarrow \quad k = \frac{10\text{mV}}{0.67\text{mV}} = 14.93$$

Problem 8.3-02 – Continued

The folded-cascode op amp as a comparator can be modeled by a single dominant pole. This pole is found as,

$$p_1 = \frac{1}{R_{out}C_L} \text{ where } R_{out} \approx g_{m9}r_{ds9}r_{ds11}||[g_{m7}r_{ds7}(r_{ds2}||r_{ds5})]$$

$g_{m9}=\sqrt{2\cdot 75\cdot 110\cdot 36}$ =771µS, $g_{ds9}=g_{ds11}$=75x10^{-6}·0.04 = 3µS, g_{ds2}=50x10^{-6}(0.04)=2µS

$g_{m7}=\sqrt{2\cdot 75\cdot 50\cdot 80}$ =775µS, g_{ds5}=125x10^{-6}·0.05 = 6.25µS, g_{ds7}=50x10^{-6}(0.05)=3.75µS

$$g_{m9}r_{ds9}r_{ds11} = (771\mu S)\left(\frac{1}{3\mu S}\right)\left(\frac{1}{3\mu S}\right) = 85.67\text{M}\Omega$$

$$g_{m7}r_{ds7}(r_{ds2}||r_{ds5} \approx (775\mu S)\left(\frac{1}{3.75\mu S}\right)\left(\frac{1}{2\mu S}||\frac{1}{6.25\mu S}\right) = 25.05\text{M}\Omega\ ,$$

$$R_{out} \approx 85.67\text{M}\Omega||25.05\text{M}\Omega = 19.4\text{M}\Omega$$

The dominant pole is found as, $p_1 = \frac{1}{R_{out}C_L} = \frac{1}{19.4\text{x}10^6 5\text{pF}}$ = 10,318 rps

The time constant is τ_1 = 96.9µs.

For a dominant pole system, the step response is, $v_{out}(t) = A_{vd}(1-e^{-t/\tau_1})V_{in}$

The slope is the largest at t = 0. Evaluating this slope gives,

$$\frac{dv_{out}}{dt} = \frac{A_{vd}}{\tau_1}e^{-t/\tau_1}V_{in} \quad \text{For } t = 0\text{, the slope is } \frac{A_{vd}}{\tau_1}V_{in} = \frac{7464}{96.9\mu s}(10\text{mV}) = 0.77\text{V}/\mu s$$

The slew rate of this op amp/comparator is $SR = \frac{I_3}{C_L} = \frac{100\mu A}{5\text{pF}}$ = 20V/µs

Therefore, the comparator does not slew and its propagation delay time is found from the linear response as,

$$t_P = \tau_1\ln\left(\frac{2k}{2k\text{-}1}\right) = 96.9\mu s\cdot\ln\left(\frac{2\cdot 14.93}{2\cdot 14.93\text{-}1}\right) = (96.9\mu s)(0.0341) = \underline{\underline{3.3\mu s}}$$

Problem 8.3-03

Find the open loop gain of Fig. 8.3-3 if the two-stage op amp is the same as Ex. 6.3-1 without the compensation and $W_{10}/L_{10} = 10(W_8/L_8) = 100(W_6/L_6)$, $W_9/L_9 = (K_P'/K_N')(W_8/L_8)$, $W_{11}/L_{11} = (K_P'/K_N')(W_{10}/L_{10})$ and the quiescent current in M8 and M9 is 100μA and in M10 and M11 is 500μA. What is the propagation time delay if C_{II} = 100pF and the step input is large enough to cause slewing?

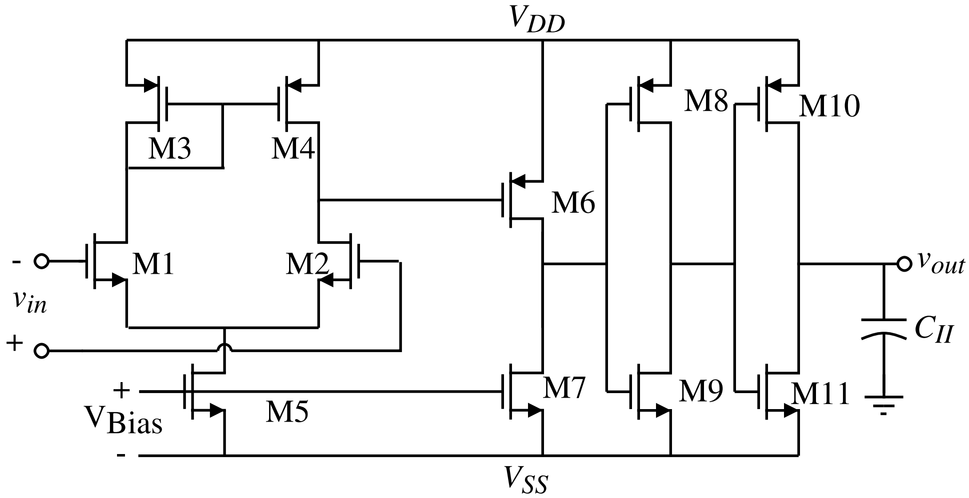


Figure 8.3-3 Increasing the capacitive drive of a two-stage, open-loop comparator.

Solution

From Ex. 6.3-1, we know that the small-signal gain to the input of the M8-M9 inverter is 7696 V/V. The gain of the M8-M9 and M10-M11 push-pull inverters are given as,

$$A_{v8,9} = -\frac{g_{m8} + g_{m9}}{g_{ds8} + g_{ds9}} \quad \text{and} \quad A_{v10,11} = -\frac{g_{m10} + g_{m12}}{g_{ds10} + g_{ds12}}$$

Since $W_6/L_6 = 94$ then $W_8/L_8 = 940$ and $W_9/L_9 = (50/110)940 = 427$.

Now, $g_{m8} = g_{m9} = \sqrt{2{\cdot}50{\cdot}940{\cdot}100}$ μS = 3,066μS, g_{ds8} = 0.04·100μS = 4μS and g_{ds9} = 0.05·100μS = 5μS.

$$\therefore\ A_{v8,9} = -\frac{3{,}066 + 3{,}066}{4+5} = -681.3 \text{ V/V}$$

Since $W_6/L_6 = 94 W_{10}/L_{10} = 9400$ and $W_{11}/L_{11} = (50/110)9400 = 4270$.

Now, $g_{m10} = g_{m12} = \sqrt{2{\cdot}50{\cdot}9400{\cdot}500}$ μS = 21.68mS, g_{ds10} = 0.04·500μS = 20μS and g_{ds9} = 0.05·500μS = 25μS.

$$\therefore\ A_{v10,11} = -\frac{21.68\text{x}2\text{x}10^3}{20+25} = -963.5 \text{ V/V} \Rightarrow \text{Total gain} = 7696{\cdot}681{\cdot}963 = \underline{\underline{5.052\text{x}10^9 \text{ V/V}}}$$

$$t_p = C\frac{\Delta V_o}{I} \quad \text{where } I = \frac{K_P W_{10}}{2L_{10}}(V_{SG10}-|V_{TP}|)^2 = 235\text{x}10^3(5-0.7)^2 = 4.345\text{A}$$

$$\therefore\quad t_p = 100\text{x}10^{-12}\left(\frac{2.5\text{V}}{4.345\text{A}}\right) = \underline{\underline{57.5\ \text{x}10^{-12}\ \text{sec.}}}$$

Problem 8.3-04

Fig. P8.3-4 shows a circuit called a clamped comparator. Use the parameters of Table 3.1-2 and calculate the gain of this comparator. What is the positive and negative slew rate of this comparator if the load capacitance is 5 pF?

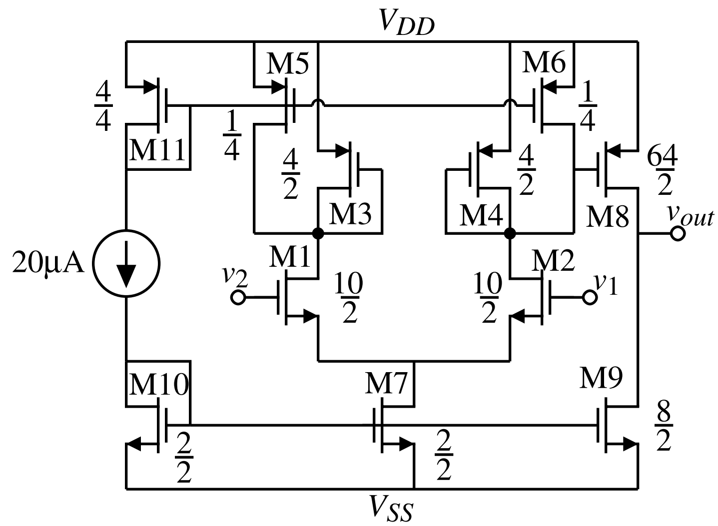


Fig. P8.3-4

Solution

$I_7 = 20\ \mu A$

$I_1 = I_2 = 10\ \mu A$

$I_5 = I_6 = 5\ \mu A$

So, $I_3 = I_4 = 5\ \mu A$

$I_8 = 80\ \mu A$

The small-signal voltage gain is

$$A_v = \frac{g_{m2}g_{m8}}{2g_{m4}(g_{ds8}+g_{ds9})}$$

or, $A_v = 83$ V/V

The negative slew rate is

$$SR^- = -\frac{I_9}{C_L} = \underline{\underline{-16\text{V/µs}}}$$

To calculate the positive slew rate

$$V_{SG8}(\min) = |V_{T4}| + \sqrt{\frac{2I_4(\max)}{K_P S_4}}$$

or, $V_{SG8}(\min) = 0.7 + \sqrt{\dfrac{2(15\mu)}{(50\mu)(2)}} = 1.25$ V

So, $I_8(\max) = 242\ \mu A$

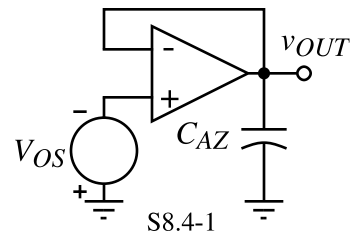
or, $SR^+ = \dfrac{I_8(\max)}{C_L} = \underline{\underline{48.4\text{V/µs}}}$

Problem 8.4-01

If the comparator used in Fig. 8.4-1 has a dominant pole at 10^4 radians/sec and a gain of 10^3, how long does it take C_{AZ} to charge to 99% of its final value, V_{OS}? What is the final value that the capacitor, C_{AZ}, will charge to if left in the configuration of Fig. 8.4-1(b) for a long time?

Solution

The output voltage for the circuit shown can be expressed as,



$$V_{out}(s) = (-V_{OS} - V_{out}(s))\left(\frac{A_v(0)}{1+\frac{s}{|p_1|}}\right)$$

This can be solved for the transfer $V_{out}(s)/V_{OS}$ as follows,

$$\frac{V_{out}(s)}{V_{OS}(s)} = \frac{\frac{A_v(0)}{1+\frac{s}{|p_1|}}}{1+\frac{A_v(0)}{1+\frac{s}{|p_1|}}} = \frac{A_v(0)}{1+A_v(0)+\frac{s}{|p_1|}} = \frac{A_v(0)|p_1|}{s+(1+A_v(0))\,|p_1|}$$

Assuming $V_{OS}(s)$ is a step function then,

$$V_{out}(s) = -\frac{V_{OS}}{s}\left(\frac{A_v(0)|p_1|}{s+(1+A_v(0))\,|p_1|}\right) = -\frac{A_v(0)V_{OS}}{1+A_v(0)}\left[\frac{1}{s} - \frac{1}{s+(1+A_v(0)|p_1|)}\right]$$

Taking the inverse Laplace transform gives,

$$v_{out}(t) = -\frac{A_v(0)V_{OS}}{1+A_v(0)}\left[1 - e^{-[1+A_v(0)]|p_1|t}\right]$$

Let $v_{out}(t) = -0.99V_{OS}$ and solve for the time T.

$$v_{out}(t) = -0.99V_{OS} = -\frac{1000V_{OS}}{1000+1}\left[1 - e^{-1001\cdot 10^4 T}\right]$$

$$1-\frac{1001}{1000}\cdot\frac{99}{100} = 0.0090 = e^{-1001\cdot 10^4 T} \Rightarrow \qquad 110.99 = e^{1001\cdot 10^4 T}$$

$\therefore \qquad T = 0.9990\text{x}10^{-7}\, ln(110.99) = \underline{\underline{0.47\mu s}}$

As $t \to \infty$, $v_{out}(t) \to -\frac{1000V_{OS}}{1000+1} = \underline{\underline{0.999V_{OS}}}$

Problem 8.4-02

Use the circuit of Fig. 8.4-9 and design a hysteresis characteristic that has $V_{TRP}^{-} = 0$V and $V_{TRP}^{+} = 1$V if $V_{OH} = 2$V and $V_{OL} = 0$V. Let $R_1 = 100\text{k}\Omega$.

Solution

Given, $V_{TRP}^{+} = 1\text{ V}$

$V_{TRP}^{-} = 0\text{ V}$

$V_{OH} = 2\text{ V}$

$V_{OL} = 0\text{ V}$

and, $R_1 = 100\ K\Omega$

Now, $V_{TRP}^{+} = \left(\dfrac{R_1 + R_2}{R_2}\right)V_{REF} - \dfrac{R_1}{R_2}V_{OL}$

or, $\left(\dfrac{R_1 + R_2}{R_2}\right)V_{REF} = 1$ (1)

Also, $V_{TRP}^{-} = \left(\dfrac{R_1 + R_2}{R_2}\right)V_{REF} - \dfrac{R_1}{R_2}V_{OH}$

or, $\left(\dfrac{R_1 + R_2}{R_2}\right)V_{REF} = \dfrac{R_1}{R_2}2$

From Equation (1)

$\dfrac{R_1}{R_2}2 = 1$

or, $R_2 = 2R_1 = 200\ K\Omega$

and, $V_{REF} = \dfrac{2}{3}\text{ V}$

Problem 8.4-03

Repeat Problem 8.4-2 for Fig. 8.4-10.

Solution

Given, $V_{TRP}^{+} = 1\ \text{V}$

$V_{TRP}^{-} = 0\ \text{V}$

$V_{OH} = 2\ \text{V}$

$V_{OL} = 0\ \text{V}$

and, $R_1 = 100\ K\Omega$

Now, $V_{TRP}^{-} = \left(\dfrac{R_2}{R_1 + R_2}\right) V_{OL} + \left(\dfrac{R_2}{R_1 + R_2}\right) V_{REF}$

or, $V_{REF} = 0\ \text{V}$

Also, $V_{TRP}^{+} = \left(\dfrac{R_2}{R_1 + R_2}\right) V_{OH} + \left(\dfrac{R_2}{R_1 + R_2}\right) V_{REF}$

or, $V_{TRP}^{+} = \left(\dfrac{R_2}{R_1 + R_2}\right) V_{OH}$

or, $R_1 = R_2 = 100\ K\Omega$

Problem 8.4-04

Assume that all transistors in Fig. 8.4-11 are operating in the saturation mode. What is the gain of the positive feedback loop, M6-M7 using the *W/L* values and currents of Ex. 8.4-2?

Solution

The loop-gain in the positive feedback loop can be expressed as

$$|LG| = \frac{g_{m6}g_{m7}}{(g_{m4} + g_{ds4} + g_{ds2} + g_{ds6})(g_{m3} + g_{ds1} + g_{ds3} + g_{ds7})}$$

Now, $S_1 = S_2 = S_6 = S_7 = 10$, and $S_3 = S_4 = 2$

$I_5 = 20\ \mu A$

So, $I_3 = \dfrac{10}{6}\ \mu A$, and $I_6 = \dfrac{50}{6}\ \mu A$

And, $g_{m6} = 91.3\ \mu S$

$g_{m7} = 91.3\ \mu S$

$g_{m3} = 18.3\ \mu S$

$g_{m4} = 18.3\ \mu S$

So, $|LG| = \underline{\underline{22.6}}$

Problem 8.4-05

Repeat Ex. 8.4-1 to design $V_{TRP}^{+} = - V_{TRP}^{-} = 0.5$V.

Solution

Given, $V_{TRP}^{+} = 0.5$ V

$V_{TRP}^{-} = -0.5$ V

$V_{OH} = 2$ V

$V_{OL} = -2$ V

Now, $V_{TRP}^{-} = \left(\dfrac{R_2}{R_1+R_2}\right)V_{OL} + \left(\dfrac{R_2}{R_1+R_2}\right)V_{REF}$

or, $$-0.5 = \left(\dfrac{R_2}{R_1+R_2}\right)(-2) + \left(\dfrac{R_2}{R_1+R_2}\right)V_{REF} \qquad (1)$$

Also, $V_{TRP}^{+} = \left(\dfrac{R_2}{R_1+R_2}\right)V_{OH} + \left(\dfrac{R_2}{R_1+R_2}\right)V_{REF}$

or, $$0.5 = \left(\dfrac{R_2}{R_1+R_2}\right)(2) + \left(\dfrac{R_2}{R_1+R_2}\right)V_{REF} \qquad (2)$$

Solving Equations (1) and (2), we get

$R_1 = 3R_2$, and $V_{REF} = 0$ V

Problem 8.4-06

Repeat Ex. 8.4-2 if i_5 = 50μA. Confirm using a simulator.

Solution

$$I_5 = 50 \quad \mu A$$

$$S_1 = S_2 = 5\ ,\ S_6 = S_7 = 10\ , \text{and } S_3 = S_4 = 2$$

To calculate the positive trip point

$$I_3 = \frac{50}{6} = 8.33 \quad \mu A$$

$$I_2 = I_5 - I_1 = 50 - 8.33 = 41.67 \quad \mu A$$

$$V_{GS1} = V_{T1} + \sqrt{\frac{2I_1}{K'_N S_1}} = 0.874 \quad \text{V}$$

$$V_{GS2} = V_{T2} + \sqrt{\frac{2I_2}{K'_N S_2}} = 1.089 \quad \text{V}$$

or, $V_{TRP}^{+} = V_{GS2} - V_{GS1} = \underline{\underline{0.215\text{V}}}$

Based on a similar analysis, the negative trip point will be

$$I_4 = \frac{50}{6} = 8.33 \quad \mu A$$

$$I_1 = 41.67 \quad \mu A$$

$$V_{GS2} = 0.874 \quad \text{V}$$

$$V_{GS1} = 1.089 \quad \text{V}$$

$$V_{TRP}^{-} = V_{GS2} - V_{GS1} = \underline{\underline{-0.215\text{V}}}$$

Problem 8.5-01

List the advantages and disadvantages of the switched capacitor comparator of Fig. 8.5-1 over an open-loop comparator having the same gain and frequency response.

Solution

	Advantages	Disadvantages
Fig. 8.5-1	Can remove input offset voltage Positive terminal on ground eliminates need for good ICMR	Requires switches Charge feedthrough Must be stable in autozero mode
Open-loop Comparator	Stability not of concern Continuous time operation	Requires good ICMR Can't remove input offset voltage

Problem 8.5-02

If the current and *W/L* values of the two latches in Fig. 8.5-3 are identical, which latch will be faster? Why?

Solution

The closed loop gain of the NMOS latch can be given by

$$A_{vn} = \left(\frac{g_m}{g_{ds}}\right)^2 = \sqrt{\frac{2K'_N(W/L)}{I\lambda_N^2}}$$

The closed loop gain of the PMOS latch can be given by

$$A_{vp} = \left(\frac{g_m}{g_{ds}}\right)^2 = \sqrt{\frac{2K'_P(W/L)}{I\lambda_P^2}}$$

It can be seen that

$$\frac{A_{vn}}{A_{vp}} = 3.4375$$

Thus, the NMOS latch would be faster (as it has larger small-signal loop gain).

Problem 8.5-03

Repeat Ex. 8.5-1 if $\Delta V_{out} = 0.5\text{V}(V_{OH}\text{-}V_{OL})$.

Solution

The propagation delay of the latch can be expressed as

$$t_p = \tau_L \ln\left(\frac{\Delta V_{out}}{\Delta V_{in}}\right)$$

where, $\tau_L = 108$ ns

or, $$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right)$$

When $\Delta V_{in} = 0.01(V_{OH} - V_{OL})$

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right) = \underline{\underline{422 \text{ ns}}}$$

When $\Delta V_{in} = 0.1(V_{OH} - V_{OL})$

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right) = \underline{\underline{174 \text{ ns}}}$$

Problem 8.5-04

Repeat Ex. 8.5-1 if the dc latch current is 50µA.

Solution

$$g_m = 332 \quad \mu S$$
$$g_{ds} = 2 \quad \mu S$$

So, the latch gain is

$$A_v = 166 \text{ V/V}$$

The latch time constant is given by

$$\tau_L = 0.67 C_{ox} \sqrt{\frac{WL^3}{2K'_N I}} = 48 \text{ ns}$$

When, $V_{in} = 0.01(V_{OH} - V_{OL})$

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right) = \underline{\underline{188 \text{ ns}}}$$

When, $V_{in} = 0.1(V_{OH} - V_{OL})$

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right) = \underline{\underline{76.8 \text{ ns}}}$$

Problem 8.5-05

Redevelop the expression for $\Delta V_{out}/\Delta V_i$ for the circuit of Fig. P8.5-5 where $\Delta v_{out} = v_{o2} - v_{o1}$ and $\Delta V_i = v_{i1} - v_{i2}$.

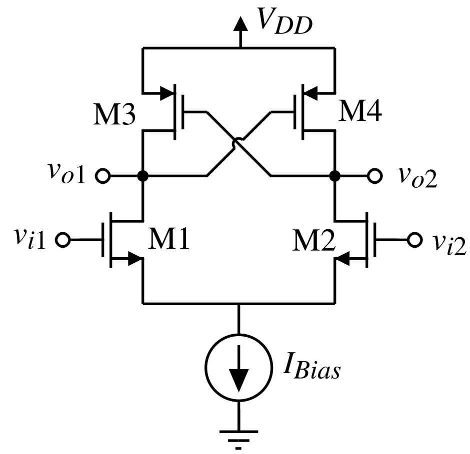


Figure P8.5-5

Solution

Referring to the figure and applying nodal analysis

$$g_{m1}v_{i1} + g_{ds1}v_{o1} + g_{m3}v_{o2} + g_{ds3}v_{o1} = 0$$

or,

$$g_{m1}v_{i1} + (g_{ds1} + g_{ds3})v_{o1} + g_{m3}v_{o2} = 0 \qquad (1)$$

Similarly, applying nodal analysis

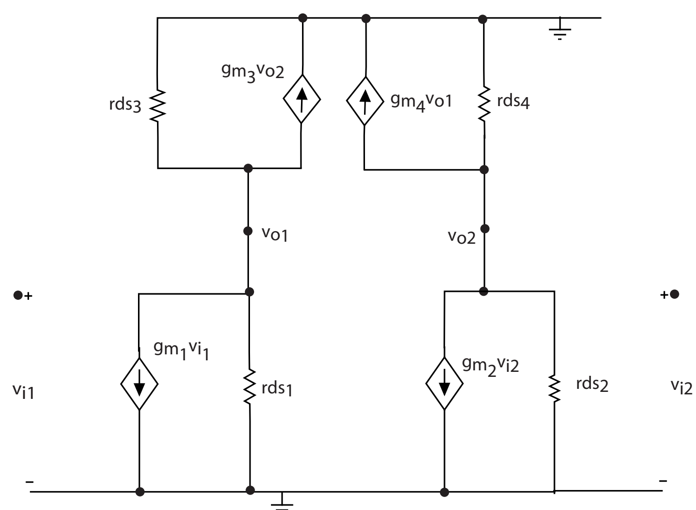
$$g_{m2}v_{i2} + (g_{ds2} + g_{ds4})v_{o2} + g_{m4}v_{o1} = 0 \qquad (2)$$

Subtracting Equation (2) from Equation (1), we get

$$g_{m1}(v_{i1} - v_{i2}) = (-g_{m3} + g_{ds1} + g_{ds3})(v_{o2} - v_{o1})$$

or,

$$\frac{(v_{o2} - v_{o1})}{(v_{i1} - v_{i2})} = \frac{g_{m1}}{(-g_{m3} + g_{ds1} + g_{ds3})}$$



Problem 8.5-06

Compare the dynamic latch of Fig. 8.5-8 with the NMOS and PMOS latches of Fig. 8.5-3.

Solution

	Advantages	Disadvantages
Fig. 8.5-3	Work with smaller power supply	Class A output – can't source and sink with the same current-slow
Fig. 8.5-8	Push-pull is good for sinking and sourcing a lot of current -fast	Needs larger power supply

Problem 8.5-07

Use the worst case values of the transistor parameters in Table 3.1-2 and calculate the worst case voltage offset for the NMOS latch of Fig. 8.5-3(a).

Solution

The offset voltage can be expressed as

$$|V_{OS}| = |V_{o2} - V_{o1}| = |V_{T1} + V_{dsat1} - V_{T2} - V_{dsat2}|$$

or, $$|V_{OS}| = \left[2\Delta V_T + \sqrt{\frac{2I_1}{K_1'S_1}} - \sqrt{\frac{2I_2}{K_2'S_2}}\right]$$

Assuming, $I_1 = I_2 = 10\ \mu A$, and $S_1 = S_2 = 10$

$$|V_{OS}| = \left[2(0.15) + \sqrt{\frac{2(10\mu)}{0.9(110\mu)(10)}} - \sqrt{\frac{2(10\mu)}{1.1(110\mu)(10)}}\right]$$

or, $$|V_{OS}| = 0.314\ \text{V}$$

Problem 8.6-01

Assume an op amp has a low frequency gain of 1000 V/V and a dominant pole at -10^4 radians/sec. Compare the -3dB bandwidths of the configurations in Fig. P8.6-1(a) and (b) using this op amp.

Solution

Given, $A_v(0) = 1000$, and $p_1 = 10$ Krad/s

Thus, the gain-bandwidth frequency is

$$GB = A_v(0)p_1 = 10\ \text{Mrad/s}$$

a) The closed-loop gain is (-25). Thus, the –3 dB bandwidth becomes

$$\omega_{-3dB} = \frac{GB}{25} = 400\ \text{Krad/s}$$

b) The closed-loop gain of each gain stage is (-5). Thus, the –3 dB bandwidth becomes

$$\omega_{-3dB} = \frac{GB}{5} = 2000\ \text{Krad/s}$$

There would be two poles at 2 Mrad/s at the output; each being created by a single gain stage.

Problem 8.6-02

What is the gain and -3dB bandwidth (in Hz) of Fig. P8.6-2 if C_L = 1pF? Ignore reverse bias voltage effects on the pn junctions and assume the bulk-source and bulk-drain areas are given by W x5µm.

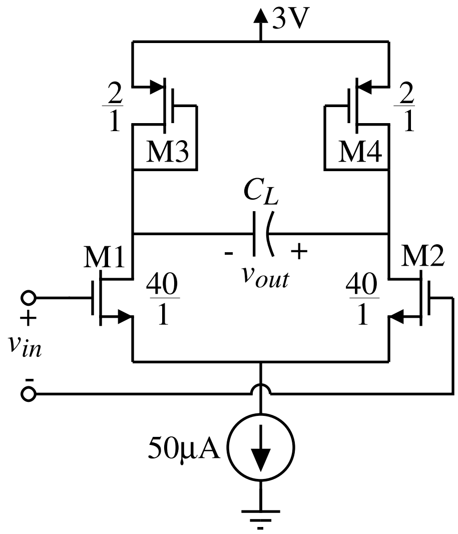


Fig. P8.6-2

Solution

$$A_v = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{K'_N S_1}{K'_P S_3}} = 6.6 \quad \text{V/V}$$

The single-ended output resistance is

$$R_o = \frac{1}{g_{m3}} = 14.14 \quad K\Omega$$

The pole frequency at the output is given by

$$p_1 = -\frac{1}{R_o\left(2C_L + C_{gs3} + C_{bd3} + C_{gd1} + C_{bd1}\right)}$$

or, $$p_1 \cong -\frac{1}{R_o\left(2C_L + C_{bd1}\right)}$$

or, $p_1 = -5.15$ MHz $\rightarrow f_{\text{-3dB}} = \underline{\underline{5.15 \text{ MHz}}}$

Problem 8.6-03

What is the gain and -3dB bandwidth (in Hz) of Fig. P8.6-3 if C_L = 1pF? Ignore reverse bias voltage effects on the pn junctions and assume the bulk-source and bulk-drain areas are given by W x5µm. The W/L ratios for M1 and M2 are 10µm/1µm and for the remaining PMOS transistors the W/L ratios are all 2µm/1µm.

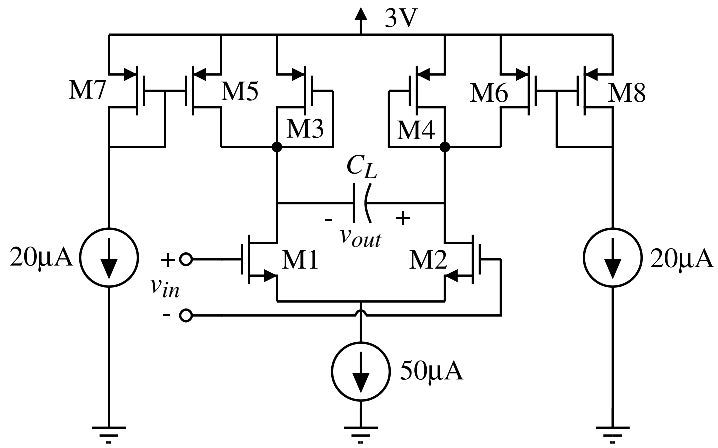
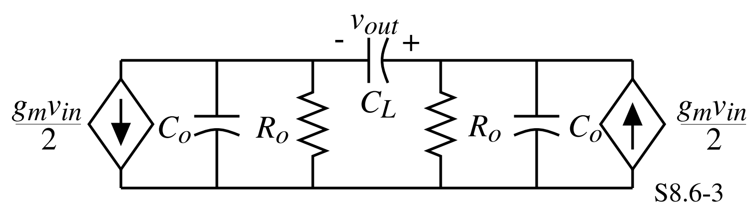


Fig. P8.6-3

Solution

A small-signal model which can be used to solve this problem is shown.



The voltage gain and the –3dB bandwidth can be expressed as,

$$\frac{v_{out}}{v_{in}} = g_m R_o \quad \text{and} \quad \omega_{\text{-3dB}} = \frac{1}{(C_L + 0.5C_o)2R_o}$$

The various values in the above relationships are:

$$g_m = \sqrt{2 \cdot K_N(W_1/L_1)I_{D1}} = \sqrt{2 \cdot 110 \cdot 10 \cdot 25}\ \mu\text{S} = 234.5\mu\text{S}$$

$$R_o \approx \frac{1}{g_{m3}} \| r_{ds1} \| r_{ds3} \| r_{ds5}, \quad g_{m3} = \sqrt{2 \cdot K_P(W_1/L_1)I_{D3}} = \sqrt{2 \cdot 50 \cdot 2 \cdot 5}\ \mu\text{S} = 31.62\mu\text{S}$$

$$r_{ds1} = \frac{1}{0.04 \cdot 25\mu\text{A}} = 1\text{M}\Omega, \ r_{ds3} = \frac{1}{0.05 \cdot 5\mu\text{A}} = 4\text{M}\Omega \text{ and } r_{ds5} = \frac{1}{0.04 \cdot 20\mu\text{A}} = 0.8\text{M}\Omega$$

$$\therefore \ R_o = 31.623\text{k}\Omega \| 1\text{M}\Omega \| 4\text{M}\Omega \| 0.8\text{M}\Omega = 29.31\text{k}\Omega$$

$$C_o \approx C_{gs3} + C_{bd1} + C_{bd3} + C_{bd5} \qquad C_{gs3} = CGSO \cdot W_5 + 0.67 \cdot C_{ox} \cdot W_5 \cdot L_5$$

$$= 220\text{x}10^{-12}\text{F/m} \cdot 2\text{x}10^{-6}\text{m} + 0.67 \cdot 24.7\text{x}10^{-4}\text{F/m}^2 \cdot 2\text{x}10^{-12}\text{m}^2 = 3.73\text{fF}$$

$$C_{bd1} = CJ \cdot AS + CJSW \cdot PS = 770\text{x}10^{-6}\text{F/m}^2 \cdot 50\text{x}10^{-12}\text{m}^2 + 380\text{x}10^{-12}\text{F/m} \cdot 30\text{x}10^{-6}\text{m}$$

$$= 38.5\text{fF} + 11.4\text{fF} = 49.9\text{fF}$$

$$C_{bd3} = C_{bd5} = 560\text{x}10^{-6}\text{F/m}^2 \cdot 10\text{x}10^{-12}\text{m}^2 + 350\text{x}10^{-12}\text{F/m} \cdot 14\text{x}10^{-6}\text{m} = 10.5\text{fF}$$

$$\therefore \ C_o = 74.6\text{fF} \ \rightarrow \ \omega_{\text{-3dB}} = \frac{1}{(1.073\text{pF})58.62\text{k}\Omega} = 16.445\text{x}10^6\text{rads/sec}$$

Finally, $f_{\text{-3dB}} = \underline{\underline{2.62\text{MHz}}}$ and $A_v = \underline{\underline{6.873\text{V/V}}}$

Problem 8.6-04

Assume that a comparator consists of an amplifier cascaded with a latch. Assume the amplifier has a gain of 5V/V and a -3dB bandwidth of $1/\tau_L$, where τ_L is the latch time constant and is equal to 10ns. Find the propagation time delay for the overall configuration if the applied input voltage is $0.05(V_{OH}\text{-}V_{OL})$ and the voltage applied to the latch from the amplifier is (a) $\Delta V_i = 0.05(V_{OH}\text{-}V_{OL})$, (b) $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$, (c) $\Delta V_i = 0.15(V_{OH}\text{-}V_{OL})$ and (d) $\Delta V_i = 0.2(V_{OH}\text{-}V_{OL})$. Assume that the latch is enabled as soon as the output of the amplifier is equal to $0.05(V_{OH}\text{-}V_{OL})$. From your results, what value of ΔV_i would give minimum propagation time delay?

Solution

The transfer function of the amplifier is $$A_v(s) = \frac{A_v(0)}{s\tau_L+1}$$

The output voltage of the amplifier is $v_o(t) = A_v(0)[1\text{-}e^{-t/\tau_L}]\Delta V_i$

Let $\Delta V_i = x\cdot(V_{OH}\text{-}V_{OL})$, therefore the delay of the amplifier can be found as

$$x(V_{OH}\text{-}V_{OL}) = A_v(0)[1\text{-}e^{-t1/\tau_L}]0.05(V_{OH}\text{-}V_{OL}) = 5[1\text{-}e^{-t1/\tau_L}]0.05(V_{OH}\text{-}V_{OL})$$

or

$$x = 0.25[1\text{-}e^{-t1/\tau_L}] \quad \rightarrow \quad t_1 = \tau_L\, ln\left(\frac{1}{1\text{-}4x}\right)$$

The delay of the latch can be found as

$$t_2 = \tau_L\, ln\left(\frac{V_{OH}\text{-}V_{OL}}{2x(V_{OH}\text{-}V_{OL})}\right) = \tau_L\, ln\left(\frac{1}{2x}\right)$$

The propagation time delay of the comparator can be expressed in terms of x as,

$$t_p = t_1+t_2 = \tau_L\, ln\left(\frac{1}{1\text{-}4x}\right) + \tau_L\, ln\left(\frac{1}{2x}\right) = \tau_L\, ln\left(\frac{1}{2x\text{-}8x^2}\right)$$

Thus,

$$x = 0.05 = 1/20 \quad \Rightarrow \quad \tau_p = t_1 + t_2 = 2.23\text{ns}+2.30\text{ns} = \underline{\underline{25.26\text{ns}}}$$

$$x = 0.1 = 1/10 \quad \Rightarrow \quad \tau_p = t_1 + t_2 = 5.11\text{ns}+16.09\text{ns} = \underline{\underline{21.20\text{ns}}}$$

$$x = 0.15 \quad \Rightarrow \quad \tau_p = t_1 + t_2 = 9.16\text{ns}+12.04\text{ns} = \underline{\underline{21.20\text{ns}}}$$

$$x = 0.2 = 1/5 \quad \Rightarrow \quad \tau_p = t_1 + t_2 = 16.09\text{ns}+9.16\text{ns} = \underline{\underline{25.26\text{ns}}}$$

Note that differentiating t_p with respect to x and setting to zero gives

$$x_{min} = 1/8 = 0.125$$

Therefore, minimum delay of $\underline{\underline{20.08\text{ns}}}$ is achieved when $\underline{\underline{x = 1/8}}$.

Problem 8.6-05

Assume that a comparator consists of two identical amplifiers cascaded with a latch. Assume the amplifier has the characteristics given in the previous problem. What would be the normalized propagation time delay if the applied input voltage is $0.05(V_{OH}\text{-}V_{OL})$ and the voltage applied to the latch is $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$?

Solution

The transfer function of the amplifiers is $$A_v(s) = \left(\frac{A_v(0)}{s\tau_L+1}\right)^2 = \left(\frac{5}{s\tau_L+1}\right)^2$$

The output voltage of the amplifiers is

$$V_o(s) = \frac{\frac{25}{\tau_L^2}}{(s+1/\tau_L)^2}\cdot\frac{0.05(V_{OH}\text{-}V_{OL})}{s} = \frac{1.25(V_{OH}\text{-}V_{OL})}{\tau_L^{\ 2}}\left[\frac{a}{s} + \frac{b}{s+(1/\tau_L)} + \frac{c}{(s+(1/\tau_L))^2}\right]$$

or $$H(s) = \frac{1}{s(s+(1/\tau_L))^2} = \frac{a}{s} + \frac{b}{s+(1/\tau_L)} + \frac{c}{(s+(1/\tau_L))^2}$$

Solving for a, b, and c, by partial fraction expansion gives

$$a = sH(s)\Big|_{s=0} = \tau_L^2, \quad c = [s+(1/\tau_L)]^2\cdot H(s)\Big|_{s=-1/\tau_L} = -\tau_L$$

and $$\frac{d}{da}\left[\frac{1}{s} = a[s+(1/\tau_L)]^2 + b[s+(1/\tau_L)] + c\right] \Rightarrow -\frac{1}{s^2} = 2a[s+(1/\tau_L)] + b$$

∴ Let $s=-1/\tau_L$ to get $b = -\tau_L^2$

$$V_o(s) = 1.25(V_{OH}\text{-}V_{OL})\left[\frac{1}{s} - \frac{1}{s+(1/\tau_L)} - \frac{\tau_L}{[s+(1/\tau_L)]^2}\right]$$

Taking the inverse Laplace transform gives,

$$v_o(t) = 1.25(V_{OH}\text{-}V_{OL})\left[1 - e^{-t/\tau_L} - \frac{t}{\tau_L}e^{-t/\tau_L}\right]$$

Setting $v_o(t) = 0.05(V_{OH}\text{-}V_{OL})$ and solving for the amplifier delay, t_1, gives

$$\frac{t_1}{\tau_L} = ln\left[\frac{1.25}{1.2} + \frac{1.25}{1.2}\frac{t_1}{\tau_L}\right] = ln\left[1.041667\left(1+\frac{t_1}{\tau_L}\right)\right]$$

Solving iteratively gives $t_1/\tau_L = 0.313 \quad \Rightarrow \quad t_1 = 3.13\text{ns}$

The latch delay time, t_2 is found as

$$t_2 = \tau_L ln\left(\frac{V_{OH}\text{-}V_{OL}}{2\text{x}0.1(V_{OH}V_{OL})}\right) = 10\text{ns } ln(5) = 16.095\text{ns}$$

∴ $t_{comparator} = t_1 + t_2 = \underline{\underline{19.226\text{ns}}}$

Problem 8.6-06

Repeat Problem 5 if there are three identical amplifiers cascaded with a latch. What would be the normalized propagation time delay if the applied input voltage is $0.05(V_{OH}-V_{OL})$ and the voltage applied to the latch is $\Delta V_i = 0.2(V_{OH}-V_{OL})$?

Solution

The combined transfer function of the three, cascaded amplifier stage can be given as

$$A_v(s) = \frac{A_v^3}{\left(1+ {}^{s}\!/_{p}\right)^3}$$

In response to a step input, the output response of the three, cascaded amplifier stages can be approximated as

$$v_{oa}(t) = A_v^3 v_{in}\left(1 - 3e^{-t/\tau_L}\right)$$

The normalized propagation delay of the three, cascaded amplifier stages can be given by

$$t'_{p1} = \ln\left(\frac{3}{1-\dfrac{v_{oa}}{A_v^3 v_{in}}}\right)$$

The normalized propagation delay of the latch can be given by

$$t'_{p2} = \ln\left(\frac{V_{OH}-V_{OL}}{2v_{oa}}\right)$$

When $v_{in} = 0.05\left(V_{OH}-V_{OL}\right)$, and $v_{oa} = 0.1\left(V_{OH}-V_{OL}\right)$, the total normalized propagation delay is

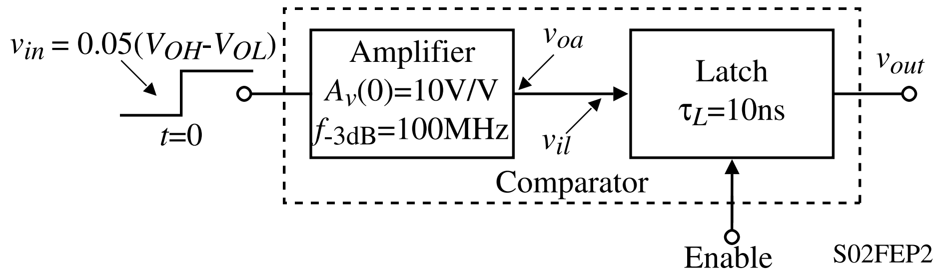
$$t'_p = t'_{p1} + t'_{p2} = 1.115 + 1.609 = 2.724$$

When $v_{in} = 0.05\left(V_{OH}-V_{OL}\right)$, and $v_{oa} = 0.2\left(V_{OH}-V_{OL}\right)$, the total normalized propagation delay is

$$\boxed{t'_p = t'_{p1} + t'_{p2} = 1.131 + 0.916 = 2.047}$$

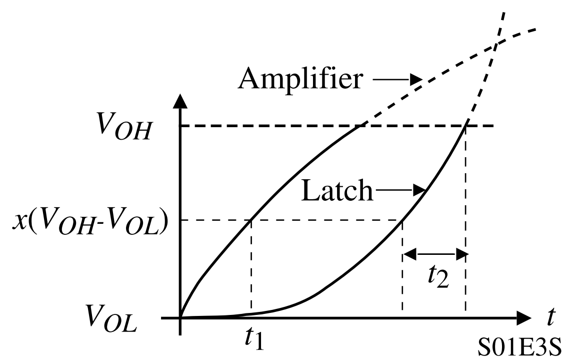
Problem 8.6-07

A comparator consists of an amplifier cascaded with a latch as shown in Figure P8.6-7. The amplifier has a voltage gain of 10 V/V and f_{-3dB} = 100 MHz and the latch has a time constant of 10 ns. The maximum and minimum voltage swings of the amplifier and latch are V_{OH} and V_{OL}. When should the latch be enabled after the application of a step input to the amplifier of $0.05(V_{OH} - V_{OL})$ to get minimum overall propagation time delay? What is the value of the minimum propagation time delay? It may be useful to recall that the propagation time delay of the latch is given as $t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2v_{il}}\right)$ where v_{il} is the latch input (ΔV_i of the text).



Solution

The solution is based on the figure shown.



We note that,

$$v_{oa}(t) = 10[1\text{-}e^{-\omega_{-3dB}t}]0.05(V_{OH}\text{-}V_{OL}).$$

If we define the input voltage to the latch as,

$$v_{il} = x\cdot(V_{OH}\text{-}V_{OL})$$

then we can solve for t_1 and t_2 as follows:

$$x\cdot(V_{OH}\text{-}V_{OL}) = 10[1\text{-}e^{-\omega_{-3dB}t_1}]0.05(V_{OH}\text{-}V_{OL}) \rightarrow x = 0.5[1\text{-}e^{-\omega_{-3dB}t_1}]$$

This gives,

$$t_1 = \frac{1}{\omega_{-3dB}} ln\left(\frac{1}{1\text{-}2x}\right)$$

From the propagation time delay of the latch we get,

$$t_2 = \tau_L\, ln\left(\frac{V_{OH}\text{-}V_{OL}}{2v_{il}}\right) = \tau_L\, ln\left(\frac{1}{2x}\right)$$

$$\therefore \quad t_p = t_1 + t_2 = \frac{1}{\omega_{-3dB}} ln\left(\frac{1}{1\text{-}2x}\right) + \tau_L\, ln\left(\frac{1}{2x}\right) \rightarrow \frac{dt_p}{dx} = 0 \text{ gives } x = \frac{\pi}{1+2\pi} = 0.4313$$

$$t_1 = \frac{10\text{ns}}{2\pi} ln\,(1+2\pi) = 1.592\text{ns}\cdot 1.9856 = \underline{\underline{3.16\text{ns}}} \text{ and } t_2 = 10\text{ns}\, ln\left(\frac{1+2\pi}{2\pi}\right) = 1.477\text{ns}$$

$$\therefore \quad t_p = t_1 + t_2 = 3.16\text{ns} + 1.477\text{ns} = \underline{\underline{4.637\text{ns}}}$$

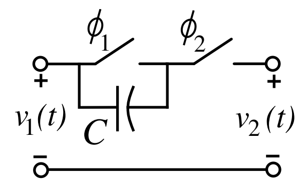
CHAPTER 9 – HOMEWORK SOLUTIONS

Problem 9.1-01

Develop the equivalent resistance expression in Table 9.1-1 for the series switched capacitor resistor emulation circuit.

Solution

The series switched capacitor is shown for reference purposes.



The average current flowing into the left-hand port can be written as,

$$i_1(average) = \frac{1}{T}\int_0^T i_1(t)dt = \frac{1}{T}\left(\int_0^{T/2} i_1(t)dt + \int_{T/2}^{T} i_1(t)dt\right)$$

or in terms of charge,

$$i_1(average) = \frac{1}{T}\int_0^{T/2} dq_1(t) + \frac{1}{T}\int_{T/2}^{T} dq_1(t) = \frac{q_1(T) - q_1(T/2)}{T}$$

By following through the sequence of switching, we see that,

$$q_1(T/2) = 0 \ \text{ and } q_1(T) = C[v_1(T) - v_2(T)]$$

$$\therefore \qquad i_1(average) = \frac{C[v_1(T) - v_2(T)]}{T} \approx \frac{C[V_1 - V_2]}{T}$$

The average current of a series resistance, R, can be expressed as

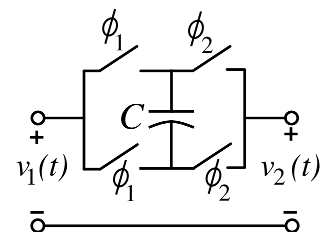
$$i_1(average) = \frac{[V_1 - V_2]}{R}$$

Equating the average currents gives

$$\boxed{R = \frac{T}{C}}$$

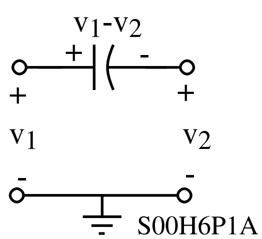
Problem 9.1-02

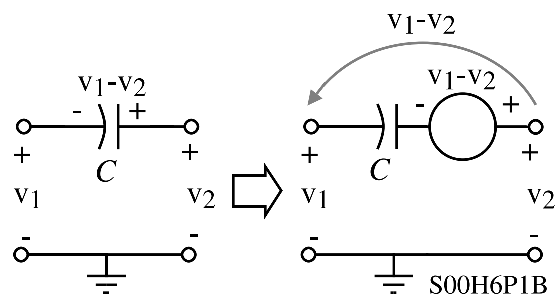
Develop the equivalent resistance expression for the bilinear switched capacitor resistor equivalent circuit shown below assuming that the clock frequency is much larger than the frequency of the signal.



Solution

ϕ_1 phase, $0<t<0.5T$: ϕ_2 phase, $0.5T<t<T$:





$$i_{Av} = \frac{1}{T}\int_0^T i(t)dt = \frac{2}{T}\int_{0.5T}^T i(t)dt = \frac{2}{T}\int_{0.5T}^T dq(t) = \frac{2}{T}2C(v_1\text{-}v_2) = \frac{4C}{T}(v_1\text{-}v_2)$$

$$\therefore\ R_{eq} = \frac{(v_1\text{-}v_2)}{i_{Av}} = \frac{T}{4C} \qquad \Rightarrow \qquad \boxed{R_{eq} = \frac{T}{4C}}$$

Problem 9.1-03

What is the accuracy of a time constant implemented with a resistor and capacitor having a tolerance of 10% and 5%, respectively. What is the accuracy of a time constant implemented by a switched capacitor resistor emulation and a capacitor if the tolerances of the capacitors are 5% and the relative tolerance is 0.5%. Assume that the clock frequency is perfectly accurate.

Solution

Continuous time accuracy:

$$\frac{d\tau_C}{\tau_C} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} = 10\%+5\% = \underline{\underline{15\%}}$$

Discrete-time accuracy:

$$\frac{d\tau_D}{\tau_D} = \frac{dC_2}{C_2} - \frac{dC_1}{C_1} - \frac{df_c}{f_c} = \underline{\underline{0.5\%}}$$

Problem 9.1-04

Repeat Example 9.1-3 using a series switched capacitor resistor emulation.

Solution

Problem 9.1-05

Find the z-domain transfer function for the circuit shown in Fig. 9.1-5. Let $\alpha = C_2/C_1$ and find an expression for the discrete time frequency response following the methods of Ex. 9.1-4. Design (find α) a first-order, highpass circuit having a -3dB frequency of 1kHz following the methods of Ex. 9.1-5. Assume that the clock frequency is 100kHz. Plot the frequency response for the resulting discrete time circuit and compare with a first-order, highpass, continuous time circuit.

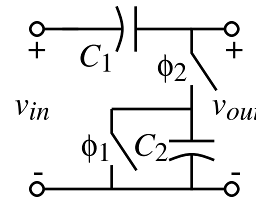
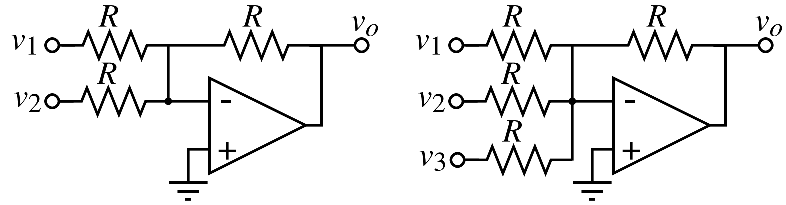


Figure P9.1-5

Solution

Problem 9.2-01

Fig. P9.2-1 shows two inverting summing amplifiers. Compare the closed-loop frequency response of these two summing amplifiers if the op amp is modeled by $A_{vd}(0) = 10{,}000$ and $GB = 1$MHz.



(a.) (b.)

Figure P9.2-1 (a.) 2-input inverting summer. (b.) 3-input inverting summer.

Solution

A model for calculating the closed-loop frequency response is shown.

Solving for the output voltage,

$$V_{out} = -A\left(\frac{R}{(n+2)R}V_{out} + \frac{R}{(n+2)R}V_1\right)$$

$$V_{out}\left(1 + \frac{AR}{(n+2)R}\right) = -\frac{AR}{(n+2)R}V_1$$

$$\therefore \quad \frac{V_{out}}{V_1} = \frac{-\frac{A}{(n+2)}}{1+\frac{A}{n+2}} = \frac{-\frac{1}{n+2}}{\frac{1}{A} + \frac{1}{n+2}} \quad \text{We know that } A(s) = \frac{A_{vd}(0)}{1+\frac{s}{\omega_a}} \approx \frac{A_{vd}(0)\omega_a}{s} = \frac{GB}{s}$$

Substituting gives,

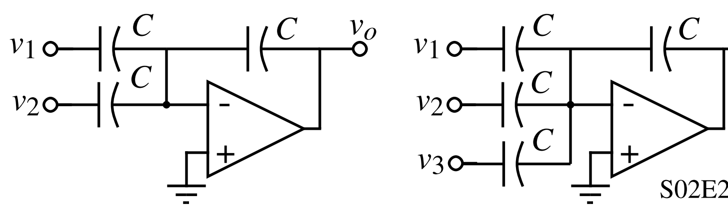
$$\frac{V_{out}}{V_1} = \frac{-\frac{1}{n+2}}{\frac{s}{GB} + \frac{1}{n+2}} = \frac{-\frac{GB}{n+2}}{s + \frac{GB}{n+2n}} = A_o\frac{\omega_{-3\text{dB}}}{s + \omega_{-3\text{dB}}}$$

$$\therefore \quad \omega_{-3\text{dB}} = \frac{GB}{n+2} \quad \text{and} \quad A_o = -1$$

For $n = 1$, $f_{-3\text{dB}} = GB/3 = 0.33\text{MHz}$ and for $n = 2$, $f_{-3\text{dB}} = GB/4 = 0.250\text{MHz}$

Problem 9.2-02

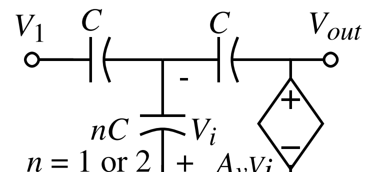
Two switched-capacitor summing amplifiers are shown. Find the value of the –3dB frequency of the closed-loop frequency response, v_o/v_1, with the remaining inputs shorted, of these two summing amplifiers if the op amp is modeled by $A_{vd}(0)$ = 10,000 and GB = 1MHz.



S02E2P3A

Solution

A model for calculating the closed-loop frequency response is shown.



S02E2S3

Solving for the output voltage,

$$V_{out} = -A\left(\frac{C}{(n+2)C}V_{out} + \frac{C}{(n+2)C}V_1\right)$$

$$V_{out}\left(1+\frac{AC}{(n+2)C}\right) = -\frac{AC}{(n+2)C}V_1$$

$$\therefore \qquad \frac{V_{out}}{V_1} = \frac{-\frac{A}{(n+2)}}{1+\frac{A}{n+2}} = \frac{-\frac{1}{n+2}}{\frac{1}{A}+\frac{1}{n+2}} \qquad \text{We know that } A(s) = \frac{A_{vd}(0)}{1+\frac{s}{\omega_a}} \approx \frac{A_{vd}(0)\omega_a}{s} = \frac{GB}{s}$$

Substituting gives,

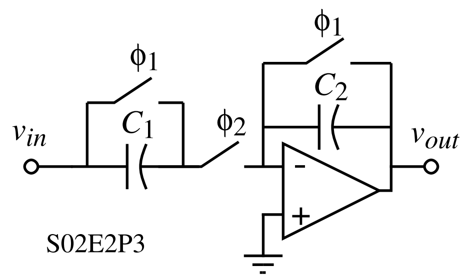
$$\frac{V_{out}}{V_1} = \frac{-\frac{1}{n+2}}{\frac{s}{GB}+\frac{1}{n+2}} = \frac{-\frac{GB}{n+2}}{s+\frac{GB}{n+2n}} = A_o\frac{\omega_{-3\text{dB}}}{s+\omega_{-3\text{dB}}}$$

$$\therefore \qquad \omega_{-3\text{dB}} = \frac{GB}{n+2} \quad \text{and} \quad A_o = -1$$

For n = 1, $f_{-3\text{dB}} = GB/3 = 0.33\text{MHz}$ and for n = 2, $f_{-3\text{dB}} = GB/4 = 0.250\text{MHz}$

Problem 9.2-03

Find the z-domain transfer function for $H^{ee}(z)$ for the switched capacitor circuit shown.



S02E2P3

Solution

In phase ϕ_2, the circuit is simply a charge amplifier whose transfer function is given as

$$H^{ee}(z) = \frac{V_{out}^{e}(z)}{V_{in}^{e}(z)} = -\frac{C_1}{C_2}$$

Problem 9.2-04

Verify the transresistance of Fig. 9.2-6a.

Solution

Positive transresistance realization:

$$R_T = \frac{v_1(t)}{i_2(t)} = \frac{v_1}{i_2(average)}$$

If we assume $v_1(t)$ is ≈ constant over one period of the clock, then we can write

$$i_2(average) = \frac{1}{T}\int_{T/2}^{T} i_2(t)dt = \frac{q_2(T) - q_2(T/2)}{T} = \frac{Cv_C(T) - Cv_C(T/2)}{T} = \frac{Cv_1}{T}$$

Substituting this expression into the one above shows that $\boxed{R_T = T/C}$

Problem 9.2-05

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oe}(z)$. (2.) If $C_1 = 10C_2$, plot the magnitude and phase response of the switched capacitor circuit from 0 Hz to the clock frequency (f_c). Assume that the op amp is ideal for this problem.

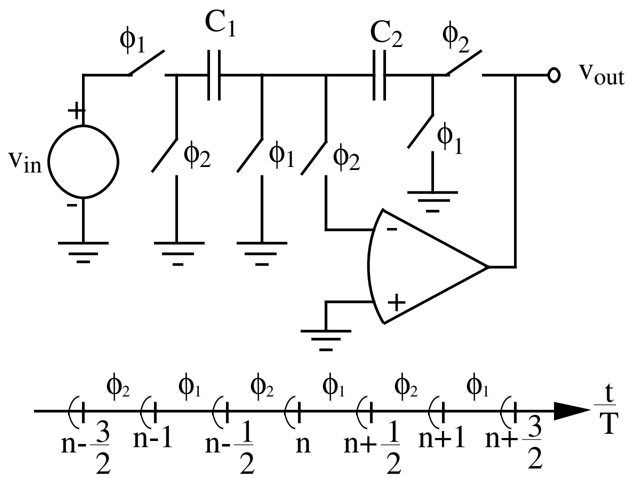


Figure P9.2-5

Solution

(1.) This circuit is a noninverting amplifier with a minimum number of switches.

ϕ_1: $t = (n\text{-}1)T$

$$v^o_{C1}(n\text{-}1) = v^o_{in}(n\text{-}1) \quad \text{and} \quad v^o_{C2}(n\text{-}1) = 0$$

ϕ_2: $t = (n\text{-}0.5)T$

$$v^e_{out}(n\text{-}0.5) = -\frac{C_1}{C_2}\left[-v^o_{in}(n\text{-}1)\right] = \frac{C_1}{C_2}v^o_{in}(n\text{-}1)$$

$$\therefore \quad V^e_{out}(z) = \frac{C_1}{C_2}z^{-1/2}\,v^o_{in}(z) \quad \rightarrow \quad H^{oe}(z) = \frac{C_1}{C_2}z^{-1/2} = \underline{\underline{10z^{-1/2}}}$$

(2.) $H^{oe}(e^{j\omega T}) = 10e^{-j\omega T/2} = 10e^{-j2\pi f/2f_c} = 10e^{-j\pi f/f_c}$

Plotting this transfer function gives,

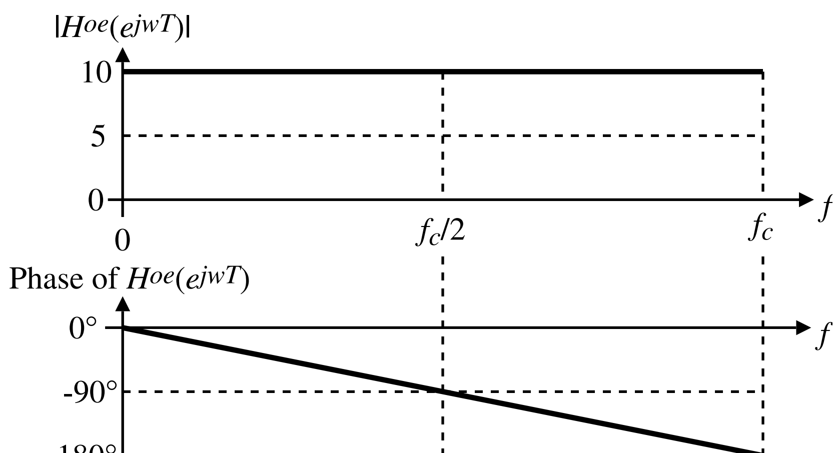


Fig. S9.2-05

Problem 9.2-06

Find $H^{oe}(z)$ $(=V_{out}^{e}(z)/V_{in}^{o}(z))$ of the switched capacitor circuit shown in Fig. P9.2-6. Replace z by $e^{j\omega T}$ and identify the magnitude and phase response of this circuit. Assume $C_1 = C_2$. Sketch the magnitude and phase response on a linear-linear plot from f=0 to f=f_c. What is the magnitude and phase at $f = 0.5f_c$?

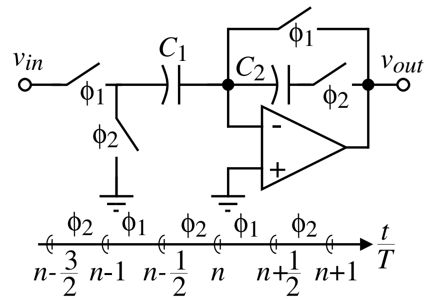
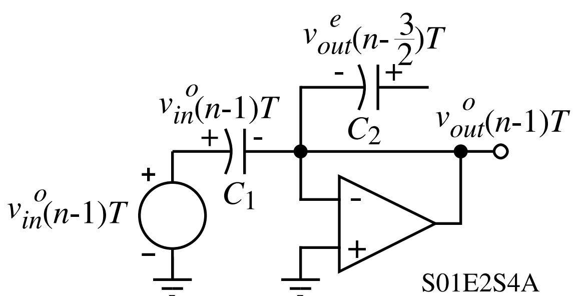


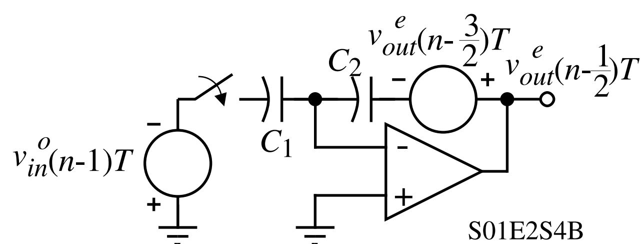
Figure P9.2-6

Solution

ϕ_1, t=(n-1)T:
Circuit:

ϕ_2, t=(n-0.5)T:
Circuit:





Writing the output,

$$v_{out}^{e}(n\text{-}0.5)) = v_{out}^{e}(n\text{-}1.5)) + \frac{C_1}{C_2}v_{in}^{o}(n\text{-}1)) \;\rightarrow\; V_{out}^{e}(z)) = z^{-1}V_{out}^{e}(z) + \frac{C_1}{C_2}\;z^{-0.5}V_{in}^{o}(z))$$

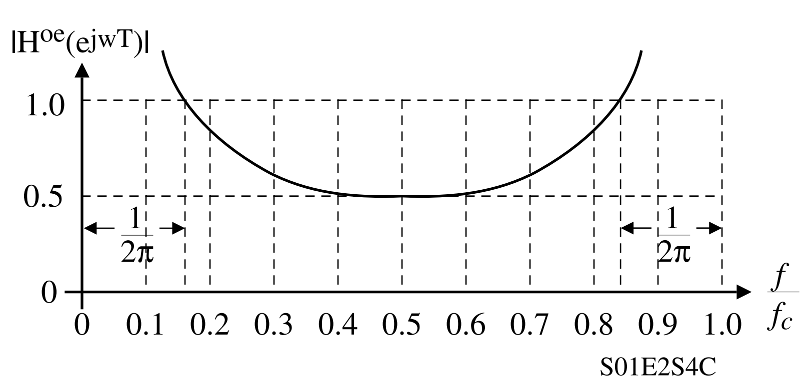
$$\therefore\;\; H^{oe}(z) = \frac{V_{out}^{e}(z)}{V_{in}^{o}(z)} = \frac{(C_1/C_2)z^{-0.5}}{1\text{-}z^{-1}}$$

Replacing z by $e^{j\omega T}$ gives $H^{oe}(e^{j\omega T}) = \dfrac{(C_1/C_2)e^{-j\omega T/2}}{1\text{-}e^{-j\omega T}}\,\text{x}\,\dfrac{e^{j\omega T/2}}{e^{j\omega T/2}} = \dfrac{(C_1/C_2)}{e^{j\omega T/2}\text{-}e^{-j\omega T}}$

$$H^{oe}(e^{j\omega T}) = \frac{(C_1/C_2)}{2jsin(\omega T/2)}\,\text{x}\,\frac{\omega T}{\omega T} = \frac{C_1}{j\omega C_2 f}\;\frac{\omega T/2}{sin(\omega T/2)}$$ (note there is no phase error)

If $C_1 = C_2$, then $H^{oe}(e^{j\omega T}) = \dfrac{f_c}{j2\pi f}\;\dfrac{\pi f/f_c}{sin(\pi f/f_c)}$

Sketch of frequency response:



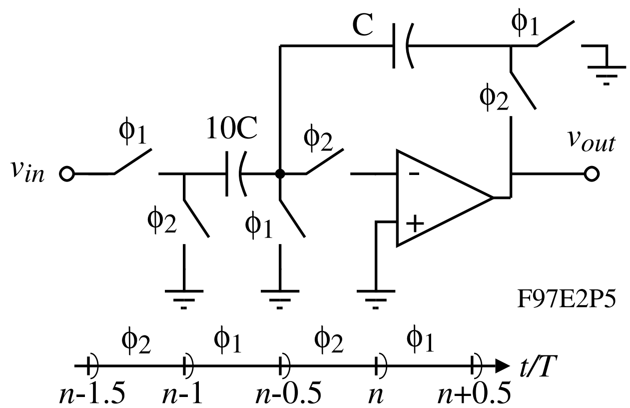
f/f_c	$\lvert H^{oe}(e^{j2\pi f/f_c})\rvert$
$1/2\pi$	1
0.5	0.5
$1\text{-}0.5\pi$	1

Phase shift is a constant -90°.

Problem 9.2-07

(a.) Find $H^{oo}(z)$ for the switched capacitor circuit shown. Ignore the fact that the op amp is open loop during the ϕ_1 phase and assume that the output is sampled during ϕ_2 and held during ϕ_1. Note that some switches are shared between the two switched capacitors.

(b.) Sketch the magnitude and phase of the sampled data frequency response from 0 to the clock frequency in Hertz.



F97E2P5

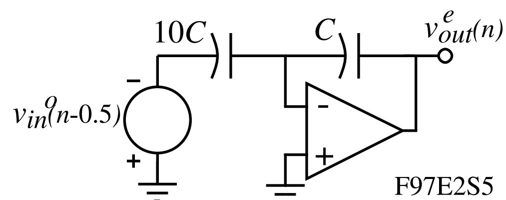
Solution:

$\phi_1(n\text{-}0.5)$:

During this phase, the 10C capacitor is charged to $v_{in}^o(n\text{-}0.5)$ and the output is sampled and held.

$\phi_2(n)$:

Model for calculating v_{out}^e(n),



F97E2S5

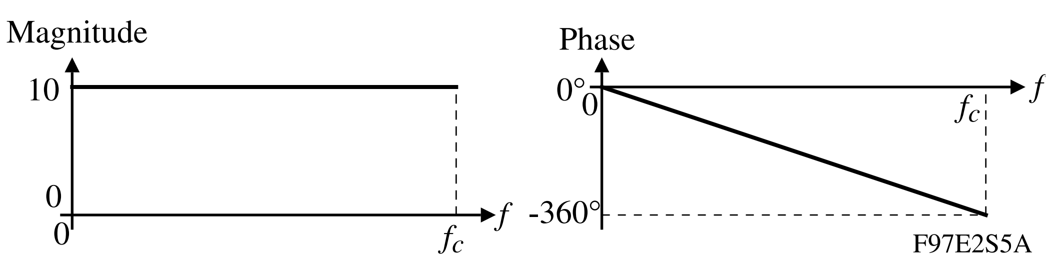
$\therefore\ v_{out}^e(n) = 10v_{in}^o(n\text{-}0.5)$

Since the output is sampled and held during the next phase period, we can write

$$v_{out}^o(n+0.5) = v_{out}^e(n) = 10v_{in}^o(n\text{-}0.5) \quad \rightarrow \quad V_{out}^o(z) = 10z^{-1}V_{in}^o(z)$$

or $\boxed{H^{oo}(z) = 10z^{-1}}$

b.)



F97E2S5A

Problem 9.2-08

In the circuit shown, the capacitor C_1 has been charged to a voltage of V_{in} (v_{in}>0). Assuming that C_2 is uncharged, find an expression for the output voltage, V_{out}, after the ϕ_1 clock is applied. Assume that rise and fall times of the ϕ_1 clock are slow enough so that the channel of the NMOS transistor switch tracks the gate voltage. The on and off voltages of ϕ_1 are 10V and 0V, respectively. Evaluate the dc offset at the output if the various parameters for this problem are V_T = 1V, $C_{gs} = C_{gd}$ = 100fF, C_1 = 5pF, and C_2 = 1pF.

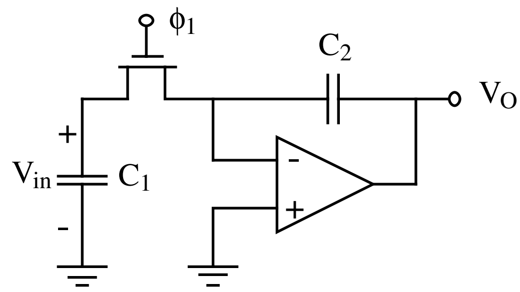


Figure P9.2-8

Solution

Since the problem does not give the value of V_{in} or the slope of the gate voltage, we shall assume that the contribution to the feedthrough due to the channel can be neglected. Therefore, the output voltage after the switch opens up can be expressed as,

$$V_o = -\frac{C_1}{C_2}V_{in} - \left(\frac{C_{gd}}{C_{gd}+C_1}\right)(V_T) = -5V_{in} - \frac{1}{11} = -5V_{in} - \frac{1}{11}$$

The dc offset is 1/11V or 91mV.

A closer look at the problem reveals that there will also be feedthrough during the turn-on part of the ϕ_1 clock which should be considered. However, if we are going to consider this then we should also consider how C_1 was charged. It is most likely the complete circuit looks like the one shown.

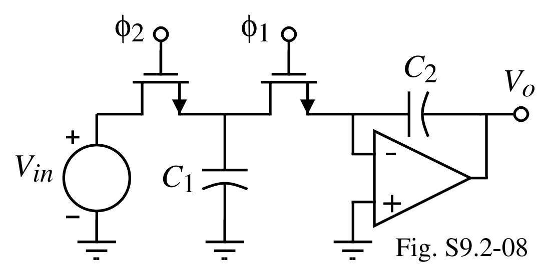


Fig. S9.2-08

When ϕ_2 is turned off, the voltage across C_1 is,

$$V_{C1}(\phi_2 \text{ off}) = V_{in} - \left(\frac{C_{gd}}{C_{gd}+C_1}\right)(V_{in}+V_T) = V_{in} - \frac{1}{11}V_{in} - \frac{1}{11}$$

When $\phi_1$turns on, the voltage across C_1 is,

$$V_{C1}(\phi_1 \text{ on}) = V_{C1}(\phi_2 \text{ off}) + \left(\frac{C_{gd}}{C_{gd}+C_1}\right)(V_T) = V_{in} - \frac{1}{11}V_{in} - \frac{1}{11} + \frac{1}{11} = V_{in} - \frac{1}{11}V_{in}$$

Finally, when $\phi_1$turns off, the voltage across C_1 is,

$$V_{C1}(\phi_1 \text{ off}) = -5V_{C1}(\phi_1 \text{ on}) - \left(\frac{C_{gd}}{C_{gd}+C_1}\right)(V_T) = 5V_{in} - \frac{5}{11}V_{in} - \frac{1}{11} = -\frac{51}{11}V_{in} - \frac{1}{11}$$

The dc offset is still the same as above.

Problem 9.2-09

A switched-capacitor amplifier is shown. What is the maximum clock frequency that would permit the ideal output voltage to be reached to within 1% if the op amp has a dc gain of 10,000 and a single dominant pole at -100 rads/sec.? Assume ideal switches.

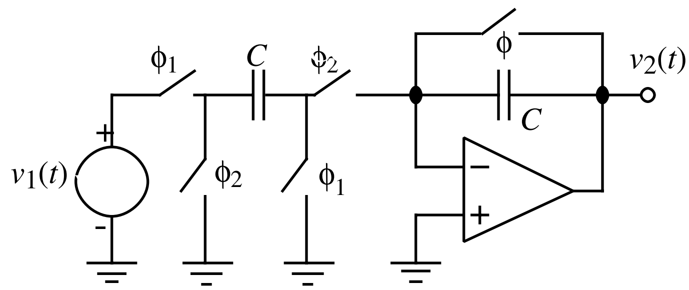
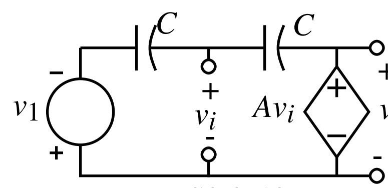


Figure P9.2-9

Solution

Model at t=0+ for the ϕ_2 phase:



S9.2-12

$$\text{where } A = \frac{10^4}{\frac{s}{100}+1} \approx \frac{10^6}{s}$$

if $\omega >> 100$.

$$V_o(s) = AV_i(s) = A\left[+\frac{V_1(s)}{2} - \frac{V_o(s)}{2}\right] \quad \rightarrow \quad V_o(s)\left[1+\frac{A}{2}\right] = \frac{A}{2}V_1(a)$$

$$\therefore \quad V_o(s) = \frac{\frac{A}{2}}{1+\frac{A}{2}}V_1(a) = \frac{\frac{1}{2}}{\frac{1}{A}+\frac{1}{2}}V_1(a) \approx \frac{\frac{1}{2}}{\frac{s}{10^6}+\frac{1}{2}}V_1(a) = \frac{0.5\text{x}10^6}{s+0.5\text{x}10^6}V_1(a)$$

$$v_o(t) = \mathrm{L}^{-1}\left[\frac{0.5\text{x}10^6}{s+0.5\text{x}10^6}\cdot\frac{V_1}{s}\right] = \frac{A}{s} + \frac{B}{s+0.5\text{x}10^6}$$

$$A = \frac{0.5\text{x}10^6}{s+0.5\text{x}10^6}V_1 \Big|_{s=0} = V_1 \quad \text{and} \quad B = \frac{0.5\text{x}10^6}{s}V_1 \Big|_{s=0.5\text{x}10^6} = -V_1$$

$$\therefore \quad v_o(t) = V_1[1-\mathrm{e}^{-0.5\text{x}10^6 t}]$$

Let $t = T$ correspond to $v_o(T) = 0.99V_1$

$$\therefore \quad 0.99V_1 = V_1[1-\mathrm{e}^{-0.5\text{x}10^6 T}] \quad \rightarrow \quad 100 = \mathrm{e}^{0.5\text{x}10^6 T}$$

$$ln(100) = 0.5\text{x}10^6 T \quad \rightarrow \quad T = 2\text{x}10^{-6} ln(100) = 9.21\mu\text{s}$$

Assuming a square wave, T would be half the period so the minimum clock frequency would be

$$f_{clock}(\text{min}) = \frac{2}{T} = \underline{\underline{54.287\text{kHz}}}$$

Problem 9.2-10

The switched capacitor circuit in Fig. 9.2-9 is an amplifier that avoids shorting the output of the op amp to ground during the ϕ_1 phase period. Use the clock scheme shown along with the timing and find the z-domain transfer function, $H^{oo}(z)$. Sketch the magnitude and phase shift of this amplifier from zero frequency to the clock frequency, f_c.

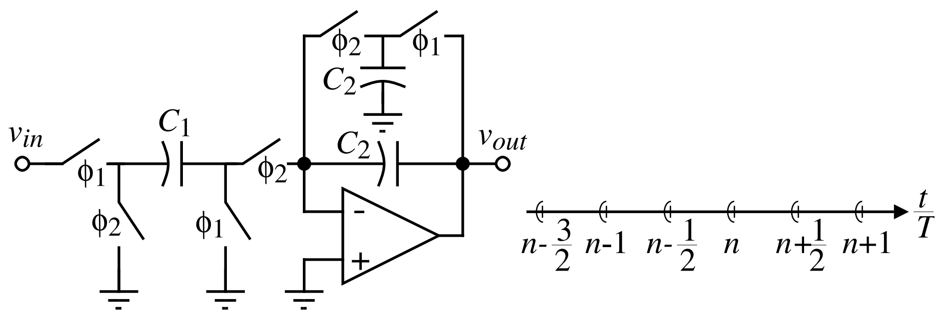


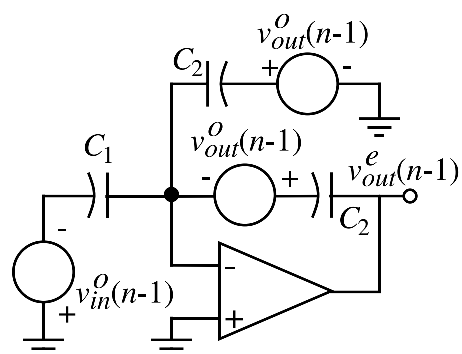
Fig. P9.2-13

Solution

ϕ_1: $(n\text{-}1) \le t/T < (n\text{-}0.5)$

$v^o_{c1}(n\text{-}1) = v^o_{in}(n\text{-}1)$ and $v^o_{c2}(n\text{-}1) = v^o_{out}(n\text{-}1)$

ϕ_2: $(n\text{-}0.5) \le t/T < (n)$



$$v^e_{out}(n\text{-}0.5) = v^o_{out}(n\text{-}1) + \frac{C_1}{C_2} v^o_{in}(n\text{-}1) - \frac{C_2}{C_2} v^o_{out}(n\text{-}1)$$

or

$$v^e_{out}(n\text{-}0.5) = \frac{C_1}{C_2} v^o_{in}(n\text{-}1)$$

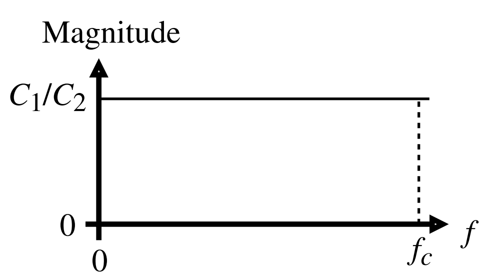
ϕ_1: $(n) \le t/T < (n+0.5)$

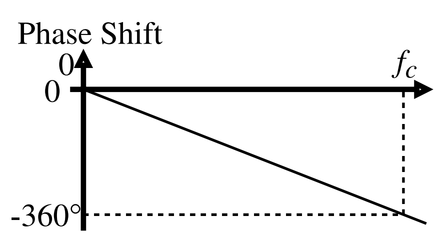
$$v^o_{out}(n) = v^e_{out}(n\text{-}1) = \frac{C_1}{C_2} v^o_{in}(n\text{-}1) \quad \rightarrow \quad V^o_{out}(z) = z^{-1} \frac{C_1}{C_2} V^o_{in}(z) \quad \rightarrow \quad \boxed{H^{oo}(z) = \frac{C_1}{C_2} z^{-1}}$$

Substitituting z^{-1} by $e^{-j\omega T}$ gives

$$H^{oo}(e^{j\omega T}) = \frac{C_1}{C_2} e^{-j\omega T}$$

The magnitude and phase response is given below.





Problem 9.2-11

(a.) Give a schematic drawing of a switched capacitor realization of a voltage amplifier having a gain of H^{oo} = +10V/V using a two-phase nonoverlapping clock. Assume that the input is sampled on the ϕ_1 and held during ϕ_2. Use op amps, capacitors, and switches with ϕ_1 or ϕ_2 indicating the phase the switch is closed.

(b.) Give a schematic of the circuit in (a.) that reduces the number of switches to a minimum number with the circuit working correctly. Assume the op amp is ideal.

(c.) Convert the circuit of (a.) to a differential implementation using the differential-in, differential-out op amp shown in Fig. P9.2-11.

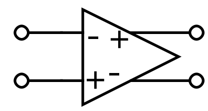
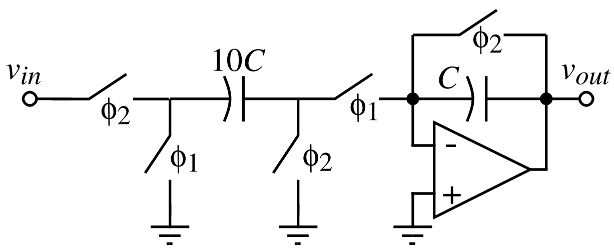


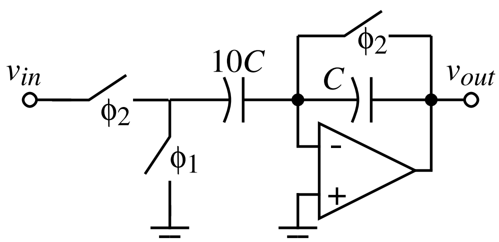
Figure P9.2-11

Solution

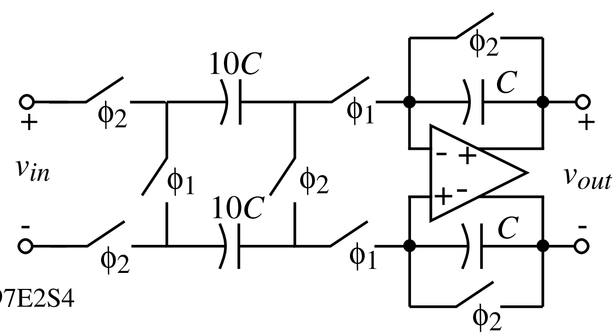
a.)



b.)



c.)



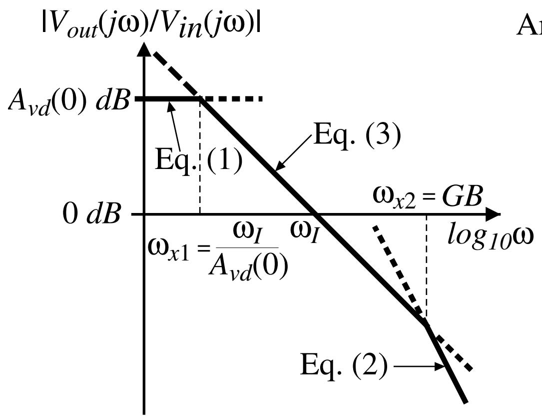
F97E2S4

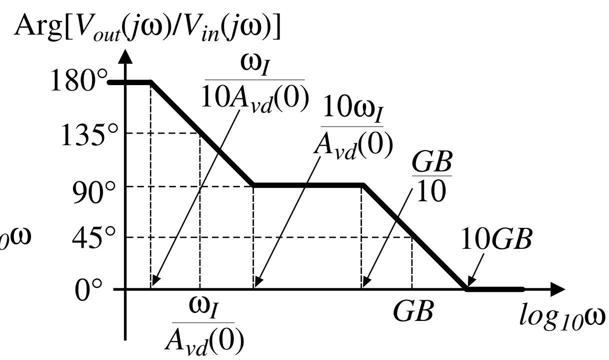
Problem 9.3-01

Over what frequency range will the integrator of Ex. 9.3-1 have a ±1° phase error?

Solution

Assuming the integrator frequency response can be represented as shown below.





The integrator phase error on the low side of the useful band is given as,

$$\text{Error} = 90° - \tan^{-1}\left(\frac{\omega_L}{\omega_I/A_{vd}(0)}\right) = 1° \qquad \rightarrow \qquad \omega_L = 57.29\,\frac{\omega_I}{A_{vd}(0)}$$

The integrator phase error on the high side of the useful band is given as,

$$\text{Error} = \tan^{-1}\left(\frac{\omega_H}{GB}\right) = 1° \qquad \rightarrow \qquad \omega_H = \frac{GB}{57.29}$$

If $A_{vd}(0)$, ω_I, and GB are given, the useful range is from ω_L to ω_H.

Problem 9.3-02

Show how Eq. (9.3-12) is developed from Fig. 9.3-4(b.).

Solution

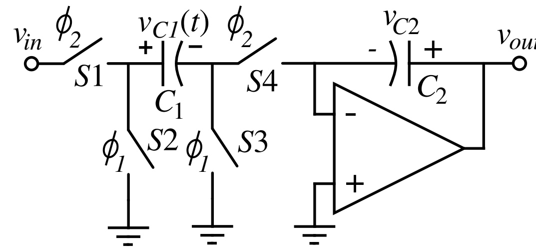


Fig. 9.3-4(b.)

Problem 9.3-03

Find the $H^{eo}(j\omega T)$ transfer function for the inverting integrator of Fig. 9.3-4b and compare with the $H^{ee}(j\omega T)$ transfer function.

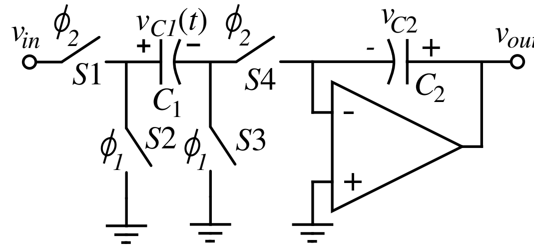


Fig. 9.3-4(b.)

Solution

Problem 9.3-04

An inverting, switched-capacitor integrator is shown. If the gain of the op amp is A_o, find the z-domain transfer function of this integrator. Identify the ideal part of the transfer function and the part due to the finite op amp gain, A_o. Find an expression for the excess phase due to A_o.

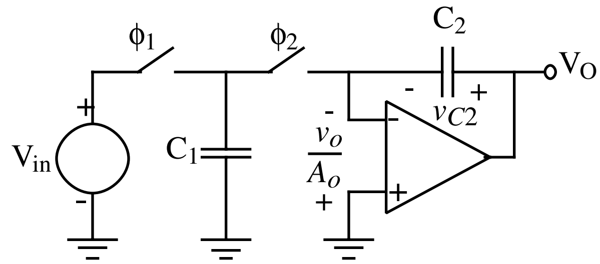


Figure P9.3-4

Solution

Let us use charge conservation to solve the problem.

$$C_2v_{C2}(nT) = C_2v_{C2}[(n\text{-}1)T] - C_1[v_{in}\,(n\text{-}1)T + v_o(nT)/A_o]$$

or

$$V_{C2}(z) = z^{-1}V_{C2}(z) - \frac{C_1}{C_2}z^{-1}V_{in}(z) - \frac{C_1}{C_2}\frac{V_o(z)}{A_o}$$

$$V_{C2}(z)[1- z^{-1}] = -\alpha\, z^{-1}V_{in}(z) - \alpha\frac{V_o(z)}{A_o}, \qquad \text{where } \alpha = \frac{C_1}{C_2}$$

$$V_{C2}(z) = \frac{-\alpha\, z^{-1}}{1- z^{-1}}V_{in}(z) - \frac{-\alpha/A_o}{1- z^{-1}}V_o(z)$$

$$\therefore \qquad V_o(z) = V_{C2}(z) - \frac{V_o(z)}{A_o} = \frac{-\alpha\, z^{-1}}{1- z^{-1}}V_{in}(z) - \frac{-\alpha/A_o}{1- z^{-1}}V_o(z) - \frac{V_o(z)}{A_o}\text{ x }\frac{1- z^{-1}}{1- z^{-1}}$$

$$V_o(z)\left[1- z^{-1} + \frac{\alpha}{A_o} + \frac{1- z^{-1}}{A_o}\right] = -\alpha\, z^{-1}V_{in}(z)$$

$$\therefore \qquad H(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{-\alpha\, z^{-1}}{1- z^{-1} + \dfrac{1+\alpha - z^{-1}}{A_o}} = \left(\frac{-\alpha\, z^{-1}}{1- z^{-1}}\right)\left(\frac{1}{1+\dfrac{1+\alpha - z^{-1}}{A_o(1- z^{-1})}}\right)$$

The first bracket is the ideal term and the second bracket is the term due to A_o.

To evaluate the excess phase due to A_o we replace z by $e^{j\omega T}$.

$$H(e^{j\omega T}) = \frac{1}{1+\dfrac{1+\alpha - z^{-1}}{A_o(1- z^{-1})}} = \frac{1}{1+\dfrac{(1+\alpha)\,e^{j\omega T/2}}{A_o(e^{j\omega T/2}- e^{-j\omega T/2})} + \dfrac{e^{j\omega T/2}}{A_o(e^{j\omega T/2}- e^{-j\omega T/2})}}$$

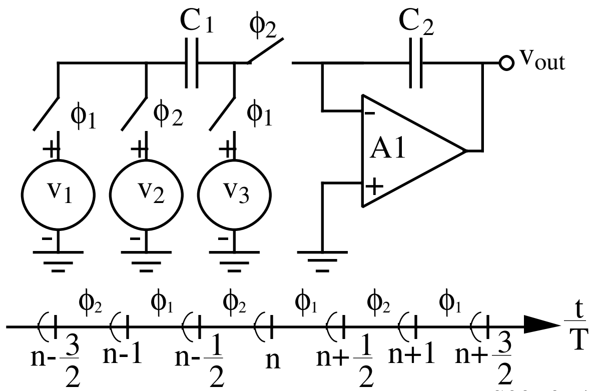
$$= \frac{1}{1\ -\ \mathrm{j}\left(\dfrac{1+\alpha}{2A_o}\right)\left(\dfrac{cos(\omega T/2) + \mathrm{j}sin(\omega T/2)}{sin(\omega T/2)}\right) + \dfrac{j}{2A_o}\left(\dfrac{cos(\omega T/2) + \mathrm{j}sin(\omega T/2)}{sin(\omega T/2)}\right)}$$

$$= \frac{1}{1\ +\ \dfrac{2+\alpha}{A_o}\ -\ \mathrm{j}\ \dfrac{\alpha}{2A_o}cot(\omega T/2)} \rightarrow \text{Arg}[H(e^{j\omega T})] = \text{-tan}^{-1}\left[\frac{\dfrac{\alpha}{2A_o}cot(\omega T/2)}{1\ +\ \dfrac{2+\alpha}{A_o}}\right]$$

$$\therefore\ \text{Excess phase} = \text{-tan}^{-1}\left[\frac{\alpha\, cot(\omega T/2)}{2A_o\ +\ 4\ +\ 2\alpha}\right] \approx \text{-tan}^{-1}\left[\frac{\alpha}{2A_o\, tan(\omega T/2)}\right] \approx -\frac{\alpha}{2A_o\, tan(\omega T/2)}$$

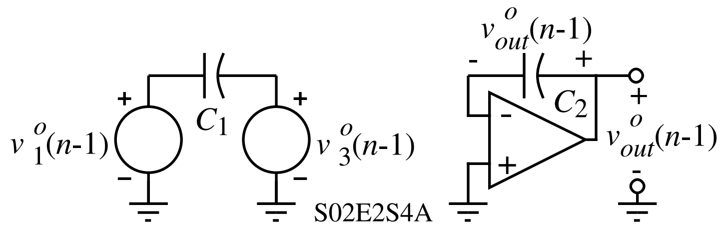
Problem 9.3-05

For the switched-capacitor circuit shown find $V^o_{OUT}(z)$ as a function of $V^o_1(z)$, $V^o_2(z)$, and $V^o_3(z)$ assuming the clock is a two-phase, nonoverlapping clock. Assume that the clock frequency is much greater than the signal bandwidth and find an approximate expression for $V_{out}(s)$ in terms of $V_1(s)$, $V_2(s)$, and $V_3(s)$. Assume that the inputs are sampled and held where necessary.



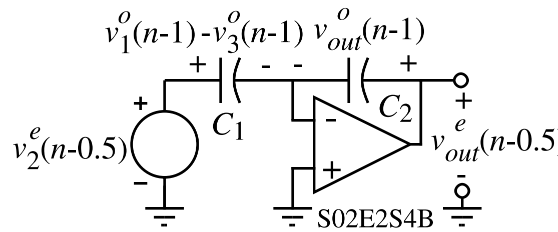
Solution

ϕ_1, $t = (n\text{-}1)T$: Model:



ϕ_2, $t = (n\text{-}0.5)T$: Model:

$$v^e_{out}(n\text{-}0.5) = v^o_{out}(n\text{-}1) - \frac{C_1}{C_2}v^e_2(n\text{-}0.5) - \frac{C_1}{C_2}v^o_1(n\text{-}1) + \frac{C_1}{C_2}v^o_3(n\text{-}1)$$



ϕ_1, $t = (n)T$:

$$v^o_{out}(n) = v^o_{out}(n\text{-}1) - \frac{C_1}{C_2}v^e_2(n\text{-}0.5) + \frac{C_1}{C_2}v^o_1(n\text{-}1) - \frac{C_1}{C_2}v^o_3(n\text{-}1)$$

$$\therefore \quad V^o_{out}(z) = z^{-1}V^o_{out}(n\text{-}1) - z^{-0.5}\frac{C_1}{C_2}V^e_2(z) + z^{-1}\frac{C_1}{C_2}V^o_1(z) - z^{-1}\frac{C_1}{C_2}V^o_3(z)$$

Replacing $V^e_2(z)$ by $z^{-0.5}V^o_2(z)$ gives

$$V^o_{out}(z) = z^{-1}V^o_{out}(n\text{-}1) - z^{-1}\frac{C_1}{C_2}V^o_2(z) + z^{-1}\frac{C_1}{C_2}V^o_1(z) - z^{-1}\frac{C_1}{C_2}V^o_3(z)$$

$$V^o_{out}(z) = -\frac{z^{-1}}{1\text{-}z^{-1}}[-V^o_1(z) + V^o_2(z) + V^o_3(z)]$$

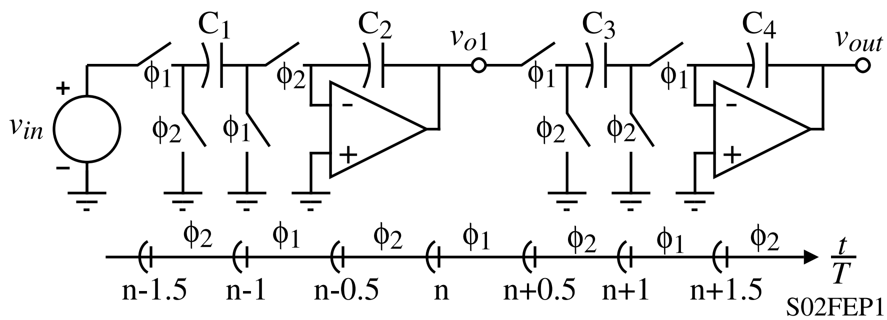
Replacing 1- z^{-1} by sT and z^{-1} by 1 gives,

$$V^o_{out}(s) = -\frac{1}{sT}[-V^o_1(s) + V^o_2(s) + V^o_3(s)]$$

$$\therefore \quad \boxed{V^o_{out}(s) = \frac{1}{sT}[V^o_1(s) - V^o_2(s) - V^o_3(s)]}$$

Problem 9.3-06

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oo}(z)$. (2.) Replace z by $e^{j\omega T}$ and plot the magnitude and phase of this switched capacitor circuit from 0 Hz to the clock frequency, f_c, if $C_1 = C_3$ and $C_2 = C_4$. Assume that the op amps are ideal for this problem. (3.) What is the multiplicative magnitude error and additive phase error at $f_c/2$?



Solution

(1.) ϕ_1 (n-1≤t/T<n-0.5):

$$q_{C1}^{o}(n\text{-}1) = C_1 v_{in}^{o}(n\text{-}1) \qquad \text{and} \qquad q_{C2}^{o}(n\text{-}1) = C_2 v_{o1}^{o}(n\text{-}1)$$

ϕ_2 (n-0.5≤t/T<n):

$$q_{C2}^{e}(n\text{-}0.5) = q_{C2}^{o}(n\text{-}1) + q_{C1}^{o}(n\text{-}1) \qquad \text{and} \qquad q_{C4}^{e}(n\text{-}0.5) = C_4 v_{out}^{e}(n\text{-}0.5)$$

ϕ_1 (n≤t/T<n+0.5):

$$q_{C2}^{o}(n) = q_{C2}^{e}(n\text{-}0.5) = q_{C2}^{o}(n\text{-}1) + q_{C1}^{o}(n\text{-}1)$$

$$v_{o1}^{o}(n) = v_{o1}^{o}(n\text{-}1) + \frac{C_1}{C_2} v_{in}^{o}(n\text{-}1) \qquad \rightarrow \qquad V_{o1}^{o}(z) = z^{-1}V_{o1}^{o}(z) + \frac{C_1}{C_2} V_{in}^{o}(z)$$

$$\therefore \qquad V_{o1}^{o}(z) = \frac{C_1/C_2}{z\text{-}1} V_{in}^{o}(z)$$

Also, $q_{C3}^{o}(n) = C_3\, v_{o1}^{o}(n)$ and $q_{C4}^{o}(n) = q_{C4}^{e}(n\text{-}0.5) - q_{C3}^{o}(n)$

$$q_{C4}^{o}(n) = q_{C4}^{o}(n\text{-}1) - q_{C3}^{o}(n) \qquad \rightarrow \qquad V_{out}^{o}(z) = z^{-1}V_{o1}^{o}(z) - \frac{C_3}{C_4} V_{o1}^{o}(z)$$

$$\therefore \qquad V_{out}^{o}(z) = \frac{-(C_3/C_4)z^{-1}}{z\text{-}1} V_{in}^{o}(z)$$

$$\therefore \qquad V_{out}^{o}(z) = \left(\frac{-(C_3/C_4)z^{-1}}{z\text{-}1}\right)\left(\frac{C_1/C_2}{z\text{-}1}\right) V_{in}^{o}(z) \;\rightarrow\; H_{oo}(z) = \frac{V_{out}^{o}}{V_{in}^{o}} = -\left(\frac{C_1C_3}{C_2C_4}\right)\frac{z}{(z\text{-}1)^2}$$

Problem 9.3-06 – Continued

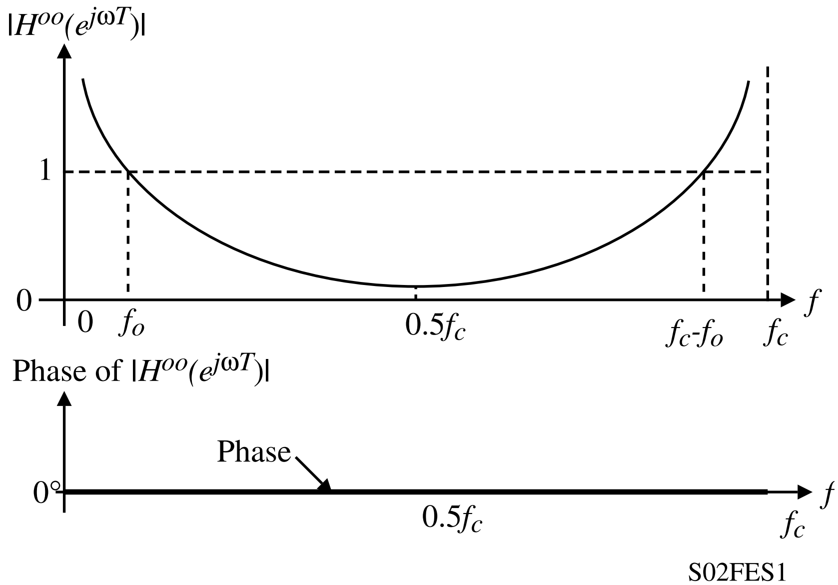
$$\therefore\ H^{oo}(e^{j\omega T}) = -\left(\frac{C_1C_3}{C_2C_4}\right)\frac{e^{j\omega T}}{(e^{j\omega T}-1)^2} = -\left(\frac{C_1C_3}{C_2C_4}\right)\frac{1}{(e^{j\omega T/2}-e^{-j\omega T/2})^2} = -\left(\frac{C_1C_3}{C_2C_4}\right)\frac{1}{(2j\sin(\omega T/2))^2}$$

$$= -\left(\frac{C_1C_3}{C_2C_4}\right)\left(\frac{(\omega T/2)}{j\omega T\sin(\omega T/2)}\right)^2 = \left(\frac{-C_1}{j\omega TC_2}\,\frac{\omega T/2}{\sin(\omega T/2)}\right)\left(\frac{C_3}{j\omega TC_4}\,\frac{\omega T/2}{\sin(\omega T/2)}\right)$$

$$= \left(\frac{-\omega_{o1}}{j\omega}\right)\left(\frac{-\omega_{o2}}{j\omega}\right)\left(\frac{(\omega T/2)}{\sin(\omega T/2)}\right)^2 = \left(\frac{-\omega_o}{j\omega}\right)^2\left(\frac{(\omega T/2)}{\sin(\omega T/2)}\right)^2$$

If $C_1 = C_3$ and $C_2 = C_4$, $\omega_{o1} = C_1/(TC_2)$, and $\omega_{o2} = C_3/(TC_4)$.

The frequency response is plotted below.



$$\therefore\ \text{The magnitude error} = \left(\frac{(\omega T/2)}{\sin(\omega T/2)}\right)^2 = \left(\frac{(\pi/2)}{\sin(\pi/2)}\right)^2 = \frac{\pi^2}{4} = 2.467$$

Phase error = 0°

Problem 9.3-07

Find $H^{oo}(z)$ $(=V^{o}_{out}(z)/V^{o}_{in}(z))$ of the switched capacitor circuit shown. Replace z by $e^{j\omega t}$ and identify the magnitude and phase response of this circuit. Assume $C_1/C_2 = \pi/25$. Sketch the exact magnitude and phase response on a linear-linear plot from f=0 to f=f_c. What is the magnitude and phase at f = 0.5f_c? Assume that the op amp is ideal.

Solutions

ϕ_2; $(n\text{-}0.5)<t/T<n$

At $t=0^+$ we have the following model:

We can write,

$$v^{e}_{out}(n-0.5) = v^{o}_{out}(n-1) - \frac{C_1}{C_2} v^{o}_{in}(n-1)$$

But $v^{e}_{out}(n) = v^{e}_{out}(n-0.5) = v^{o}_{out}(n-1) - \dfrac{C_1}{C_2} v^{o}_{in}(n-1)$

$$\therefore \qquad V^{o}_{out}(z) = z^{-1}V^{o}_{out}(z) - \frac{C_1}{C_2} z^{-1}V^{o}_{in}(z) \qquad \rightarrow \qquad H^{oo}(z) = \frac{\frac{C_1}{C_2}z^{-1}}{1-z^{-1}}$$

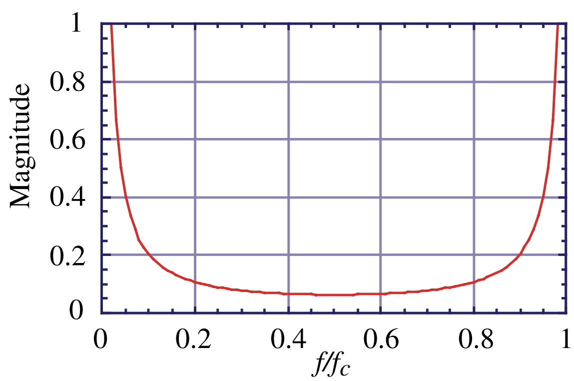
$$H^{oo}(e^{j\omega T}) = -\frac{C_1}{C_2}\left(\frac{e^{-j\omega T}}{1-e^{-j\omega T}}\right)\frac{e^{j\omega T/2}}{e^{j\omega T/2}} = -\frac{C_1}{C_2}\frac{e^{-j\omega T/2}}{e^{j\omega T/2}-e^{-j\omega T/2}} = -\frac{C_1}{C_2}\frac{e^{-j\omega T/2}}{2j\sin(\omega T/2)} \times \frac{\omega T}{\omega T}$$

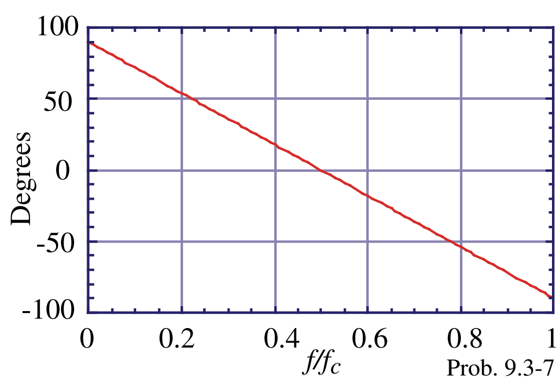
$$= \left(-\frac{C_1}{jC_2\omega T}\right)\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)\left(e^{-j\omega T/2}\right) = \left(-\frac{\omega_o}{j\omega}\right)\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)\left(e^{-j\omega T/2}\right)$$

For $f = 0.5f_c$ we get $\dfrac{\omega T}{2} = \dfrac{2\pi f_c}{2\cdot 2f_c} = \dfrac{\pi}{2}$ and $\omega_o = \dfrac{C_1}{C_2T} = \dfrac{\pi}{25}f_c$

$$\therefore \quad |H^{oo}(e^{j\pi})| = \left(\frac{f_c/50}{f_c/2}\right)\left(\frac{\pi/2}{\sin(\pi/2)}\right) = \frac{1}{25}\frac{\pi}{2} = \underline{\underline{0.06283}} \quad \text{and} \quad \text{Arg}[H^{oo}(e^{j\pi})] = +90°-90° = \underline{\underline{0°}}$$

Plots:





Prob. 9.3-7

Problem 9.3-08

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{ee}(z)$. (2.) If $C_2 = 0.2\pi C_1$, plot the magnitude and phase response of the switched capacitor circuit from 0 rps to the clock frequency (ω_c). Assume that the op amp is ideal for this problem. It may be useful to remember that Eulers formula is $e^{\pm jx} = \cos(x)\pm j\sin(x)$.

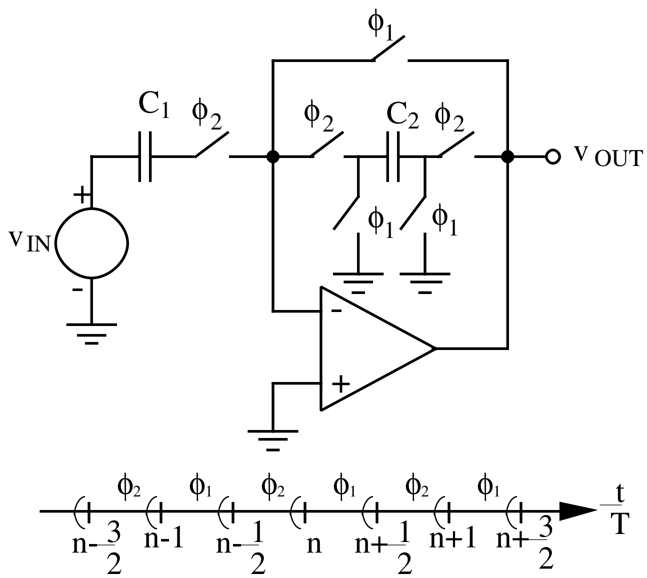


Figure P9.3-8

Solution

ϕ_1: $t=(n-1)T$

The capacitor, C_1, simply holds the voltage, $v_{in}^{e}(n\text{-}1.5)$ and $C_2 = 0\text{V}$.

ϕ_2: $t=(n-0.5)T$

The model for this phase is given.

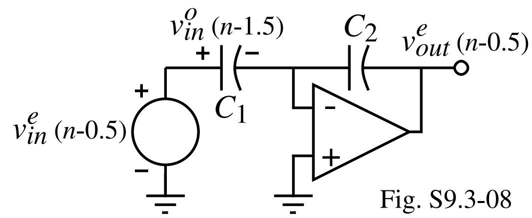


Fig. S9.3-08

The equation for this phase can be written as,

$$v_{out}^{e}(n\text{-}0.5) = -\frac{C_1}{C_2}\, v_{in}^{e}(n\text{-}0.5) + \frac{C_1}{C_2}\, v_{in}^{e}(n\text{-}1.5)$$

Converting to the z-domain gives,

$$z^{-1/2}V_{out}^{e}(z) = -\frac{C_1}{C_2}z^{-1/2}V_{in}^{e}(z) + \frac{C_1}{C_2}z^{-3/2}V_{in}^{e}(z) \quad\rightarrow\quad V_{out}^{e}(z) = -\frac{C_1}{C_2}V_{in}^{e}(z) + \frac{C_1}{C_2}z^{-1}V_{in}^{e}(z)$$

$$\therefore \qquad \frac{V_{out}^{e}(z)}{V_{in}^{e}(z)} = -\frac{C_1}{C_2}(1-z^{-1}) \qquad\rightarrow\qquad \frac{V_{out}^{e}(j\omega)}{V_{in}^{e}(j\omega)} = H^{ee}(j\omega) = -\frac{C_1}{C_2}(1-e^{-j\omega T})\text{x}\frac{e^{j\omega T/2}}{e^{j\omega T/2}}$$

$$H^{ee}(j\omega) = \frac{5}{\pi}\left(\frac{e^{j\omega T/2}- e^{-j\omega T/2}}{e^{j\omega T/2}}\right) = \frac{5}{\pi}[j2\sin(\omega T/2)]\, e^{-j\omega T/2} = \frac{10}{\pi}\frac{j\omega T}{2}\left(\frac{\sin(\omega T/2)}{\omega T/2}\right)e^{-j\omega T/2}$$

$$H^{ee}(j\omega) = j\,\frac{10f}{f_c}\left(\frac{\sin(\omega T/2)}{\omega T/2}\right)e^{-j\omega T/2}$$

Plotting gives,

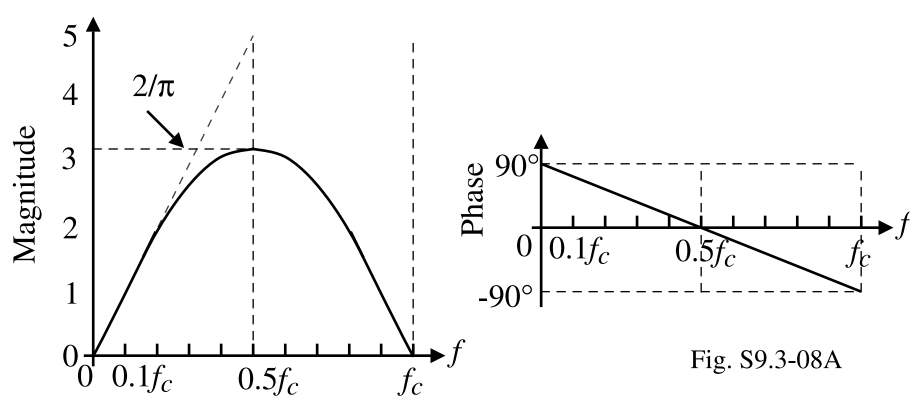
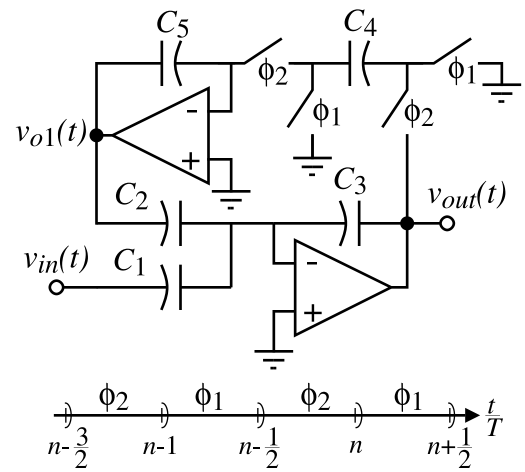


Fig. S9.3-08A

Problem 9.3-09

Find the z-domain transfer function, $H^{oo}(z)$, for the circuit shown. Assume that $C_2 = C_3 = C_4 = C_5$. Also, assume that the input is sampled during ϕ_1 and held through ϕ_2. Next, let the clock frequency be much greater than the signal frequency and find an expression for $H^{oo}(j\omega)$. What kind of circuit is this?



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Solution

ϕ_1: n-1<(t/T)≤n-0.5

$$v_{C4}{}^{o}(n\text{-}0.5) = v_{out}{}^{o}(n\text{-}0.5)$$

$$v_{out}{}^{o}(n\text{-}0.5) = -\frac{C_1}{C_3}v_{in}{}^{o}(n\text{-}0.5) - \frac{C_2}{C_3}v_{o1}(n\text{-}0.5) = v_{out}{}^{e}(n\text{-}1)$$

ϕ_2: n-0.5<(t/T)≤n

$$v_{o1}{}^{e}(n) = v_{o1}{}^{o}(n\text{-}0.5) - \frac{C_4}{C_5}v_{out}{}^{e}(n) \quad \text{and} \quad v_{out}{}^{e}(n) = -\frac{C_2}{C_3}v_{o1}{}^{e}(n) - \frac{C_1}{C_3}v_{in}{}^{e}(n)$$

$$\therefore \; v_{out}{}^{e}(n) = -\frac{C_2}{C_3}\left[v_{o1}{}^{o}(n\text{-}0.5) - \frac{C_4}{C_5}v_{out}{}^{e}(n)\right] - \frac{C_1}{C_3}v_{in}{}^{e}(n)$$

ϕ_1: n<(t/T)≤n+0.5

$$v_{out}{}^{o}(n+0.5) = -\frac{C_1}{C_3}v_{in}{}^{o}(n+0.5) - \frac{C_2}{C_3}v_{o1}{}^{o}(n+0.5) \rightarrow V_{out}{}^{o}(z) = -\frac{C_1}{C_3}V_{in}{}^{o}(z) - \frac{C_2}{C_3}V_{o1}{}^{o}(z)$$

but, $\quad v_{o1}{}^{o}(n+0.5) = v_{o1}{}^{e}(n) = v_{o1}{}^{o}(n\text{-}0.5) + \dfrac{C_4}{C_5}v_{out}{}^{o}(n\text{-}0.5)$

$$V_{o1}{}^{o}(z) = z^{-1}V_{o1}{}^{o}(z) - \frac{C_4}{C_5}V_{out}{}^{o}(z) \quad \rightarrow \quad V_{o1}{}^{o}(z)[1\text{-}z^{-1}] = -\frac{C_4}{C_5}V_{out}{}^{o}(z)$$

Substituting into the above expression for $V_{out}{}^{o}(z)$ gives

$$V_{out}{}^{o}(z) = -\frac{C_1}{C_3}V_{in}{}^{o}(z) + \frac{C_2}{C_3}\left(\frac{C_4}{C_5}\frac{1}{1\text{-}z^{-1}}\right)V_{out}{}^{o}(z) \quad \rightarrow \quad H^{oo}(z) = \frac{-C_1/C_3}{1 - \left(\frac{C_2C_4}{C_3C_5}\right)\frac{1}{1\text{-}z^{-1}}}$$

If $C_2C_4 = C_3C_5$, then $\boxed{H^{oo}(z) = \frac{C_1}{C_3}\left[\frac{1\text{-}z^{-1}}{z^{-1}}\right]} \rightarrow H^{oo}(s) \approx \frac{C_1}{C_3}\left[\frac{1\text{-}(1\text{-}sT)}{1}\right] = \frac{C_1}{C_3}sT$

(This is a lot easier with z-domain models.)

$$\therefore \; \boxed{H^{oo}(j\omega) \approx \frac{j\omega}{C_3/C_1T} = \frac{j\omega}{\omega_D} \text{ where } \omega_D = \frac{C_3}{TC_1}}$$

This circuit is a noninverting switched capacitor differentiator.

Problem 9.4-01

Repeat Ex. 9.4-1 for the positive switched capacitor transresistance circuit of Fig. 9.4-3.

Solution

TBD

Problem 9.4-02

Use the z-domain models to verify Eqs. (9.2-19) and (9.2-23) of Sec. 9.2 for Fig. 9.2-4(b.).

Solution

TBD

Problem 9.4-03

Repeat Ex. 9.4-5 assuming that the op amp is ideal (gain = ∞). Compare with the results of Ex. 9.4-5 (Hint: use Fig. 9.4-8b).

Solution

TBD

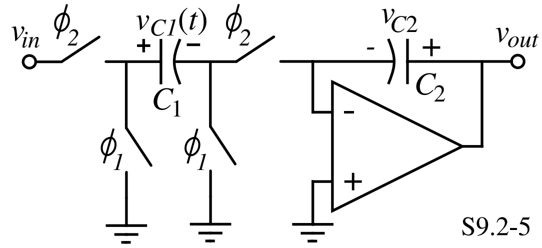
Problem 9.4-04

Repeat Ex. 9.4-5 assuming the op amp gain is 100V/V. Compare with the results of Ex. 9.4-5.

Solution

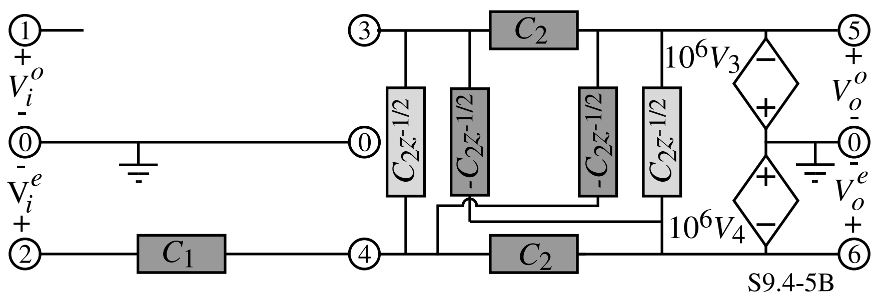
Problem 9.4-05

Repeat Ex. 9.4-5 for the inverting switched capacitor integrator in Fig. 9.3-4(b).



Solution

The z-domain model for this circuit is shown below.



$$\omega_I = \frac{1}{R_1C_2} = \frac{f_cC_1}{C_2} \qquad \Rightarrow \qquad \frac{C_1}{C_2} = \frac{2\pi f_I}{f_c} = \frac{2\pi(10\text{kHz})}{100\text{kHz}} = \frac{\pi}{5} = 0.62832$$

$\therefore$ Let C_2 = 1F and C_1 = 0.62832F

SPICE Input File

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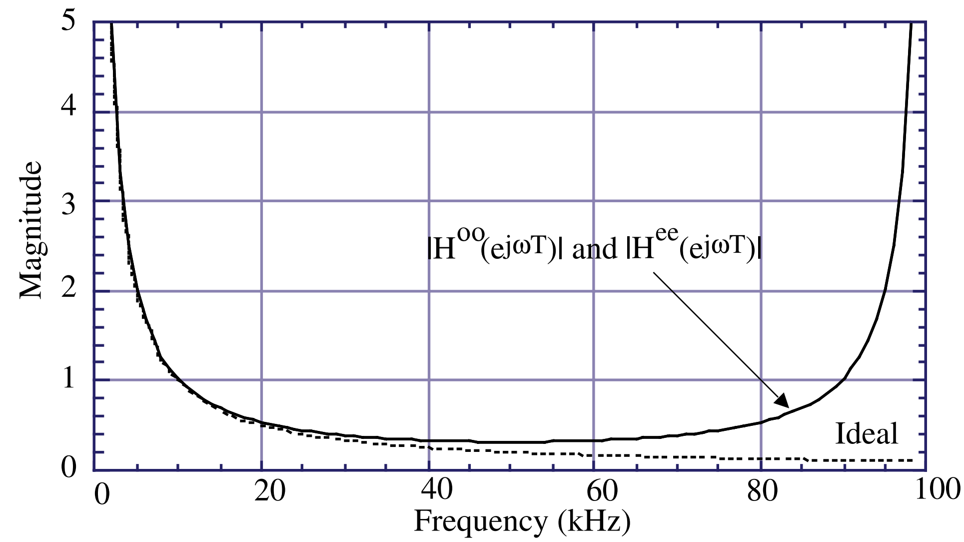
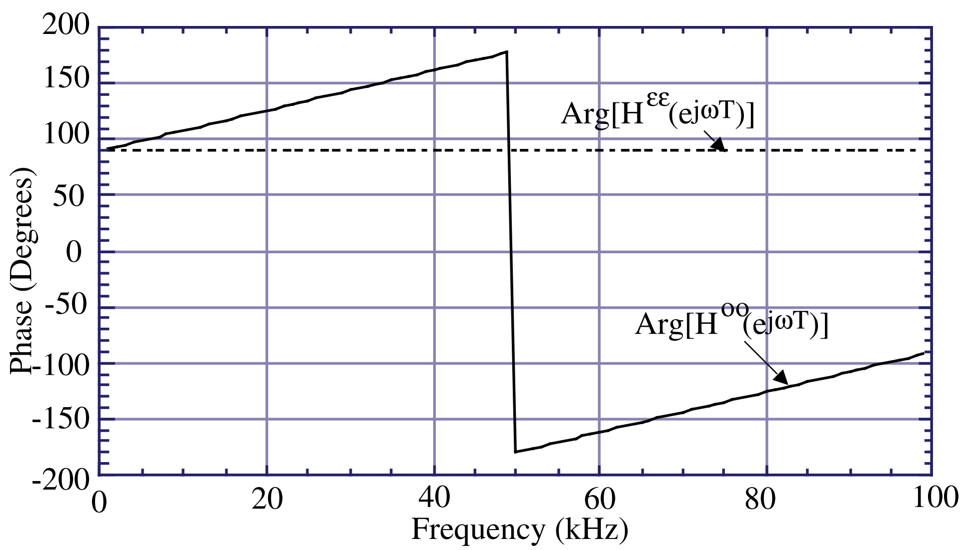
Problem 9.4-5 Solution
R24 2 5 1.592
X43PC2 4 3 43 DELAY
G43 4 3 43 0 1
R35 3 5 1.0
X56PC2 5 6 56 DELAY
G56 5 6 56 0 1
R46 4 6 1.0
X36NC2 3 6 36 DELAY
G36 6 3 36 0 1
X45NC2 4 5 45 DELAY
G45 5 4 45 0 1
EODD 6 0 4 0 1E6
EVEN 5 0 3 0 1E6
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5U
RDO 3 0 1K
.ENDS DELAY
.AC LIN 99 1K 99K
.PRINT AC V(6) VP(6) V(5) VP(5)
.PROBE
.END
```

Problem 9.4-05 - Continued

Plot of the results is below.





Solution 9.4-5

Problem 9.5-01

Develop Eq. (9.5-6) for the inverting low pass circuit obtained from Fig. 9.1-5(a.) by reversing the phases of the leftmost two switches. Verify Eq. (9.5-7).

Solution

TBD

Problem 9.5-02

Use SPICE to simulate the results of Ex. 9.5-1.

Solution

The SPICE model for this problem is given as

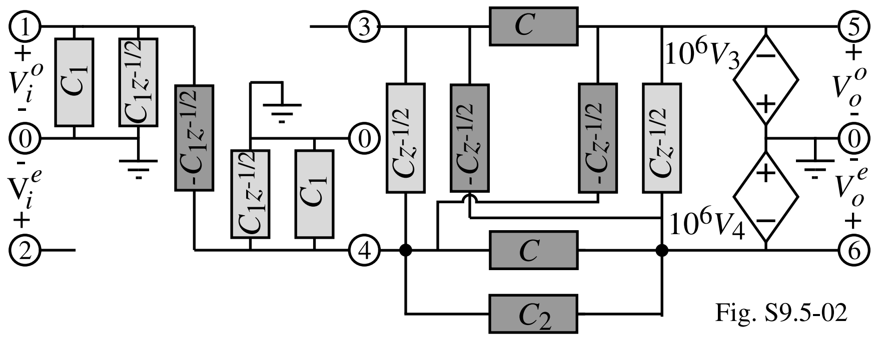


Fig. S9.5-02

The SPICE input file is:

```
PROBLEM 9.5-2 SOLUTION
VIN 1 0 DC 0 AC 1
R10C1 1 0 1.592
X10PC1 1 0 10 DELAY
G10 1 0 10 0 0.6283
X14NC1 1 4 14 DELAY
G14 4 1 14 0 0.6283
R40C1 4 0 1.592
X40PC1 4 0 40 DELAY
G40 4 0 40 0 0.6283
X43PC2 4 3 43 DELAY
G43 4 3 43 0 1
R35 3 5 1.0
X56PC2 5 6 56 DELAY
G56 5 6 56 0 1
R46 4 6 1.0
X36NC2 3 6 36 DELAY
G36 6 3 36 0 1
X45NC2 4 5 45 DELAY
G45 5 4 45 0 1
*R35C2 3 5 15.9155
R46C2 4 6 15.9155
EVEN 6 0 4 0 1E6
EODD 5 0 3 0 1E6
********************
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5U
RDO 3 0 1K
.ENDS DELAY
********************
.AC LIN 1000 1 100K
.PRINT AC V(6) VP(6) V(5) VP(5) VDB(5) VDB(6)
.PROBE
.END
```

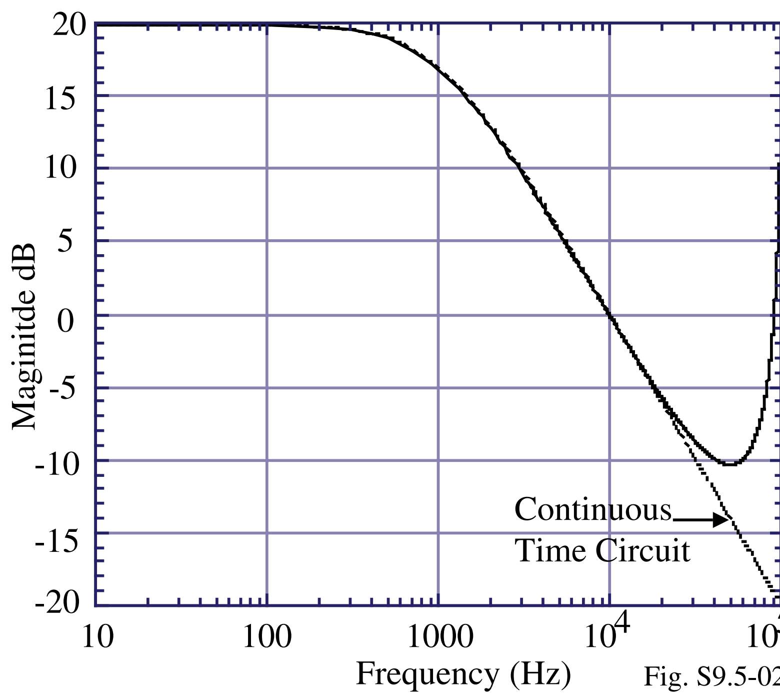


Fig. S9.5-02A

Problem 9.5-03

Repeat Ex. 9.5-1 for a first-order, lowpass circuit with a low frequency gain of +1 and a -3dB frequency of 5kHz.

Solution

TBD

Problem 9.5-04

Design a switched capacitor realization for a first-order , lowpass circuit with a low frequency gain of -10 and a -3dB frequency of 1kHz using a clock of 100kHz.

Solution

TBD

Problem 9.5-05

Design a switched capacitor realization for a first-order , highpass circuit with a high frequency gain of -10 and a -3dB frequency of 1kHz using a clock of 100kHz.

Solution

TBD

Problem 9.5-06

Repeat Ex. 9.5-2 for a treble boost circuit having 0dB gain from dc to 1kHz and an increase of gain at +20dB/dec. from 1kHz to 10kHz with a gain of +20dB from 10kHz and above (the mirror of the response of Fig. 9.5-7 around 1kHz).

Solution

TBD

Problem 9.5-07

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oo}(z)$. (2.) Plot the magnitude and phase response of the switched capacitor circuit from 0 rps to the clock frequency (ω_c). Assume that the op amp is ideal for this problem. It may be useful to remember that Eulers formula is $e^{\pm jx} = \cos(x) \pm j\sin(x)$.

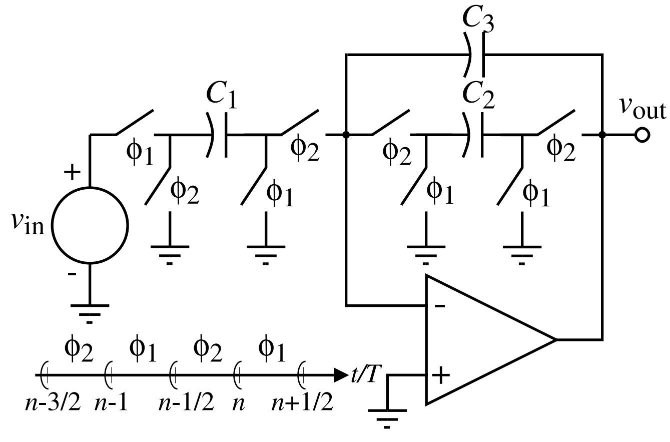


Figure P9.5-7

Solution

ϕ_1, $(n\text{-}1) \le t/T < (n\text{-}0.5)$:

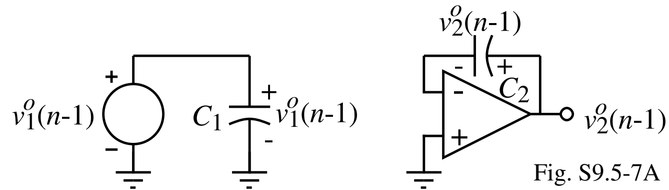


Fig. S9.5-7A

ϕ_2, $(n\text{-}0.5) \le t/T < (n)$:

From the equivalent circuit shown, we can write,

$$v_2^e(n\text{-}0.5) = v_2^o(n\text{-}1) - \frac{C_2}{C_3} v_2^e(n\text{-}0.5) + \frac{C_1}{C_3} v_1^o(n\text{-}1)$$

But, $v_2^o(n) = v_2^e(n\text{-}0.5) =$

$$v_2^o(n\text{-}1) - \frac{C_2}{C_3} v_2^o(n) + \frac{C_1}{C_3} v_1^o(n\text{-}1)$$

which gives,

$$V_2(z) = z^{-1} V_2(z) - \frac{C_2}{C_3} V_2(z) + \frac{C_1}{C_3} z^{-1} V_1(z)$$

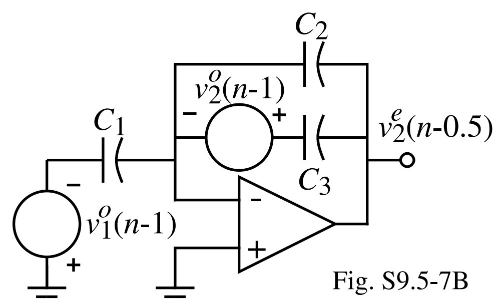


Fig. S9.5-7B

$$\therefore \boxed{\frac{V_2(z)}{V_1(z)} = H^{oo}(z) = \frac{(C_1/C_3)z^{-1}}{1 + (C_2/C_3) - z^{-1}}} \rightarrow H^{oo}(e^{j\omega T}) = \frac{(C_1/C_3)e^{-j\omega T}}{1 + (C_2/C_3) - e^{-j\omega T}}$$

$$|H^{oo}(e^{j\omega T})| = \frac{0.2}{\sqrt{(1.1 - \cos\omega T)^2 + \sin^2\omega T}} \text{ and } \mathrm{Arg}[H^{oo}(e^{j\omega T})] = -\omega T - \tan^{-1}\left(\frac{\sin\omega T}{1.1 - \cos\omega T}\right)$$

Replace ωT by $2\pi f/f_c$ and plot as a function of f/f_c to get the following plots.

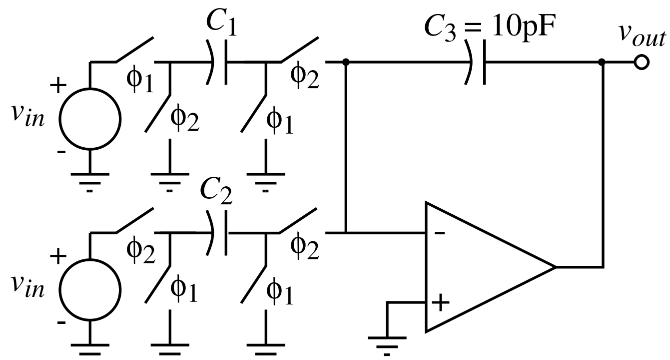
Problem 9.5-08

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (a.) Find the z-domain expression for $H^{oo}(z)$. (b.) Use your expression for $H^{oo}(z)$ to design the values of C_1 and C_2 to achieve a realization to

$$H(s) = \frac{10{,}000}{s+1000}$$

if the clock frequency is 100kHz and C_3 = 10pF. Assume that the op amp is ideal.

Solution



(a.) Converting the problem into a summing integrator gives:

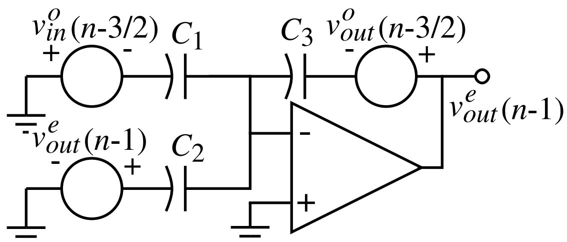
ϕ_1: $(n\text{-}1.5)\le t/T<(n\text{-}1)$

$v^o_{C1}(n\text{-}1.5) = v^o_{in}(n\text{-}1.5)$, $v^o_{C2}(n\text{-}1.5) = 0$

and $v^o_{C3}(n\text{-}1.5) = v^o_{out}(n\text{-}1.5)$

ϕ_2: $(n\text{-}1)\le t/T<(n\text{-}0.5)$

The eq. circuit at t = 0+ is shown. ∴



$v^e_{out}(n\text{-}1) =$

$$\frac{C_1}{C_3}v^o_{in}(n\text{-}1.5) - \frac{C_2}{C_3}v^o_{out}(n\text{-}0.5) + v^o_{out}(n\text{-}1.5)$$

ϕ_1: $(n\text{-}0.5)\le t/T<(n)$

$$v^o_{out}(n\text{-}0.5) = v^e_{out}(n\text{-}1) = \frac{C_1}{C_3}v^o_{in}(n\text{-}1.5) - \frac{C_2}{C_3}v^o_{out}(n\text{-}0.5) + v^o_{out}(n\text{-}1.5)$$

Transforming to the z-domain gives, $V^o_{out}(z) = z^{-1}\frac{C_1}{C_3}V^o_{in}(z) - \frac{C_2}{C_3}V^o_{out}(z) + z^{-1}V^o_{out}(z)$

Solving for $H^{oo}(z)$ gives, $\boxed{H^{oo}(z) = \frac{V^o_{out}(z)}{V^o_{in}(z)} = \frac{z^{-1}C_1}{C_2+C_3-C_3z^{-1}} = \frac{C_1}{z(C_2+C_3) - C_3}}$

(b.) Assume that $f \ll f_c$ and let $z \approx 1+sT$. Substituting into the above gives

$$H^{oo}(s) \approx \frac{C_1}{(1+sT)[C_2+C_3] - C_3} = \frac{C_1}{C_2+C_3-C_3+sT(C_2+C_3)} = \frac{C_1/C_2}{sT(C_2+C_3)/C_2 + 1}$$

Equating this result with the $H(s)$ in the problem statement gives

$$\frac{C_1}{C_2}=10,\ \ 1+\frac{C_3}{C_2}=\frac{f_c}{1000} \Rightarrow \boxed{C_2=C_3/99=10\text{pF}/99=0.101\text{pF}} \text{ and } \boxed{C_1=10C_2=1.01\text{pF}}$$

Problem 9.5-09

Find $H^{oo}(z)$ of the switched capacitor circuit shown. Replace z by $e^{j\omega T}$ and identify the magnitude and phase response of this circuit.

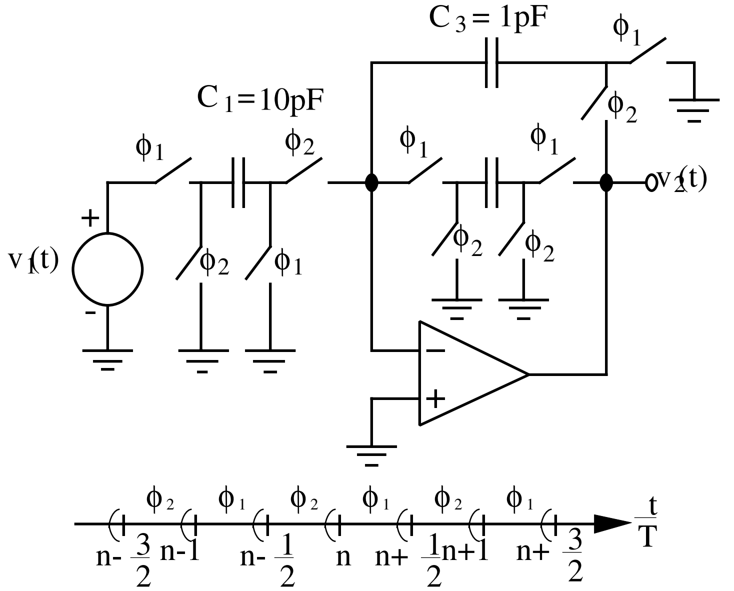


Figure P9.5-9

Solution

ϕ_2, $(n\text{-}0.5) \le t/T < (n)$:

With the ϕ_2 switches closed, the model is shown below.

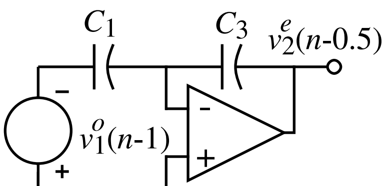


Fig. S9.5-9A

The output is given as,

$$v_2^e(n\text{-}0.5) = +\frac{C_1}{C_3}\, v_1^o(n\text{-}1)$$

ϕ_1, $(n) \le t/T < (n+0.5)$:

The model for this case is shown. The output is written as,

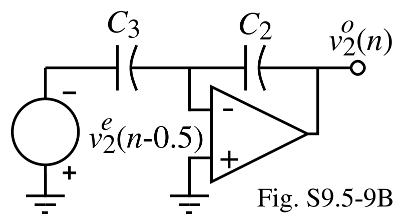


Fig. S9.5-9B

$$v_2^o(n) = +\frac{C_3}{C_2}\, v_2^e(n\text{-}0.5) = +\frac{C_3}{C_2}\cdot\frac{C_1}{C_3}\, v_1^o(n\text{-}1) = \frac{C_1}{C_2}\, v_1^o(n\text{-}1)$$

$$\therefore \qquad V_2^o(z) = \frac{C_1}{C_3} z^{-1} V_1^o(z) \qquad \rightarrow \qquad \boxed{\frac{V_2^o(z)}{V_1^o(z)} = H^{oo}(z) = \frac{C_1}{C_2} z^{-1}}$$

$$\boxed{|H^{oo}(e^{j\omega T})| = \frac{C_1}{C_2} = 10} \qquad \text{and} \qquad \boxed{|\mathrm{Arg}[H^{oo}(e^{j\omega T})] = -\omega T}$$

Comment: Note that this configuration is an amplifier that avoids taking the output of the op amp to zero when the feedback capacitor is shorted out. Therefore, slew rate limitation of the op amp is avoided.

Problem 9.5-10

The switched capacitor circuit shown is used to realize an audio bass-boost circuit. Find

$$H(e^{j\omega T}) = \frac{V_{out}(e^{j\omega T})}{V_{in}(e^{j\omega T})}$$

assuming that $f_c >> f_{signal}$. If $C_2 = C_4 = 1000\text{pF}$ and $f_c = 10\text{kHz}$, find the value of C_1 and C_3 to implement the following transfer function.

$$\frac{V_{out}(s)}{V_{in}(s)} = -10\left(\frac{\frac{s}{100} + 1}{\frac{s}{10} + 1}\right)$$

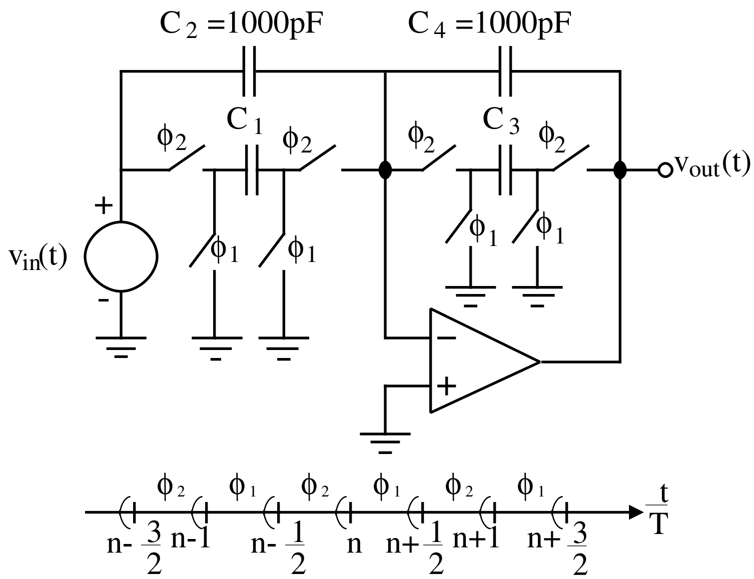
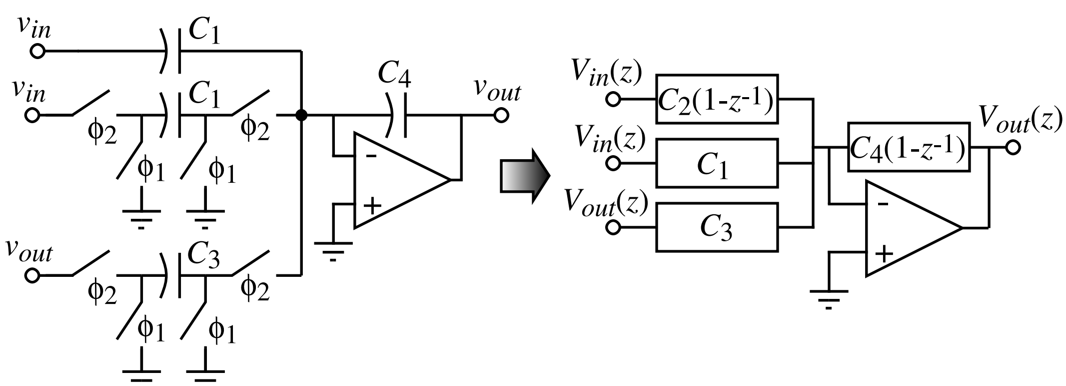


Figure P9.5-10

Solution

Write the circuit as the following summing integrator and replacing with *z*-domain models gives:



Summing currents gives,

$$C_2(1-z^{-1})V_{in}(z) + C_1V_{in}(z) + C_3V_{out}(z) + C_4(1-z^{-1})V_{out}(z) = 0$$

Transforming to the *s*-domain by $1-z^{-1} \approx -sT$ gives,

$$sT\ C_2\ V_{in}(s) + C_1V_{in}(s) + C_3V_{out}(s) + sT\ C_4\ V_{out}(s) = 0$$

$$\therefore\ H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\left(\frac{sT\ C_2 + C_1}{sT\ C_4 + C_3}\right) = -\left(\frac{C_1}{C_3}\right)\left(\frac{\frac{sT\ C_2}{C_1} + 1}{\frac{sT\ C_4}{C_3} + 1}\right) = -10\left(\frac{\frac{s}{100} + 1}{\frac{s}{10} + 1}\right)$$

Therefore, $\frac{C_1}{C_3} = 10$, $\frac{C_1}{TC_2} = 100$ and $\frac{C_3}{TC_4} = 10$

$$\therefore\ \boxed{C_1 = \frac{100C_2}{f_c} = \frac{100\cdot 1000\text{pF}}{10{,}000} = 10\text{pF}} \quad \text{and} \quad \boxed{C_3 = 1\text{pF}}$$

Problem 9.6-01

Combine Figs. 9.6-2a and 9.6-2b to form a continuous time biquad circuit. Replace the negative resistor with an inverting op amp and find the s-domain frequency response. Compare your answer with Eq. (9.6-1).

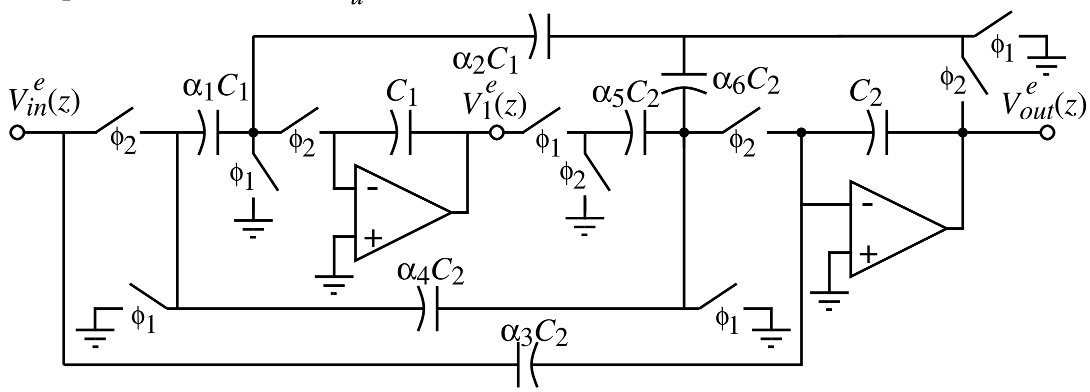
Solution

TBD

Problem 9.6-02

(a.) Use the low-Q switched capacitor biquad circuit shown to design the capacitor ratios of a lowpass second-order filter with a pole frequency of 1kHz, Q = 5 and a gain at dc of -10 if the clock frequency is 100kHz. What is the total capacitance in terms of C_u?

(b.) Find the clock frequency, f_c, that keeps all capacitor ratios less than 10:1. What is the total capacitance in terms of C_u for this case?



Design Eqs: $\alpha_1 = \dfrac{K_0T}{\omega_o}$, $\alpha_2 = |\alpha_5| = \omega_oT$, $\alpha_3 = K_2$, $\alpha_4 = K_1T$, and $\alpha_6 = \dfrac{\omega_oT}{Q}$.

Solution

(a.) $H(s) = \dfrac{-10\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \Rightarrow K_o = 10\omega_o^2, K_1 = K_2 = 0,\ \omega_o = 2000\pi$, and $Q = 5$

$\therefore \quad \alpha_1 = \dfrac{10\omega_o^2T}{\omega_o} = 10\omega_oT$, $\alpha_2 = |\alpha_5| = \omega_oT$, $\alpha_3 = \alpha_4 = 0$, and $\alpha_6 = \dfrac{\omega_oT}{Q} = \dfrac{\omega_oT}{5}$

$\omega_oT = \dfrac{2\pi f_o}{f_c} = \dfrac{2\pi}{100} = 0.06283 \Rightarrow \boxed{\alpha_1 = 0.6283,\ \alpha_2{=}|\alpha_5|\ 0.06283,\ \alpha_6{=}0.01256}$

$$\boxed{\text{Total capacitance} = \frac{1}{0.6283} + \frac{1}{0.06283} + 2 + \frac{1}{0.01256} + \frac{1}{0.06283} = 115.45C_u}$$

(b.) $\dfrac{\omega_o}{5f_c} = 0.1 \Rightarrow \boxed{f_c = 2\omega_o = 4000\pi = 12.566\text{kHz}}$

Now, $\alpha_1 = 5$, $\alpha_2 = |\alpha_5| = 0.5$, and $a_6 = 0.1$

$$\boxed{\text{Total capacitance} = 5 + \frac{1}{.5} + 1 + \frac{1}{0.1} + \frac{1}{0.5} + 1 = 21C_u}$$

Problem 9.6-03

A Tow-Thomas continuous time filter is shown. Give a discrete-time realization of this filter using strays-insensitive integrators. If the clock frequency is much greater than the filter frequencies, find the coefficients, a_i and b_i, of the following z-domain transfer function in terms of the capacitors of the discrete-time realization.

$$H(z) = \frac{a_0 + a_1z^{-1} + a_2z^{-2}}{b_0 + b_1z^{-1} + b_2z^{-2}}$$

Solution

The development of a discrete-time realization of the Tow-Thomas continuous time filter is shown to the right.

Using z-domain analysis, we can solve for the desired transfer function and find the coefficients.

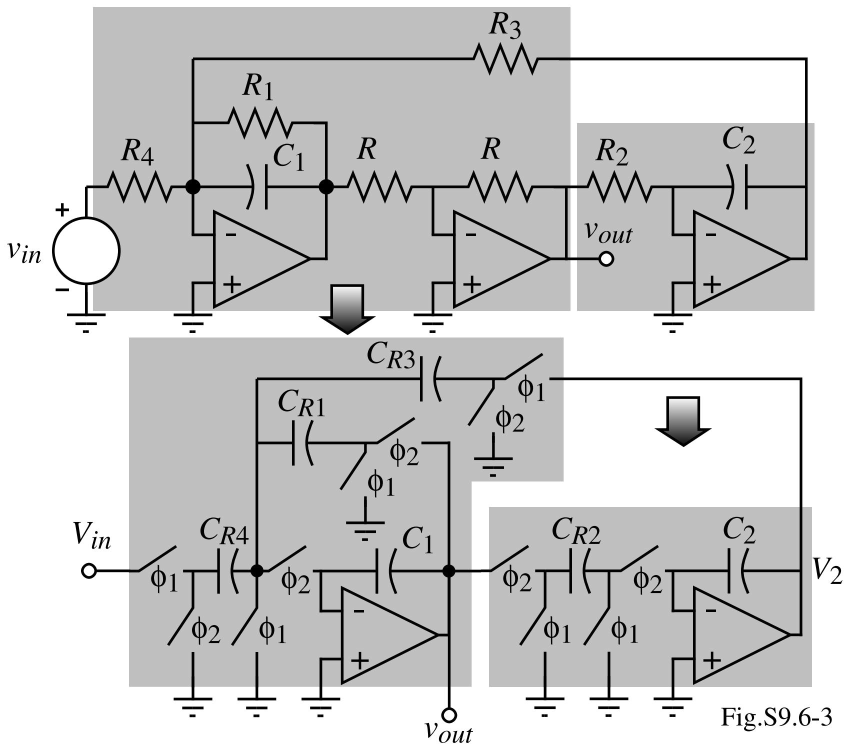


Fig.S9.6-3

$$V_{out}(z) = \frac{1}{1 - z^{-1}}\left[\frac{C_{R4}}{C_1}z^{-1}V_{in}(z) - \frac{C_{R1}}{C_1}z^{-1}V_{out}(z) + \frac{C_{R3}}{C_1}z^{-1}V_2(z)\right] \quad \text{and} \quad V_2(z) = -\frac{C_{R2}/C_2}{1 - z^{-1}}V_{out}(z)$$

$$\therefore \quad V_{out}(z) = \frac{1}{1 - z^{-1}}\left[\frac{C_{R4}}{C_1}z^{-1}V_{in}(z) - \frac{C_{R1}}{C_1}z^{-1}V_{out}(z) + \frac{C_{R2}C_{R3}}{C_1C_2}\,\frac{z^{-1}}{1 - z^{-1}}V_{out}(z)\right]$$

$$V_{out}(z)\left[(1 - z^{-1})^2 - \frac{C_{R1}}{C_1}(1 - z^{-1}) + \frac{C_{R2}C_{R3}}{C_1C_2}z^{-1}(1 - z^{-1})\right] = z^{-1}(1 - z^{-1})\frac{C_{R4}}{C_1}V_{in}(z)$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{(z^{-1} - z^{-2})\frac{C_{R4}}{C_1}}{1 + 2z^{-1} + z^{-2} + \frac{C_{R1}}{C_1} - \frac{C_{R1}}{C_1}z^{-1} + \frac{C_{R2}C_{R3}}{C_1C_2}z^{-1} - \frac{C_{R2}C_{R3}}{C_1C_2}z^{-2}}$$

Equating coefficients gives,

$$a_0 = 0,\ a_1 = \frac{C_{R4}}{C_1},\ a_2 = -\frac{C_{R4}}{C_1},\ b_0 = 1 + \frac{C_{R1}}{C_1},\ b_1 = 2 - \frac{C_{R1}}{C_1} + \frac{C_{R2}C_{R3}}{C_1C_2} \text{ and } b_2 = 1-\frac{C_{R2}C_{R3}}{C_1C_2}$$

Problem 9.6-04

Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = \frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + b_0}$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of second-order circuit is this?

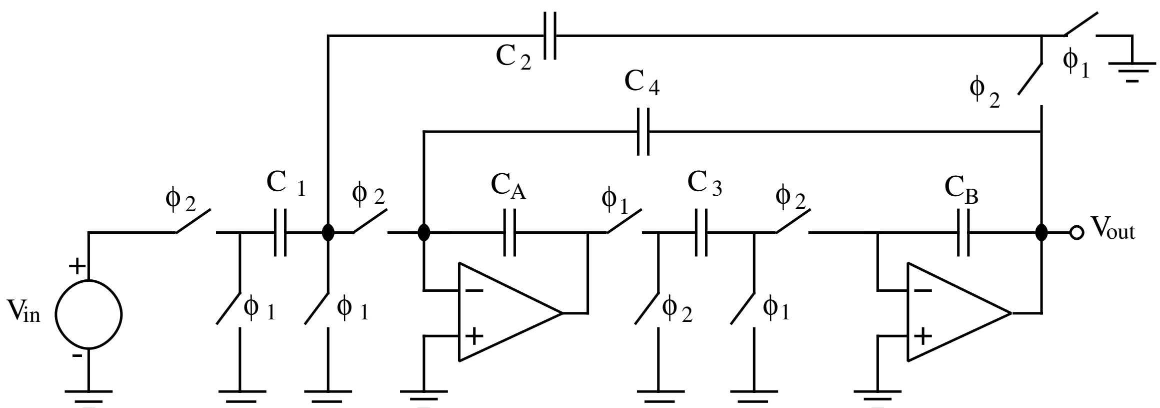


Figure P9.6-4

Solution

$$V_1(z) = \left(\frac{z}{z-1}\right)\frac{C_1}{C_A}V_{in}(z) - \left(\frac{z}{z-1}\right)\frac{C_2}{C_A}V_{out}(z) - \frac{C_4}{C_A}V_{out}(z) \quad \text{and} \quad V_{out}(z) = \left(\frac{1}{z-1}\right)\frac{C_3}{C_A}V_1(z)$$

Where $V_1(z)$ is the output of the first integrator. If $\alpha_{1\mathrm{A}} = C_1/C_A$, $\alpha_{3\mathrm{B}} = C_3/C_B$, $\alpha_{2\mathrm{A}} = C_2/C_A$, and $\alpha_{4\mathrm{A}} = C_4/C_A$ then we can write the following.

$$V_{out}(z) = \left(\frac{\alpha_{3\mathrm{B}}}{z-1}\right)\left[-\frac{\alpha_{1\mathrm{A}}z}{z-1}V_{in}(z) - \frac{\alpha_{2\mathrm{A}}z}{z-1}V_{out}(z) - \alpha_{4\mathrm{A}}V_{out}(z)\right]$$

$$\therefore \quad V_{out}(z)\left[1 + \frac{\alpha_{2\mathrm{A}}\alpha_{3\mathrm{B}}z}{(z-1)^2} + \frac{\alpha_{3\mathrm{B}}\alpha_{4\mathrm{A}}z}{z-1}\right] = \frac{\alpha_{1\mathrm{A}}\alpha_{3\mathrm{B}}z}{(z-1)^2}V_{in}(z)$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\alpha_{1\mathrm{A}}\alpha_{3\mathrm{B}}z}{(z-1)^2+\alpha_{2\mathrm{A}}\alpha_{3\mathrm{B}}z+(z-1)\alpha_{3\mathrm{B}}\alpha_{4\mathrm{A}}} = \boxed{\frac{-\alpha_{1\mathrm{A}}\alpha_{3\mathrm{B}}z}{z^2+(\alpha_{2\mathrm{A}}\alpha_{3\mathrm{B}}+\alpha_{3\mathrm{B}}\alpha_{4\mathrm{A}}-2)z+(1-\alpha_{3\mathrm{B}}\alpha_{4\mathrm{A}})}}$$

If $\omega T = sT << 1$, then $z \approx 1$ unless there are terms like $(z-1)$ in which case $z-1 \approx sT$. Therefore,

$$H(s) \approx \frac{-\alpha_{1\mathrm{A}}\alpha_{3\mathrm{B}}}{s^2T^2+sT\alpha_{3\mathrm{B}}\alpha_{4\mathrm{A}}+\alpha_{2\mathrm{A}}\alpha_{3\mathrm{B}}} = \frac{-\dfrac{\alpha_{1\mathrm{A}}\alpha_{3\mathrm{B}}}{T^2}}{s^2+s\dfrac{\alpha_{3\mathrm{B}}\alpha_{4\mathrm{A}}}{T}+\alpha_{2\mathrm{A}}\alpha_{3\mathrm{B}}} = \frac{-\dfrac{C_1C_3}{C_AC_B}\dfrac{1}{T^2}}{s^2+s\dfrac{C_3C_4}{C_BC_A}\dfrac{1}{T}+\dfrac{C_2C_3}{C_AC_B}}$$

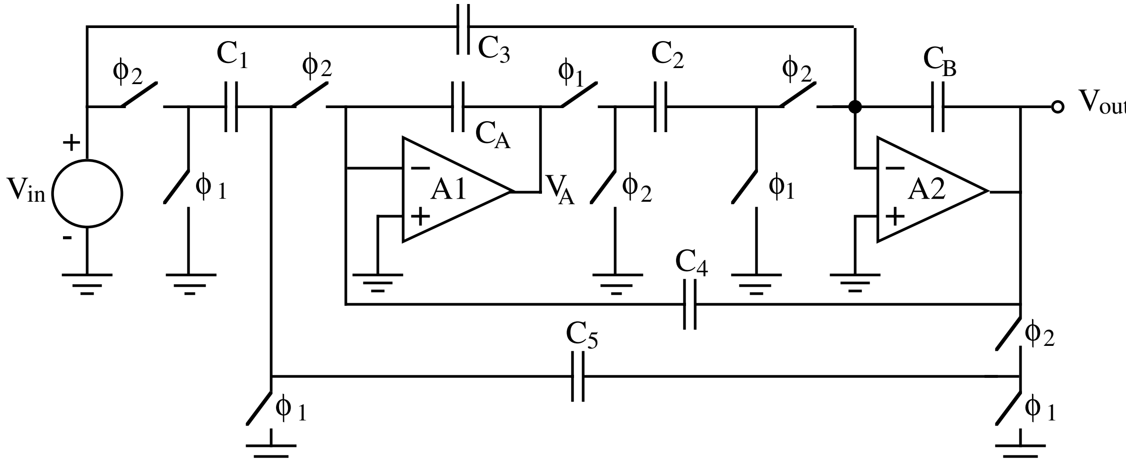
This circuit is a second-order bandpass transfer function.

Problem 9.6-05

Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = -\left[\frac{a_2z^2 + a_1z + a_0}{z^2 + b_1z + b_0}\right]$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of circuit is this?



Solution

For the output voltage of the first integrator, V_A, we can write,

$$V_A = f_1(V_A,V_{in},V_{out}) = \frac{-C_1}{C_A}\left(\frac{z}{z-1}\right)V_{in} - \frac{C_5}{C_A}\left(\frac{z}{z-1}\right) V_{out} - \frac{C_4}{C_A} V_{out}$$

Similarily for the output voltage of the second integrator, V_{out}, we can write,

$$V_{out} = f_2(V_A,V_{in}) = \frac{C_2}{C_B}\left(\frac{1}{z-1}\right)V_A - \frac{C_3}{C_B} V_{in}$$

Combining equations gives,

$$V_{out} = \frac{-z}{(z-1)^2}\left(\frac{C_2C_5}{C_AC_B}\right) V_{out} - \frac{z}{(z-1)^2}\left(\frac{C_1C_2}{C_AC_B}\right) V_{in} - \frac{1}{z-1}\left(\frac{C_2C_4}{C_AC_B}\right) V_{out} - \frac{C_3}{C_B} V_{in}$$

$$V_{out}\left[1 + \frac{z}{(z-1)^2}\left(\frac{C_2C_5}{C_AC_B}\right) + \frac{1}{z-1}\left(\frac{C_2C_4}{C_AC_B}\right)\right] = -\left[\frac{z}{(z-1)^2}\left(\frac{C_1C_2}{C_AC_B}\right) - \frac{C_3}{C_B}\right]V_{in}$$

$$V_{out}\left[(z-1)^2 + (z-1)\left(\frac{C_2C_4}{C_AC_B}\right) + z\left(\frac{C_2C_5}{C_AC_B}\right)\right] = -\left[(z-1)^2\frac{C_3}{C_B} + z\left(\frac{C_1C_2}{C_AC_B}\right)\right]V_{in}$$

$$\therefore \quad \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\left[\frac{C_3}{C_B}z^2+\left(\frac{C_1C_2}{C_AC_B} - 2\frac{C_3}{C_B}\right)z + \frac{C_3}{C_B}\right]}{z^2 + \left(\frac{C_2(C_4+C_5)}{C_AC_B} - 2\right)z + \left(1 - \frac{C_2C_4}{C_AC_B}\right)} = -\left[\frac{a_2z^2+a_1z+a_0}{z^2+b_1z+b_0}\right]$$

Thus,

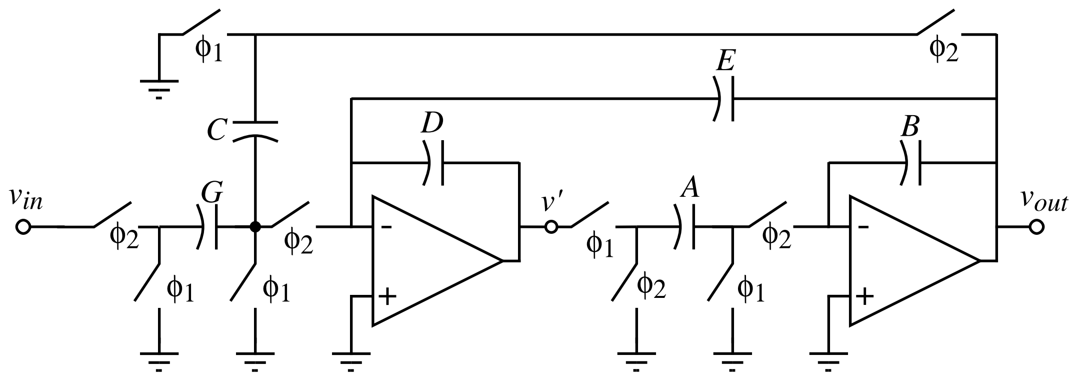
$$\boxed{a_2=C_3/C_B,\ a_1=\frac{C_1C_2}{C_AC_B} - \frac{2C_3}{C_B},\ a_0=C_3/C_B,\ b_1=\frac{C_2(C_4+C_5)}{C_AC_B} - 2 \text{ and } b_0=1-\frac{C_2C_4}{C_AC_B}}$$

Problem 9.6-06

Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = -\left[\frac{a_2z^2 + a_1z + a_0}{z^2 + b_1z + b_0}\right]$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of circuit is this? What is the pole frequency, ω_o, and pole Q?



Solution

$$V'(z) = -\left(\frac{G}{D}\right)\frac{z}{z-1}V_{in}(z) - \left(\frac{C}{D}\right)\frac{z}{z-1}V_{out}(z) - \left(\frac{E}{D}\right)V_{out}(z)$$

$$V_{out}(z) = \frac{A}{B}\frac{V'}{z-1} = \frac{A}{B}\frac{z}{z-1}\left[-\left(\frac{G}{D}\right)\frac{z}{z-1}V_{in}(z) - \left(\frac{C}{D}\right)\frac{z}{z-1}V_{out}(z) - \left(\frac{E}{D}\right)V_{out}(z)\right]$$

$$= -\frac{AG}{BD}\frac{z}{(z-1)^2}V_{in}(z) - \frac{AC}{BD}\frac{z}{(z-1)^2}V_{out}(z) - \frac{AE}{BD}\frac{V_{out}(z)}{z-1}$$

$$V_{out}(z)\left[1 + \frac{AE}{BD}\frac{1}{z-1} + \frac{AC}{BD}\frac{z}{(z-1)^2}\right] = -\frac{AG}{BD}\frac{z}{(z-1)^2}V_{in}(z)$$

$$\therefore \quad \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\frac{AG}{BD}z}{(z-1)^2+\frac{AE}{BD}(z-1)+\frac{AC}{BD}z} \rightarrow \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\frac{AG}{BD}z}{z^2+\left(\frac{AE}{BD}+\frac{AC}{BD}-2\right)z+\left(1-\frac{AE}{BD}\right)}$$

Thus, $\boxed{a_2 = a_0 = 0,\ a_1 = \frac{AG}{BD},\ b_1 = \frac{AE}{BE} + \frac{AC}{BD} - 2,\ \text{and}\ b_0 = 1 - \frac{AE}{BD}}$

Problem 9.6-07

The switched capacitor circuit shown below realizes the following z-domain transfer function

$$H(z) = -\left(\frac{a_2z^2 + a_1z + a_0}{b_2z^2 + b_1z + 1}\right)$$

where

C_6=a_2/b_2, C_5=$(a_2-a_0)/b_2C_3$, $C_1=\frac{a_0+a_1+a_2}{b_2C_3}$, $C_4=\frac{1-(b_0/b_2)}{C_3}$ and $C_2C_3 = \frac{1+b_1+b_2}{b_2}$. Design a switched capacitor realization for the function

$$H(s) = \frac{-10^6}{s^2 + 100s + 10^6}$$

where the clock frequency is 10 kHz. Use the bilinear transformation, $s = (2/T)[(z-1)/(z+1)]$, to map H(s) to H(z). Choose $C_2 = C_3$ and assume that $C_A = C_B = 1$.

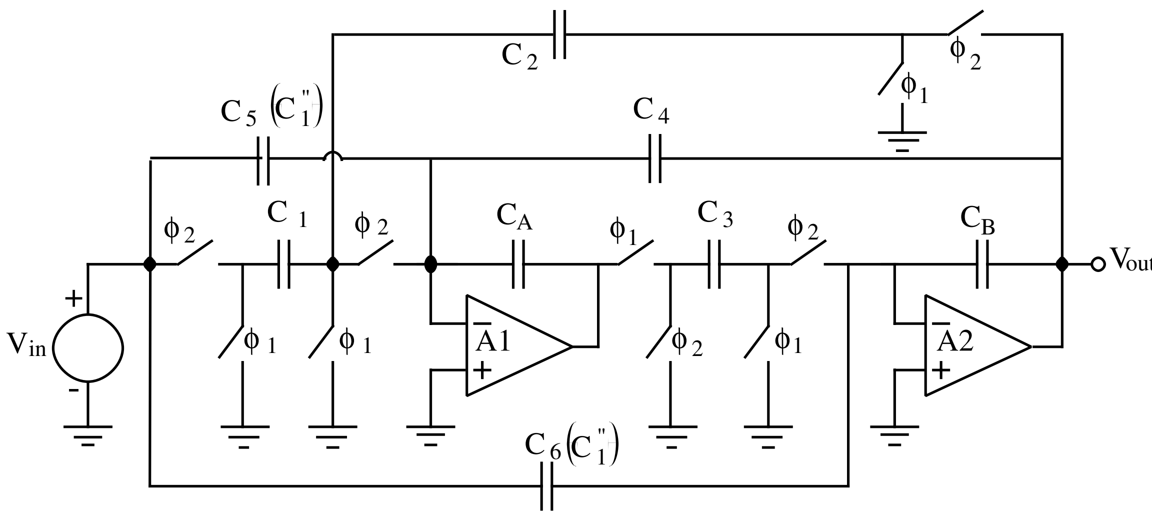


Figure P9.6-7

Solution

Apply the bilinear transformation

$$s = \frac{2}{T}\left(\frac{z-1}{z+1}\right) = 2\text{x}10^4\left(\frac{z-1}{z+1}\right)$$

to $H(s)$ to get,

$$H(z) = \frac{-10^6}{4\text{x}10^8\left(\frac{z-1}{z+1}\right)^2+200\text{x}10^4\left(\frac{z-1}{z+1}\right)\left(\frac{z+1}{z+1}\right)+10^6\left(\frac{z+1}{z+1}\right)^2}$$

$$= \frac{-10^6(z^2+2z+1)}{4\text{x}10^8(z^2-2z+1)+2\text{x}10^6(z^2-1)+10^6(z^2+2z+1)}$$

$$= \frac{-(10^6z^2+2\text{x}10^6z+10^6)}{(4\text{x}10^8+2\text{x}10^6+10^6)z^2+(-8\text{x}10^8+2\text{x}10^6)z+(4\text{x}10^8-2\text{x}10^6+10^6)}$$

Problem 9.6-07 - Continued

$$= \frac{-(10^6z^2+2\text{x}10^6z+10^6)}{4.03\text{x}10^8z^2-7.98\text{x}10^8z+3.99\text{x}10^8} = \frac{-(0.002506z^2+0.005013z+0.002506)}{1.010025z^2-2.0000z+1}$$

Now equating to the coefficients,

$$C_6 = \frac{a_2}{b_2} = \frac{0.002506}{1.010025} = 0.002481,\ C_5 = \frac{a_2\text{-}a_0}{b_2C_3} = 0,$$

$$C_2C_3 = \frac{1+b_1+b_2}{b_2} = \frac{1+(-2)+1.010025}{1.010025} = 0.009925 \quad \Rightarrow C_2 = C_3 = 0.099627$$

$$C_1 = \frac{a_0+b_1+b_2}{b_2C_3} = \frac{0.002506+0.005013+0.002506}{1.010025\cdot 0.0099627} = 0.099633$$

$$C_4 = \frac{1+(b_0/b_2)}{C_3} = \frac{1\text{-}(1/1.010025)}{0.099627} = 0.099627$$

$\therefore$ $\boxed{C_1\text{=}0.099633,\ C_2\text{=}C_3\text{=}0.099627,\ C_4\text{=}0.099627,\ C_5\text{=}0,\ C_6\text{=}\ 0.002481}$

$$C_{max}/C_{min} = 1/0.002625 = \underline{\underline{403.06}}$$

Normalize all capacitors by 0.002625 to get

$$\Sigma C_\mu = [(403.6)2+(37.953)2+37.953+37.955+1] = \underline{\underline{958.9C_\mu}}$$

Problem 9.7-01

Find the minimum order of a Butterworth and Chebyshev filter approximation to a filter with the specifications of T_{PB} = -3dB, T_{SB} = -40dB, and Ω_n = 2.0.

Solution

For the Butterworth approximation, use Eq. (9.7-7) and for the Chebyshev approximation use Eq. (9.7-12), both with $\varepsilon = 1$. The results are shown below.

N	$T_{SB}(\text{dB}) = -10log_{10}(1+2^{2N})$	$T_{SB}(\text{dB}) = -10log_{10}[1+cosh^2(Ncosh^{-1}2)]$
1	-6.99 dB	-6.99 dB
2	-12.30 dB	-16.99 dB
3	-18.13 dB	-28.31 dB
4	-24.10 dB	-39.74 dB
5	-30.11 dB	-51.17 dB
6	-36.12 dB	
7	-42.14 dB	

The minimum order for the Butterworth is 7 while the minimum order for the Chebyshev i 5 and in many cases 4 would work.

Problem 9.7-02

Find the transfer function of a fifth-order, Butterworth filter approximation expressed as products of first- and second-order terms. Find the pole frequency, ω_p and the Q for each second-order term.

Solution

From Table 9.7-1 we get,

$$T(s) = \frac{1}{(s+1)(s^2+0.61804s+1)(s^2+1.84776s+1)}$$

The pole frequency and Q for a general second order term of (s^2+a_1s+1) is

$$\omega_p = 1 \text{ and } Q = \frac{1}{a_1}$$

For both second order terms, the pole frequency is 1 radian/sec.

For the first second-order term, the $Q = 1.61804$.

For the second, second-order term, the $Q = 0.541196$.

Problem 9.7-03

Redesign the second stage of Ex. 9.7-5 using the high-Q biquad and find the total capacitance required for this stage. Compare with the example.

Solution

$$T_{n2}(s_n) = \frac{0.9883}{s_n{}^2 + 0.1789s_n + 0.9883} \qquad \Rightarrow \qquad \omega_{n2} = 0.9941 \text{ and } Q_2 = 5.557$$

For the lowpass high-Q biquad, $K_1 = K_2 = 0 \quad \Rightarrow \quad \alpha_{32} = \alpha_{62} = 0$ and $K_0 = \omega_{n2}{}^2$

$$\therefore \qquad \alpha_{22} = |\alpha_{52}| = \omega_{n2}T_n = 0.9941\frac{\omega_{PB}}{f_c} = \underline{\underline{0.3123}}$$

$$\alpha_{12} = \frac{\omega_{n2}{}^2T_n}{\omega_{n2}} = \omega_{n2}T_n = \underline{\underline{0.3123}}$$

$$\alpha_{42} = \frac{1}{Q} = \underline{\underline{0.1800}}$$

Schematic of the second-stage:

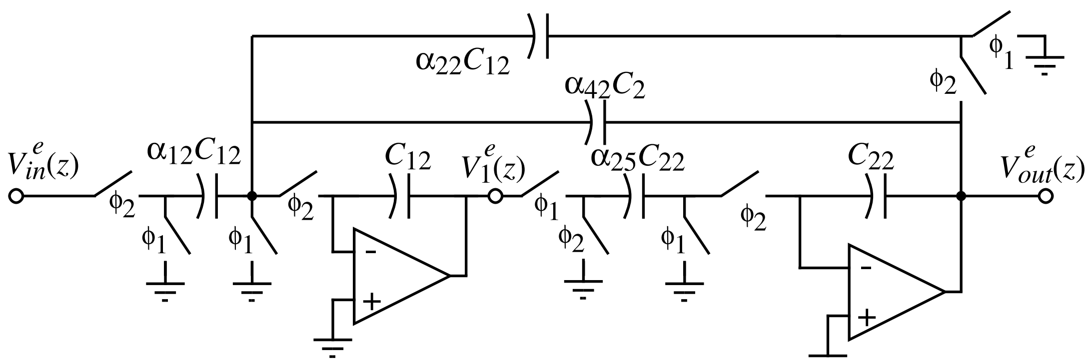


Figure S9.7-03

Total capacitance is:

$$\Sigma C = \left(1 + \frac{2(0.3123)}{0.1880} + \frac{1}{0.1800}\right) + \left(1 + \frac{1}{0.3123}\right) = 10.027{+}4.202 = \underline{\underline{14.229C_\mu}}$$

Note that this value is 17.32 when a low-Q stage is used.

Problem 9.7-04

Design a cascaded, switched capacitor, 5th-order, lowpass filter using the cascaded approach based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{1}{(s_n+1)(s_n{}^2+0.61804s_n+1)(s_n{}^2+1.61804s_n+1)}$$

The passband of the filter is to 1000Hz. Use a clock frequency of 100kHz and design each stage giving the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio, and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

Stage 1, First-Order Stage (Use Fig. 9.5-1):

$$T_1(s_n) = \frac{\alpha_{11}/\alpha_{21}}{(s_nT_n/\alpha_{21})+1} = \frac{1}{s_n+1} \quad \Rightarrow \quad \alpha_{11} = \alpha_{21} \quad \text{and} \quad \alpha_{21} = T_n$$

$$\alpha_{11} = \alpha_{21} = T_n = \frac{\omega_{PB}}{f_c} = \frac{2000\pi}{100{,}000} = \underline{\underline{0.06283}}$$

$$\frac{C_{max}}{C_{min}} = \frac{1}{0.06283} = \underline{\underline{15.92}} \quad \text{and} \quad \Sigma C = 2 + \frac{1}{0.06283} = \underline{\underline{19.92C_\mu}}$$

Stage 2, Second-order Stage (Use Low-Q Lowpass Biquad):

$$T_2(s_n) = \frac{1}{s_n{}^2+1.61804s_n+1} \quad \Rightarrow \quad \omega_{n2} = 1 \text{ rad/sec and } Q_2 = 0.61804$$

From the low-Q biquad relationships, $K_1 = K_2 = 0 \quad \Rightarrow \quad \alpha_{32} = \alpha_{42} = 0$

$$\alpha_{22} = |\alpha_{52}| = \omega_nT_n = \underline{\underline{0.06283}} \quad \text{and} \quad \alpha_{62} = \frac{\omega_nT_n}{Q_2} = \frac{0.06283}{0.61804} = \underline{\underline{0.1017}}$$

$$\frac{C_{max}}{C_{min}} = \frac{1}{0.1017} = \underline{\underline{9.837}}$$

and $$\Sigma C = \left(2 + \frac{1}{0.06283}\right) + \left(\frac{1}{0.06283} + \frac{0.1017}{0.06283} + 1\right) = \underline{\underline{36.45C_\mu}}$$

Stage 3, Second-order Stage (Use Low-Q Lowpass Biquad):

$$T_3(s_n) = \frac{1}{s_n{}^2+0.61804s_n+1} \quad \Rightarrow \quad \omega_{n2} = 1 \text{ rad/sec and } Q_2 = 1.6180$$

From the low-Q biquad relationships, $K_1 = K_2 = 0 \quad \Rightarrow \quad \alpha_{33} = \alpha_{43} = 0$

$$\alpha_{23} = |\alpha_{53}| = \omega_nT_n = \underline{\underline{0.06283}} \quad \text{and} \quad \alpha_{62} = \frac{\omega_nT_n}{Q_2} = \frac{0.06283}{1.6180} = \underline{\underline{0.0391}}$$

$$\frac{C_{max}}{C_{min}} = \frac{1}{0.0391} = \underline{\underline{25.59}}$$

and $$\Sigma C = \left(2 + \frac{1}{0.06283}\right) + \left(\frac{1}{0.0391} + \frac{0.06283}{0.0391} + 1\right) = \underline{\underline{46.10C_\mu}}$$

Problem 9.7-04 – Continued

Schematic:

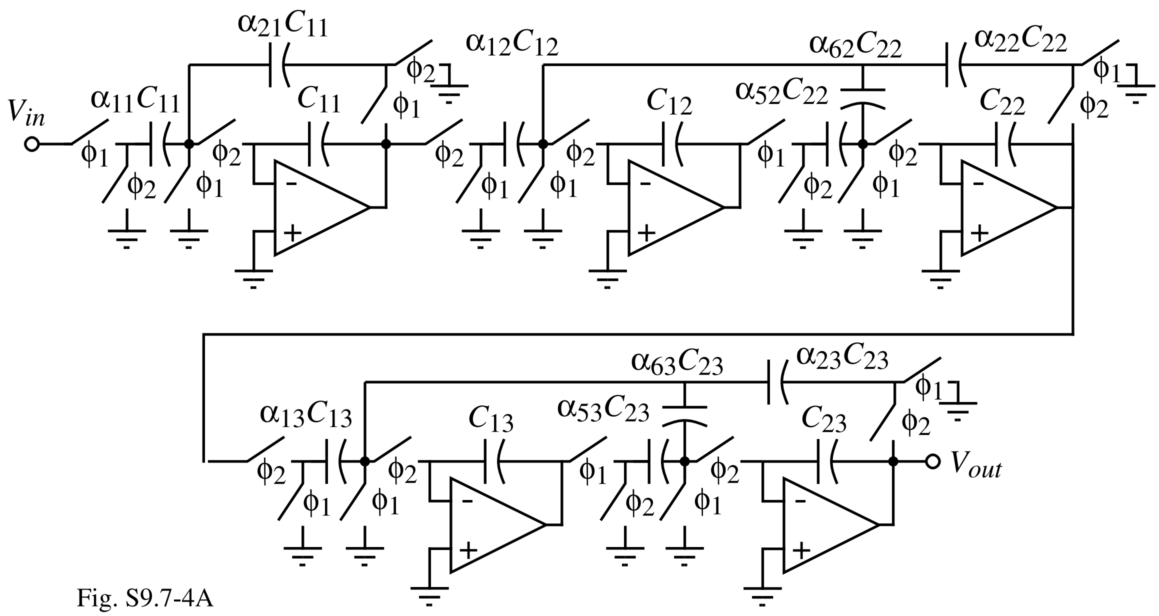


Fig. S9.7-4A

SPICE File:

```
*** HW9 PROBLEM2 (Problem 9.7-4) ***
*** Node 21 and 22 are outputs
VIN 1 0 DC 0 AC 1
*** STAGE1 ***
XNC11 1 2 3 4 NC1
XUSCP11 3 4 5 6 USCP
XPC21 5 6 3 4 PC1
XAMP11 3 4 5 6 AMP
*** STAGE2 ***
XPC12 5 6 7 8 PC1
XUSCP12 7 8 9 10 USCP
XPC22 7 8 13 14 PC1
XAMP12 7 8 9 10 AMP
XNC52 9 10 11 12 NC1
XUSCP22 11 12 13 14 USCP
XPC62 11 12 13 14 PC2
XAMP22 11 12 13 14 AMP
*** STAGE3 ***
XPC13 13 14 15 16 PC1
XPC23 15 16 21 22 PC1
XUSCP43 15 16 21 22 USCP1
XUSCP13 15 16 17 18 USCP
XAMP13 15 16 17 18 AMP
XNC53 17 18 19 20 NC1
XUSCP23 19 20 21 22 USCP
XAMP23 19 20 21 22 AMP
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
```

Problem 9.7-05

Repeat Problem 9.7-3 for a 5th-order, highpass filter having the same passband frequency. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

TBD

Problem 9.7-06

Repeat Problem 9.7-3 for a 5th-order, bandpass filter having center frequency of 1000Hz and a -3dB bandwidth of 500Hz. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

TBD

Problem 9.7-07

Design a switched capacitor 6th-order, bandpass filter using the cascaded approach and based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{2}{(s_n+1)(s_n{}^2+2s_n+2)}$$

The center frequency of the bandpass filter is to be 1000Hz with a bandwidth of 100Hz. Use a clock frequency of 100kHz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

TBD

Problem 9.7-08

Design a switched capacitor, third-order, highpass filter based on the lowpass normalized prototype transfer function of Problem 9.7-7. The cutoff frequency (f_{PB}), is to be 1000Hz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

TBD

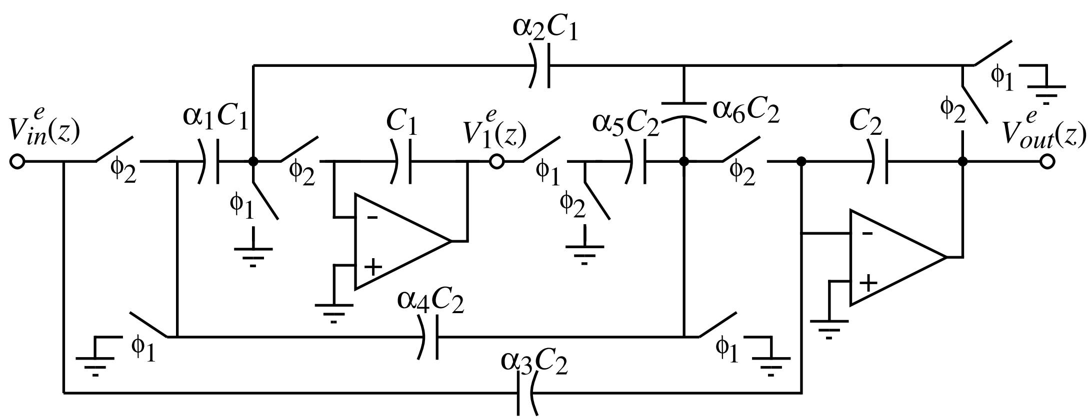
<u>Problem 9.7-09</u>

Design a switched capacitor, third-order, highpass filter based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{0.5(s_n{}^2+4)}{(s_n+1)(s_n{}^2+2s_n+2)}$$

The cutoff frequency (f_{PB}), is to be 1000Hz. Use a clock frequency of 100kHz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use the low-Q biquad given below for the second-order stage. The approximate s-domain transfer function for the low-Q biquad is,

$$H^{ee}(s_n) = \frac{-\left[\alpha_3 s_n{}^2 + \dfrac{s_n\alpha_4}{T_n} + \dfrac{\alpha_1\alpha_5}{T_n{}^2}\right]}{s_n{}^2 + \dfrac{s_n\alpha_6}{T_n} + \dfrac{\alpha_2\alpha_5}{T_n{}^2}}$$



Low Q, switched capacitor, biquad realization.

<u>Solution</u>

Perform a normalized lowpass to normalized highpass transformation:

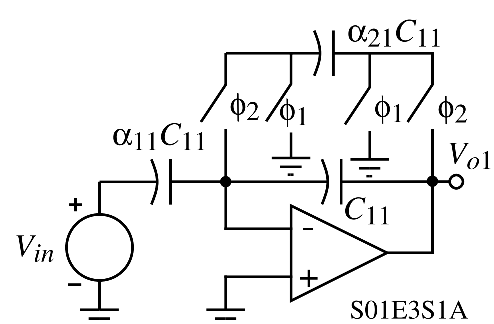
$$H_{hpn}(s_n) = \frac{0.5\left(\dfrac{1}{s_n{}^2}+4\right)}{\left(\dfrac{1}{s_n}+1\right)\left(\dfrac{1}{s_n{}^2}+\dfrac{2}{s_n}+2\right)} = \frac{0.5s_n(4s_n{}^2+1)}{(s_n+1)(1+2s_n+2s_n{}^2)} = \left(\frac{s_n}{s_n+1}\right)\left(\frac{s_n{}^2+0.25}{s_n{}^2+s_n+0.5}\right)$$

First-order stage design:

Equating currents at the inverting input of the op amp gives,

$$\alpha_{11}(1\text{-}z^{-1})V_{in}^e(z) + \alpha_{21}V_{o1}^e(z) + (1\text{-}z^{-1})V_{o1}^e(z) = 0$$

Solving for the $H^{ee}(z)$ tranfer function gives,



Problem 9.7-09 - Continued

$$H^{ee}(z) = \frac{V_{o1}^{e}(z)}{V_{in}^{e}(z)} = \frac{-\alpha_{11}(1-z^{-1})}{\alpha_{21} + (1-z^{-1})} \quad \rightarrow \quad H^{ee}(s_n) \approx \frac{V_{o1}^{e}(s_n)}{V_{in}^{e}(s_n)} = \frac{-\alpha_{11}s_nT_n}{\alpha_{21}+s_nT_n} = \frac{-\alpha_{11}s_n}{s_n+ \dfrac{\alpha_{21}}{T_n}}$$

Equating with the normalized highpass transfer function gives,

$$\alpha_{11} = \underline{\underline{1}} \text{ and } \alpha_{21} = T_n = \frac{\omega_{PB}}{f_c} = \frac{2000\pi}{100{,}000} = \underline{\underline{0.06283}}$$

$$\Sigma C_\mu = \frac{2}{0.06283} + 1 = 32.832C_\mu$$

Next, consider the second-order stage design:

Equating $H^{ee}(s)$ with $\left(\dfrac{s_n{}^2+0.25}{s_n{}^2+s_n+0.5}\right)$ gives,

$$\alpha_{32} = \underline{\underline{1}},\ \alpha_{42} = \underline{\underline{0}},\ \alpha_{12}\alpha_{52} = 0.25T_n{}^2,\ \alpha_{62}=T_n = \frac{2000\pi}{100{,}000} = \underline{\underline{0.06823}} \text{ and } \alpha_{22}\alpha_{52} = \frac{T_n{}^2}{2}$$

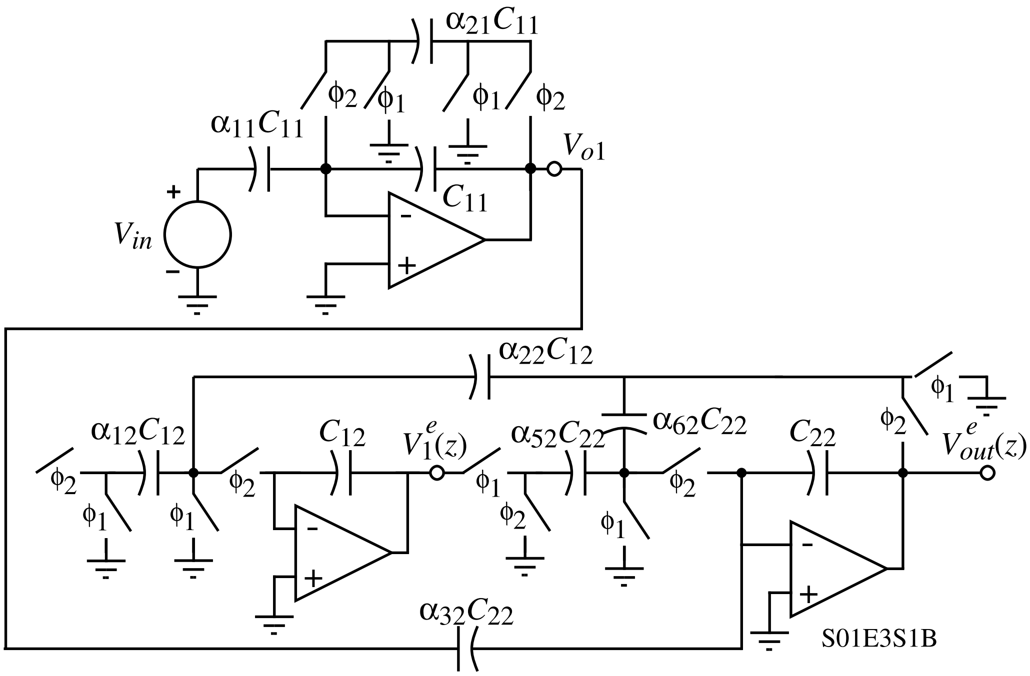
Let $\alpha_{22} = \alpha_{52}$, then $\alpha_{22} = \alpha_{52} = \dfrac{T_n}{\sqrt{2}} = \dfrac{\omega_{PB}}{\sqrt{2}f_c} = \dfrac{2000\pi}{\sqrt{2}\ 100{,}000} = \underline{\underline{0.04443}}$

Therefore, $\alpha_{12} = \dfrac{T_n{}^2}{4\alpha_{52}} = \dfrac{\sqrt{2}T_n}{4} = \underline{\underline{0.02221}}$

$$\Sigma C_\mu = \left[\left(1+ \frac{0.04443}{0.2221} + \frac{1}{0.02221}\right) + \left(1+ \frac{0.06283}{0.04443} + \frac{2}{0.04443}\right)\right] = 48.025+47.4287$$

Total $\Sigma C_\mu = 32.832 + 48.025 + 47.429 = \underline{\underline{127.84C_\mu}}$ $\quad C_{max}/C_{min} = 1/0.02221 = \underline{\underline{45.025}}$

Filter schematic:



Problem 9.7-09 – Continued

```
.SUBCKT NC1 1 2 3 4
RNC1 1 0 15.916
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.06283
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.06283
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.06283
RNC2 4 0 15.916
.ENDS NC1
.SUBCKT PC1 1 2 3 4
RPC1 2 4 15.916
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 9.8328
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT USCP1 1 2 3 4
R1 1 3 1.6181
R2 2 4 1.6181
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 0.6180
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 0.6180
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 0.6180
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 0.6180
.ENDS USCP1
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 1000 10 99K
.PROBE
.END
```

Problem 9.7-10

Write the minimum set of state equations for each of the circuits shown below. Use voltage analogs of current (R=1Ω). The state equations should be in the form of the state variable equal to other state variables, including itself.

Solution

(a)

$$V_1 = \frac{1}{s_n C_{1n}}\left[\frac{V_{in}}{R_{0n}} - \frac{V_1}{R_{0n}} - V_2'\right]$$

$$V_2' = \frac{1}{s_n L_{2n}}(V_1 - V_{out})$$

$$V_{out} = \frac{1}{s_n C_{3n}}\left[V_2' - \frac{V_{out}}{R_{4n}} - \frac{V_1}{R_{0n}}\right]$$

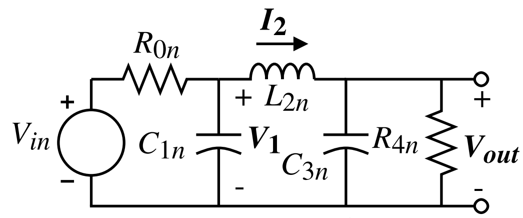


Fig. S9.7-10A

∴

$$V_1' = \frac{1}{s_n L_{1bn} + \dfrac{1}{s_n C_{1n}}}[V_1 - V_{out}]$$

$$= \frac{\dfrac{s_n}{L_{1bn}}}{s_n^2 + 1}[V_1 - V_{out}]$$

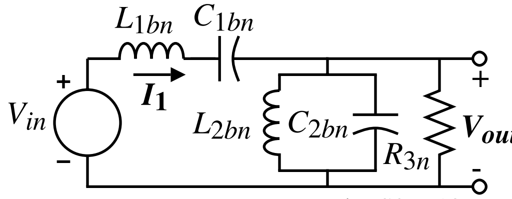


Fig. S9.7-10B

$$V_{out} = \frac{1}{s_n C_{2bn} + \dfrac{1}{s_n L_{2bn}}}\left(V_1' - \frac{V_{out}}{R_{4n}}\right) = \frac{\dfrac{s_n}{C_{2bn}}}{s_n^2 + 1}\left(V_1' - \frac{V_{out}}{R_{4n}}\right)$$

∴ The simplest way to work this one is make the following transformation (see pp. 228-230 of *Switched Capacitor Circuits*, P.E. Allen and E.S. Sanchez, Van Nostrand Reinhold,1984).

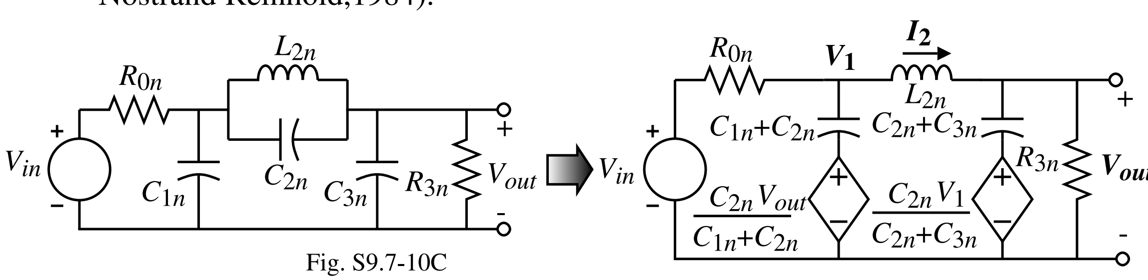


Fig. S9.7-10C

$$V_1 = \frac{1}{s_n(C_{1n} + C_{2n})}\left[\frac{V_{in}}{R_{0n}} - \frac{V_1}{R_{0n}} - V_2'\right] + \frac{C_{2n}}{C_{1n} + C_{2n}}V_{out}$$

$$V_2' = \frac{1}{s_n L_{2n}}(V_1 - V_{out})$$

$$V_{out} = \frac{1}{s_n(C_{2n} + C_{3n})}\left[V_2' - \frac{V_{out}}{R_{3n}}\right] + \frac{C_{2n}}{C_{2n} + C_{3n}}V_{out}$$

Problem 9.7-11

Give a continuous time and switched capacitor implementation of the following state equations. Use minimum number of components and show the values of the capacitors and the phasing of each switch (ϕ_1 and ϕ_2). Give capacitor values in terms of the parameters of the state equations and Ω_n and f_c for the switched capacitor implementations.

1.) $V_1 = \frac{1}{sK}[-\alpha_1 V_1 + \alpha_2 V_2 - \alpha_3 V_3]$

2.) $V_1 = \frac{s}{s^2+1}[-\alpha_1 V_1 + \alpha_2 V_2 - \alpha_3 V_3]$

$\therefore\ V_1 = \frac{1}{sK}[-\alpha_1 V_1 + \alpha_2 V_2] + \alpha_3 V_3$

Solution

1.)

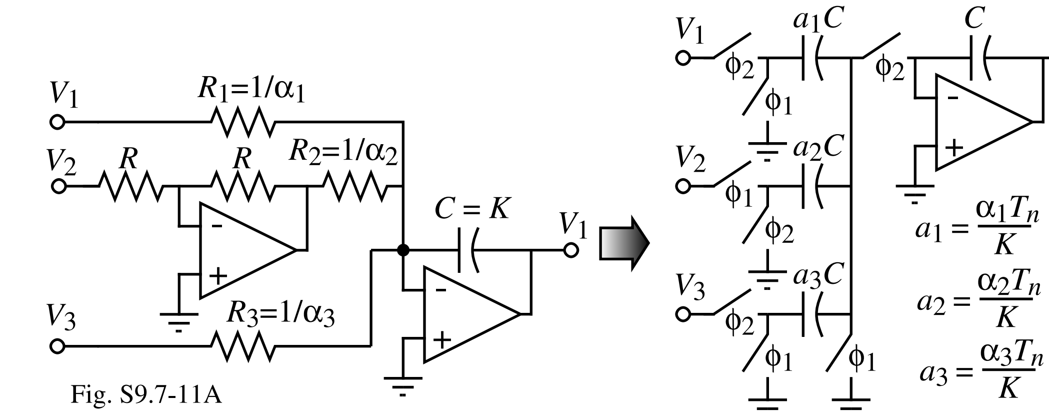


Fig. S9.7-11A

2.)

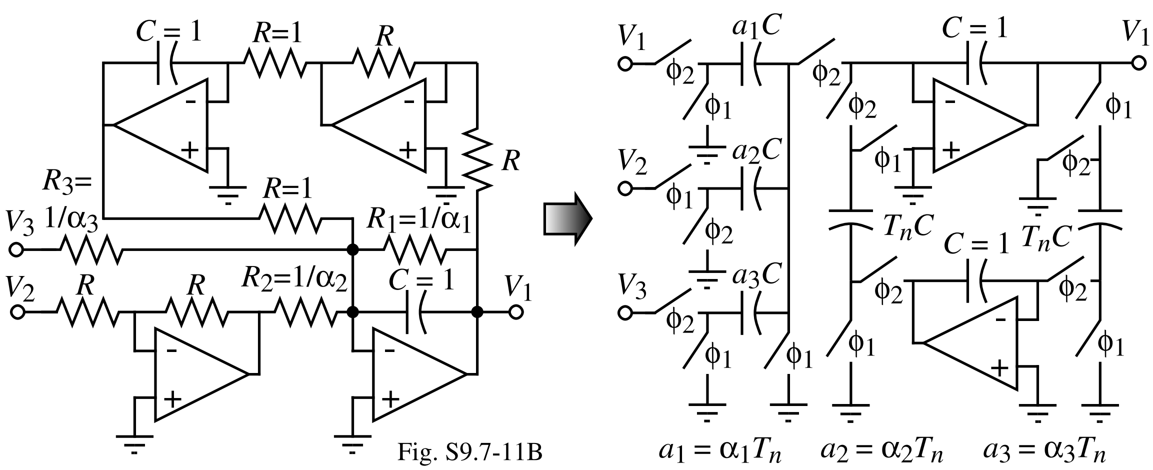


Fig. S9.7-11B

Problem 9.7-11 - Continued

3.)

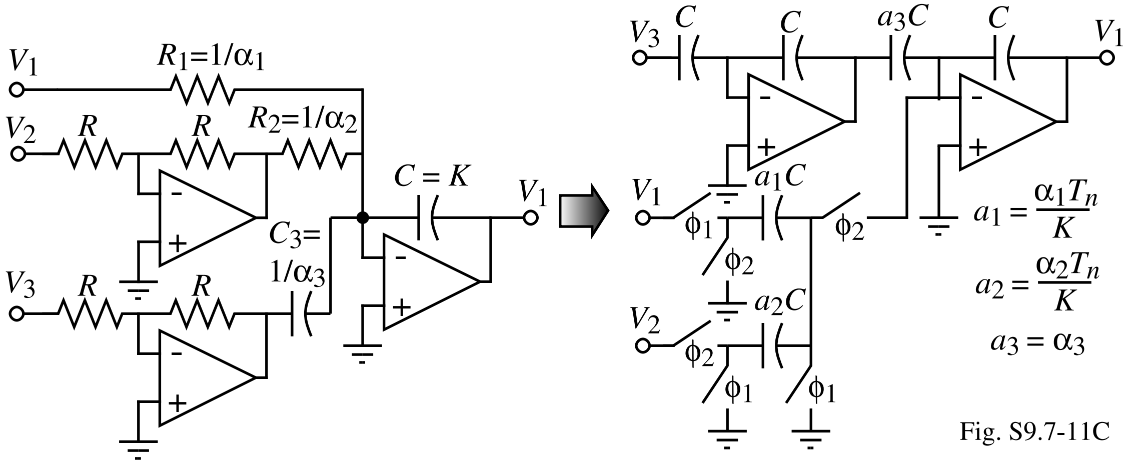


Fig. S9.7-11C

Problem 9.7-12

Find a switched capacitor, realization of the low-pass normalized RLC ladder filter shown. The cutoff frequency of the low-pass filter is 1000Hz and the clock frequency is 100kHz. Give the value of all capacitors in terms of the integrating capacitor of each stage and show the correct phasing of switches. What is the C_{max}/C_{min} and the total units of capacitance for this filter? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

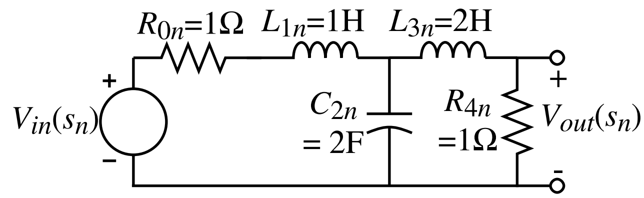


Figure P9.7-12

Solution

The state equations are:

$$V_s = I_1R_{on}+sL_{1n}I_1+V_2 \rightarrow I_1 = \frac{1}{sL_{1n}}\left(V_s - \frac{RI_1R_{on}}{R} - V_2\right) \rightarrow \boxed{V_1' = \frac{R}{sL_{1n}}\left(V_s - \frac{V_1'R_{on}}{R} - V_2\right)}$$

$$I_1 - I_3 = sC_{2n}V_2 \;\rightarrow\; V_1' - V_3' = sRC_{2n}V_2 \;\rightarrow\; \boxed{V_2 = \frac{1}{sRC_{2n}}(V_1' - V_3')}$$

$$V_2 = sL_{3n}I_3 + I_3R_{4n} \;\rightarrow\; I_3 = \frac{1}{sL_{3n}}(V_2 - I_3R_{4n}) \;\rightarrow\; V_3' = \frac{R}{sL_{3n}}\left(V_2 - \frac{R_{4n}}{R}V_3'\right)$$

But, $V_{out} = I_3R_{4n} = V_3'\frac{R_{4n}}{R} \;\rightarrow V_3' = \frac{R}{R_{4n}}V_{out} \;\rightarrow\; \boxed{V_{out} = \frac{R_{4n}}{sL_{3n}}(V_2 - V_{out})}$

Normalized realizations:

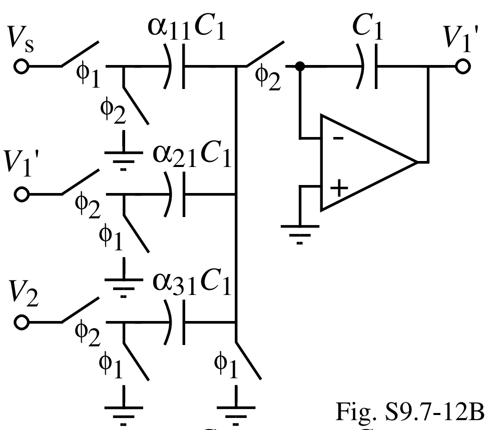


Fig. S9.7-12B

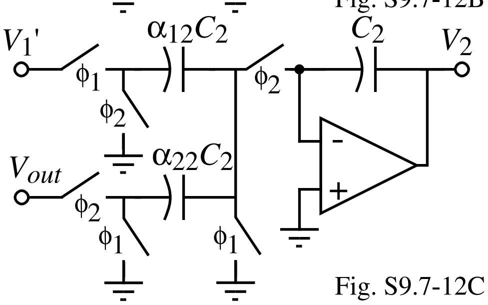


Fig. S9.7-12C

$$V_1' \approx \frac{1}{sT_n}[\alpha_{11}V_s - \alpha_{21}V_1' - \alpha_{31}V_2]$$

Comparing with the first state equation:

$$\frac{\alpha_{11}}{T_n} = \frac{R}{L_{1n}} \;\rightarrow\; \alpha_{11} = \frac{RT_n}{L_{1n}} = \frac{R\Omega_n}{f_cL_{1n}} = \frac{1\cdot 2000\pi}{10^5\cdot 1}$$

$$\alpha_{11} = \pi/50 = \underline{\underline{0.0628}} = \alpha_{21}$$

$$\frac{\alpha_{31}}{T_n} = \frac{R_{on}}{L_{1n}} \;\rightarrow\; \alpha_{31} = \frac{R_{on}\Omega_n}{f_cL_{1n}} = \alpha_{11} = \underline{\underline{0.0628}}$$

$$V_2 \approx \frac{1}{sT_n}[\alpha_{12}V_1' - \alpha_{22}V_{out}]$$

Comparing with the second state equation:

$$\frac{\alpha_{12}}{T_n} = \frac{1}{RC_{2n}} \;\rightarrow\; \alpha_{12} = \frac{T_n}{RC_{2n}} = \frac{\Omega_n}{Rf_cC_{2n}} = \frac{1\cdot 2000\pi}{1\cdot 2\cdot 10^5}$$

$$\alpha_{12} = \pi/100 = \underline{\underline{0.0314}} = \alpha_{22}$$

Problem 9.7-12 – Continued

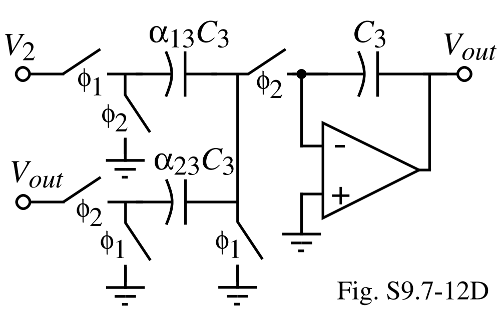


Fig. S9.7-12D

$$V_{out} \approx \frac{1}{sT_n}[\alpha_{13}V_2 - \alpha_{23}V_{out}]$$

Comparing with the third state equation:

$$\frac{\alpha_{13}}{T_n} = \frac{1}{R_{4n}L_{3n}}$$

$$\alpha_{13} = \frac{T_n}{R_{4n}L_{3n}} = \frac{\Omega_n}{R_{4n}f_cL_{3n}} = \frac{1\cdot 2000\pi}{1\cdot 10^5}$$

$$\alpha_{13} = \pi/50 = \underline{\underline{0.0628}} = \alpha_{23}$$

Connect the above three circuits together to get the resulting filter.

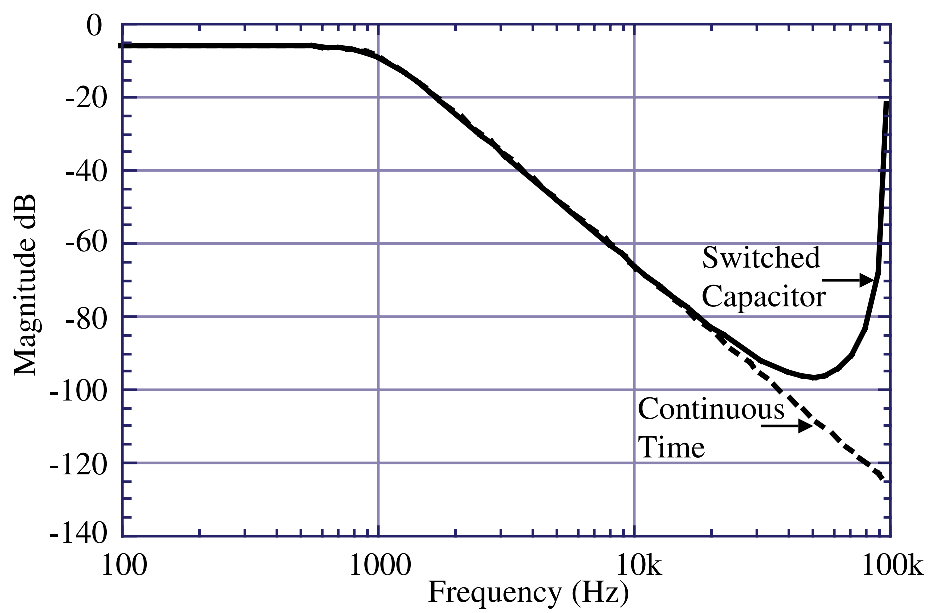
The $C_{max}/C_{min} = 1/\alpha_{12} = \underline{\underline{31.83}}$. The units of capacitances normalized to each integrating capacitor is 3 + (1/0.0628) = 18.91 for the first stage, 2 + (1/0.0314) = 33.83 for the second stage and 2 + (1/0.0628) = 17.91for the third stage. The total units of capacitance for this filter is <u>70.66 units</u>.

The SPICE simulation file for this filter is shown below.

```
SPICE File for Problem 9.7-12
*** Node 13 and 14 are Switched Cap outputs
*** Node 23 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1' STAGE ***
XNC11 1 2 3 4 NC1
XPC21 9 10 3 4 PC1
XPC31 5 6 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP
*** V2 STAGE ***
XNC12 5 6 7 8 NC2
XPC22 13 14 7 8 PC2
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** VOUT STAGE ***
XNC13 9 10 11 12 NC1
XPC23 13 14 11 12 PC1
XUSCP3 11 12 13 14 USCP
XAMP3 11 12 13 14 AMP
*** RLC LADDER NETWORK ***
R1 1 21 50
L1 21 22 7.9577E-3
C2 22 0 6.3662E-6
L3 22 23 7.9577E-3
R2 23 0 50
**************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 15.9155
```

Problem 9.7-12 – Continued

```
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.062832
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.062832
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.062832
RNC2 4 0 15.9155
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 31.831
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.031416
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.031416
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.031416
RNC2 4 0 31.831
.ENDS NC2
.SUBCKT PC1 1 2 3 4
RPC1 2 4 15.9155
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 31.831
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 100 10 199K
.PRINT AC VDB(13) VDB(14) VDB(23) VP(13) VP(14) VP(23)
.END
```



<u>Problem 9.7-13</u>

Design a switched capacitor realization of the low-pass prototype filter shown in Fig. 9.7-13 assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

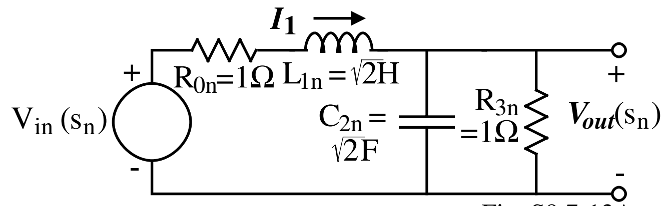


Fig. S9.7-13A

<u>Solution</u>

The state equations are:

$$V_{in} = I_1R_{on}+sL_{1n}I_1+V_{out} \quad \rightarrow \quad \boxed{V_1' = \frac{R}{sL_{1n}}\left(V_{in} - \frac{V_1'R_{on}}{R} - V_{out}\right)}$$

$$I_1 - \frac{V_{out}}{R_{3n}} = sC_{2n}V_{out} \quad \rightarrow \quad \boxed{V_{out} = \frac{1}{sRC_{2n}}\left(V_1' - \frac{R}{R_{3n}}V_{out}\right)}$$

The normalized realizations for these equations are:

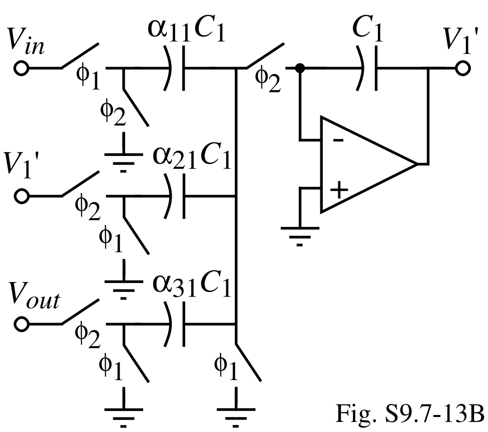


Fig. S9.7-13B

$$V_1' \approx \frac{1}{sT_n}[\alpha_{11}V_{in} - \alpha_{21}V_1' - \alpha_{31}V_{out}]$$

Comparing with the first state equation:

$$\frac{\alpha_{11}}{T_n} = \frac{R}{L_{1n}} \rightarrow \alpha_{11} = \frac{RT_n}{L_{1n}} = \frac{R\Omega_n}{f_cL_{1n}} = \frac{1\cdot 2000\pi}{10^5\cdot\sqrt{2}}$$

$$\alpha_{11} = \underline{\underline{0.04443}} = \alpha_{21}$$

$$\frac{\alpha_{31}}{T_n} = \frac{R_{on}}{L_{1n}} \rightarrow \alpha_{31} = \frac{R_{on}\Omega_n}{f_cL_{1n}} = \alpha_{11} = \underline{\underline{0.04443}}$$

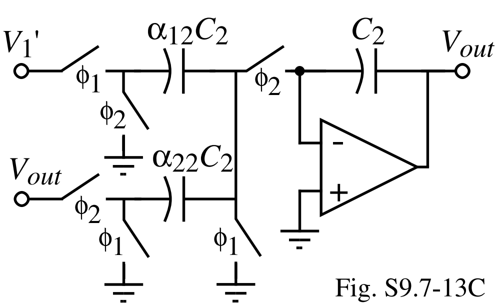


Fig. S9.7-13C

$$V_{out} \approx \frac{1}{sT_n}[\alpha_{12}V_1' - \alpha_{22}V_{out}]$$

Comparing with the second state equation:

$$\frac{\alpha_{12}}{T_n} = \frac{1}{RC_{2n}} \rightarrow \alpha_{12} = \frac{T_n}{RC_{2n}} = \frac{\Omega_n}{Rf_cC_{2n}} = \frac{1\cdot 2000\pi}{1\cdot 10^5\cdot\sqrt{2}}$$

$$\alpha_{12} = \underline{\underline{0.04443}} = \alpha_{22}$$

Connect the above two circuits together to get the resulting filter.

Problem 9.7-13 – Continued

The $C_{max}/C_{min} = 1/\alpha_{12} = \underline{\underline{22.508}}$. The units of capacitances normalized to each integrating capacitor is 3 + (1/0.04443) = 25.51 for the first stage and 2 + (1/0.0314) = 24.51 for the second stage. The total units of capacitance for this filter is 50.158 units.

The SPICE simulation file for this filter is shown below.

```
SPICE File for Problem 9.7-13
*** Node 9 and 10 are Switched Cap outputs
*** Node 22 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1' STAGE ***
XNC11 1 2 3 4 NC1
XPC21 5 6 3 4 PC1
XPC31 9 10 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP
*** VOUT STAGE ***
XNC12 5 6 7 8 NC2
XPC22 9 10 7 8 PC2
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** RLC LADDER NETWORK ***
R1 1 21 50
L1 21 22 11.254E-3
C2 22 0 4.50158E-6
R2 22 0 50
**************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 22.5079
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.04443
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.04443
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.04443
RNC2 4 0 22.5079
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 22.5079
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.04443
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.04443
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.04443
RNC2 4 0 22.5079
.ENDS NC2
.SUBCKT PC1 1 2 3 4
RPC1 2 4 22.5079
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 22.5079
```

Problem 9.7-13

```
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 20 10 199K
.PRINT AC VDB(9) VDB(10) VDB(23) VP(9) VP(10) VP(23)
.END
```

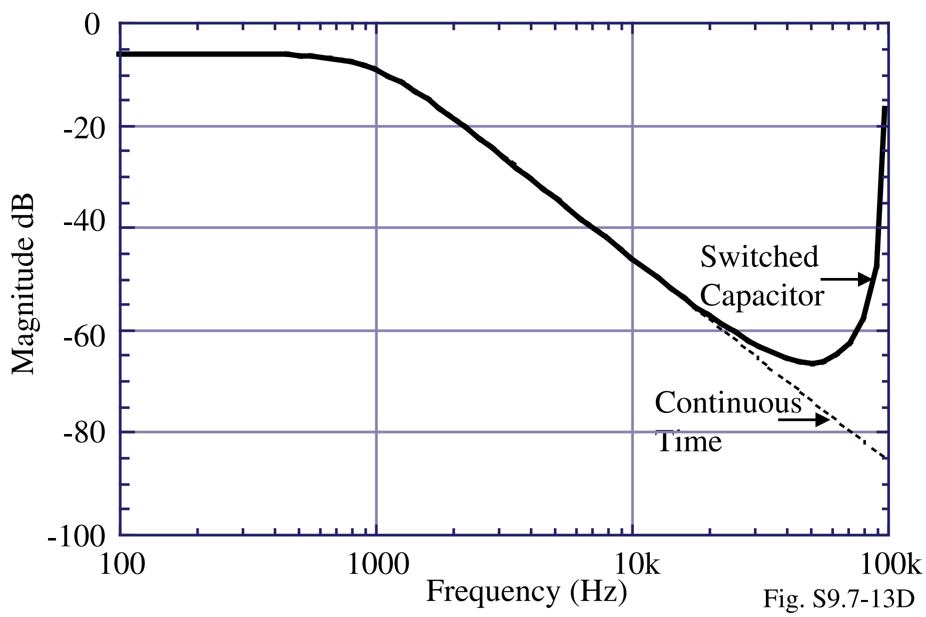


Fig. S9.7-13D

Problem 9.7-14

Design a switched capacitor realization of the low-pass prototype filter shown assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is C_{max}/C_{min}?

Solution

First normalize T by $\Omega_n = 2000\pi$ to get $T_n = \Omega_n T = 2000\pi/100{,}000 = 0.06283$

The state equations are:

$$V_{in} = (I_2 + sC_{1n}V_1)R_{0n} + V_1 \quad \rightarrow \qquad V_1 = \frac{1}{sR_{0n}C_{1n}}\left[V_{in} - V_1 - \frac{R_{0n}}{R}V_2'\right]$$

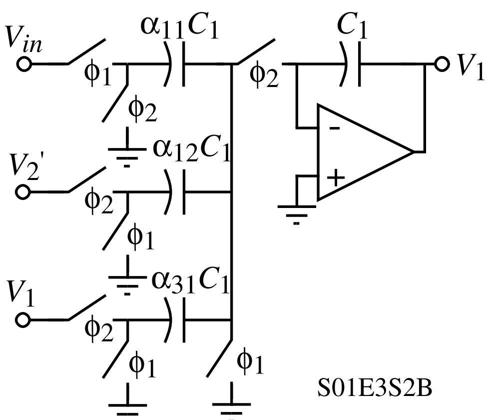
and

$$V_1 = I_2 sL_{2n} + I_2 R_{3n} \quad \rightarrow V_1 = \frac{sL_{2n}}{R} + \frac{R_{3n}}{R}V_2' \quad \rightarrow V_2' = \frac{R}{sL_{2n}}\left[V_1 - \frac{R_{3n}}{R}V_2'\right]$$

Since $V_2' = V_{out}$, we can write

$$V_{out} = \frac{R}{sL_{2n}}\left[V_1 - \frac{R_{3n}}{R}V_{out}\right]$$

Realization of the first state equation:



S01E3S2B

$$V_1(z) = \left(\frac{1}{z_n - 1}\right)[\alpha_{11}V_{in} - \alpha_{21}V_2' - \alpha_{31}V_1]$$

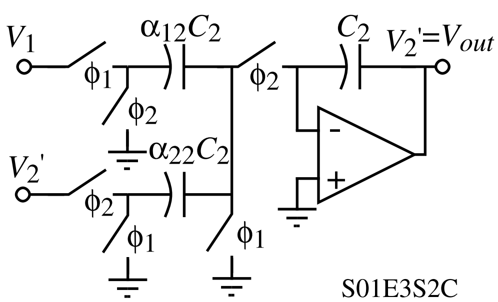
Let $z_n \approx 1 + s_nT_n$ to get

$$V_1(s) = \frac{1}{s_nT_n}[\alpha_{11}V_{in}(s_n) - \alpha_{21}V_2'(s_n) - \alpha_{31}V_1(s_n)]$$

$$\therefore\ \alpha_{11} = \frac{RT_n}{R_{0n}C_{1n}} = \frac{\Omega_n}{f_cC_{1n}} = \frac{2000\pi}{\sqrt{2}\ 10^5} = 0.0444$$

Since, $R = R_{0n}$, then $\alpha_{21} = \alpha_{31} = \alpha_{11} = 0.4444$

Realization of the second state equation:



S01E3S2C

$$V_{out}(z) = \left(\frac{1}{z_n - 1}\right)[\alpha_{12}V_1 - \alpha_{22}V_2']$$

Let $z_n \approx 1 + s_nT_n$ to get

$$V_{out}(s) = \frac{1}{s_nT_n}[\alpha_{12}V_1(s_n) - \alpha_{22}V_2'(s_n)]$$

$$\therefore\ \alpha_{12} = \frac{T_n}{L_{2n}} = \frac{\Omega_n}{f_cL_{2n}} = \frac{2000\pi}{\sqrt{2}\ 10^5} = 0.0444$$

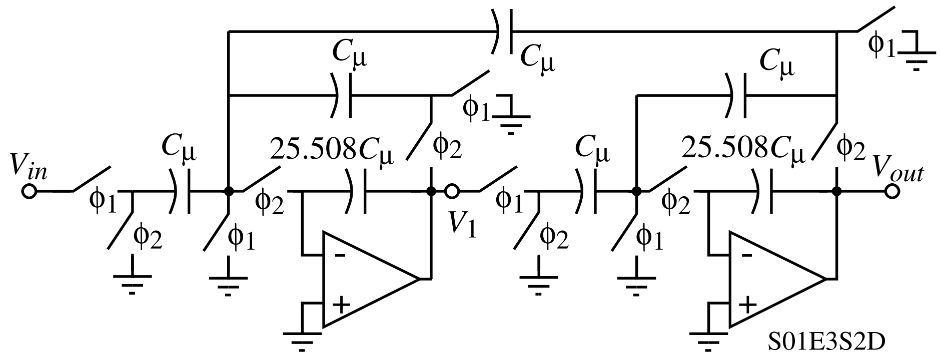
$\alpha_{12} = \alpha_{22} = 0.4444$

Problem 9.7-14 – Continued

$$\frac{C_{max}}{C_{min}} = \frac{1}{0.0444} = \underline{\underline{22.508}}$$

$$\Sigma C = [(22.508+3) + (22.508+2)]C_\mu = \underline{\underline{50.0158C_\mu}}$$

Realization:



Problem 9.7-15

Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

The state equations are:

$$V_{in} = sL_{1n}I_1 + V_2 \quad \rightarrow \quad I_1 = \frac{1}{sL_{1n}}(V_{in} - V_2) \quad \rightarrow \quad \boxed{V_1' = \frac{R}{sL_{1n}}(V_{in} - V_2)}$$

$$V_2 = \frac{1}{sC_{2n}}(I_1 - I_3) \quad \rightarrow \quad V_2 = \frac{1}{sRC_{2n}}(V_1' - V_3') \quad \rightarrow$$

$$\boxed{V_2 = \frac{1}{sRC_{2n}}\left(V_1' - \frac{R}{R_{4n}}V_2\right)}$$

$$I_3 = \frac{1}{sL_{3n}}(V_2 - V_{out}) \quad \rightarrow \quad V_{out} = I_3R_{4n} \quad \rightarrow \quad \boxed{V_{out} = \frac{R_{4n}}{sL_{3n}}(V_2 - V_{out})}$$

The normalized realizations for these equations are:

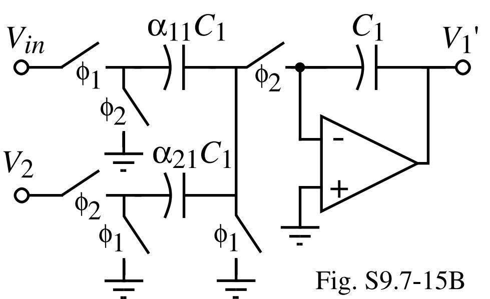


Fig. S9.7-15B

$$V_1' \approx \frac{1}{sT_n}[\alpha_{11}V_{in} - \alpha_{21}V_2]$$

Comparing with the first state equation:

$$\frac{\alpha_{11}}{T_n} = \frac{R}{L_{1n}} \quad \rightarrow \quad \alpha_{11} = \frac{RT_n}{L_{1n}} = \frac{R\Omega_n}{f_cL_{1n}} = \frac{1\cdot 2000\pi}{10^5\cdot 0.5}$$

$$\alpha_{11} = \underline{\underline{0.125664}} = \alpha_{21}$$

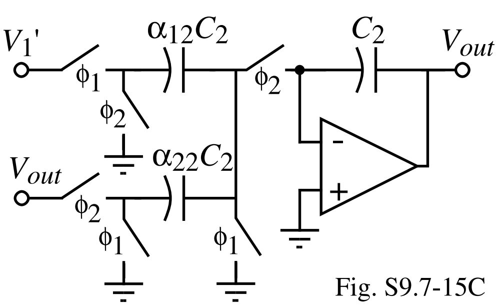


Fig. S9.7-15C

$$V_{out} \approx \frac{1}{sT_n}[\alpha_{12}V_1' - \alpha_{22}V_{out}]$$

Comparing with the second state equation:

$$\frac{\alpha_{12}}{T_n} = \frac{1}{RC_{2n}} \rightarrow \alpha_{12} = \frac{T_n}{RC_{2n}} = \frac{\Omega_n}{Rf_cC_{2n}} = \frac{2000\pi}{10^5\cdot(4/3)}$$

$$\alpha_{12} = \underline{\underline{0.047124}} = \alpha_{22}$$

Problem 9.7-15 – Continued

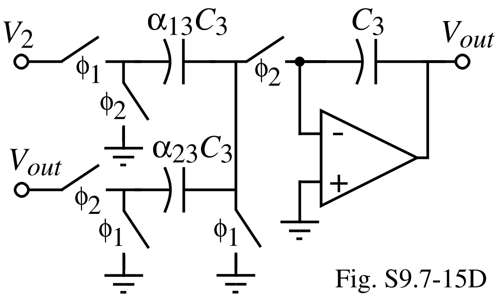


Fig. S9.7-15D

$$V_{out} \approx \frac{1}{sT_n}[\alpha_{13}V_2 - \alpha_{23}V_{out}]$$

Comparing with the third state equation:

$$\frac{\alpha_{13}}{T_n} = \frac{1}{R_{4n}L_{3n}}$$

$$\alpha_{13} = \frac{T_n}{R_{4n}L_{3n}} = \frac{\Omega_n}{R_{4n}f_cL_{3n}} = \frac{2000\pi}{10^5(3/2)}$$

$$\alpha_{13} = \underline{\underline{0.041888}} = \alpha_{23}$$

Connect the above three circuits together to get the resulting filter.

The $C_{max}/C_{min} = 1/\alpha_{13} = \underline{\underline{23.87}}$. The units of capacitances normalized to each integrating capacitor is 2 + (1/0.126) = 9.936 for the first stage, 2 + (1/0.0471) = 23.231 for the second stage and 2 + (1/0.0419) = 25.8671for the third stage. The total units of capacitance for this filter is $\underline{\underline{\text{59.03 units}}}$.

The SPICE simulation file for this filter is shown below.

```
SPICE File for Problem 9.7-15
*** Node 13 and 14 are Switched Cap outputs
*** Node 22 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1' STAGE ***
XNC11 1 2 3 4 NC1
XPC21 9 10 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP
*** V2 STAGE ***
XNC12 5 6 7 8 NC2
XPC22 13 14 7 8 PC2
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** VOUT STAGE ***
XNC13 9 10 11 12 NC3
XPC23 17 18 11 12 PC3
XUSCP3 11 12 13 14 USCP
XAMP3 11 12 13 14 AMP
*** RLC LADDER NETWORK ***
L1 1 21 3.9789E-3
C2 21 0 4.2441E-6
L3 21 22 11.9366E-3
R4 22 0 50
**************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 7.957729
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.125664
```

Problem 9.7-15 – Continued

```
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.125664
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.125664
RNC2 4 0 7.957729
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 21.2206
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.047124
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.047124
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.047124
RNC2 4 0 21.2206
.ENDS NC2
.SUBCKT NC3 1 2 3 4
RNC1 1 0 23.8732
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.041888
XNC2 1 4 14 DELAY
GNC2 4 1 14 0.041888
XNC3 4 0 40 DELAY
GNC3 4 0 40 0.041888
RNC2 4 0 23.8732
.ENDS NC3
.SUBCKT PC1 1 2 3 4
RPC1 2 4 7.957729
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 21.2206
.ENDS PC2
.SUBCKT PC3 1 2 3 4
RPC1 2 4 23.8732
.ENDS PC3
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 20 10 200K
.PRINT AC VDB(13) VDB(14) VDB(22)
+VP(13) VP(14) VP(22)
.END
```

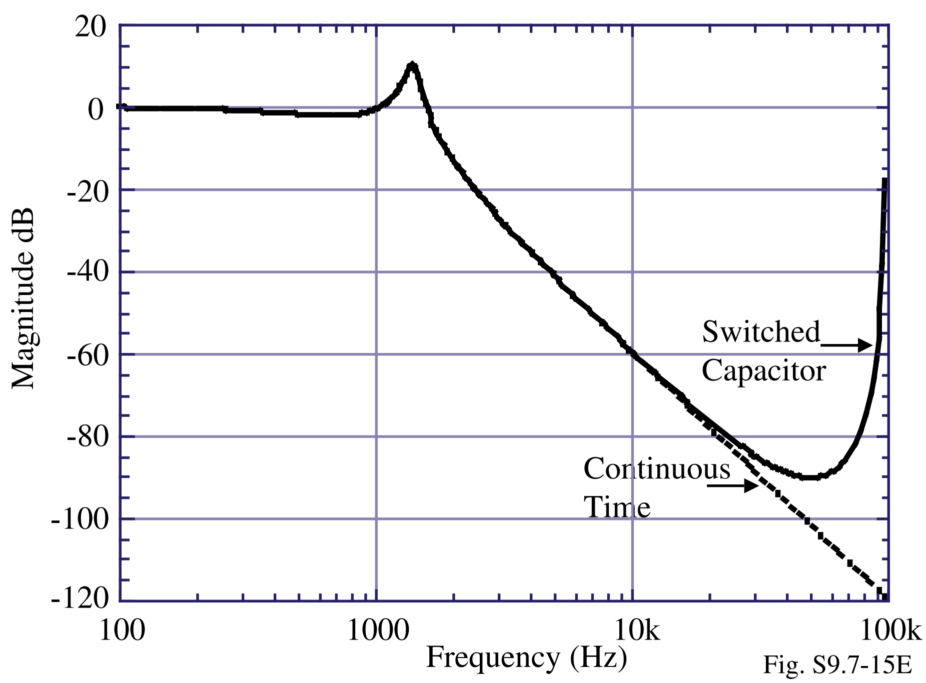
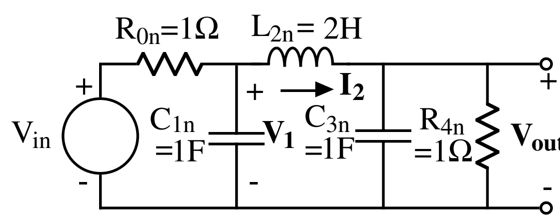


Fig. S9.7-15E

Problem 9.7-16

Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C (the capacitor connected from op amp output to inverting input). Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}?



Solution

Normalize $T = 1/f_c$ by $\Omega_n = 2000\pi$ to get $T_n = \Omega_n T$.

State Equations:

1.) $$\frac{V_{in} - V_1}{R_{0n}} = sC_{1n}V_1 + I_2 \Rightarrow V_1 = \frac{1}{sC_{1n}}\left(\frac{V_{in}}{R_{0n}} - \frac{V_1}{R_{0n}} - I_2\right) = \frac{1}{sC_{1n}R_{0n}}\left(V_{in} - V_1 - \frac{R_{0n}V_2'}{R}\right)$$

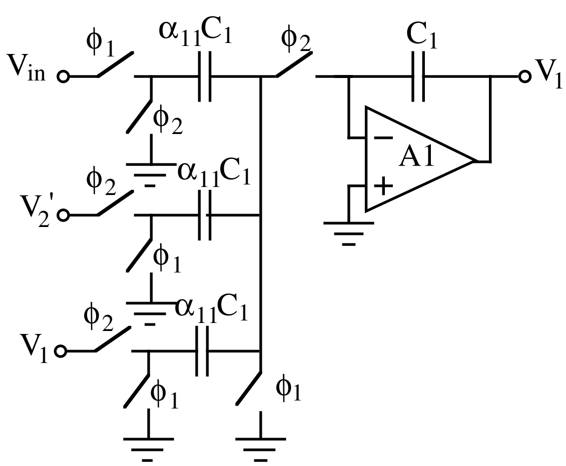
or $$\boxed{V_1 = \frac{1}{sC_{1n}R_{0n}}\left(V_{in} - V_1 - \frac{R_{0n}V_2'}{R}\right)}$$ where $V_2' = RI_2$

2.) $$I_2 = \frac{1}{sL_{2n}}(V_1 - V_{out}) \Rightarrow \boxed{V_2' = \frac{R}{sL_{2n}}(V_1 - V_{out})}$$

3.) $$I_2 = sC_{3n}V_{out} + \frac{V_{out}}{R_{4n}} \Rightarrow V_{out} = \frac{1}{sC_{3n}}\left(I_2 - \frac{V_{out}}{R_{4n}}\right) \Rightarrow \boxed{V_{out} = \frac{1}{sC_{3n}R}\left(V_2' - \frac{RV_{out}}{R_{4n}}\right)}$$

Realizations (Assume $R = R_{0n} = R_{4n}$):

1.)



$$V_1 = \frac{1}{z_n - 1}\left[\alpha_{11}V_{in} - \alpha_{11}z_nV_2' - \alpha_{11}z_nV_1\right]$$

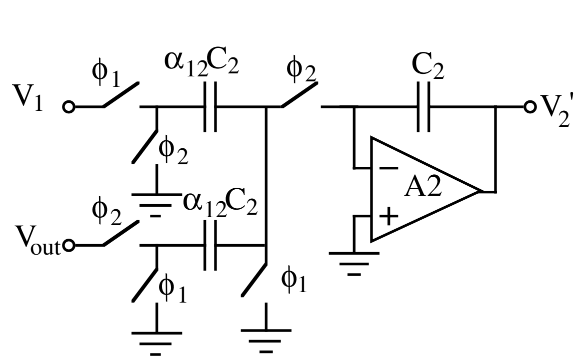
Assume $sT_n \ll 1$ and let $z_n \approx 1 + sT_n$ to get

$$V_1(s) \approx \frac{\alpha_{11}}{sT_n}(V_{in} - V_2' - V_1)$$

$$\therefore\ \alpha_{11} = \frac{T_n}{C_{1n}R_{0n}} = \frac{2000\pi}{10^5 \cdot 1} = 0.0628$$

Problem 9.7-16 – Continued

2.)



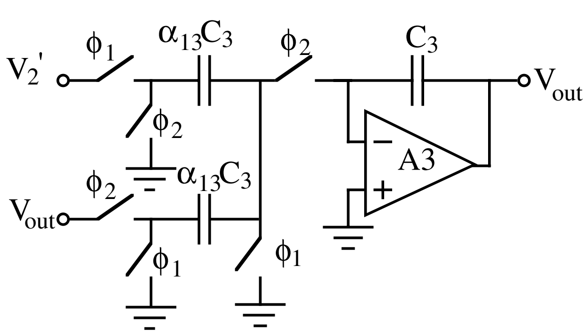
$$V_2' = \frac{1}{z_n-1}\,[\alpha_{12}V_1 - \alpha_{12}z_nV_{out}]$$

Assume sT_n <<1 and let $z_n \approx 1+sT_n$ to get

$$V_1(s) \approx \frac{\alpha_{12}}{sT_n}(V_1 - V_{out})$$

$$\therefore\ \alpha_{12} = \frac{RT_n}{L_{2n}} = \frac{2000\pi}{10^5 \cdot 2} = 0.0314$$

3.)



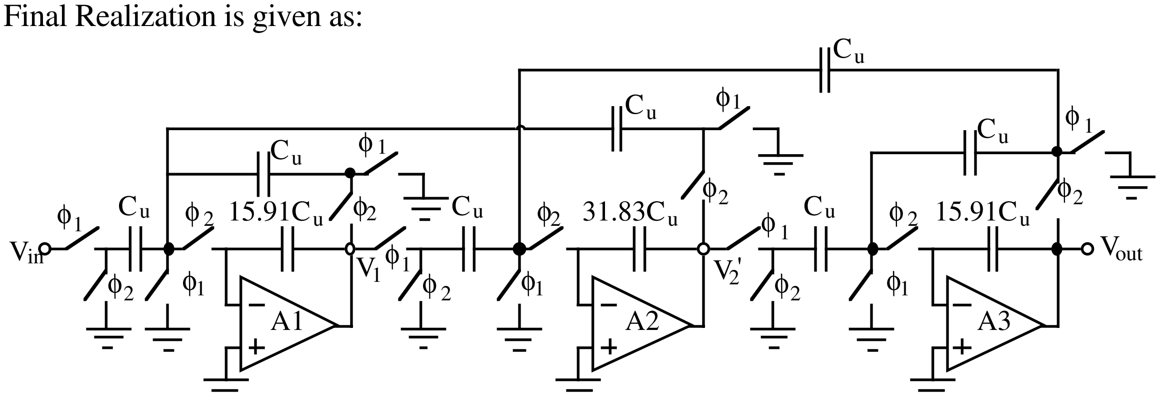
$$V_{out} = \frac{1}{z_n-1}\,[\alpha_{13}V_2' - \alpha_{13}z_nV_{out}]$$

Assume sT_n <<1 and let $z_n \approx 1+sT_n$ to get

$$V_{out}(s) \approx \frac{\alpha_{13}}{sT_n}(V_2' - V_{out})$$

$$\therefore\ \alpha_{12} = \frac{T_n}{RC_{3n}} = \frac{2000\pi}{10^5 \cdot 1} = 0.0628$$

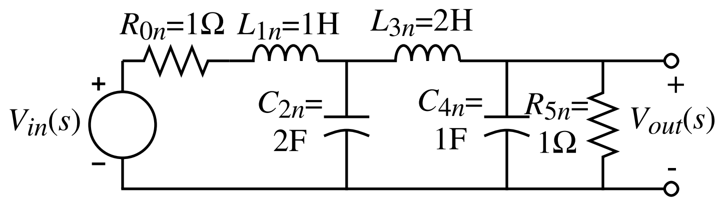
Final Realization is given as:



The total capacitance is $70.65C_u$ where C_u is a unit capacitance. The largest C_{max}/C_{min} ratio is 31.83.

Problem 9.7-17

Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 200 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C (the capacitor connected from op amp output to inverting input). Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}?



FigS9.7-17

Solution

First we must normalize the clock period, T, by $\Omega_n = 2000\pi$ to get $T_n = \Omega_n T = \Omega_n/f_c$.

The state equations for the bold variables above are:

1.) $V_{in} = R_{0n}I_1 + sL_1I_1 + V_2 = \dfrac{R_{0n}}{R}V_1' + \dfrac{sL_1}{R}V_1' + V_2 \rightarrow V_1' = \dfrac{R}{sL_{1n}}\left(V_{in} - \dfrac{R_{0n}}{R}V_1' - V_2\right)$

2.) $V_2 = \dfrac{1}{sRC_{2n}}(V_1' - V_3')$

3.) $V_3' = \dfrac{R}{sL_{3n}}(V_2 - V_{out})$

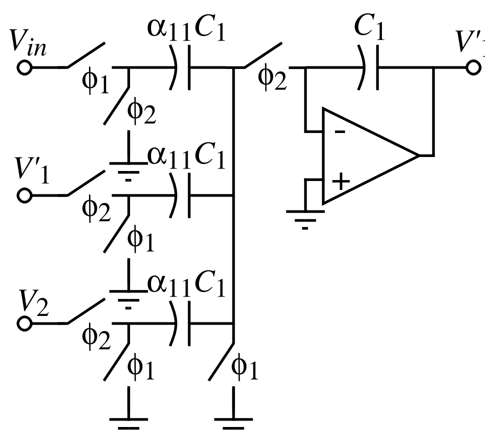
4.) $I_3 = sC_{4n}V_{out} + \dfrac{V_{out}}{R_{5n}} \rightarrow V_{out} = \dfrac{1}{sRC_{4n}}\left(V_3' - \dfrac{R}{R_{5n}}V_{out}\right)$

Realizing each of these four state equations is done as follows:

1.) $V_1'(z_n) = \dfrac{1}{z_n - 1}[\alpha_{11}V_{in} - \alpha_{11}z_nV_2 - \alpha_{11}z_nV_1']$

$$V_1'(s) \approx \frac{\alpha_{11}}{sT_n}[V_{in} - V_2 - V_1']$$

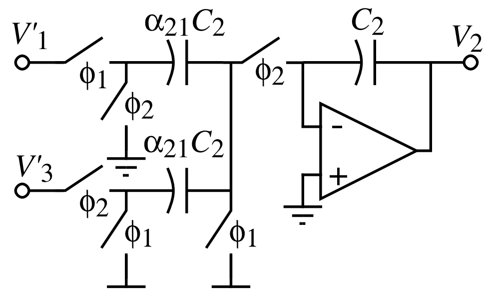
$$\therefore\ \alpha_{11} = \frac{T_nR}{L_{1n}} = \frac{2000\pi}{10^5\cdot 1} = 0.0314$$



2.) $V_2(z_n) = \dfrac{1}{z_n - 1}[\alpha_{21}V_1' - \alpha_{21}z_nV_3']$

$$V_2(s) \approx \frac{\alpha_{21}}{sT_n}[V_1' - V_3']$$

$$\therefore\ \alpha_{21} = \frac{T_n}{RC_{2n}} = \frac{2000\pi}{10^5\cdot 2} = 0.0159$$

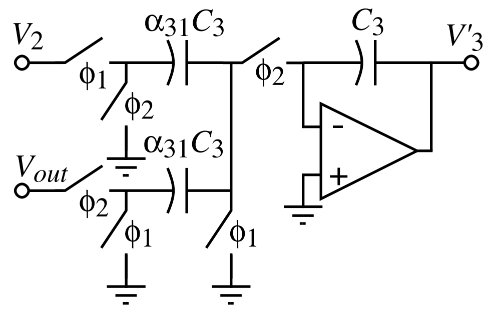


Problem 9.7-17 - Continued

3.) $V_3'(z_n) = \frac{1}{z_n - 1}[\alpha_{31}V_2 - \alpha_{31}z_nV_{out}]$

$V_3'(s) \approx \frac{\alpha_{31}}{sT_n}[V_2 - V_{out}]$

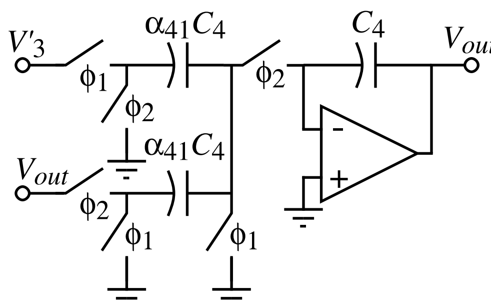
$\therefore\ \alpha_{31} = \frac{T_nR}{L_{3n}} = \frac{2000\pi}{10^5\cdot 2} = 0.0159$



4.) $V_{out}(z_n) = \frac{1}{z_n - 1}[\alpha_{41}V_3' - \alpha_{41}z_nV_{out}]$

$V_{out}(s) \approx \frac{\alpha_{41}}{sT_n}[V_3' - V_{out}]$

$\therefore\ \alpha_{41} = \frac{T_n}{RC_{4n}} = \frac{2000\pi}{10^5\cdot 1} = 0.0314$



The actual filter realization is obtained by connecting the above four circuits as indicated by their terminal voltages.

Total capacitance:

For each stage, make the smallest capacitor equal to C_u and sum capacitors.

Stage 1: $3C_u + (C_u/0.0314) = 31.8C_u + 3C_u = 34.8C_u$
Stage 2: $2C_u + (C_u/0.0159) = 63.7C_u + 2C_u = 65.7C_u$
Stage 3: $2C_u + (C_u/0.0159) = 63.7C_u + 2C_u = 65.7C_u$
Stage 4: $2C_u + (C_u/0.0314) = 31.8C_u + 2C_u = 33.8C_u$
Total capacitance = $200C_u$

$\frac{C_{max}}{C_{min}} = 63.7$

SPICE File:

```
*** HW9 PROBLEM3 (Problem 9.7-17) ***
*** Node 17 and 18 are Switched Cap outputs
*** Node 23 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1' STAGE ***
XNC11 1 2 3 4 NC1
XPC21 9 10 3 4 PC1
XPC31 5 6 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP

*** V2 STAGE ***
XNC12 5 6 7 8 NC2
XPC22 13 14 7 8 PC2
```

Problem 9.7-17 – Continued

```
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** V3' STAGE ***
XNC13 9 10 11 12 NC2
XPC23 17 18 11 12 PC2
XUSCP3 11 12 13 14 USCP
XAMP3 11 12 13 14 AMP
*** VOUT STAGE ***
XNC14 13 14 15 16 NC1
XPC24 17 18 15 16 PC1
XUSCP4 15 16 17 18 USCP
XAMP4 15 16 17 18 AMP
*** RLC LADDER NETWORK ***
R1 1 21 50
L1 21 22 7.9577E-3
C2 22 0 6.3662E-6
L3 22 23 15.9155E-3
C4 23 0 3.1831E-6
R2 23 0 50
**************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=2.5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 31.8269
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.03142
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.03142
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.03142
RNC2 4 0 31.8269
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 63.6537
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.01571
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.01571
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.01571
RNC2 4 0 63.6537
.ENDS NC2
.SUBCKT PC1 1 2 3 4
RPC1 2 4 31.8269
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 63.6537
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 1000 10 199K
.PROBE
.END
```

Problem 9.7-18

Use the low-pass, normalized prototype filter of Fig. P9.7-14 to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 500Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

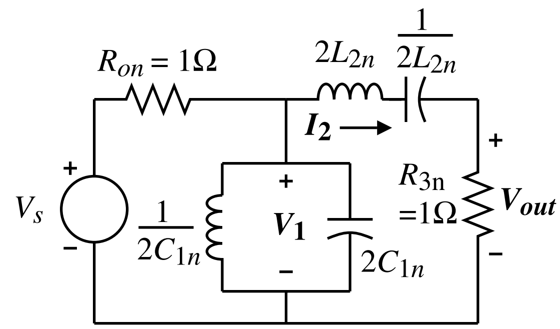
Solution

1.) Normalize by $s = \left(\frac{\omega_r}{BW}\right)p = \frac{1000}{500}p = 2p$

2.) Transform the normalized circuit to bandpass using the transformation,

$$s = p + \frac{1}{p}$$

The resulting circuit is shown.



3.) The state equations for this bandpass circuit can be written as follows.

$$V_1 = \frac{\frac{s}{2RC_{1n}}}{s^2+1}\left[\frac{R}{R_{on}}(V_{in}\text{-}V_1)\text{-}V_2'\right]$$

where $V_2' = I_2 \cdot R$ and $R = 1$.

$$V_{out} = \frac{R_{3n}}{R}\,V_2' = \frac{R_{3n}}{R}\left(\frac{\frac{sR}{2L_{2n}}}{s^2+1}\right)(V_1\text{-}V_{out}) = \left(\frac{\frac{sR_{3n}}{2L_{2n}}}{s^2+1}\right)(V_1\text{-}V_{out})$$

4.) The SC realization of each second-order block is given as,

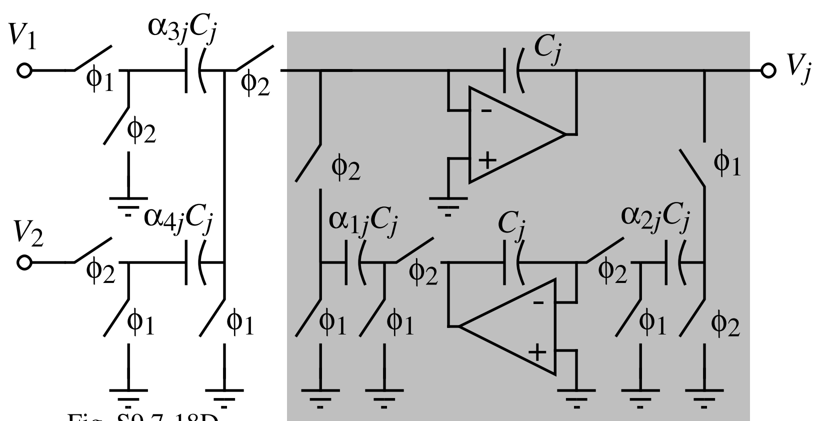


Fig. S9.7-18D

Problem 9.7-18 – Continued

If f_{clock}>>f_r, then $V_j(s)$ of the above realization can be written as,

$$V_j(s) \approx \left(\frac{s}{s^2 + \frac{\alpha_{1j}\alpha_{2j}}{T_n^2}}\right)\left[\frac{\alpha_{3j}}{T_n}V_1 - \frac{\alpha_{4j}}{T_n}V_2\right] \qquad \text{where } T_n = \Omega_n T = \omega_r T$$

5.) Comparing the state equations with the above transfer function gives,

j = 1 or V_1: $\alpha_{11}\alpha_{21} = T_n^2 \rightarrow \alpha_{11} = \alpha_{21} = T_n = \omega_r T = \frac{\omega_r}{f_{clock}} = \frac{2\pi x10^3}{10^5} = \underline{\underline{0.02\pi}}$

$$\alpha_{31} = \alpha_{41} = \alpha_{51} = \frac{T_n}{R_{on}2C_{1n}} = \frac{\omega_r T}{2\sqrt{2}} = \frac{2\pi x10^3}{2\sqrt{2}x10^5} = \underline{\underline{0.0071\pi}}$$

j = 2 or V_{out}: $\alpha_{12}\alpha_{22} = T_n^2 \rightarrow \alpha_{12} = \alpha_{22} = T_n = \omega_r T = \frac{\omega_r}{f_{clock}} = \frac{2\pi x10^3}{10^5} = \underline{\underline{0.02\pi}}$

$$\alpha_{32} = \alpha_{42} = \frac{T_n}{R_{on}2L_{2n}} = \frac{\omega_r T}{2\sqrt{2}} = \frac{2\pi x10^3}{2\sqrt{2}x10^5} = \underline{\underline{0.0071\pi}}$$

6.) Filter realization:

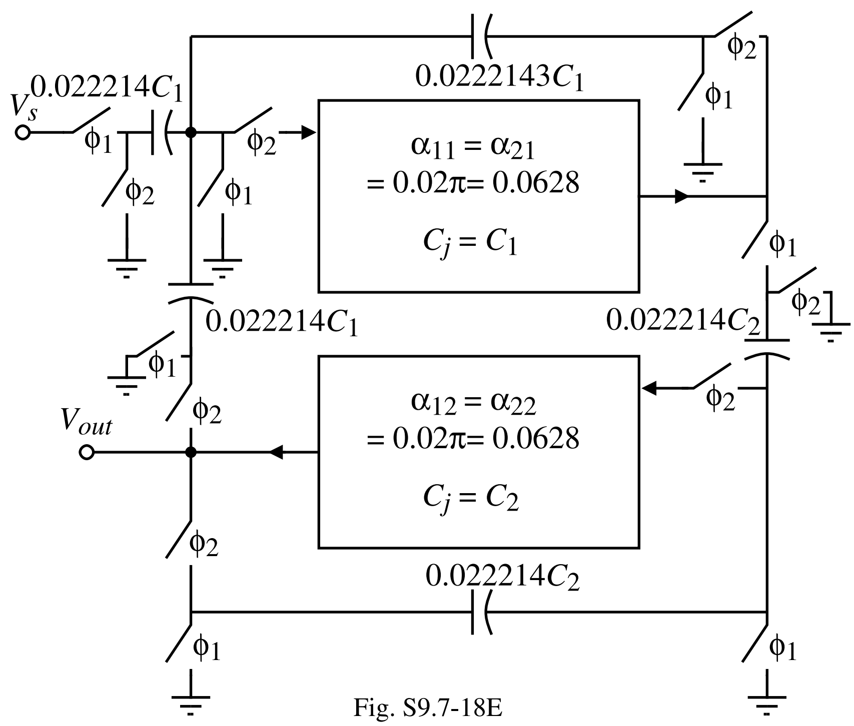


Fig. S9.7-18E

Problem 9.7-18 – Continued

7.) To create the SPICE input file, the above figure needs to be expanded which is done below.

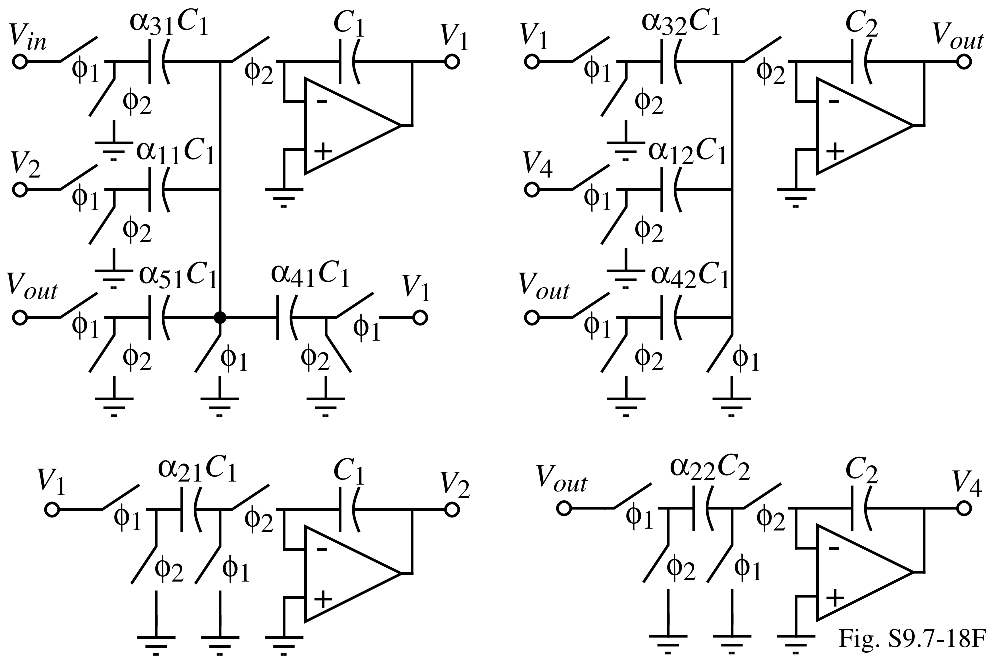


Fig. S9.7-18F

8.) The SPICE simulation file for this filter is shown below.

```
SPICE File for Problem 9.7-18
*** Node 13 and 14 are Switched Cap outputs
*** Node 23 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1 STAGE ***
XPC11 9 10 3 4 PC2
XNC31 1 2 3 4 NC1
XPC41 5 6 3 4 PC1
XPC51 13 14 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP
*** V2 STAGE ***
XNC21 5 6 7 8 NC2
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** VOUT STAGE ***
XPC12 17 18 11 12 PC2
XNC32 5 6 11 12 NC1
XPC42 13 14 11 12 PC1
XUSCP3 11 12 13 14 USCP
XAMP3 11 12 13 14 AMP
*** V4 STAGE ***
XNC22 13 14 15 16 NC2
XUSCP4 15 16 17 18 USCP
XAMP4 15 16 17 18 AMP
*** RLC LADDER NETWORK ***
R0 1 21 50
C1 21 0 9.0032E-6
L1 21 0 2.8135E-3
```

Problem 9.7-18 – Continued

```
L2 21 22 22.5079E-3
C2 22 23 1.125395E-6
R3 23 0 50
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 45.015816
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.022214
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.022214
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.022214
RNC2 4 0 45.015816
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 15.91549
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.062832
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.062832
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.062832
RNC2 4 0 15.91549
.ENDS NC2
.SUBCKT PC1 1 2 3 4
RPC1 2 4 45.015816
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 15.91549
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 20 100 100K
.PRINT AC VDB(17) VDB(18) VDB(23) VP(17) VP(17) VP(23)
.END
```

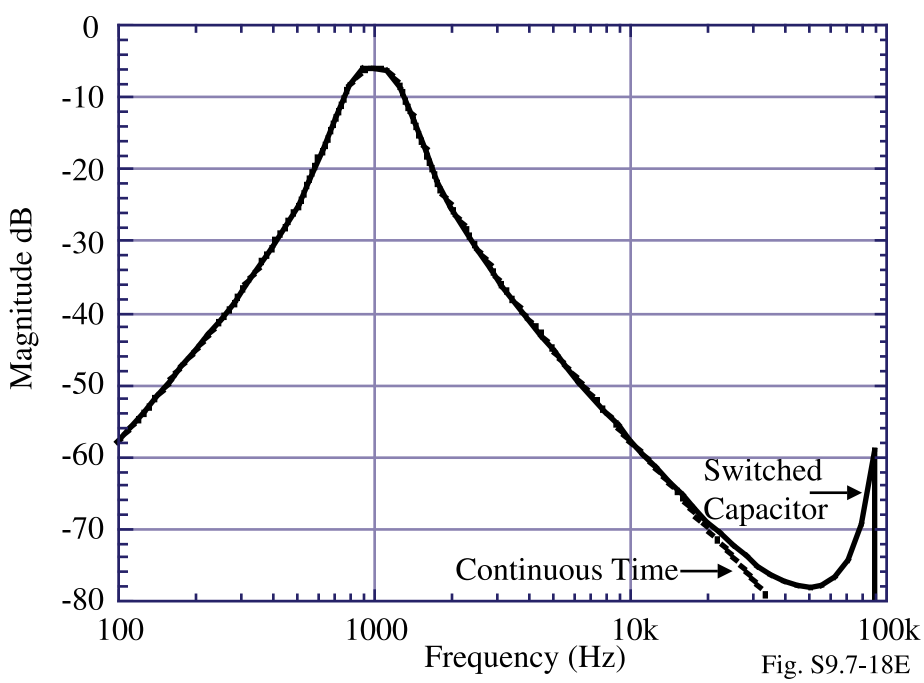


Fig. S9.7-18E

Problem 9.7-19

Use the low-pass, normalized prototype filter of Fig. P9.7-13 to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 500Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

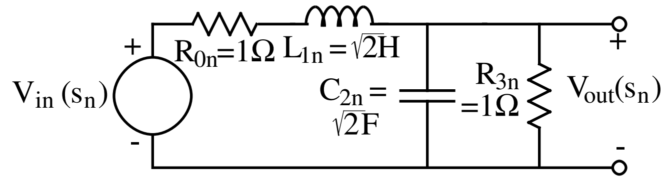


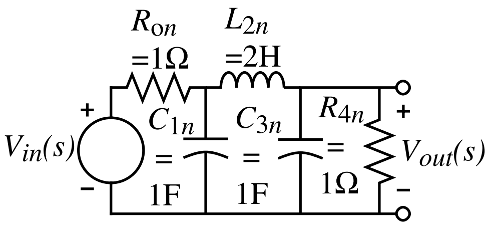
Figure P9.7-13

Solution

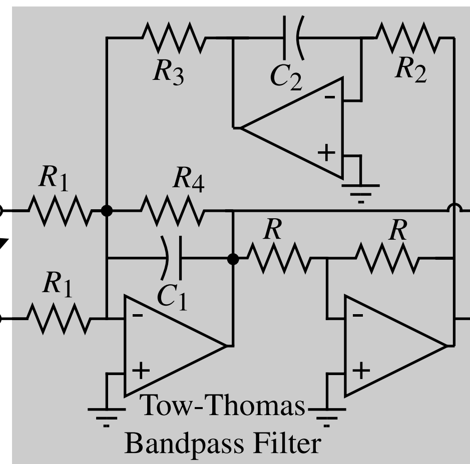
TBD

Problem 9.7-20

Use the low-pass, normalized prototype filter shown to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 100Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

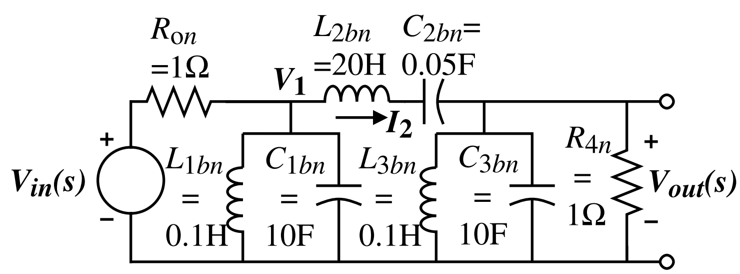


$$-\frac{V_o^-}{V_1} = \frac{V_o^+}{V_1} = \frac{\left(\frac{R_4}{R_1}\right)\frac{s}{R_4C_1}}{s^2 + \frac{s}{R_4C_1} + \frac{1}{R_2R_3C_1C_2}}$$



Solution

The bandpass normalized filter is shown using the values of f_r = 1000 Hz and BW = 100 Hz to scale the elements by 10. The state variables and the input voltage are shown in bold.



The state equations are:

1.)

$$\frac{V_{in} - V_1}{R_{0n}} = I_2 + (sC_{1bn} + \frac{1}{sL_{1bn}})\, V_1 \;\rightarrow\; \frac{V_{in}}{R_{0n}} - \frac{V_2'}{R} = \left(\frac{1}{R_{0n}} + sC_{1bn} + \frac{1}{sL_{1bn}}\right) V_1$$

or

$$V_1 = \frac{\frac{s}{C_{1bn}R}}{s^2 + \frac{s}{R_{0n}C_{1bn}} + \frac{1}{L_{1bn}C_{1bn}}}\left(V_2' - \frac{V_{in}}{R_{0n}}\right) = \frac{0.1s}{s^2+0.1s+1}(V_2' - V_{in})$$

2.)

$$I_2 = \frac{V_2'}{R} = \frac{V_2 - V_{out}}{sL_{2bn} + \frac{1}{sC_{2bn}}} = \frac{\frac{s}{L_{2bn}}}{s^2 + \frac{1}{L_{2bn}C_{2bn}}}(V_1 - V_{out}) \rightarrow V_2' = \frac{0.05s}{s^2 + 1}(V_1 - V_{out})$$

3.)

$$V_{out} = \frac{\frac{V_2'}{R}}{sC_{3bn} + \frac{1}{sL_{3bn}} + \frac{1}{R_{4n}}} = \frac{0.1V_2'}{s^2 + 0.01s + 1}$$

Problem 9.7-20 - Continued

Now we need to design each Tow-Thomas bandpass circuit. If $R_2 = R_3 = 1\Omega$ and $C_1 = C_2 = 1$F of the Tow-Thomas circuit then the transfer function becomes,

$$\frac{V_o^+}{V_1} = \frac{\frac{s}{R_{i1}}}{s^2 + \frac{s}{R_{i4}} + 1} \quad \text{where } i \text{ corresponds to the } i\text{-th stage}$$

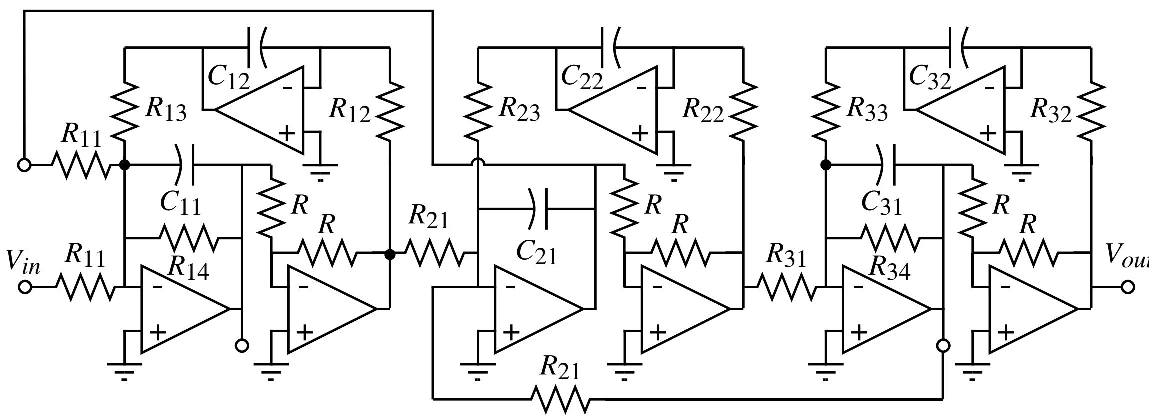
Therefore the design of each stage is:

Stage 1: $R_{11} = 10\Omega$, $R_{14} = 10\Omega$, $R_{12} = R_{13} = 1\Omega$, and $C_{11} = C_{12} = 1$F

Stage 2: $R_{21} = 20\Omega$, $R_{24} = \infty$, $R_{22} = R_{23} = 1\Omega$, and $C_{21} = C_{22} = 1$F

Stage 3: $R_{31} = 10\Omega$, $R_{34} = 10\Omega$, $R_{32} = R_{33} = 1\Omega$, and $C_{31} = C_{32} = 1$F

Next, denormalizing by 2000π and impedance denormalizing by 10^5 gives,



where

$$\boxed{R = R_{11} = R_{14} = 1\text{M}\Omega,\ R_{12} = R_{13} = 100\text{k}\Omega, \text{ and } C_{11} = C_{12} = 1.59\text{nF}}$$

$$\boxed{R = R_{21} = 2\text{M}\Omega,\ R_{24} = \infty,\ R_{22} = R_{23} = 100\text{k}\Omega, \text{ and } C_{21} = C_{22} = 1.59\text{nF}}$$

and

$$\boxed{R = R_{31} = R_{32} = 1\text{M}\Omega, R_{32} = R_3 = 100\text{k}\Omega, \text{ and } C_{31} = C_{32} = 1.59\text{nF}}$$

SPICE File:

```
*** HW9 PROBLEM4 (Problem 9.7-20) ***
*** Node 13 and 14 are Switched Cap outputs
*** Node 23 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1 STAGE ***
XNC41 1 2 3 4 NC41
XPC411 9 10 3 4 PC41
XPC412 5 6 3 4 PC41
XLQBQ1 3 4 5 6 LQBIQUAD
```

Problem 9.7-20 – Continued

```
*** V2' STAGE ***
XNC42 5 6 7 8 NC42
XPC421 13 14 7 8 PC42
XLQBQ2 7 8 9 10 LQBIQUAD
*** VOUT STAGE ***
XNC43 9 10 11 12 NC41
XPC431 13 14 11 12 PC41
XLQBQ3 11 12 13 14 LQBIQUAD
*** RLC LADDER NETWORK ***
R1 1 21 50
C11 21 0 3.1831E-5
L11 21 0 7.9577E-4
L21 21 22 0.1592
C21 22 23 1.5915E-7
C31 23 0 3.1831E-5
L31 23 0 7.9577E-4
R2 23 0 50
*************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC5 1 2 3 4
RNC1 1 0 15.916
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.06283
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.06283
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.06283
RNC2 4 0 15.916
.ENDS NC5
.SUBCKT NC41 1 2 3 4
RNC1 1 0 159.1596
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.006283
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.006283
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.006283
RNC2 4 0 159.1596
.ENDS NC41
.SUBCKT NC42 1 2 3 4
RNC1 1 0 318.2686
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.003142
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.003142
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.003142
RNC2 4 0 318.2686
.ENDS NC42
```

Problem 9.7-20 – Continued

```
.SUBCKT PC2 1 2 3 4
RPC1 2 4 15.916
.ENDS PC2
.SUBCKT PC41 1 2 3 4
RPC1 2 4 159.1596
.ENDS PC41
.SUBCKT PC42 1 2 3 4
RPC1 2 4 318.2686
.ENDS PC42
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
.SUBCKT LQBIQUAD 5 6 7 8
XPC2 7 8 1 2 PC2
XUSCP1 1 2 3 4 USCP
XAMP1 1 2 3 4 AMP
XNC5 3 4 5 6 NC5
XUSCP2 5 6 7 8 USCP
XAMP2 5 6 7 8 AMP
.ENDS LQBIQUAD
*** ANALYSIS ***
.AC DEC 1000 10 99K
.PROBE
.END
```

Problem 9.7-21

Use the low-pass, normalized prototype filter shown to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 100Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

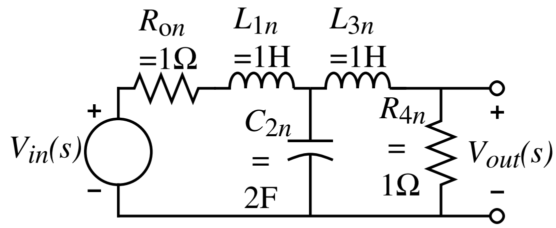


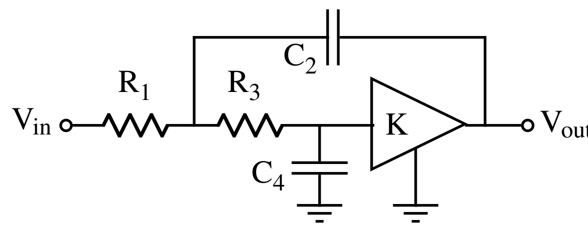
Figure P9.7-21

Solution

TBD

Problem 9.7-22

A second-order, lowpass, Sallen and Key active filter is shown along with the transfer function in terms of the components of the filter.



a.) Define $n = R_3/R_1$ and $m = C_4/C_2$ and let $R_1 = R$ and $C_2 = C$. Develop the design equations for Q and ω_o if K = 1.

b.) Use these equations to design for a second-order, lowpass, Butterworth anti-aliasing filter with a bandpass frequency of 10kHz. Let $R_1 = R = 10\text{k}\Omega$ and find the value of C_2, R_3, and C_4.

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{K}{R_1R_3C_2C_4}}{s^2+s\left[\dfrac{1}{R_3C_4}+\dfrac{1}{R_1C_2}+\dfrac{1}{R_3C_2}-\dfrac{K}{R_3C_4}\right]+\dfrac{1}{R_1R_3C_2C_4}}$$

Solution

a.) The expressions for Q and ω_o are

$$\omega_o = \frac{1}{\sqrt{R_1R_3C_2C_4}} \quad \text{and} \quad \frac{\omega_o}{Q} = \frac{1}{R_3C_4}+\frac{1}{R_1C_2}+\frac{1}{R_3C_2}-\frac{K}{R_3C_4}$$

If K = 1, then $\omega_o = \dfrac{1}{\sqrt{R_1R_3C_2C_4}}$ and $\dfrac{1}{Q} = \sqrt{\dfrac{R_3C_4}{R_1C_2}} + \sqrt{\dfrac{R_1C_4}{R_3C_2}}$.

Define $n = \dfrac{R_3}{R_1}$ and $m = \dfrac{C_4}{C_2}$ and let $R_1 = R$ and $C_2 = C$. Therefore,

$$\omega_o^2 = \frac{1}{mn(R_1C_2)^2} \Rightarrow \boxed{\omega_o = \frac{1}{\sqrt{mn}R_1C_2} = \frac{1}{\sqrt{mn}RC}}$$

and $$\boxed{\frac{1}{Q} = \sqrt{mn} + \sqrt{\frac{m}{n}} = \sqrt{mn}\left(1+\frac{1}{n}\right)}$$

b.) A normalized Butterworth second-order lowpass function is

$$\frac{V_{out}}{V_{in}} = \frac{1}{s^2+\sqrt{2}s+1} \Rightarrow \omega_o = 1 \text{ rad/sec and } Q = 0.707$$

Let $R_1 = R = 1\Omega$ and $C_2 = C = 1\text{F}$. $\therefore$ $\sqrt{mn} = 1$ and $\sqrt{2} = 1\cdot\left(1+\dfrac{1}{n}\right) = 1+\dfrac{1}{n}$

From the above, $n = \dfrac{1}{\sqrt{2}-1} = 2.4142$ and $m = \dfrac{1}{2.4142} = 0.4142$

$\therefore$ $R_3 = 2.4142\Omega$ and $C_4 = 0.4142\text{F}$

Denormalizing by $10^4\Omega$ and 20,000π (rads/sec) gives

$$\boxed{R_1 = 10\text{k}\Omega,\ R_3 = 24.142\text{k}\Omega,\ C_1 = 1.59\text{nF and } C_4 = 0.659\text{nF}}$$

Problem 9.7-23

The circuit shown is to be analyzed to determine its capability to realize a second-order transfer function with complex conjugate poles. Find the transfer function of the circuit and determine and verify the answers to the following questions:

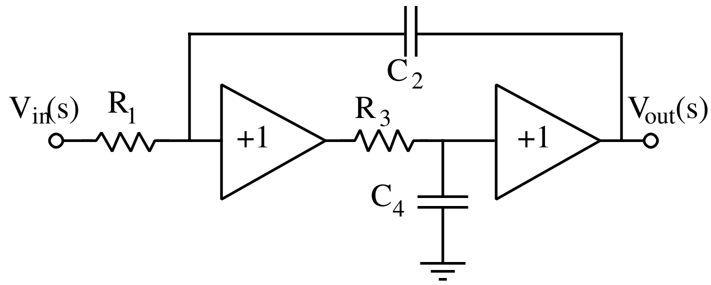


Figure P9.7-23

1.) Is the circuit low-pass, bandpass, high-pass, or other?

2.) Find H_o, ω_o, and Q in terms of R_1, C_2, R_3, and C_4.

3.) What elements would you adjust to independently tune Q and ω_o?

Solution

a.) $$V_{out} = \left(\frac{(1/sC_4)}{R_3+(1/sC_4)}\right)V_1 = \frac{V_1}{sR_3C_4+1}$$

$$V_1 = \left(\frac{R_1}{R_1+(1/sC_2)}\right)V_{out} + \left(\frac{(1/sC_2)}{R_1+(1/sC_2)}\right)V_{in} = \frac{sR_1C_2V_{out}}{sC_2R_1+1} + \frac{V_{in}}{sC_2R_1+1}$$

$\therefore$ $$V_{out} = \left(\frac{1}{sR_3C_4+1}\right)\left(\frac{sR_1C_2V_{out}}{sC_2R_1+1} + \frac{V_{in}}{sC_2R_1+1}\right)$$

$$V_{out}(sR_3C_4+1)(sR_1C_2+ 1) = sR_1C_2V_{out} + V_{in}$$

$$V_{out}[s^2R_1R_3C_2C_4 + sR_1C_2+ sR_3C_4 - sR_1C_2 + 1] = V_{in}$$

$\therefore$ $$\frac{V_{out}}{V_{in}} = \frac{1}{s^2R_1R_3C_2C_4+sR_3C_4+1} = \frac{\frac{1}{R_1R_3C_2C_4}}{s^2+\frac{s}{R_1C_2} + \frac{1}{R_1R_3C_2C_4}} = \frac{H_o\omega_o^2}{s^2+\left(\frac{\omega_o}{Q}\right)s + \omega_o}$$

$\therefore$ Filter is low-pass.

b.) From the previous results, $H_o = 1$, $\omega_o = \dfrac{1}{\sqrt{R_1R_3C_2C_4}}$, and $Q = \omega_o R_1C_2 = \sqrt{\dfrac{R_1C_2}{R_3C_4}}$

c.) To tune ω_o but not Q, adjust the product of R_1R_3 (C_2C_4) keeping the ratio R_1/R_3 (C_2/C_4) constant.

To tune Q but not ω_o, adjust the ratio R_1/R_3 (C_2/C_4) keeping the product of R_1R_3 (C_2C_4) constant.

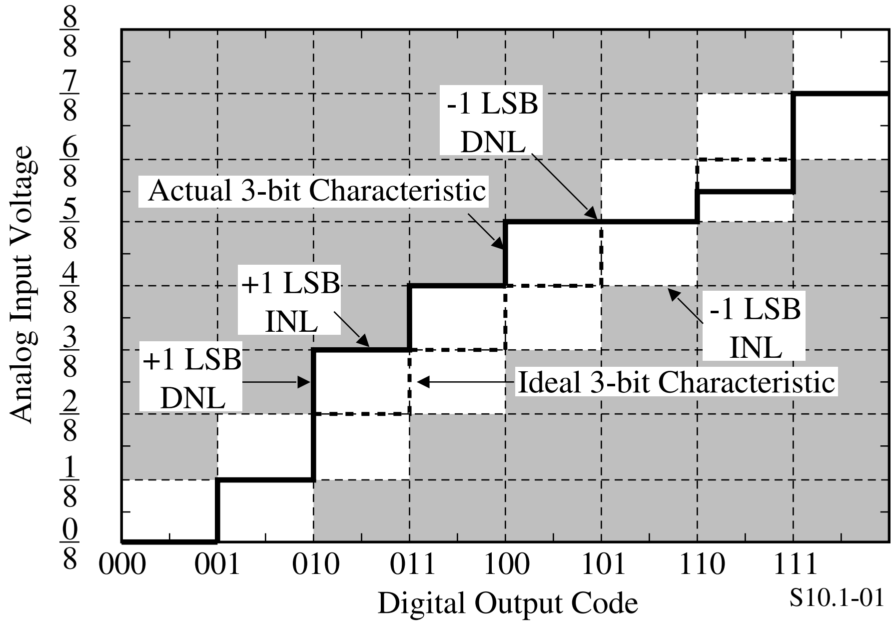
CHAPTER 10 – HOMEWORK SOLUTIONS

Problem 10.1-01

Plot the analog output versus the digital word input for a three-bit D/A converter that has ±1 LSB *DNL* and ±1 LSB *INL*. Assume an arbitrary analog full-scale value.

Solution

Below is a characteristic of a 3-bit DAC. The shaded area is not permitted in order to maintain ±1 LSB *INL*.

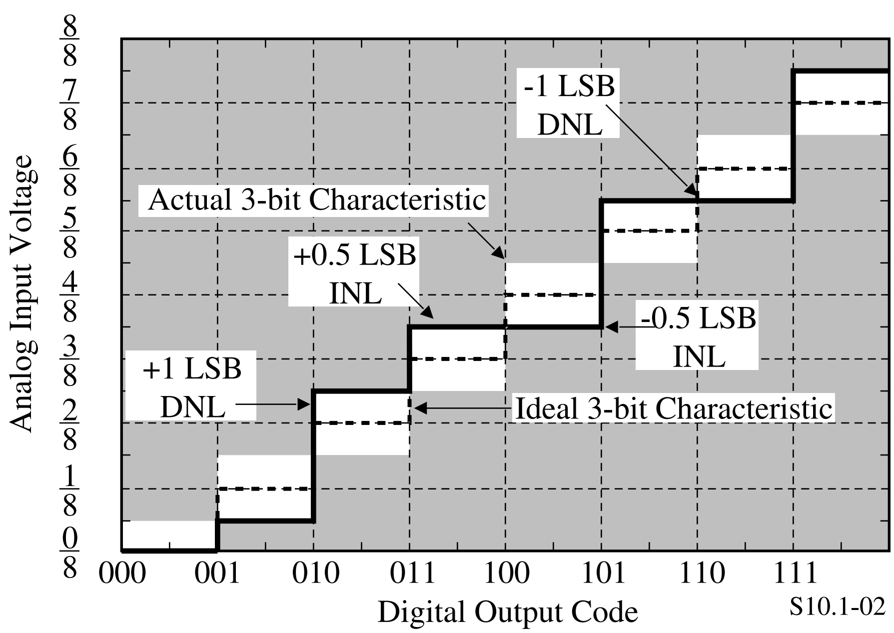


Problem 10.1-02

Repeat the above problem for ±1.5 LSB *DNL* and ±0.5 LSB integral linearity.

Solution

The shaded area is not permitted in order to maintain ±0.5 LSB *INL*. Note that the *DNL* cannot exceed ±1 LSB.

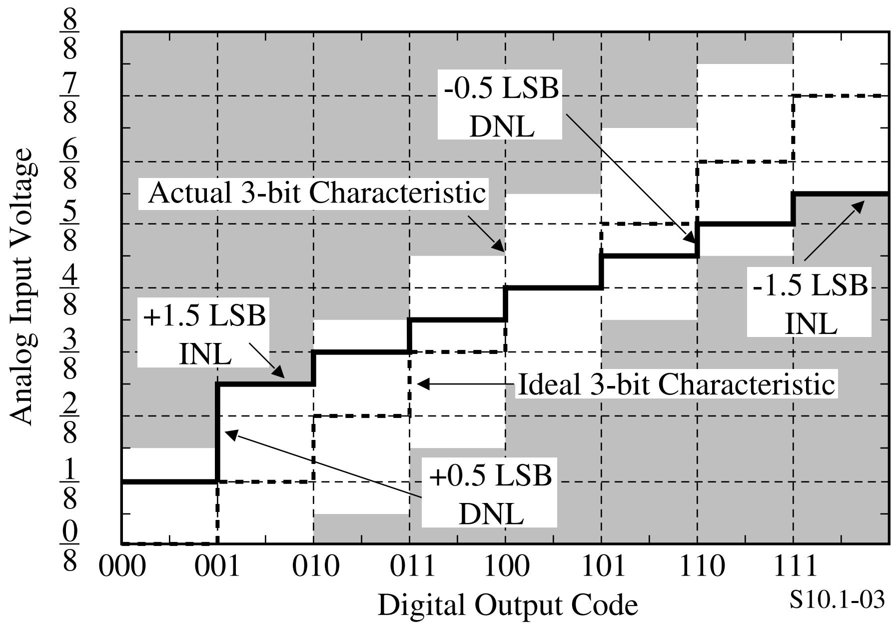


Problem 10.1-03

Repeat Prob. 1, for ±0.5 LSB differential linearity and ±1.5 LSB integral linearity.

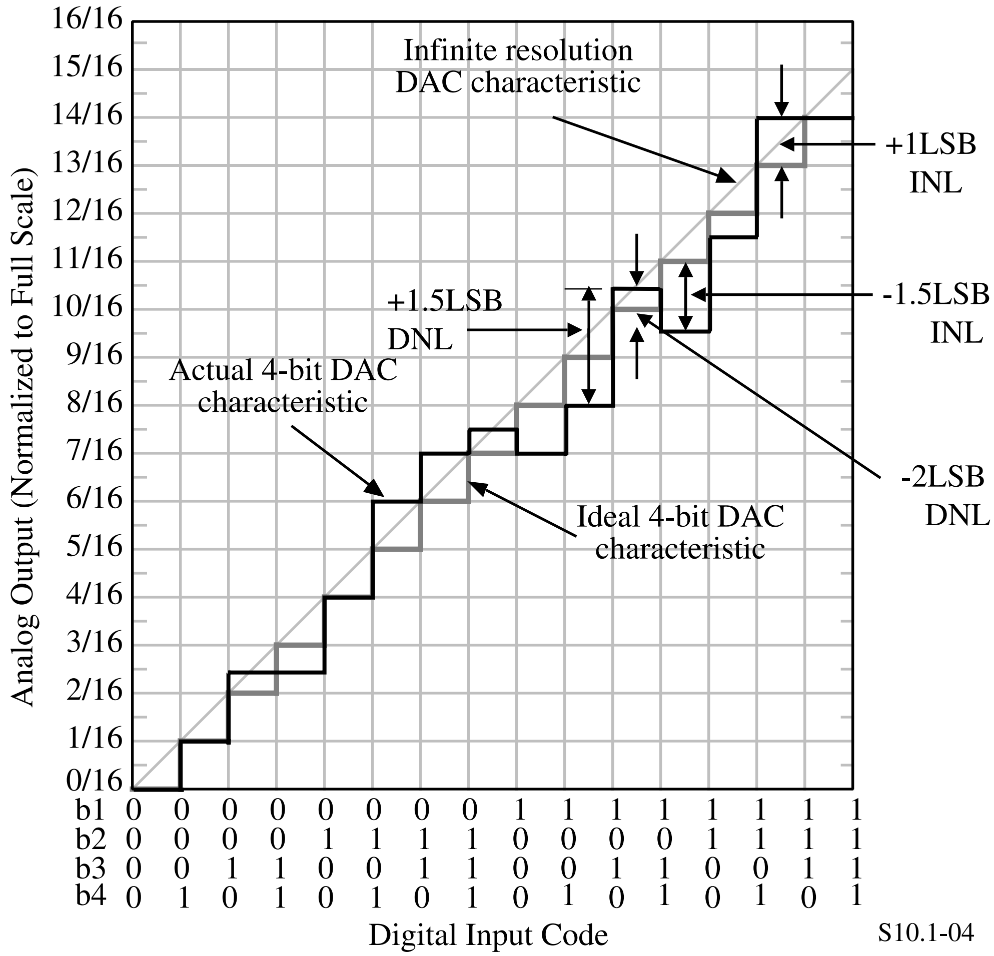
Solution

The shaded area is not permitted in order to maintain ±1.5 LSB *INL*.



Problem 10.1-04

The transfer characteristics of an ideal and actual 4-bit digital-analog converter are shown in Fig. P10.1-4. Find the ±INL and ±DNL in terms of LSBs. Is the converter monotonic or not?



Solution

INL: +1LSB, -2.5LSB, DNL: +1.5LSB, -2LSB, the converter is not monotonic.

Problem 10.1-05

A 1V peak-to-peak sinusoidal signal is applied to an ideal 10 bit DAC which has a V_{REF} of 5V. Find the SNR of the digitized analog output signal.).

Solution

A 1V peak sinusoideal signal is applied to an ideal 10 bit DAC which has a V_{REF} of 5V. Find the SNR of the digitized analog output signal.

Solution

The SNR_{max} = 6.02dB/bit x 10bits + 1.76dB = 61.96dB

The maximum output signal is 2.5V peak. Therefore, the 1V peak signal is 7.96dB smaller to give a *SNR* of the digitized analog output as 61.96-7.96 = 54dB

$\therefore \boxed{SNR = 54\text{dB}}$

Problem 10.1-06

How much noise voltage in rms volts can a 1V reference voltage have and not cause errors in a 14-bit D/A converter? What must be the fractional temperature coefficient (ppm/°C) for the reference voltage of this D/A converter over the temperature range of 0°C to 100°C?

Solution

The rms equivalent of a 1V reference voltage is $\frac{1}{2\sqrt{2}}$V. Multiplying by $\frac{1}{2^{14}}$ gives

$$\text{Rms noise} = \frac{1}{2\sqrt{2}\cdot 2^{14}} = 21.6\mu\text{V(rms)} \quad\rightarrow\quad \boxed{\text{Rms noise} = 21.6\mu\text{V}}$$

To be within ±0.5*LSB*, the voltage change must be less than or equal to 2^{-15}.

$$\therefore\ \text{ppm/C°} = \frac{\frac{\Delta V}{V}}{\Delta T} = \frac{\frac{2^{-15}}{1}}{100\text{C°}} = \frac{1}{2\cdot 16{,}384\cdot 100} = 0.3052\text{pppm/C°} \quad\rightarrow\quad \boxed{0.3052\text{ppm/C°}}$$

Problem 10.1-07

If the quantization level of an analog-to-digital converter is Δ, prove that the rms quantization noise is given as $\Delta/\sqrt{12}$.

Solution

Assume the quantizer signal appears as follows.

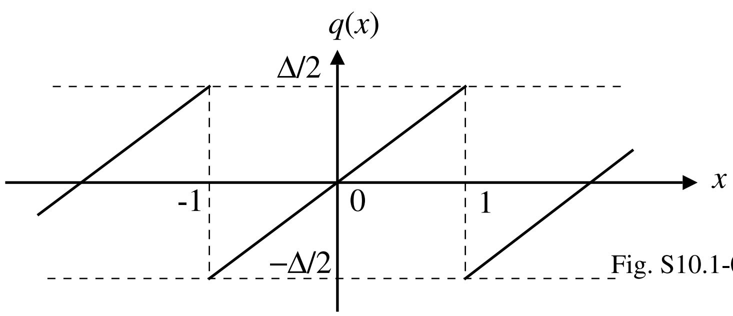


Fig. S10.1-07

The rms value of $q(x)$ is $\sqrt{\frac{1}{T}\int_0^T q^2(x)dx}$ where $q(x) = 0.5\Delta x$ and $T = 2$.

$$\therefore\ \text{rms value of } q(x) = \sqrt{\frac{1}{2}\int_{-1}^{1}\frac{\Delta^2}{4}x^2dx} = \sqrt{\frac{\Delta^2}{8}\left.\frac{x^3}{3}\right|_{-1}^{1}} = \sqrt{\frac{\Delta^2}{8}\left(\frac{1}{3}+\frac{1}{3}\right)} = \frac{\Delta}{\sqrt{12}}$$

rms value of $q(x) = \underline{\underline{\Delta/\sqrt{12}}}$

<u>Problem 10.2-01</u>

Find I_o in terms of I_1, I_2, I_3, and I_4 for the circuit shown.

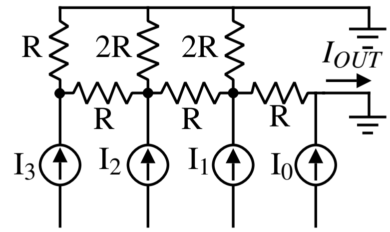


Figure P10.2-1

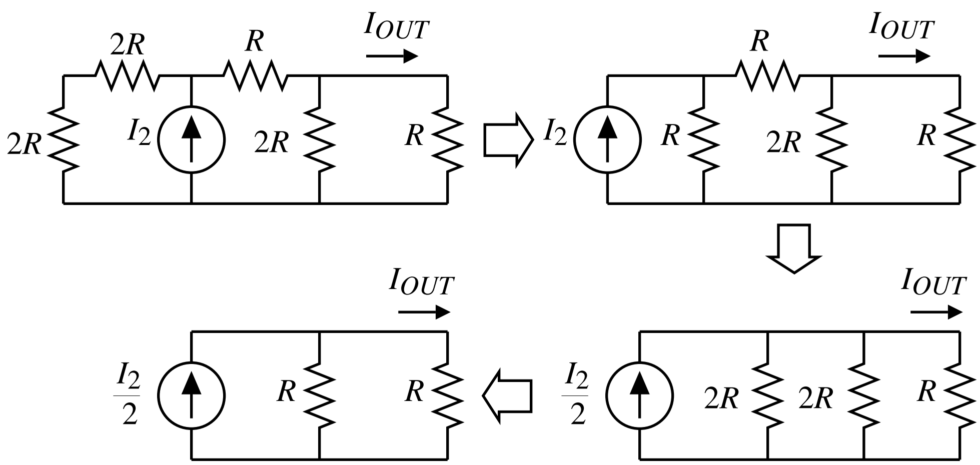
<u>Solution</u>

$$\boxed{I_{OUT} = I_0}$$

I_1 sees R to the right and R to the left so that $\boxed{I_{OUT} = \frac{I_1}{2}}$

.

I_2 requires the use of Norton's theorem to see the results.



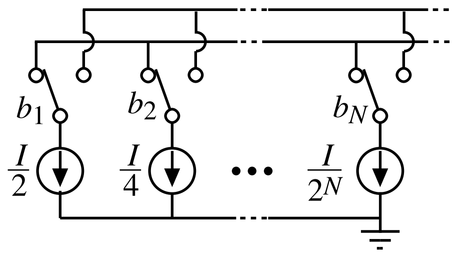
S10.2-01A

$\therefore$ $\boxed{I_{OUT} = \frac{I_2}{4}}$

Repeating the above process for I_8 will give $I_{OUT} = \boxed{I_{OUT} = \frac{I_3}{8}}$

Problem 10.2-02

A digital-analog converter uses the binary weighted current sinks shown. b_1 is the MSB and b_N is the LSB.



a.) For each individual current sink, find the tolerance in ±percent necessary to keep INL less than ±0.5LSB if N = 4 assuming all other bits are ideal.

b.) Considering the influence of all current sinks, what is the worst case tolerances in ±percent for each sink?

Solution

a.) An LSB = $\frac{I}{2^N}$, therefore each sink must have the accuracy of ±0.5 LSB = $\frac{\pm I}{2^{N+1}} = \frac{I}{32}$.

I/2: $\frac{I}{2} \pm \frac{I}{2^{N+1}} = \frac{I}{2} \pm \frac{I}{32} = \frac{I}{2}\left(1 \pm \frac{1}{16}\right) \Rightarrow$

$$\boxed{\text{Tolerance of } \frac{I}{2} = \frac{\pm\frac{1}{16}}{1}\,\text{x}100\% = \frac{\pm 100}{16}\% = \pm 6.25\%}$$

I/4: $\frac{I}{4} \pm \frac{I}{32} = \frac{I}{4}\left(1 \pm \frac{1}{8}\right) \Rightarrow$ $\boxed{\text{Tolerance of } \frac{I}{4} = \frac{\pm\frac{1}{8}}{1}\,\text{x}100\% = \frac{\pm 100}{8}\% = \pm 12.5\%}$

$$\boxed{\text{Similarly, the tolerance of } I/8 \text{ and } I/16 \text{ are } \pm 25\% \text{ and } \pm 50\%\text{, respectively.}}$$

$$\boxed{\text{The tolerance of the ith current sink} = \frac{2^{i-N}}{2}\,\text{x}100\%}$$

b.) In this case, assume that all errors add for a worst case approach. Let this error be x. Therefore we can write,

$$\left(\frac{I}{2} + x\right) + \left(\frac{I}{4} + x\right) + \left(\frac{I}{8} + x\right) + \left(\frac{I}{16} + x\right) \le \left(\frac{I}{2} + \frac{I}{4} + \frac{I}{8} + \frac{I}{16}\right) + \frac{I}{32}$$

or

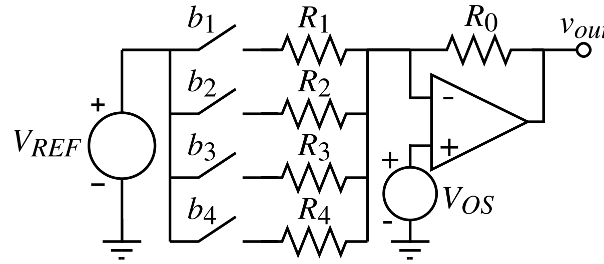
$$\left(\frac{I}{2} + \frac{I}{4} + \frac{I}{8} + \frac{I}{16}\right) + 4x \le \left(\frac{I}{2} + \frac{I}{4} + \frac{I}{8} + \frac{I}{16}\right) + \frac{I}{32} \Rightarrow x = \frac{I}{4\cdot 32} = \frac{I}{128}$$

Thus the tolerances of part a.) are all decreased by a factor of 4 to give ±1.5625%, ±3.125%, ±6.25%, and ±12.5% for I/2, I/4, I/8, and I/16, respectively.

$$\boxed{\frac{I}{2} \Rightarrow \pm 1.5625\%,\ \frac{I}{4} \Rightarrow \pm 3.125\%,\ \frac{I}{8} \Rightarrow \pm 6.25\% \text{ and } \frac{I}{16} \Rightarrow \pm 12.5\%}$$

$$\boxed{\text{The tolerance of the ith current sink} = \frac{2^{i-N}}{2N}\,\text{x}100\%}$$

Problem 10.2-03



A 4-bit, binary weighted, voltage scaling digital-to-analog converter is shown. (a.) If $R_0 = 7R/8$, $R_1 = 2R$, $R_2 = 4R$, $R_3 = 8R$, $R_4 = 16R$, and $V_{OS} = 0$V, sketch the digital-analog transfer curve on the plot on the next page. (b.) If $R_0 = R$, $R_1 = 2R$, $R_2 = 4R$, $R_3 = 8R$, $R_4 = 16R$, and $V_{OS} = (1/15)V_{REF}$, sketch the digital-analog transfer curve on the plot shown. (c.) If $R_0 = R$, $R_1 = 2R$, $R_2 = 16R/3$, $R_3 = 32R/5$, $R_4 = 16R$, and $V_{OS} = 0$V, sketch the digital-analog transfer curve on the previous transfer curve. For this case, what is the value of DNL and INL? Is this D/A converter monotonic or not?

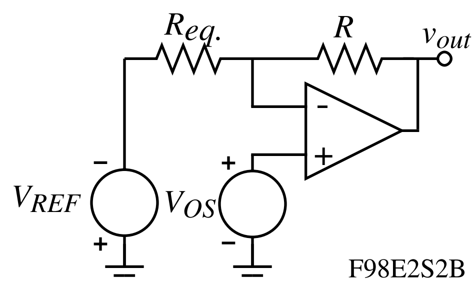
Solutions

(a.) $$v_{out} = R_0\left(\frac{b_1}{R_1} + \frac{b_2}{R_2} + \frac{b_3}{R_3} + \frac{b_4}{R_4}\right)V_{REF} = \frac{7}{8}\left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)V_{REF}$$

$$v_{out} = \left(\frac{7}{16} + \frac{7}{24} + \frac{7}{64} + \frac{7}{128}\right)V_{REF} = \frac{7}{8}\text{ x ideal characteristic}$$

(b.) The equivalent circuit is given as shown.

$$R_{eq} = \frac{R}{\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}}$$



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$$v_{out} = \frac{R_0}{R_{eq.}}(V_{REF}+V_{OS}) + V_{OS}$$

$$v_{out} = \left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)(V_{REF}-V_{OS}) + V_{OS}$$

$$v_{out} = \left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)\left(\frac{16V_{REF}}{15}\right) + \frac{V_{REF}}{15}$$

$\therefore$ $\boxed{\text{Gain error of 1/16 and offset of } V_{REF}/15.}$

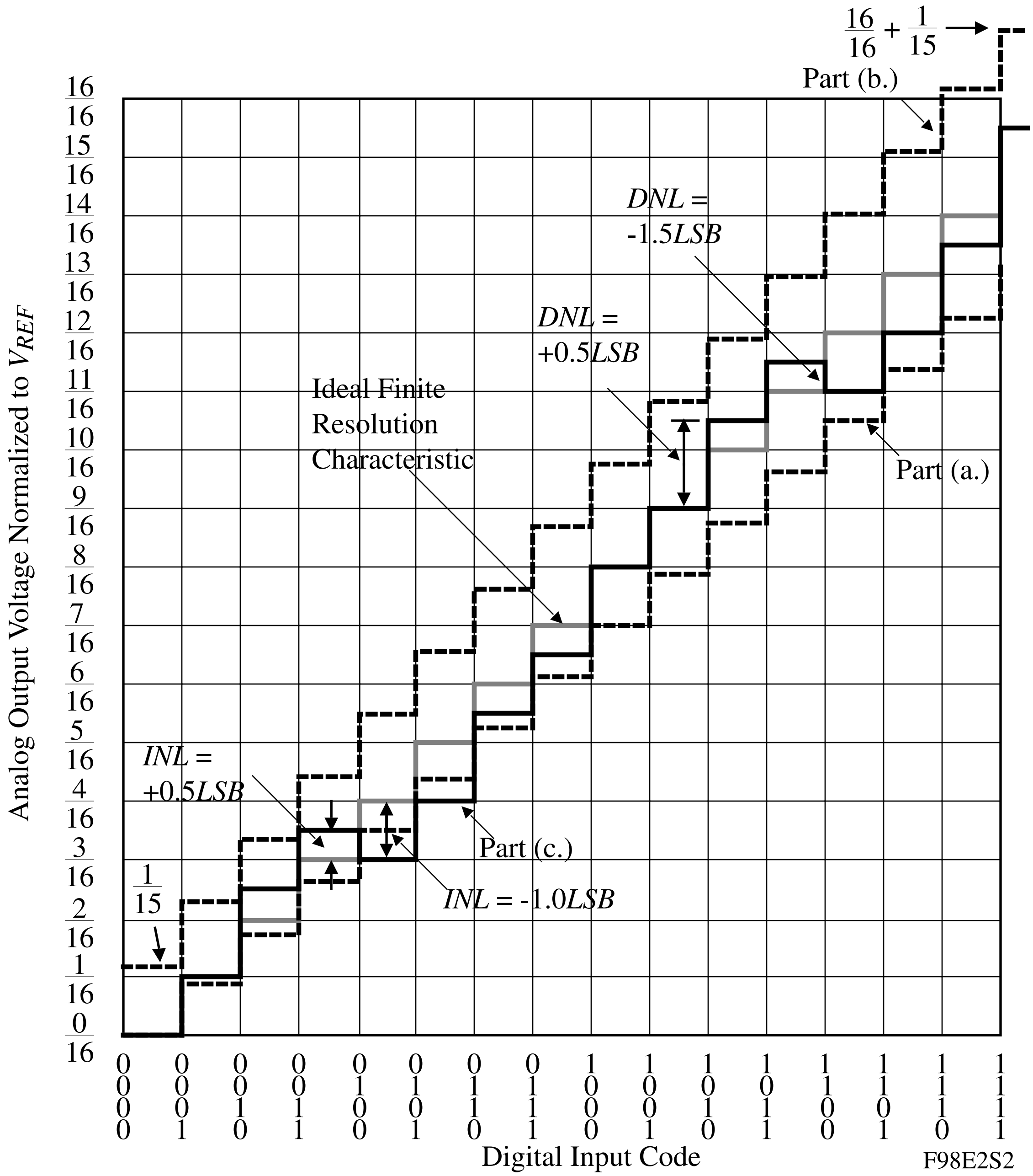
(c.) $$v_{out} = R_0\left(\frac{b_1}{R_1} + \frac{b_2}{R_2} + \frac{b_3}{R_3} + \frac{b_4}{R_4}\right)V_{REF} = \left(\frac{b_1}{2} + \frac{3b_2}{16} + \frac{5b_3}{32} + \frac{b_4}{16}\right)V_{REF}$$

$$= \left(\frac{16b_1}{32} + \frac{12b_2}{32} + \frac{5b_3}{32} + \frac{2b_4}{32}\right)V_{REF} \rightarrow \text{Used to generate the plot on the next page}$$

$\therefore$ $\boxed{INL = +0.5LSB \text{ and } -1.0LSB \qquad DNL = +0.5LSB \text{ and } -1.5LSB}$

$\boxed{\text{This DAC is not monotonic.}}$

Problem 10.2-3 - Continued



Problem 10.2-04

A 4-bit digital-to-analog converter characteristic using the DAC of Fig. P10.2-3 is shown in Fig. P10.2-4. (a.) Find the *DNL* and the *INL* of this converter. (b.) What are the values of R_1 through R_4, that correspond to this input-output characteristic? Find these values in terms of R_0.

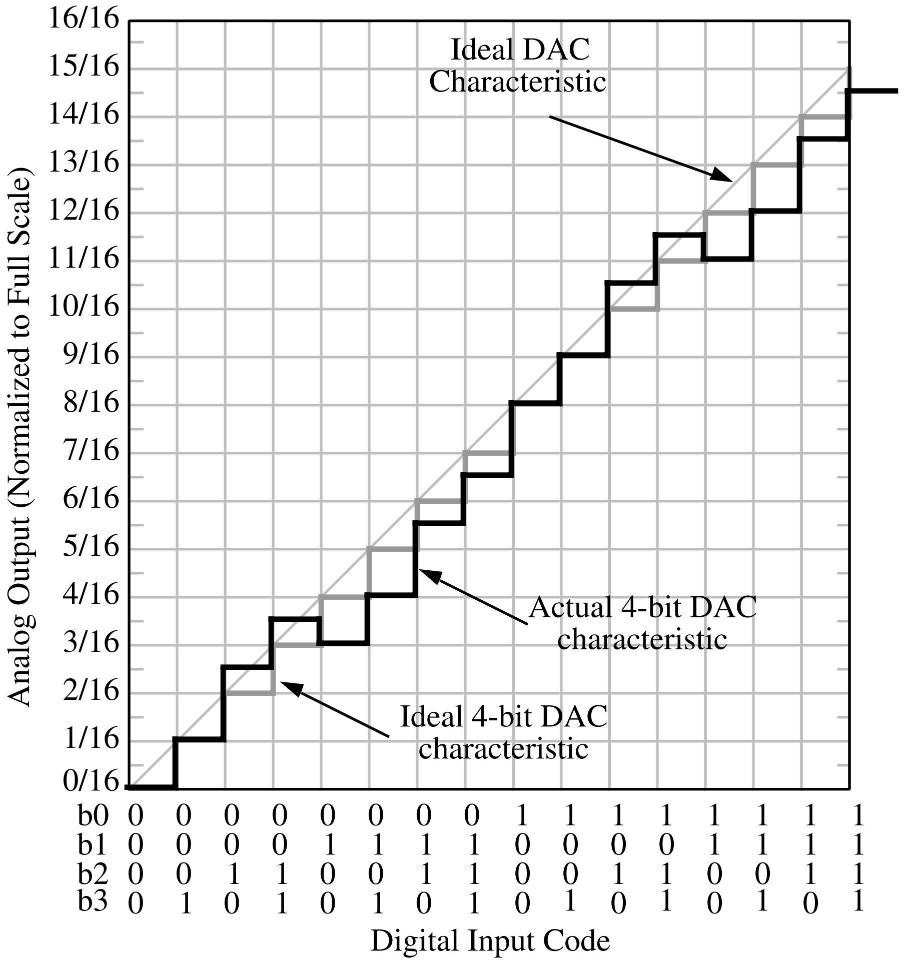


Figure P10.2-4

Solution

(a.) INL = +0.5LSB and –2.0 LSB, DNL = +0.5LSB and –1.5LSB.

(b.) Note that v_{OUT} can be written as,

$$v_{OUT} = -R_0\left[\frac{b_0}{R_1} + \frac{b_1}{R_2} + \frac{b_2}{R_3} + \frac{b_3}{R_4}\right] V_{REF}$$

For 0001, $|v_{OUT}| = \dfrac{V_{REF}}{16} \rightarrow R_4 = 16\,R_0$. For 0010, $|v_{OUT}| = \dfrac{5V_{REF}}{32} \rightarrow R_3 = \dfrac{32}{5}R_0$.

For 0100, $|v_{OUT}| = \dfrac{3V_{REF}}{16} \rightarrow R_2 = \dfrac{16}{3}\,R_0$. For 1000, $|v_{OUT}| = \dfrac{V_{REF}}{2} \rightarrow R_1 = 2\,R_0$

Problem 10.2-05

For the DAC of Fig. P10.2-3, design the values of R_1 through R_4 in terms of R_0 to achieve an ideal 4-bit DAC. What value of input offset voltage, V_{OS}, normalized to V_{REF} will cause an error? If the op amp has a differential voltage gain of

$$A_{vd}(s) = \frac{10^6}{s + 100}$$

at what frequency or rate of conversion will an error in conversion occur due to the frequency response of the op amp? Assume that the rate of application of digital words to be converted is equivalent to the application of a sinusoidal signal of equivalent frequency.

Solution

The values of the resistors are $R_1 = 2R_0$, $R_2 = 4R_0$, $R_3 = 8R_0$, and $R_4 = 16R_0$.
A model for the input offset voltage influence on the DAC is shown. The output voltage is,

$$v_{OUT} = -\frac{R}{R_{EQ.}}V_{REF} + \left(\frac{R + R_{EQ.}}{R_{EQ.}}\right)V_{OS}$$

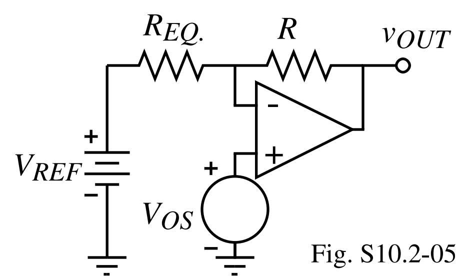


Fig. S10.2-05

We see that the largest influence of V_{OS} is when $R_{EQ.}$ is minimum which is $R_1||R_2||R_3||R_4 = (16/15)R$.

$$\therefore \quad \left(1 + \frac{15}{16}\right)V_{OS} \le 0.5\text{LSB} = \frac{1}{32}V_{REF}$$

$$\frac{V_{OS}}{V_{REF}} \le \left(\frac{1}{32}\right)\left(\frac{16}{31}\right) = \frac{1}{62} = \underline{\underline{0.01613}}$$

For the maximum conversion rate, the worst case occurs when the loop gain is smallest. The loop gain is given as

$$LG = -\left(\frac{R_{EQ.}}{R + R_{EQ.}}\right)A_{vd}$$

Which is minimum when $R_{EQ.} = (16/15)R$. The ideal output normalized to V_{REF} is,

$$\frac{v_{OUT}(\text{ideal})}{V_{REF}} = -\left(\frac{R}{R_{EQ.}}\right) = -\frac{15}{16}$$

The actual output normalized to V_{REF} is,

$$\frac{v_{OUT}(\text{actual})}{V_{REF}} = \frac{-\dfrac{A_{vd}R}{R + R_{EQ.}}}{1 + \dfrac{A_{vd}R_{EQ.}}{R + R_{EQ.}}} = \frac{-\dfrac{15}{31}}{\dfrac{1}{A_{vd}} + \dfrac{16}{31}} = \frac{-\dfrac{15}{31}}{\dfrac{s}{10^6} + \dfrac{16}{31}}$$

where we have assumed that $\omega >> 100$ rads/sec which gives $A_{vd}(s) \approx 10^6/s$.

An error occurs when $\left|\dfrac{v_{OUT}(\text{actual})}{V_{REF}}\right| \ge \dfrac{15}{16} - \dfrac{1}{32} = \dfrac{29}{32}$ (Actual is always less than ideal)

$$\frac{\dfrac{15}{31}}{\sqrt{\left(\dfrac{\omega_{\max}}{10^6}\right)^2 + \left(\dfrac{16}{31}\right)^2}} \ge \frac{29}{32} \quad \rightarrow \quad \left(\frac{16}{31}\right)^2 + \left(\frac{\omega_{\max}}{10^6}\right)^2 \le \left(\frac{15}{31}\right)^2\left(\frac{32}{29}\right)^2$$

$$\frac{\omega_{\max}}{10^6} \le \sqrt{\left(\frac{15}{31} \text{ x } \frac{32}{29}\right)^2 - \left(\frac{16}{31}\right)^2} = 0.1367$$

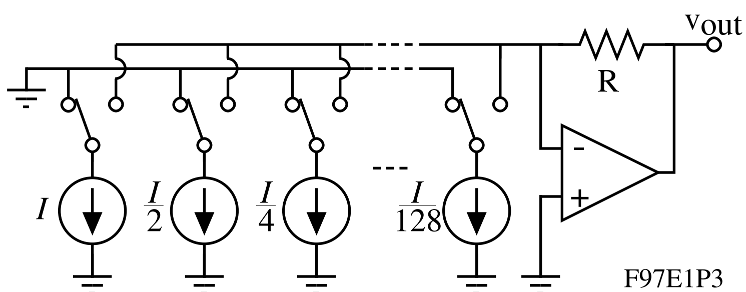
Problem 10.2-05- Continued

$\therefore \quad \omega_{max} \leq 0.1367\text{x}10^6$ rads/sec. $\quad \rightarrow \quad f_{max} \leq \underline{\underline{21.76 \text{ kHz}}}$

Note that 21.76 kHz is much greater than 15.9 Hz (100 rads/sec.) so that the approximation used for $A_{vd}(s)$ is valid.

Problem 10.2-06

An 8-bit current DAC is shown. Assume that the full scale range is 1V. (a.) Find the value of I if R = 1kΩ. (b.) Assume that all aspects of the DAC are ideal except for the op amp. If the differential voltage gain of the op amp has a single pole frequency response with a dc gain of 10^5. Find the unity gainbandwidth, GB, in Hz that gives a worst case conversion time of 2μs. (c.) Again assume that all aspects of the DAC are ideal except for the op amp. The op amp is ideal except for a finite slew rate. Find the minimum slew rate, SR, in V/μs that gives a worst case conversion time of 2μs.



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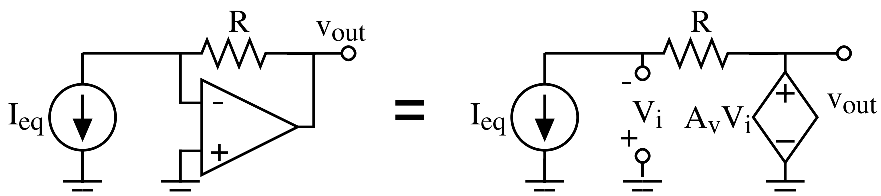
Solution

(a.) FSR = 2I·R = 1V $\Rightarrow$ I = 1V/2kΩ = 500μA $\quad \therefore \quad \boxed{I = 500\mu A}$

(b.) Model for part b.

I_{eq} = all bits switched to the op amp input.

The worst case occurs when all bits are switched to the op amp.



$$\therefore \; V_{out} = A_v V_i = A_v[RI_{eq} - V_{out}] \;\Rightarrow\; V_{out}(1+A_v) = A_v RI_{eq} \;\Rightarrow\; V_{out} = \frac{RI_{eq}}{\frac{1}{A_v} + 1}$$

or $\quad V_{out}(s) = \dfrac{RI_{eq}}{\frac{s}{GB} + 1}$ $\quad$ Assuming a step input gives $V_{out}(s) = \left(\dfrac{RI_{eq}}{\frac{s}{GB} + 1}\right)\dfrac{1}{s}$

$$\therefore \quad \mathcal{L}^{-1}[V_{out}(s)] = v_{out}(t) = RI_{eq}[1 - e^{-GB\cdot t}]\,\mu(t)$$

$$\text{Error}(t) = RI_{eq} - v_{out}(t) \;\Rightarrow\; \text{Error}(T) = e^{-GB\cdot T} = 1/2^{8+1} = 1/512 \;\Rightarrow\; e^{GB\cdot T} = 512$$

If T= 2μs, then GB is given as GB = $0.5\text{x}10^6 \ln(512) = 3.119\text{x}10^6$ $\therefore$ $\boxed{GB = 0.496MHz}$

(c.) Slew Rate:

Want ΔV/ΔT = 1V/2μs = 0.5V/μs assuming a ΔV ≈ 1V. $\therefore$ $\boxed{SR = 0.5V/\mu s}$

Problem 10.2-07

What is the necessary relative accuracy of resistor ratios in order for a voltage-scaling DAC to have a 8-bit resolution?

Solution

Since the voltage scaling DAC has very small DNL errors, let the 8-bit accuracy requirement be determined by the INL error.

$$INL = 2^{N-1}\frac{\Delta R}{R} \leq 0.5 \qquad \rightarrow \qquad \frac{\Delta R}{R} \leq \frac{1}{2}\,\frac{2}{2^N} = \frac{1}{2^N} = \frac{1}{256}$$

$$\therefore \qquad \boxed{\frac{\Delta R}{R} \leq 0.39\%}$$

Problem 10.2-08

If the binary controlled switch b_1 of Fig. P10.2-3 is closed at $t = 0$, find the time it takes the output to achieve its final stage ($-V_{REF}/2$) by assuming that this time is 4 times the time constant of this circuit. The differential voltage gain of the op amp is given as

$$A_{vd}(s) = \frac{10^6}{s + 10}\,.$$

Solution

The model show will be used for this solution.

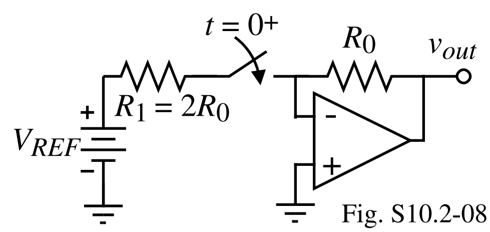


Fig. S10.2-08

The transfer function for this problem can be written as,

$$\frac{V_{out}(s)}{V_{in}(s)} = -\left(\frac{R_0}{R_1}\right)\frac{\frac{R_1A_{vd}(s)}{R_1+R_0}}{1+\frac{R_1A_{vd}(s)}{R_1+R_0}} = -0.5$$

$$\frac{1}{\frac{1.5}{A_{vd}(s)}+1} \approx -0.5\,\frac{1}{\frac{1.5s}{GB}+1} = -\,0.5\left(\frac{0.667\text{x}10^6}{s+0.667\text{x}10^6}\right)$$

For a step input of magnitude V_{REF}, we can write,

$$V_{out}(s) = -0.5\left(\frac{0.667\text{x}10^6}{s+0.667\text{x}10^6}\right)\frac{V_{REF}}{s} = -0.5\left[\frac{1}{s} - \frac{1}{s+0.667\text{x}10^6}\right]V_{REF}$$

The inverse Laplace transform gives,

$$v_{out}(t) = -0.5[1-e^{-0.667\text{x}10^6 t}]V_{REF}$$

The time constant of this circuit is $1/(0.667\text{x}10^6) = 1.5\mu\text{s}$ which means that it will take 6µs for the DAC to convert the switch change to the output voltage.

$\therefore$ <u>Time for conversion = 6µs</u>.

Problem 10.2-09

What is the necessary relative accuracy of capacitor ratios in order for a charge-scaling DAC to have 11-bit resolution?

Solution

Perfect *DNL* will be impossible to achieve so let us use *INL* to answer the question and see what the *DNL* is based on the *INL*.

$$INL = 2^{N\text{-}1}\frac{\Delta C}{C} \le 0.5 \qquad \rightarrow \qquad \frac{\Delta C}{C} \le \frac{1}{2}\,\frac{2}{2^N} = \frac{1}{2^N} = \frac{1}{2048}$$

$$\therefore \qquad \boxed{\frac{\Delta C}{C} \le 0.0488\%}$$

The corresponding $DNL = (2^N\text{-}1)\dfrac{\Delta C}{C} \approx \pm 1\text{LSB}$

Problem 10.2-10

For the charge scaling DAC of Fig. 10.2-10, investigate the influence of a load capacitor, C_L, connected in parallel with the terminating capacitor. (a.) Find an expression for v_{OUT} as a function of C, C_L, the digital bits, b_i, and V_{REF}. (b.) What kind of static error does C_L introduce? (c.) What is the largest value of C_L/C possible before an error is introduced in this DAC?

Solution

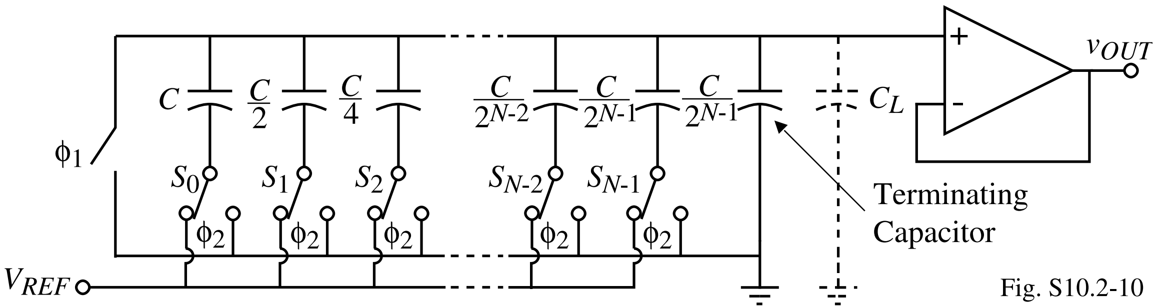


Fig. S10.2-10

(a.) Charge conservation gives,

$$C_{Total}v_{OUT} = \left(b_0C + b_1\frac{C}{2} + b_2\frac{C}{4} + \cdots + b_{N-2}\frac{C}{2^{N-2}} + b_{N-1}\frac{C}{2^{N-1}}\right)V_{REF}$$

where $C_{Total} = 2C + C_L$.

$$v_{OUT} = \left(\frac{C}{2C + C_L}\right)\left(b_0 + \frac{b_1}{2} + \frac{b_2}{4} + \cdots + \frac{b_{N-2}}{2^{N-2}} + \frac{b_{N-1}}{2^{N-1}}\right)V_{REF}$$

$$\therefore \qquad v_{OUT} = \left(\frac{1}{1 + \frac{C_L}{2C}}\right)\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^{N}}\right)V_{REF}$$

(b.) If $C_L << 2C$, then $v_{OUT} \approx \left(1 - \frac{C_L}{2C}\right)\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^{N}}\right)V_{REF}$

which introduces a gain error.

(c.) From the previous result, the error term can be written as,

$$\frac{C_L}{2C}\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^{N}}\right)V_{REF} \le \frac{1}{2}\frac{V_{REF}}{2^N} = 0.5 \text{ LSB}$$

$$\frac{C_L}{C} \le \frac{1}{2^N\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^{N}}\right)} \approx \frac{1}{2^N} \quad \text{when all bits are 1 and } N > 1.$$

Problem 10.2-11

Express the output of the D/A converter shown in Fig. P10.2-11 during the ϕ_2 period as a function of the digital bits, b_i, the capacitors, and the reference voltage, V_{REF}. If the op amp has an offset of V_{OS}, how is this expression for the output changed? What kind of error will the op amp offset cause?

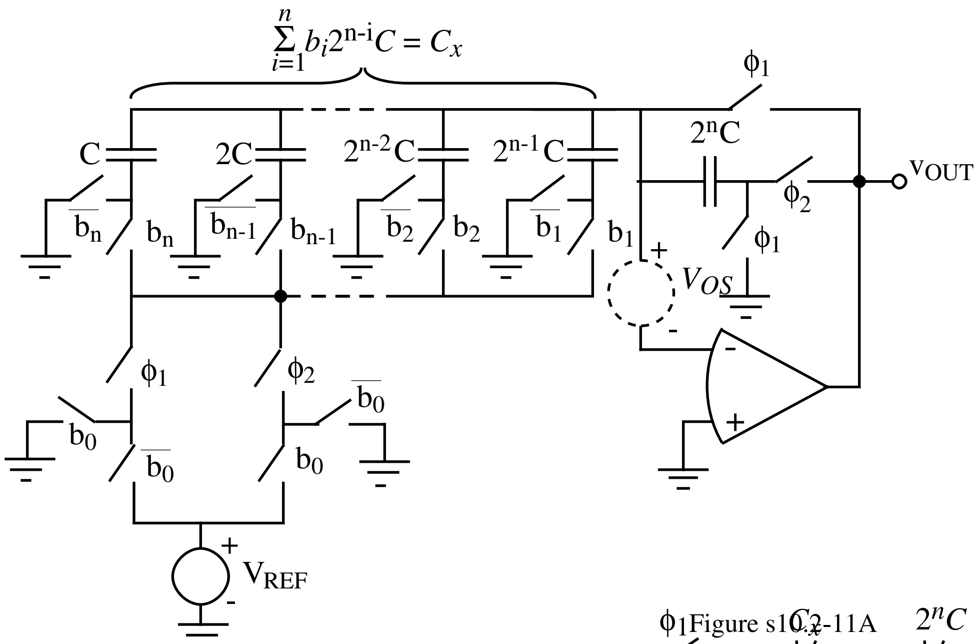


Figure s10.2-11A

Solution

$V_{OS} = 0$:

$$b_0 = 1: \quad v_{OUT} = -\frac{C_x}{2^n C} V_{REF}$$

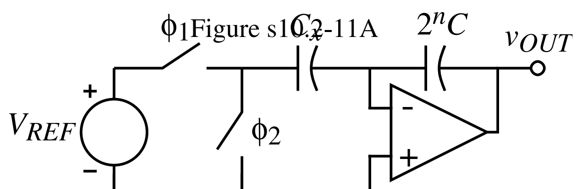


Fig. S10.2-11B

$$v_{OUT} = -\left(\frac{\sum_{n}^{i=1} b_i 2^n 2^{-i} C}{2^n C}\right) V_{REF} \quad \rightarrow \quad \boxed{v_{OUT} = -\left(\sum_{n}^{i=1} \frac{b_i}{2^i}\right) V_{REF}}$$

$(b_0 = 1)$

$b_0 = 0$: Reverse ϕ_1 and ϕ_2 to get,

$$\boxed{v_{OUT} = +\left(\sum_{n}^{i=1} \frac{b_i}{2^i}\right) V_{REF}} \quad (b_0 = 0)$$

Problem 10.2-11 – Continued

$V_{OS} \neq 0$:

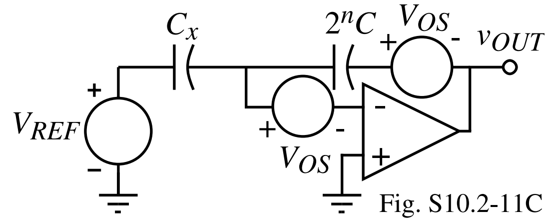


Fig. S10.2-11C

At ϕ_2 we have,

From this circuit, we can write that,

$C_x(V_{REF} - V_{OS}) = 2^nC(V_{OS} - V_{OS} - v_{OUT})$

or

$$v_{OUT} = -\frac{C_x}{2^nC}(V_{REF} - V_{OS})$$

$\therefore$

$$\boxed{v_{OUT} = -\left(\sum_{n}^{i=1} \frac{b_i}{2^i}\right)(V_{REF} - V_{OS})} \qquad (b_0 = 1)$$

and

$$\boxed{v_{OUT} = +\left(\sum_{n}^{i=1} \frac{b_i}{2^i}\right)(V_{REF} - V_{OS})} \qquad (b_0 = 0)$$

V_{OS} causes a gain error.

Problem 10.2-12

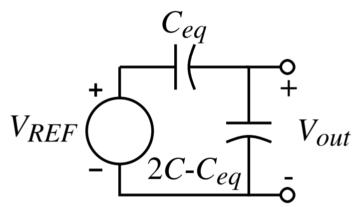
Develop the equivalent circuit of Fig. 10.2-11 from Fig. 10.2-10.

Solution

For each individual capacitor connected only to V_{REF} we can write,

$$V_{out} = V_{REF}\ \frac{C}{2C},\ V_{out} = V_{REF}\ \frac{C}{4C},\ V_{out} = V_{REF}\ \frac{C}{8C},\ \ldots..$$

Note that the numerator consists only of the capacitances connected to V_{REF}. If these capacitors sum up to C_{eq}. then the remaining capacitors must be $2C - C_{eq}$. Therefore, we have,



S10.2-12

Problem 10.2-13

If the tolerance of the capacitors in the 8-bit, binary-weighted array shown in Fig. P10.2-13 is ±0.5%, what would be the worst case *DNL* in units of *LSBs* and at what transition does it occur?

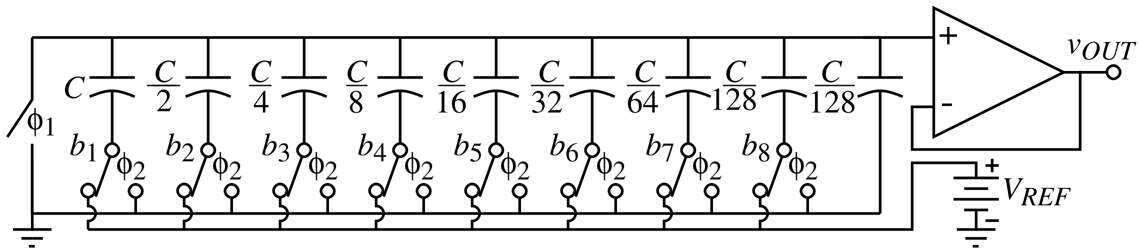


Figure P10.2-13

Solution

The worst case *DNL* occurs at the transition form 01111111 to 10000000.

+DNL:

Ideally, $v_{OUT} = \dfrac{C_{eq}}{2C\text{-}C_{eq} + C_{eq}} V_{REF}$. The worst case is found by assuming that all of the C_{eq} capacitors are maximu and the $2C\text{-}C_{eq}$ capacitors are minimum. However, for the above transition, the maximum, worst case positive step can be written as

$$\text{Max. step} = v_{OUT}(10000000) - v_{OUT}(01111111) = V_{REF}\left[\frac{1.005}{2} - \frac{0.995}{2}\left(1 - \frac{1}{128}\right)\right]$$

$$= \frac{V_{REF}}{2}\left[1.005 - 0.995\left(1 - \frac{1}{128}\right)\right] = \frac{V_{REF}}{2}[1.005 - 0.995(0.9922)]V_{REF}$$

$$= 0.008887V_{REF}$$

An LSB = $V_{REF}/256 = 0.003906V_{REF}$

$$\therefore \quad \boxed{+\text{DNL} = \frac{0.008887}{0.003906} - 1 = 2.275 - 1 = 1.275 \text{ LSB}}$$

-DNL:

For this case, let the C_{eq} capacitors be minimum and the $2C\text{-}C_{eq}$ capacitors be maximum. Following the same development as above gives,

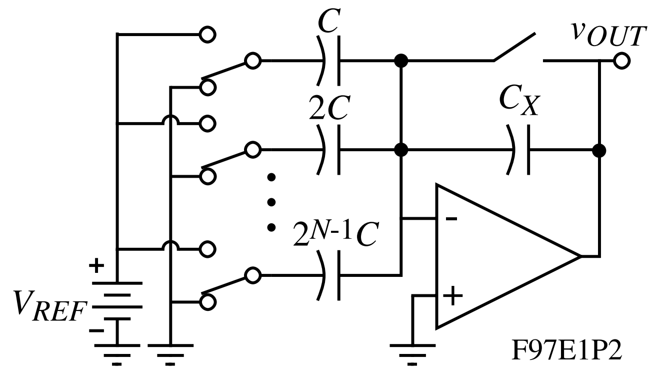
$$\text{Min. step} = v_{OUT}(10000000) - v_{OUT}(01111111) = V_{REF}\left[\frac{0.995}{2} - \frac{1.005}{2}\left(1 - \frac{1}{128}\right)\right]$$

$$= \frac{V_{REF}}{2}\left[0.995 - 1.005\left(1 - \frac{1}{128}\right)\right] = \frac{V_{REF}}{2}[0.995 - 1.005(0.9922)]V_{REF}$$

$$= -0.001074V_{REF}$$

$$\therefore \quad \boxed{-\text{DNL} = \frac{-0.001074}{0.003906} - 1 = -0.2750 - 1 = -1.275 \text{ LSB}}$$

Problem 10.2-14



F97E1P2

A binary weighted DAC using a charge amplifier is shown. At the beginning of the digital to analog conversion, all capacitors are discharged. If a bit is 1, the capacitor is connected to V_{REF} and if the bit is 0 the capacitor is connected to ground.

a.) Design C_X to get

$$v_{OUT} = \left(\frac{b_1}{2} + \frac{b_2}{4} + \cdots + \frac{b_N}{2^N}\right) V_{REF}\,.$$

b.) Identify the switches by b_i where $i = 1$ is the MSB and $i = N$ is the LSB.

c.) Find the maximum component spread (largest value/smallest value) for the capacitors.

d.) Is this DAC fast or slow? Why?

e.) Can this DAC be nonmonotonic?

f.) If the relative accuracy of the capacitors are 0.2% (regardless of capacitor sizes) what is the maximum value of N for ideal operation?

Solution

a.) Solving for v_{OUT} gives

$$v_{OUT} = \left(\frac{C}{C_X} + \frac{2C}{C_X} + \cdots + \frac{2^{N-1}C}{C_X}\right) V_{REF}\text{, therefore } \boxed{C_X = 2^N C} \text{ which gives}$$

$$v_{OUT} = \left(\frac{1}{2^N} + \frac{1}{2^{N-1}} + \cdots + \frac{1}{2}\right) V_{\text{REF}}$$

b.) See schematic for switch identification.

c.) The maximum component spread is C_X/C which is $\boxed{\text{Max. component spread} = 2^N}$

d.) This DAC should be fast because there are no floating nodes.

e.) Yes, the DAC can be nonmonotonic.

f.) Let C_{eq} be all capacitors connected to V_{REF}. $\therefore\ \dfrac{v_{out}}{V_{REF}} = -\dfrac{C_{eq}}{C_x}$.

For the worst case, let C_{eq} be $C_{eq} + \Delta C_{eq}$ and C_x be $C_x - \Delta C_x$ which gives

$$\frac{v_{out}'}{V_{REF}} = -\frac{C_{eq}+\Delta C_{eq}}{C_x-\Delta C_x} = -\frac{C_{eq}}{C_x}\left(\frac{1+\Delta C_{eq}/C_{eq}}{1-\Delta C_x/C_x}\right) = -\frac{C_{eq}}{C_x}\left(\frac{1+0.002}{1-0.002}\right) = -\frac{C_{eq}}{C_x}\left(\frac{501}{499}\right)$$

$$\therefore\ \left|\frac{v_{out}}{V_{REF}} - \frac{v_{out}'}{V_{REF}}\right| = \left|-\frac{C_{eq}}{C_x} + \left(\frac{501}{499}\right)\frac{C_{eq}}{C_x}\right| = \frac{2}{499}\frac{C_{eq}}{C_x} \le \frac{1}{2^{N+1}}$$

The largest value of C_{eq}/C_x is $(2^N-1)/2^N$. $\therefore\ \dfrac{2}{499} \le \dfrac{2^N}{(2^N-1)(2^N+1)} = \dfrac{1}{2^N} \Rightarrow \boxed{N = 7}$

(Note that N is almost equal to 8.)

Problem 10.2-15

A binary weighted DAC using The circuit shown is an equivalent for the operation of a DAC. The op amp differential voltage gain, $A_{vd}(s)$ is modeled as

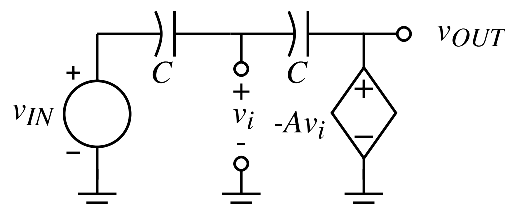
$$A_{vd}(s) = \frac{A_{vd}(0)\ \omega_a}{s + \omega_a} = \frac{GB}{s + \omega_a}.$$

a.) If ω_a goes to infinity so that $A_{vd}(s) \approx A_{vd}(0)$, what is the minimum value of $A_{vd}(0)$ that will cause a ±0.5 LSB error for an 8-bit DAC?

b.) If $A_{vd}(0)$ is larger than the value found in a.), what is the minimum conversion time for an 8-bit DAC which gives a ±0.5 LSB error if GB = 1Mhz?

Solution

a.) Model for the circuit:



$$v_i = \left(\frac{C}{C+C}\right)v_{REF} + \left(\frac{C}{C+C}\right)v_{OUT}$$

and

$$v_{OUT} = -Av_i$$

$$\therefore\ v_{OUT} = \frac{-A}{2}v_{OUT} - \frac{A}{2}v_{REF} \Rightarrow \frac{v_{OUT}}{v_{REF}} = \frac{\frac{-A}{2}}{1 + \frac{A}{2}}$$

Setting the actual gain to -1±0.5LSB gives

$$\frac{-0.5A}{1+0.5A} = -\left(1 - \frac{1}{2}\left(\frac{1}{256}\right)\right) = \frac{-511}{512} \Rightarrow -\frac{512A}{2} = -511 - \frac{511A}{2} \Rightarrow \frac{A}{2} = 511 \Rightarrow$$

$$\boxed{A = 1022}$$

b.) If $A_{vd}(s) \approx -GB/s$, then the s-domain transfer function can be written as

$$\frac{V_{out}(s)}{V_{REF}} = \frac{-GB/2}{s + GB/2} = \frac{-\omega_H}{s + \omega_H} \Rightarrow \omega_H = \frac{2\pi\cdot 10^6}{2} = \pi\cdot 10^6$$

The time domain output can be written as

$$v_{out}(t) = -1[1 - e^{-\omega_H t}]V_{REF}$$

Setting $v_{out}(t)$ = -1±0.5LSB and solving for the time, T, at which this occurs gives

$$-1 + e^{-\omega_H T} = -1 + \frac{1}{512} \Rightarrow e^{\omega HT} = 512 \Rightarrow \omega_H T = ln(512) \Rightarrow T = \frac{6.283}{3.1416\text{x}10^6}$$

or

$$\boxed{T = 1.9857\mu\text{s}}$$

Problem 10.2-16

A charge-scaling DAC is shown in Fig. P10.2-16 that uses a C-$2C$ ladder. All capacitors are discharged during the ϕ_1 phase. (a.) What value of C_F is required to make this DAC work correctly? (b.) Write an expression for v_{OUT} during ϕ_2 in terms of the bits, b_i, and the reference voltage, V_{REF}. (c.) Discuss at least two advantages and two disadvantages of this DAC compared to other types of DACs.

Solution

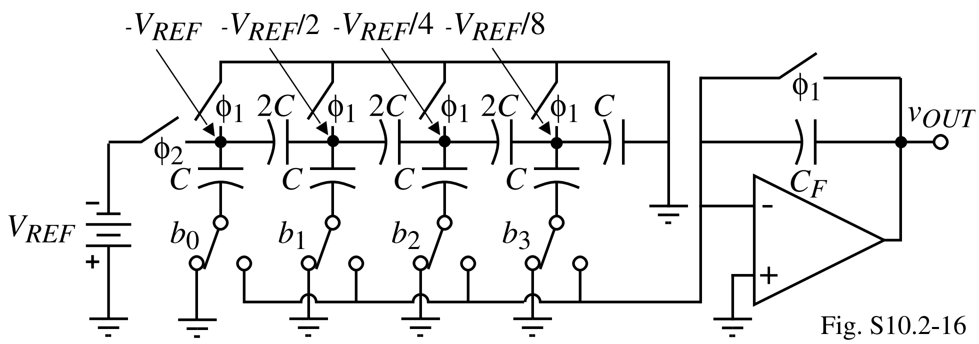


Fig. S10.2-16

(a.) $\boxed{C_F = 2C}$

(b.) $v_{OUT} = \left(\frac{b_0}{2}\right)V_{REF} + \left(\frac{b_1}{2}\right)\frac{V_{REF}}{2} + \left(\frac{b_2}{2}\right)\frac{V_{REF}}{4} + \left(\frac{b_3}{2}\right)\frac{V_{REF}}{8}$

$$\boxed{v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}\right)V_{REF}}$$

(c.) Advantages:

1.) Smaller area than binary-weighted DAC.

2.) Better accuracy because the components differ by only 2:1.

3.) Autozeros the offset of the op amp.

Disadvantages:

1.) Has floating nodes and is sensitive to parasitics.

2.) Parasitic capacitances at the floating nodes will deteriorate the accuracy.

3.) Can be nonmonotonic.

4.) Requires a two-phase, non-overlapping clock.

Problem 10.3-01

The DAC of Fig. 10.3-1 has $m = 2$ and $k = 2$. If the divisor has an incorrect value of 2, express the $\pm INL$ and the $\pm DNL$ in terms of *LSBs* and determine whether or not the DAC is monotonic. Repeat if the divisor is 6.

Solution

The general form for the output of this DAC is,

$$\frac{v_{OUT}}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{2k} + \frac{b_3}{4k}$$

$k = 2$:

$$\frac{v_{OUT}}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{4} + \frac{b_3}{8}$$

The result is:

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.12500	0.00000	1.00000	0.00000	1.00000
0	0	1	0	0.12500	0.25000	0.00000	1.00000	0.00000	2.00000
0	0	1	1	0.18750	0.37500	0.00000	1.00000	0.00000	3.00000
0	1	0	0	0.25000	0.25000	0.00000	-3.00000	0.00000	0.00000
0	1	0	1	0.31250	0.37500	0.00000	1.00000	0.00000	1.00000
0	1	1	0	0.37500	0.50000	0.00000	1.00000	0.00000	2.00000
0	1	1	1	0.43750	0.62500	0.00000	1.00000	0.00000	3.00000
1	0	0	0	0.50000	0.50000	0.00000	-3.00000	0.00000	0.00000
1	0	0	1	0.56250	0.62500	0.00000	1.00000	0.00000	1.00000
1	0	1	0	0.62500	0.75000	0.00000	1.00000	0.00000	2.00000
1	0	1	1	0.68750	0.87500	0.00000	1.00000	0.00000	3.00000
1	1	0	0	0.75000	0.75000	0.00000	-3.00000	0.00000	0.00000
1	1	0	1	0.81250	0.87500	0.00000	1.00000	0.00000	1.00000
1	1	1	0	0.87500	1.00000	0.00000	1.00000	0.00000	2.00000
1	1	1	1	0.93750	1.12500	0.00000	1.00000	0.00000	3.00000

$\therefore$ $INL = +3LSB$ and $0\ LSB$. $DNL = +1LSB$ and $-3LSB$. Nonmontonic because $DNL < 1LSB$.

$k = 6$:

$$\frac{v_{OUT}}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{12} + \frac{b_3}{24}$$

The result is on the next page:

Problem 10.3-01 – Continued

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.04167	0.00000	-0.33333	0.00000	-0.33333
0	0	1	0	0.12500	0.08333	0.00000	-0.33333	0.00000	-0.66667
0	0	1	1	0.18750	0.12500	0.00000	-0.33333	0.00000	-1.00000
0	1	0	0	0.25000	0.25000	0.00000	1.00000	0.00000	0.00000
0	1	0	1	0.31250	0.29167	0.00000	-0.33333	0.00000	-0.33333
0	1	1	0	0.37500	0.33333	0.00000	-0.33333	0.00000	-0.66667
0	1	1	1	0.43750	0.37500	0.00000	-0.33333	0.00000	-1.00000
1	0	0	0	0.50000	0.50000	0.00000	1.00000	0.00000	0.00000
1	0	0	1	0.56250	0.54167	0.00000	-0.33333	0.00000	-0.33333
1	0	1	0	0.62500	0.58333	0.00000	-0.33333	0.00000	-0.66667
1	0	1	1	0.68750	0.62500	0.00000	-0.33333	0.00000	-1.00000
1	1	0	0	0.75000	0.75000	0.00000	1.00000	0.00000	0.00000
1	1	0	1	0.81250	0.79167	0.00000	-0.33333	0.00000	-0.33333
1	1	1	0	0.87500	0.83333	0.00000	-0.33333	0.00000	-0.66667
1	1	1	1	0.93750	0.87500	0.00000	-0.33333	0.00000	-1.00000

$\therefore$ $INL = +0LSB$ and -1 LSB. $DNL = +1LSB$ and $-0.333LSB$. Montonic because $DNL \geq -0.333LSB$.

Problem 10.3-02

Repeat Problem 10.3-1 if the divisor is 3 and 5.

Solution

k=3: $v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)V_{REF} + \left(\frac{b_2}{2} + \frac{b_3}{4}\right)\frac{V_{REF}}{3} = \left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{6} + \frac{b_3}{12}\right]V_{REF}$

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.08333	0.00000	0.33333	0.00000	0.33333
0	0	1	0	0.12500	0.16667	0.00000	0.33333	0.00000	0.66667
0	0	1	1	0.18750	0.25000	0.00000	0.33333	0.00000	1.00000
0	1	0	0	0.25000	0.25000	0.00000	-1.00000	0.00000	0.00000
0	1	0	1	0.31250	0.33333	0.00000	0.33333	0.00000	0.33333
0	1	1	0	0.37500	0.41667	0.00000	0.33333	0.00000	0.66667
0	1	1	1	0.43750	0.50000	0.00000	0.33333	0.00000	1.00000
1	0	0	0	0.50000	0.50000	0.00000	-1.00000	0.00000	0.00000
1	0	0	1	0.56250	0.58333	0.00000	0.33333	0.00000	0.33333
1	0	1	0	0.62500	0.66667	0.00000	0.33333	0.00000	0.66667
1	0	1	1	0.68750	0.75000	0.00000	0.33333	0.00000	1.00000
1	1	0	0	0.75000	0.75000	0.00000	-1.00000	0.00000	0.00000
1	1	0	1	0.81250	0.83333	0.00000	0.33333	0.00000	0.33333
1	1	1	0	0.87500	0.91667	0.00000	0.33333	0.00000	0.66667
1	1	1	1	0.93750	1.00000	0.00000	0.33333	0.00000	1.00000

From the above table, INL = +1LSB and –0LSB, DNL = +0.33LSB and –1LSB. The DAC is on the threshold of nonmonotonicity.

k=5: $v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)V_{REF} + \left(\frac{b_2}{2} + \frac{b_3}{4}\right)\frac{V_{REF}}{5} = \left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{10} + \frac{b_3}{20}\right]V_{REF}$

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.05000	0.00000	-0.20000	0.00000	-0.20000
0	0	1	0	0.12500	0.10000	0.00000	-0.20000	0.00000	-0.40000
0	0	1	1	0.18750	0.15000	0.00000	-0.20000	0.00000	-0.60000
0	1	0	0	0.25000	0.25000	0.00000	0.60000	0.00000	0.00000
0	1	0	1	0.31250	0.30000	0.00000	-0.20000	0.00000	-0.20000
0	1	1	0	0.37500	0.35000	0.00000	-0.20000	0.00000	-0.40000
0	1	1	1	0.43750	0.40000	0.00000	-0.20000	0.00000	-0.60000
1	0	0	0	0.50000	0.50000	0.00000	0.60000	0.00000	0.00000
1	0	0	1	0.56250	0.55000	0.00000	-0.20000	0.00000	-0.20000
1	0	1	0	0.62500	0.60000	0.00000	-0.20000	0.00000	-0.40000
1	0	1	1	0.68750	0.65000	0.00000	-0.20000	0.00000	-0.60000
1	1	0	0	0.75000	0.75000	0.00000	0.60000	0.00000	0.00000
1	1	0	1	0.81250	0.80000	0.00000	-0.20000	0.00000	-0.20000
1	1	1	0	0.87500	0.85000	0.00000	-0.20000	0.00000	-0.40000
1	1	1	1	0.93750	0.90000	0.00000	-0.20000	0.00000	-0.60000

From the above table, INL = +0LSB and –0.6LSB, DNL = +0.6LSB and –0.2LSB. The DAC is monotonic.

Problem 10.3-03

Repeat Problem 1 if the divisor is correct (4) and the V_{REF} for the *MSB* subDAC is $0.75V_{REF}$ and the V_{REF} for the *LSB* subDAC is $1.25V_{REF}$.)

Soluiton

The analog output can be written as,

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)\frac{3V_{REF}}{4} + \left(\frac{b_2}{2} + \frac{b_3}{4}\right)\frac{5V_{REF}}{4} = \left[\frac{3b_0}{8} + \frac{3b_1}{16} + \frac{5b_2}{32} + \frac{5b_3}{64}\right]V_{REF}$$

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.07813	0.00000	0.25000	0.00000	0.25000
0	0	1	0	0.12500	0.15625	0.00000	0.25000	0.00000	0.50000
0	0	1	1	0.18750	0.23438	0.00000	0.25000	0.00000	0.75000
0	1	0	0	0.25000	0.18750	0.00000	-1.75000	0.00000	-1.00000
0	1	0	1	0.31250	0.26563	0.00000	0.25000	0.00000	-0.75000
0	1	1	0	0.37500	0.34375	0.00000	0.25000	0.00000	-0.50000
0	1	1	1	0.43750	0.42188	0.00000	0.25000	0.00000	-0.25000
1	0	0	0	0.50000	0.37500	0.00000	-1.75000	0.00000	-2.00000
1	0	0	1	0.56250	0.45313	0.00000	0.25000	0.00000	-1.75000
1	0	1	0	0.62500	0.53125	0.00000	0.25000	0.00000	-1.50000
1	0	1	1	0.68750	0.60938	0.00000	0.25000	0.00000	-1.25000
1	1	0	0	0.75000	0.56250	0.00000	-1.75000	0.00000	-3.00000
1	1	0	1	0.81250	0.64063	0.00000	0.25000	0.00000	-2.75000
1	1	1	0	0.87500	0.71875	0.00000	0.25000	0.00000	-2.50000
1	1	1	1	0.93750	0.79688	0.00000	0.25000	0.00000	-2.25000

From the above table, INL = +0.75LSB and –3LSB, DNL = +0.25LSB and –1.75LSB. The DAC is not monotonicity.

Problem 10.3-04

Find the worst case tolerance of x ($\Delta x/x$) in % that will not cause a conversion error for the DAC shown. Assume that all aspects of the DAC are ideal except for x. (Note: that the divisor is $1/x$ so that x is less than 1.)

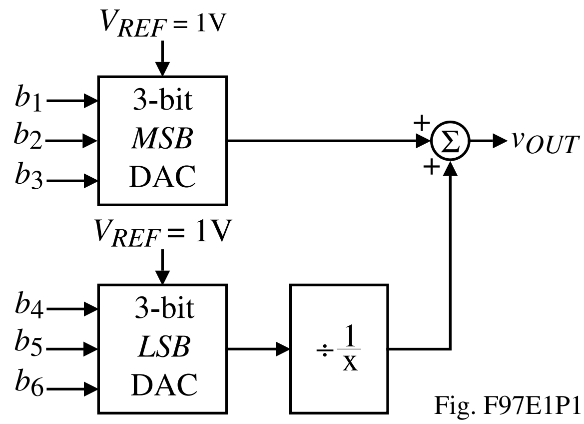


Fig. F97E1P1

Solution

The tolerance is only influenced by the bits of the *LSB* DAC. The ideal and actual outputs are given as,

$$v_{out}(\text{ideal}) = x\left[\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8}\right]$$

$$v_{out}(\text{actual}) = (x \pm \Delta x)\left[\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8}\right]$$

$\therefore$ Worst case error = $|v_{out}(\text{actual}) - v_{out}(\text{ideal})| \leq 1/2^7 \Rightarrow \Delta x\left[\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8}\right] \leq \frac{1}{2^7} = \frac{1}{128}$

The tolerance is decreased if all *LSB* bits are 1. Therefore,

$$\Delta x\left(\frac{7}{8}\right) \leq \frac{1}{128} \quad \Rightarrow \quad \Delta x \leq \frac{8}{7}\frac{1}{128} = \frac{1}{112}$$

Therefore, the factor x can be expressed as,

$$x \ \pm \ \Delta x = \frac{1}{8} \pm \frac{1}{112} = \frac{14}{112} \pm \frac{1}{112}$$

The tolerance of x is expressed as

$$\boxed{\text{Tolerance of } x \ = \frac{\pm\Delta x}{x} = \frac{\pm 1}{14} = \pm 7.143\%}$$

Problem 10.3-05

The DAC of Fig. 10.3-2 has $m = 3$ and $k = 3$. Find (a.) the ideal value of the divisor of V_{REF} designated as x. (b.) Find the largest value of x that causes a 1*LSB DNL*. (c.) Find the smallest value of x that causes a 2*LSB DNL*.

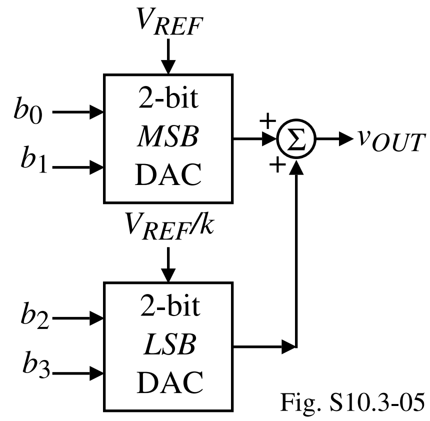


Fig. S10.3-05

Solution

a.) $v_{OUT} = V_{REF}\left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{2k} + \frac{b_3}{4k}\right]$

$\underline{k = 4}$ for ideal behavior.

b.) Let $v_{OUT}' = v_{OUT}$ when $k \neq 4$. Also note that ±1LSB = 1/16 when v_{OUT} is normalized to V_{REF}.

$$\therefore \qquad \frac{v_{OUT}' - v_{OUT}}{V_{REF}} = \pm\frac{1}{16}$$

$$\left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{1}{k}\left(\frac{b_2}{2} + \frac{b_3}{4}\right)\right] - \left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}\right] = \left(\frac{1}{k} - \frac{1}{4}\right)\left(+\frac{b_2}{2} + \frac{b_3}{4}\right) = \pm\frac{1}{16}$$

$$\left(\frac{4}{k} - 1\right)(2b_2 + b_3) = \pm 1 \rightarrow \qquad \frac{4}{k} = 1 \pm \left(\frac{1}{2b_2 + b_3}\right) = \frac{2b_2 + b_3 \pm 1}{2b_2 + b_3}$$

$$\therefore \qquad k = \frac{4(2b_2 + b_3)}{2b_2 + b_3 \pm 1}$$

Try various combinations of b_2 and b_3:

$b_2 = 0$ and $b_3 = 1 \quad \rightarrow \quad k = \frac{4}{1\pm 1} = 2, \infty$

$b_2 = 1$ and $b_3 = 0 \quad \rightarrow \quad k = \frac{8}{2\pm 1} = \frac{8}{3}, 8$

$b_2 = 1$ and $b_3 = 1 \quad \rightarrow \quad k = \frac{12}{3\pm 1} = 4, 6$

The smallest, largest value of k that maintains ±1LSB is 6. ∴ $\underline{k = 6}$
(k is ideally 4 and the smallest of the maximum values is 6)

c.) For DNL, the worst case occurs from X011 to X100.

$$\therefore \qquad \frac{v_{OUT}(\text{X100}) - v_{OUT}(\text{X011})}{V_{REF}/16} - 1 = \pm 2$$

$$\frac{1}{4} - \left(\frac{1}{2k} + \frac{1}{4k}\right) = \frac{1}{16} \pm \frac{2}{16} \qquad \rightarrow \qquad 4 - \frac{12}{k} = 1 \pm 2 \quad \rightarrow \qquad \frac{12}{k} = 3 - (\pm 2)$$

$$k = \frac{12}{3-(\pm 2)} = 12 \text{ or } 2.4 \qquad\qquad \therefore\ \underline{k = 2.4}$$

Problem 10.3-06

Show for the results of Ex. 10.3-2 that the resulting *INL* and *DNL* will be equal to –0.5*LSB* or less.

Solution

Consider only the *LSBs* because the error in the division factor only affects the *LSB* subDAC.

INL:

The worst case *INL* occurs when both b_3 and b_4 are on. Therefore,

$$\left(\frac{1}{2}+\frac{1}{4}\right)\left(\frac{6\pm1}{24}\right)=\left(\frac{3}{4}\right)\left(\frac{6\pm1}{24}\right)=\frac{6\pm1}{32}=\frac{5}{32},\frac{7}{32}$$

$$INL^{+}(\max) = V_o(\text{actual}) - V_o(\text{ideal}) = \frac{7}{32}-\frac{6}{32}=\frac{1}{32} = +0.5LSB$$

$$INL^{-}(\max) = V_o(\text{actual}) - V_o(\text{ideal}) = \frac{5}{32}-\frac{6}{32}=\frac{-1}{32} = -0.5LSB$$

Therefore, the worst case *INL* is equal to or less than ±0.5*LSB*.

DNL:

The worst case *DNL* occurs when both bits of the *LSB* subDAC change from 1 to 0. This corresponds to a change from 0011 to 0100. If the scaling factor is 7/24 corresponding to the +1/24 tolerance, then

$$\Delta V_o = V_o(0011) - V_o(0100) = \frac{5}{32}-\frac{1}{4}=\frac{5}{32}-\frac{8}{32}=\frac{3}{32}$$

$$DNL^{+} = \Delta V_o - \frac{2}{32}=\frac{3}{32}-\frac{2}{32}=\frac{1}{32} = +0.5LSB$$

If the scaling factor is 5/24 corresponding to the -1/24 tolerance, then

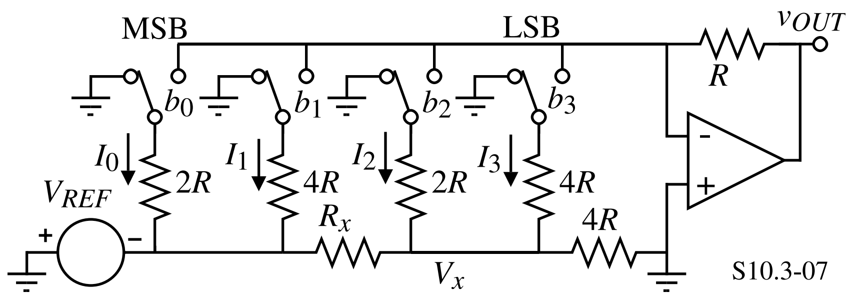
$$\Delta V_o = V_o(0011) - V_o(0100) = \frac{7}{32}-\frac{1}{4}=\frac{7}{32}-\frac{8}{32}=\frac{1}{32}$$

$$DNL^{-} = \Delta V_o - \frac{2}{32}=\frac{1}{32}-\frac{2}{32}=\frac{-1}{32} = -0.5LSB$$

Therefore, the worst case *DNL* is equal to or less than ±0.5*LSB*.

Problem 10.3-07

A 4-bit, digital-analog converter is shown in Fig. P10.3-7. When a bit is 1, the switch pertaining to that bit is connected to the op amp negative input terminal, otherwise it is connected to ground. Identify the switches by the notation b_1, b_2, b_3, or b_4 where b_i corresponds to the ith bit and b_1 is the MSB and b_4 is the LSB. Solve for the value of R_x which will give proper digital-analog converter performance.



Solution

For this circuit to operate properly, $I_0 = \frac{V_{REF}}{2R}$, $I_1 = \frac{I_0}{2}$, $I_2 = \frac{I_0}{4}$, and $I_3 = \frac{I_0}{8}$.

To achieve this result, $V_x = -\frac{V_{REF}}{4}$. The equivalent resistance seen to ground from the right of R_x can be expressed as,

$$R_{EQ} = 2R||(4R||4R) = 2R||2R = R$$

$$\therefore \quad V_x = \frac{R}{R+R_x}(-V_{REF}) = -\frac{V_{REF}}{4}$$

$$\therefore \quad \boxed{R_x = 3R}$$

Problem 10.3-08

Assume R_1=R_5=2R, R_2=R_6=4R, R_3=R_7=8R, R_4=R_8=16R and that the op amp is ideal. (a.) Find the value of R_9 and R_{10} in terms of R which gives an ideal 8-bit digital-to-analog converter. (b.) Find the range of values of R_9 in terms of R which keeps the $INL \leq \pm 0.5LSB$. Assume that R_{10} has its ideal value. Clearly state any assumption you make in working this problem. (c.) Find the range of R_{10} in terms of R which keeps the converter monotonic. Assume that R_9 has its ideal value. Clearly state any assumptions you make in working this problem.

Solution

(a.) $\boxed{R_8 = 16R \text{ and } R_9 = R}$

(b.) $v_{OUT} = V_{REF}\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}\right) + \frac{R}{R_8} V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)$

The worst case INL occurs when the bits in the MSB subDAC are zero and the bits in the LSB subDAC are one.

$$\therefore \qquad v_{OUT} = \frac{R}{R_8} V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)$$

$$v_{OUT}(\text{ideal}) = \frac{1}{16} V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)$$

$$\therefore \qquad \text{INL} = v_{OUT} - v_{OUT}(\text{ideal}) = V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)\left(\frac{R}{R_8} - \frac{1}{16}\right) = +\frac{1}{2}\frac{V_{REF}}{256}$$

$$512(0.9375)\left(\frac{R}{R_8} - \frac{1}{16}\right) = 1 \quad \rightarrow \quad \frac{R}{R_8} = 0.064583 \quad \rightarrow \quad R_8 = 15.4838R$$

Also, $\text{INL} = v_{OUT} - v_{OUT}(\text{ideal}) = V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)\left(\frac{R}{R_8} - \frac{1}{16}\right) = -\frac{1}{2}\frac{V_{REF}}{256}$

$$512(0.9375)\left(\frac{R}{R_8} - \frac{1}{16}\right) = -1 \quad \rightarrow \quad \frac{R}{R_8} = 0.060417 \rightarrow \quad R_8 = 16.5517R$$

$$\therefore \qquad \boxed{15.4838R \leq R_8 \leq 16.5517R}$$

(c.) Worst case monotonicity occurs when the bits of the LSB subDAC go from 1 to 0.

$$v_{OUT}(\text{LSBs} = 1) = \frac{V_{REF}}{16}\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16}\right) = \frac{V_{REF}}{16}\left(\frac{15}{16}\right)$$

$$v_{OUT}(b_3 = 1, \text{ all others } 0) = V_{REF}\frac{R}{R_9}\left(\frac{1}{16}\right)$$

Nonmonotonicity $\Rightarrow$ $V_{REF}\frac{R}{R_9}\left(\frac{1}{16}\right) > \frac{V_{REF}}{16}\left(\frac{15}{16}\right) \quad \rightarrow \quad \boxed{R_9 < \frac{15}{16}R}$

Problem 10.3-09

Design a ten-bit, two-stage charge-scaling D/A converter similar to Fig. 10.3-4 using two five-bit sections with a capacitive attenuator between the stages. Give all capacitances in terms of C, which is the smallest capacitor of the design.

Solution

The result is shown below.

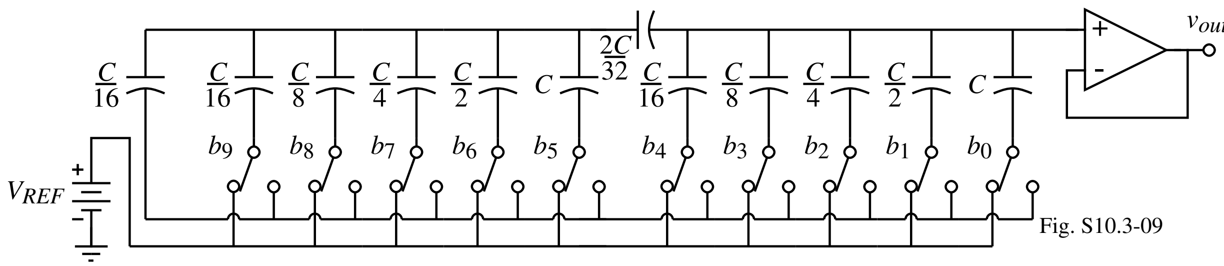


Fig. S10.3-09

The design of the connecting capacitor, C_s, is done as follows,

$$\frac{C}{16} = \frac{1}{\frac{1}{C_s} + \frac{1}{2C}} \rightarrow \quad \frac{1}{C_s} + \frac{1}{2C} = \frac{16}{C} \quad \rightarrow \quad \frac{1}{C_s} = \frac{32}{2C} - \frac{1}{2C} = \frac{31}{2C}$$

$$\therefore \qquad C_s = \frac{2C}{31}$$

Problem 10.3-10

A two-stage, charge-scaling D/A converter is shown in Fig. P10.3-10. (a.) Design C_x in terms of C, the unit capacitor, to achieve a 6-bit, two-stage, charge-scaling DAC. (b.) If C_x is in error by ΔC_x, find an expression for v_{OUT} in terms of C_x, ΔC_x, b_i and V_{REF}. (c.) If the expression for v_{OUT} in part (b.) is given as

$$v_{OUT} = \frac{V_{REF}}{8}\left(1 - \frac{17\Delta C_x}{100C_x}\right)\left[\sum_{i=1}^{3} b_i 2^{3-i} + \left(1 + \frac{8\Delta C_x}{10C_x}\right)\sum_{i=4}^{6}\frac{b_i 2^{6-i}}{8}\right]$$

what is the accuracy of C_x necessary to avoid an error using worst case considerations.

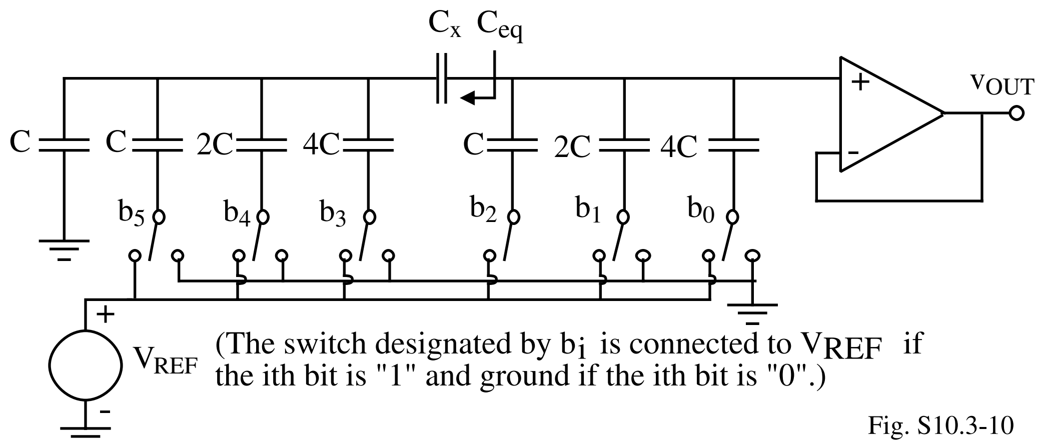


Fig. S10.3-10

Solution

(a.) The value of $C_{eq.}$ must be C. Therefore,

$$\frac{1}{C} = \frac{1}{C_x} + \frac{1}{8C} \quad\rightarrow\quad \frac{1}{C_x} = \frac{7}{8C} \quad\rightarrow\quad \boxed{C_x = \frac{8C}{7}}$$

(b.) The model for the analysis is found by using Thevenin's equivalent circuits and is ,

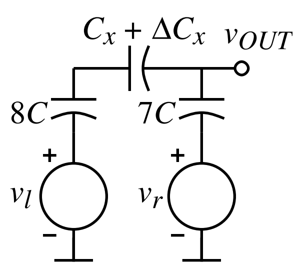


Fig. S10.3-10B

$$v_r = \sum_{i=0}^{2}\frac{b_i 2^{2-i}}{7} V_{REF}$$

$$v_l = \sum_{i=3}^{5}\frac{b_i 2^{5-i}}{8} V_{REF}$$

$$v_{OUT} = \left(\frac{\frac{1}{8C} + \frac{1}{C_x+\Delta C_x}}{\frac{1}{8C} + \frac{1}{7C} + \frac{1}{C_x+\Delta C_x}}\right) v_r + \left(\frac{\frac{1}{7C}}{\frac{1}{8C} + \frac{1}{7C} + \frac{1}{C_x+\Delta C_x}}\right) v_l$$

Problem 10.3-10 – Continued

$$v_{OUT} = \left(\frac{\frac{1}{8C} + \frac{1}{C_x(1+\Delta C_x/C_x)}}{\frac{1}{8C} + \frac{1}{7C} + \frac{1}{C_x(1+\Delta C_x/C_x)}}\right) v_r + \left(\frac{\frac{1}{7C}}{\frac{1}{8C} + \frac{1}{7C} + \frac{1}{C_x(1+\Delta C_x/C_x)}}\right) v_l$$

Let $C_x = \frac{8C}{7}$ and $\frac{\Delta C_x}{C_x} = \varepsilon$

$$\therefore \qquad v_{OUT} = \left(\frac{\frac{1}{8C} + \frac{7}{8C}\left(\frac{1}{1+\varepsilon}\right)}{\frac{1}{8C} + \frac{1}{7C} + \frac{7}{8C}\left(\frac{1}{1+\varepsilon}\right)}\right) v_r + \left(\frac{\frac{1}{7C}}{\frac{1}{8C} + \frac{1}{7C} + \frac{7}{8C}\left(\frac{1}{1+\varepsilon}\right)}\right) v_l$$

Assume that $\frac{1}{1+\varepsilon} \approx 1-\varepsilon$ to get,

$$v_{OUT} \approx \left(\frac{\frac{1}{8} + \frac{7}{8} - \frac{7\varepsilon}{8}}{\frac{1}{8} + \frac{1}{7} + \frac{7}{8} - \frac{7\varepsilon}{8}}\right) v_r + \left(\frac{\frac{1}{7}}{\frac{1}{8} + \frac{1}{7} + \frac{7}{8} - \frac{7\varepsilon}{8}}\right) v_l = \left(\frac{1 - \frac{7\varepsilon}{8}}{1 + \frac{1}{7} - \frac{7\varepsilon}{8}}\right) v_r + \left(\frac{\frac{1}{7}}{1 + \frac{1}{7} - \frac{7\varepsilon}{8}}\right) v_l$$

$$v_{OUT} = \left(\frac{7 - \frac{49\varepsilon}{8}}{8 - \frac{49\varepsilon}{8}}\right) v_r + \left(\frac{1}{8 - \frac{49\varepsilon}{8}}\right) v_l = \frac{7}{8}\left(\frac{1 - \frac{49\varepsilon}{56}}{1 - \frac{49\varepsilon}{64}}\right) v_r + \frac{1}{8\left(1 - \frac{49\varepsilon}{64}\right)} v_l$$

$$v_{OUT} = \frac{7}{8}\left(\frac{1 - \frac{49\varepsilon}{56}}{1 - \frac{49\varepsilon}{64}}\right)\left(v_r + \frac{v_l}{7\left(1 - \frac{49\varepsilon}{56}\right)}\right) \approx \frac{7}{8}\left[1 + \left(\frac{49}{64} - \frac{49}{56}\right)\varepsilon\right]\left(v_r + \frac{1}{7}\left(1 + \frac{49\varepsilon}{56}\right) v_l\right)$$

$$v_{OUT} = \frac{7}{8}\left(1 - \frac{7\varepsilon}{64}\right)\left[\sum_{i=0}^{2} \frac{b_i 2^{2-i}}{7} V_{REF} + \frac{1}{7}\left(1 + \frac{49\varepsilon}{56}\right)\sum_{i=3}^{5} \frac{b_i 2^{5-i}}{8} V_{REF}\right]$$

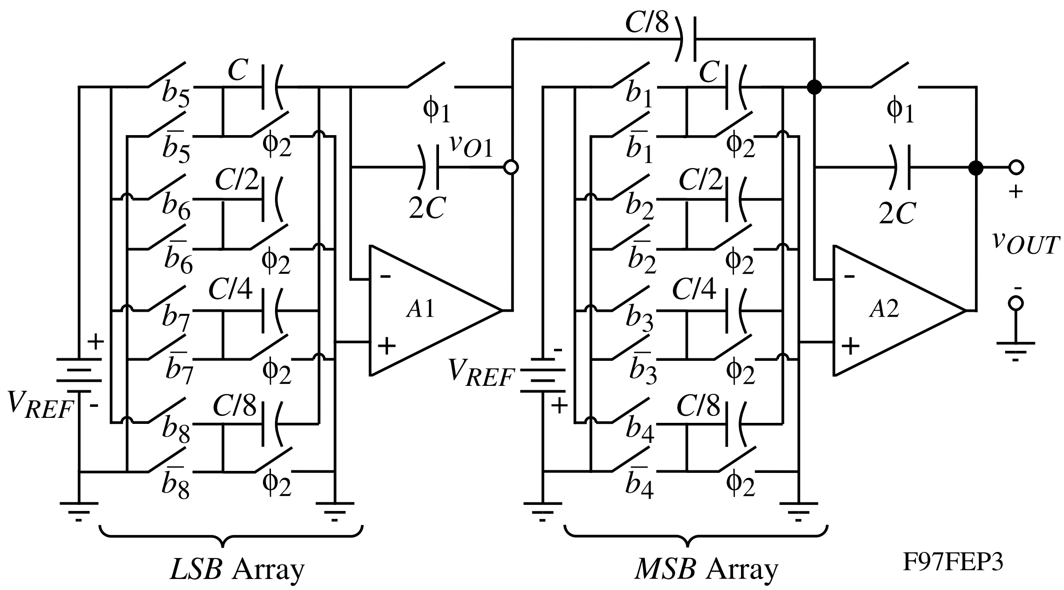
$$\therefore \qquad \boxed{v_{OUT} = \frac{V_{REF}}{8}\left(1 - \frac{7\varepsilon}{64}\right)\left[\sum_{i=0}^{2} b_i 2^{2-i} + \left(1 + \frac{7\varepsilon}{8}\right)\sum_{i=3}^{5} \frac{b_i 2^{5-i}}{8}\right]}$$

(c.) The error due to ΔC_x should be less than $\pm 0.5LSB$. Worst case is for all bits 1.

$$\therefore \qquad \left(-\frac{17\Delta C_x}{100C_x} + \frac{8\Delta C_x}{10C_x}\right)\frac{7V_{REF}}{8} \le \frac{V_{REF}}{2^{N+1}} = \frac{V_{REF}}{128} \qquad \rightarrow \qquad \boxed{\frac{\Delta C_x}{C_x} \le 1.685\%}$$

Problem 10.3-11

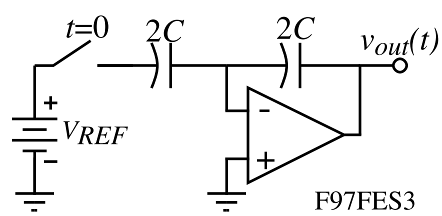
If the op amps in the circuit below have a dc gain of 10^4 and a dominant pole at 100Hz, at what clock frequency will the *effective number of bits (ENOB)* = 7bits assuming that the capacitors and switches are ideal? Use a worst case approach to this problem and assume that time responses of the *LSB* and *MSB* stages add to give the overall conversion time.



F97FEP3

Solution

The worst case approach assumes that all capacitors are switched into the op amp input and that both stages can be modelled approximately as shown.



F97FES3

With a single pole model for the op amp, it can be shown that the -3dB frequency is given as follows where $C_1 = C_2$ gives the lowest -3dB frequency.

$$\omega_H = \frac{GB \cdot C_2}{C_1+C_2} = \frac{GB}{2} = \pi x10^6 \text{ radians/sec}$$

$$\therefore \; v_{out}(t) = (C_1/C_2)[1 - e^{-\omega_H t}]V_{REF}$$

ENOB of 7 bits $\Rightarrow \quad \pm\frac{1}{2}\frac{V_{REF}}{2^7} = \pm\frac{V_{REF}}{2^8} \qquad v_{out}(T) = V_{REF} - \frac{V_{REF}}{2^8}$

$$\therefore \; 1 - \frac{1}{2^8} = 1 - e^{-\omega_H T} \;\Rightarrow\; e^{\omega_H T} = 2^8 \;\Rightarrow\; T = \frac{8}{\omega_H} ln(2) = \frac{8}{\pi x10^6} 0.693 = 1.765\mu s$$

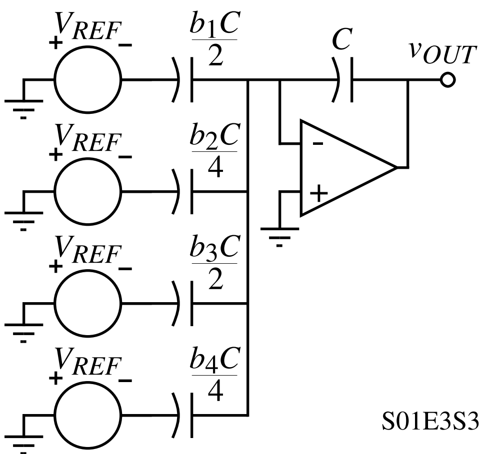
Double this time for 2 stages to $T_{clock} = 3.53\mu s \Rightarrow \boxed{f_{clock} = \frac{1}{T_{clock}} = 283\text{kHz}}$

Problem 10.3-12

The DAC shown uses two identical, 2-bit DACs to achieve a 4-bit D/A converter. Give an expression for v_{OUT} as a function of V_{REF} and the bits, b_1, b_2, b_3, and b_4 during the ϕ_2 phase period. The switches controlled by the bits are closed if the bit is high and open if the bit is low during the ϕ_2 phase period. If k = 2, express the INL (in terms of a ±LSB value) and DNL (in terms of a ±LSB value) and determine whether the converter is monotonic or not. (You may use the output-input plot on the next page if you wish.)

Solution

During the ϕ_2 phase the DAC can be modeled as:



$$v_{OUT}(\phi_2) = \left[\left(\frac{b_1}{2} + \frac{b_2}{4}\right) + \frac{1}{k}\left(\frac{b_2}{2} + \frac{b_4}{4}\right)\right] V_{REF}$$

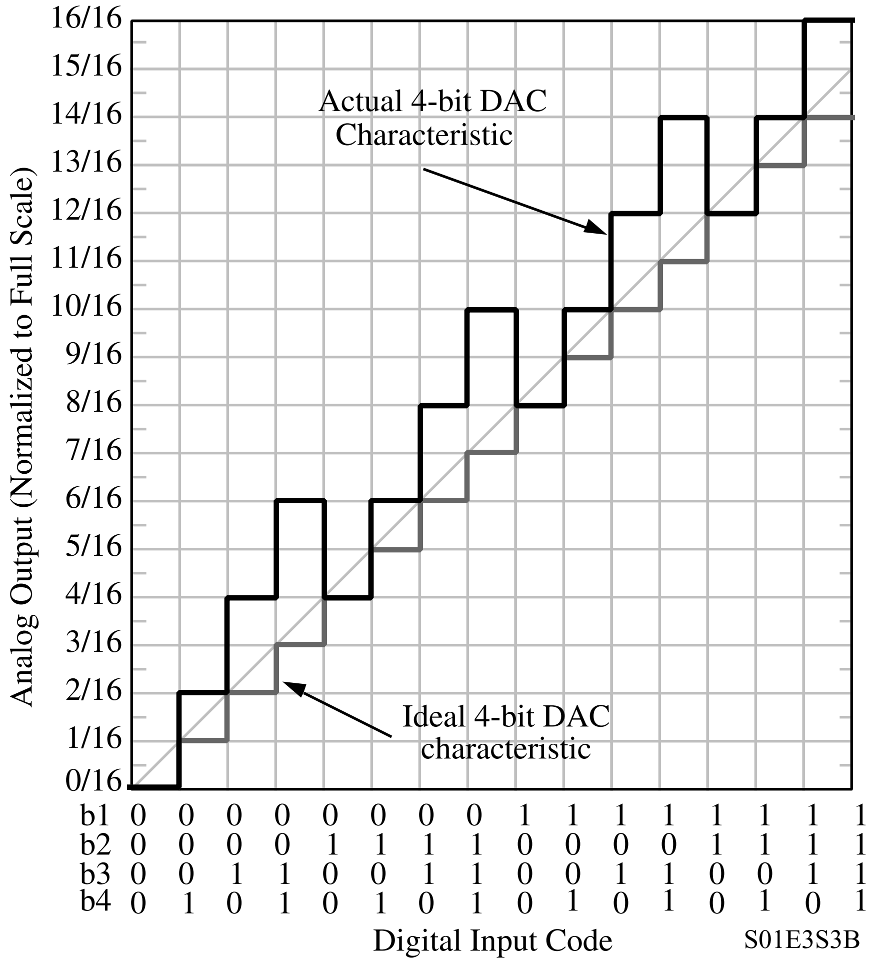
If $k = 2$, then

$$\frac{v_{OUT}(\phi_2)}{V_{REF}} = \frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{4} + \frac{b_4}{8}$$

S01E3S3

Input Digital Word	Output for $k = 4$	Output for $k = 2$
0000	0	0
0001	1/16	2/16
0010	2/16	4/16
0011	3/16	6/16
0100	4/16	4/16
0101	5/16	6/16
0110	6/16	8/16
0111	7/16	10/16
1000	8/16	8/16
1001	9/16	10/16
1010	10/16	12/16
1011	11/16	14/16
1100	12/16	12/16
1101	13/16	14/16
1110	14/16	16/16
1111	15/16	18/16

Problem 10.3-12 – Continued



The INL is +3LSB and –0LSB.

The DNL is +1LSB and –3LSB.

Converter is definitely not monotonic.

Problem 10.3-13

An N-bit DAC consists of a voltage scaling DAC of M-bits and a charge scaling DAC of K-bits (N=M+K). The accuracy of the resistors in the M-bit voltage scaling DAC is $-\Delta R/R$. The accuracy of the binary-weighted capacitors in the charge scaling DAC is $-\Delta C/C$. Assume for this problem that INL and DNL can be expressed generally as,

INL = Accuracy of component x Maximum weighting factor

DNL = Accuracy of the largest component x Corresponding weighting factor

where the weighting factor for the i-th bit is 2^{N-i+1}.

(a.) If the MSB bits use the M-bit voltage scaling DAC and the LSB bits use the K-bit charge scaling DAC, express the INL and DNL of the N-bit DAC in terms of M, K, N, $\Delta R/R$, and $\Delta C/C$. (b.) If the MSB bits use the K-bit charge scaling DAC and the LSB bits use the M-bit voltage scaling DAC, express the INL and DNL of the N-bit DAC in terms of M, K, N, $\Delta R/R$, and $\Delta C/C$.

Solution

(a.) In a M-bit voltage scaling DAC, there are 2^M resistors between V_{REF} and ground. The voltage at the bottom of the i-th resistor from the top is $v_i = \dfrac{(2^M-i)R}{(2^M-i)R + iR} V_{REF}$ where the iR resistors are above v_i and the 2^M-i resistors are below v_i. The worst case $INL(R)$ for the voltage scaling DAC is found at the midpoint where $i = 2^{M-1}$ and the resistors below are all maximum positive and the resistors above are all maximum negative. Thus,

$$INL(R) = v_{2M\text{-}1}(\text{actual}) - v_{2M\text{-}1}(\text{ideal}) = \frac{2^{M-1}(R+\Delta R)V_{REF}}{2^{M-1}(R+\Delta R) + 2^{M-1}(R-\Delta R)} - \frac{V_{REF}}{2} = \frac{\Delta R}{2R}$$

or
$$\boxed{INL(R) = \frac{2^M}{2^M}\left(\frac{\Delta R}{2R}\right) = 2^{M-1}\frac{\Delta R}{R}\ \text{LSBs}}$$

The worst case $DNL(R)$ for the voltage scaling DAC is found as the maximum step size minus the ideal step size. Thus,

$$DNL(R) = v_{step}(\text{actual}) - v_{step}(\text{ideal}) = \frac{(R\pm\Delta R)V_{REF}}{2^M R} - \frac{R}{2^M R}V_{REF} = \frac{\pm\Delta R}{2^M R}V_{REF}$$

or
$$\boxed{DNL(R) = \left(\frac{\pm\Delta R\ V_{REF}}{2^M R}\right)\frac{2^N}{2^N} = \frac{\pm 2^N}{2^M}\frac{\Delta R}{R} = \pm 2^K\frac{\Delta R}{R}\ \text{LSBs}}$$

Let us now examine the $INL(C)$ and the $DNL(C)$ of a K-bit binary-weighted capacitor array. The ideal output for the i-th capacitor is given as

$$v_{OUT}(\text{ideal}) = \frac{C/2^{i-1}}{2C}V_{REF} = \frac{V_{REF}}{2^i}\left(\frac{2^K}{2^K}\right) = \frac{2^K}{2^i}\ LSBs$$

The actual wors-case output for the i-th capacitor is given as

$$v_{OUT}(\text{actual}) = \frac{(C\pm\Delta C)/2^{i-1}}{2C}V_{REF} = \frac{V_{REF}}{2^i} \pm \frac{\Delta C\cdot V_{REF}}{2^i C} = \frac{2^K}{2^i} \pm \frac{2^K\Delta C}{2^i C}\ LSBs$$

Problem 10.3-13 — Continued

Therefore, the *INL* due to the binary-weighted capacitor array is

$$INL(C) = v_{OUT}(\text{actual}) - v_{OUT}(\text{ideal}) = \pm\frac{2^K\Delta C}{2^i C} = \pm\frac{2^{K-i}\Delta C}{C}\ LSBs$$

The worst case occurs for $i = 1$ which gives $\boxed{INL(C) = \pm\frac{2^{K-1}\Delta C}{C}\ LSBs}$

Finally, the worst case *DNL* due to the binary-weighted capacitor array is found as

$$DNL(C) = v_{OUT}(1000\ldots.) - v_{OUT}(0111\ldots.) = \frac{2^{K-1}\Delta C}{C} + \frac{2^{K-1}\Delta C}{C} = \frac{2^K\Delta C}{C}\ LSBs$$

The *INL* when the *MSBs* use voltage scaling and the *LSBs* use charge scaling is,

$$\boxed{INL = INL(R) + INL(C) = 2^{M-1}\frac{\Delta R}{R} + 2^{N-1}\frac{\Delta C}{C}}$$

where the *LSB* of the charge scaling DAC is now $VREF/2^N$ rather than $VREF/2^K$.

The *DNL* when the *MSBs* use voltage scaling and the *LSBs* use charge scaling is,

$$\boxed{DNL = DNL(R) + DNL(C) = 2^K\frac{\Delta R}{R} + 2^K\frac{\Delta C}{C} = 2^K\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)}$$

(b.) Fortunately we can use the above results for the case where the *MSBs* use the charge-scaling DAC and the *LSBs* use the voltage scaling DAC.

For *INL*(*R*) the *LSB* is now $V_{REF}/2^N$. Therefore,

$$\boxed{INL(R) = \frac{2^N}{2^N}\left(\frac{\Delta R}{2R}\right)V_{REF} = 2^{N-1}\frac{\Delta R}{R}\ LSBs}$$

For the *INL*(*C*), *K* is replaced with *N* to give,

$$\boxed{INL(C) = \pm\frac{2^{N-1}\Delta C}{C}\ LSBs}$$

For the *DNL*(*R*), the *LSB* is $V_{REF}/2^N$ so that the *DNL*(*R*) for part (b.) becomes

$$\boxed{DNL(R) = \frac{\pm\Delta R}{2^N R}V_{REF} = \frac{\pm\Delta R}{R}\ LSBs}\ )$$

Since the *MSB* for the chage scaling DAC is now *N*, the *DNL*(*C*) becomes

$$\boxed{DNL(C) = \frac{2^N\Delta C}{C}\ LSBs}$$

Combining the above results gives the *INL* and *DNL* for the case where the *MSBs* use the charge scaling DAC and the *LSBs* use the voltage DAC. The result is,

$$\boxed{INL = 2^{N-1}\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)LSBs}$$ and

$$\boxed{DNL = \left(2^{N-1}\frac{\Delta C}{C} + \frac{\Delta R}{R}\right)\ LSBs}$$

Problem 10.3-14

Below are the formulas for *INL* and *DNL* for the case where the MSB and LSB arrays of an digital-to-analog converter are either voltage or charge scaling. $n = m+k$, where m is the number of bits of the MSB array and k is the number of bits of the LSB array and n is the total number of bits. Find the values of n, m, and k and tell what type of DAC (voltage MSB and charge LSB or charge MSB and voltage LSB) if $\Delta R/R = 1\%$ and $\Delta C/C = 0.1\%$ and both the *INL* and *DNL* of the DAC combination should each be 1*LSB* or less.

DAC Combination	*INL* (LSBs)	*DNL* (LSBs)
MSB voltage (m-bits) LSB charge (k-bits)	$2^{n-1}\frac{\Delta R}{R} + 2^{k-1}\frac{\Delta C}{C}$	$2^{k}\frac{\Delta R}{R} + (2^{k}-1)\frac{\Delta C}{C}$
MSB charge (m-bits) LSB voltage (k-bits)	$2^{m-1}\frac{\Delta R}{R} + 2^{n-1}\frac{\Delta C}{C}$	$\frac{\Delta R}{R} + (2^{n}-1)\frac{\Delta C}{C}$

Solution

MSB voltage, *LSB* charge:

$$1 \geq 2^{n-1}\left(\frac{1}{100}\right) + 2^{k-1}\left(\frac{1}{1000}\right) \quad \Rightarrow \quad 1000 \geq 10{\cdot}2^{n-1} + 2^{k-1}$$

$$1 \geq 2^{k}\left(\frac{1}{100}\right) + (2^{k}-1)\left(\frac{1}{1000}\right) \quad \Rightarrow \quad 1000 \geq 10{\cdot}2^{k} + 2^{k}-1 \;\Rightarrow\; \frac{999}{11} = 90.8 \geq 2^{k} \;\Rightarrow\; k = 6$$

Substituting this k into the first equation gives

$$\frac{1000 - 32}{10} = 96.8 \geq 2^{n-1} \quad \Rightarrow \quad n = 7 \text{ which gives } m = 1 \text{ and } k = 6.$$

MSB charge, *LSB* voltage:

$$1 \geq 2^{m-1}\left(\frac{1}{100}\right) + 2^{n-1}\left(\frac{1}{1000}\right) \quad \Rightarrow \quad 1000 \geq 5{\cdot}2^{m} + 2^{n-1}$$

$$1 \geq \frac{1}{100} + (2^{n}-1)\left(\frac{1}{1000}\right) \quad \Rightarrow \quad 1000 \geq 10 + 2^{n}-1 \;\Rightarrow\; 991 \geq 2^{n} \;\Rightarrow\; n = 9$$

Substituting this n into the first equation gives

$$\frac{1000 - 256}{5} = 148.8 \geq 2^{m} \quad \Rightarrow \quad m = 7 \text{ which gives } n = 9 \text{ and } k = 2.$$

Therefore, the DAC combination where the *MSBs* are charge scaling and the *LSBs* are voltage scaling gives the most bits when both *INL* and *DNL* are 1*LSB*. The number of bits is $n = 9$ with $m = 7$ bits of charge scaling for the *MSB* DAC and $k = 2$ bits of voltage scaling for the *LSB* DAC.

Problem 10.3-15

The circuit shown is a double-decoder D/A converter. Find an expression for v_X in terms of V_1, V_2, and V_{REF} when the ϕ_2 switches are closed. If A=1, B=0, C=1, and D=1, will the comparator output be high or low if $V_{analog} = 0.8V_{REF}$?

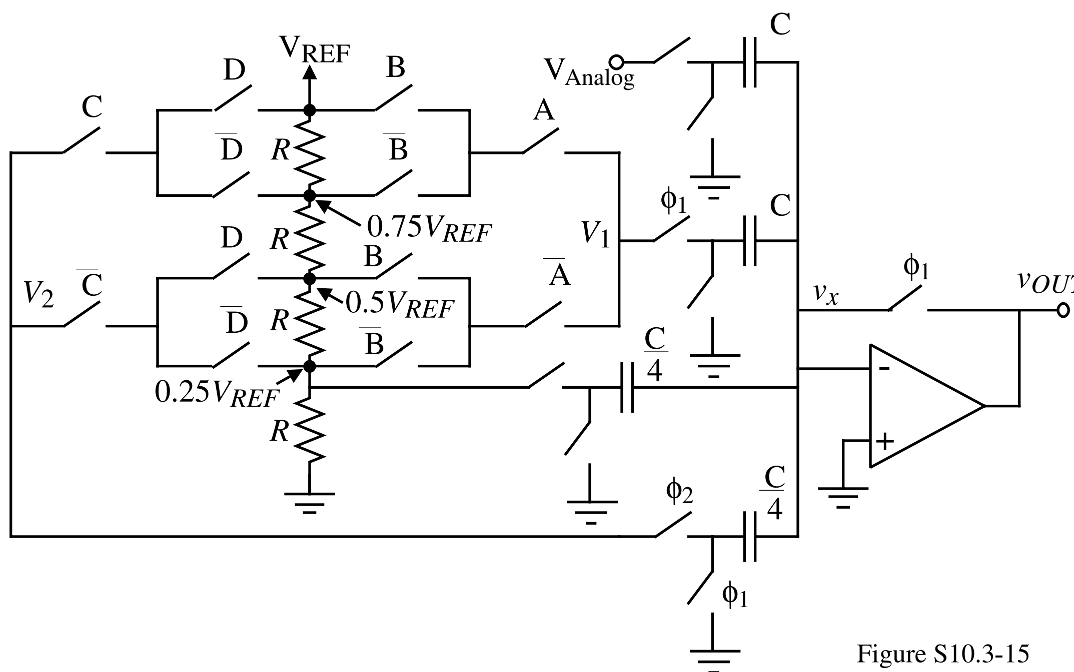


Figure S10.3-15

Solution

At ϕ_2 we have the following equivalent circuit:

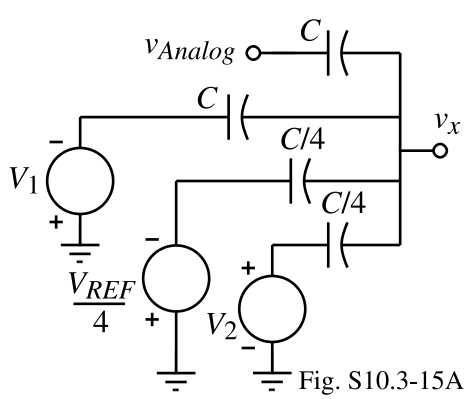


Fig. S10.3-15A

Summing the currents to zero gives,

$$sC(v_{Analog}-v_x) + sC(-V_1-v_x) + \frac{sC}{4}\left(-\frac{V_{REF}}{4} - v_x\right) + \frac{sC}{4}(V_2 - v_x) = 0$$

or

$$sCv_{Analog} - CV_1 - C\frac{V_{REF}}{16} + C\frac{V_2}{4} = v_x\left(C+C+\frac{C}{4}+\frac{C}{4}\right)$$

$$\therefore \quad \boxed{v_x = \frac{C}{C_{total}}\left(v_{Analog} - V_1 + \frac{V_2}{4} - \frac{V_{REF}}{16}\right)} = \frac{2}{5}v_{Analog} - \frac{2}{5}V_1 + \frac{V_2}{10} - \frac{V_{REF}}{16}$$

For ABCD = 1011 $\rightarrow$ $v_{Analog} - V_1 + \dfrac{V_2}{4} - \dfrac{V_{REF}}{16} = \dfrac{12V_{REF}}{16} - \dfrac{12V_{REF}}{16} + \dfrac{4V_{REF}}{16} - \dfrac{V_{REF}}{16} > 0$

Since $v_x > 0$, the comparator output will be low.

Problem 10.3-16

A 4-bit, analog-to-digital converter is shown. Clearly explain the operation of this converter for a complete conversion in a clock period-by-clock period manner, where ϕ_1 and ϕ_2 are non-overlapping clocks generated from the square ware with a period of T (i.e. ϕ_1 occurs in 0 to T/2 and ϕ_2 in T/2 to T, etc.). What will cause errors in the operation of this analog-to-digital converter?

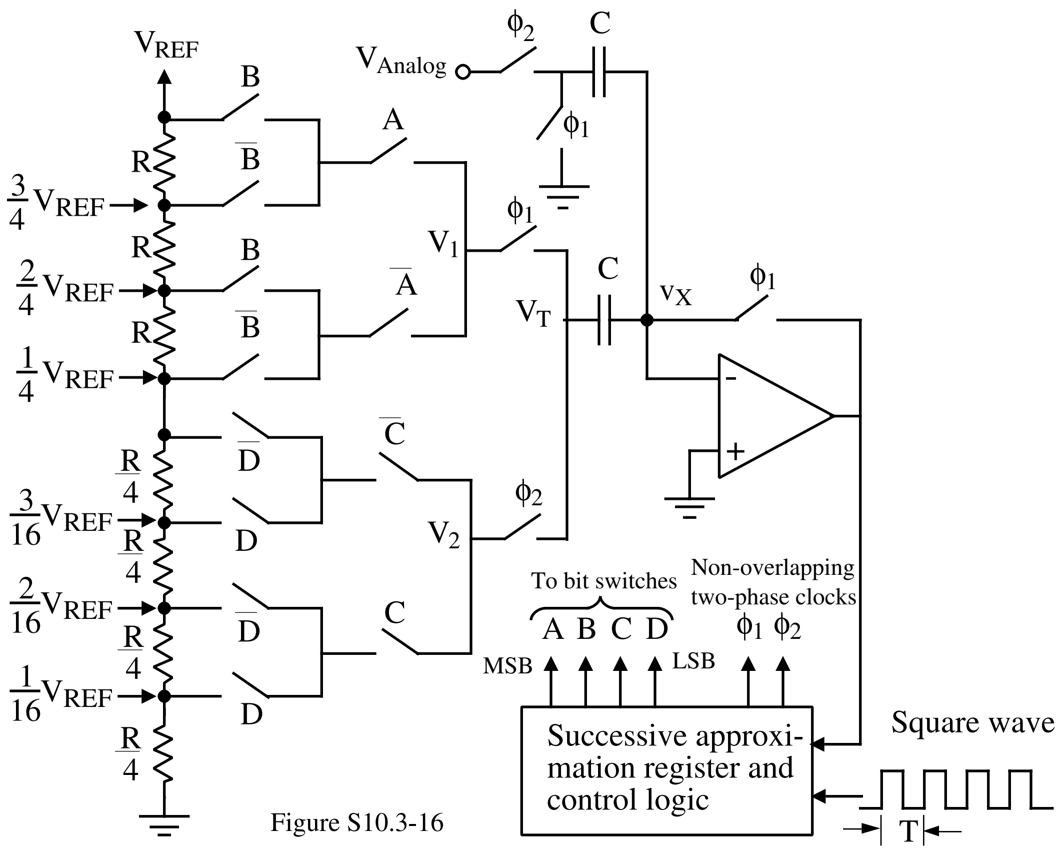


Figure S10.3-16

Solution

Consider the operation during a ϕ_1-ϕ_2 cycle. The voltage v_x can be written in general as,

$$v_x = \frac{V_{analog}}{2} - \frac{V_1}{2} + \frac{V_2}{2} = \frac{1}{2}(V_{analog} - V_1 + V_2)$$

The operation of the ADC will proceed as follows:

1.) Period 1 ($0 \leq t \leq T$):

SAR closes switches A, $\overline{B}$, $\overline{C}$, and $\overline{D}$ (1000) to get

$$v_x = \frac{1}{2}\left(V_{analog} - \frac{3}{8}V_{REF} + \frac{1}{8}V_{REF}\right) = \frac{1}{2}\left(V_{analog} - \frac{1}{2}V_{REF}\right)$$

If $v_x > 0$, then A = 1. Otherwise, A = 0 ($\overline{A}$ =1).

Problem 10.3-16 – Continued

2.) Period 2 ($T \le t \le 2T$):

a.) A = 1

SAR closes switches A,B , $\overline{\text{C}}$, and $\overline{\text{D}}$ (1100) to get

$$v_x = \frac{1}{2}\left(V_{analog} - V_{REF} + \frac{1}{4}V_{REF}\right) = \frac{1}{2}\left(V_{analog} - \frac{3}{4}V_{REF}\right)$$

b.) $\overline{\text{A}}$ = 1

SAR closes switches $\overline{\text{A}}$,B , $\overline{\text{C}}$, and $\overline{\text{D}}$ (0100) to get

$$v_x = \frac{1}{2}\left(V_{analog} - \frac{1}{2}V_{REF} + \frac{1}{4}V_{REF}\right) = \frac{1}{2}\left(V_{analog} - \frac{1}{4}V_{REF}\right)$$

If $v_x > 0$, the B = 1 (X100). Otherwise, B = 0 ($\overline{\text{B}}$ =1) (X000).

3.) Period 3 ($2T \le t \le 3T$):

At this point, V_1, will not change since A and B are known.

The SAR closes the appropriate A and B switches and C and $\overline{\text{D}}$ (XX10) to get

$$v_x = \frac{1}{2}\left(V_{analog} - V_1 + \frac{2}{16}V_{REF}\right) = \frac{1}{2}\left(V_{analog} - V_1 + \frac{1}{8}V_{REF}\right)$$

If $v_x > 0$, then C = 1 (XX10). Otherwise, C = 0 ($\overline{\text{C}}$ = 1) (XX00).

4.) Period 4 ($3T \le t \le 4T$):

a.) D = 1

SAR closes switches appropriate Aand B switcheds and C, and D (XX11) to get

$$v_x = \frac{1}{2}\left(V_{analog} - V_1 + \frac{1}{16}V_{REF}\right)$$

b.) $\overline{\text{D}}$ = 1

SAR closes switches appropriate Aand B switcheds and C, and $\overline{\text{D}}$ (XX10) to get

$$v_x = \frac{1}{2}\left(V_{analog} - V_1 + \frac{3}{16}V_{REF}\right)$$

If $v_x > 0$, then D = 1 (XXX1). Otherwise, D = 0 ($\overline{\text{D}}$ = 1) (XXX0).

Sources of error:

1.) Op amp/comparator – gain, GB, SR, settling time (offset not a problem).
2.) Resistor and capacitor matching.
3.) Switch resistance and feedthrough.
4.) Note parasitic capacitances.
5.) Reference accuracy and stability.

Problem 10.4-01

What is v_{C1} in Fig. 10.4-1 after the following sequence of switch closures? S_4, S_3, S_1, S_2, S_1, S_3, S_1, S_2, and S_1?

Solution

The plots for v_{C1}/V_{REF} and v_{C2}/V_{REF} are given below.

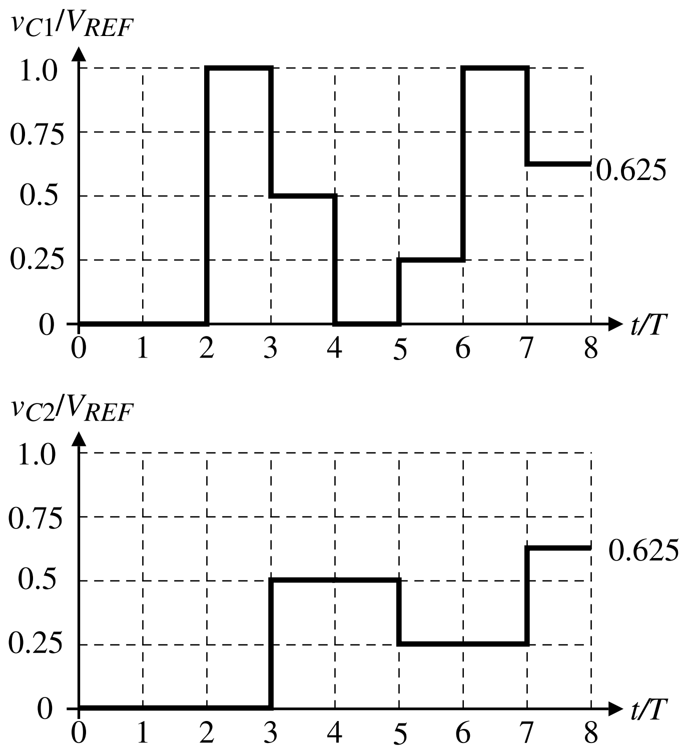


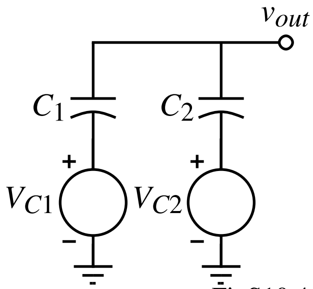
Fig. S10.4-01

Problem 10.4-02

Repeat the above problem if $C_1 = 1.05C_2$.

Solution

In the sharing phase, we have the following equivalent circuit:



FigS10.4-02

$$v_{out}(i) = V_{C1}\frac{C_1}{C_1+C_2} + V_{C2}\frac{C_2}{C_1+C_2}$$

$$= \frac{1.05}{2.05}V_{C1} + \frac{1}{2.05}V_{C2}$$

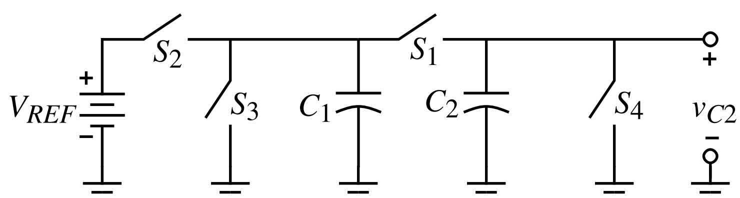
$$= 0.5122V_{C1} + 0.4878V_{C2}$$

Sharing Phase (i)	$V_{C1}(i)/V_{REF}$	$V_{C2}(i)/V_{REF}$	$V_{out}(i)/V_{REF}$
1	0	0	0
2	1	0	0.5112
3	0	0.5122	0.2498
4	1	0.2498	0.6340

Thus, at the end of the conversion, the output voltage is $0.6340V_{REF}$ rather than the ideal value of $0.6250V_{REF}$.

Problem 10.4-03

For the serial DAC shown, every time the switch S_2 opens, it causes the voltage on C_1 to be decreased by 10%. How many bits can this DAC convert before an error occurs assuming worst case conditions and letting V_{REF} = 1V? The analog output is taken across C_2.



F97E1P4

Solution

Worst case is for all 1's.

i	V_{C1}(ideal)	V_{C1}(act.)	V_{C2}(ideal)	V_{C2}(act.)	$\frac{V_{REF}}{2^{i+1}}$	$\lvert V_{C2}$(ideal) - V_{C2}(act.)$\rvert$	OK?
1	1	0.9	0.5	0.45	0.25	0.050	Yes
2	1	0.9	0.75	0.675	0.125	0.0750	Yes
3	1	0.9	0.875	0.7875	0.0625	0.0875	No

Error occurs at the third bit.

Note that the approach is to find the ideal value of V_{C2} at the ith bit and then find the range that V_{C2} could have which is $\pm V_{REF}/2^{i+1}$ and still not have an error. If the difference between the magnitude of the ideal value and actual value of V_{C2} exceeds $V_{REF}/2^{i+1}$ then an error will occur.

Problem 10.4-04

For the serial, pipeline DAC of Fig. 10.4-3 find the ideal analog output voltage if V_{REF} = 1V and the input is 10100110 from the *MSB* to the *LSB*. If the attenuation factors of 0.5 become 0.55, what is the analog output for this case?

Solution

Ignoring the delay terms,the output of Fig. 10.4-3 can be written as,

$$\frac{V_{out}}{V_{REF}} = b_0 + \frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16} + \frac{b_5}{32} + \frac{b_6}{64} + \frac{b_7}{128}$$

For 10100110 we get,

$$\frac{V_{out}}{V_{REF}}(\text{ideal}) = 1 - \frac{1}{2} + \frac{1}{4} - \frac{1}{8} - \frac{1}{16} + \frac{1}{32} + \frac{1}{64} - \frac{1}{128}$$

$$= \frac{128}{128} - \frac{64}{128} + \frac{32}{128} - \frac{16}{128} - \frac{8}{128} + \frac{4}{128} + \frac{2}{128} - \frac{1}{128} = \frac{77}{128} = 0.60156$$

If the attenuation factor is k = 0.55, the output can be re-expressed as,

$$\frac{V_{out}}{V_{REF}}(\text{actual}) = kb_0 + k^2b_1 + k^3b_2 + k^4b_3 + k^5b_4 + k^6b_5 + k^7b_6 + 8^8b_7$$

$$= +0.55 - 0.3025 + 0.1664 - 0.0915 - 0.0503 + 0.0277 + 0.0152 - 0.00837$$

$$= 0.3066$$

Problem 10.4-05

Give an implementation of the pipeline DAC of Fig. 10.4-3 using two-phase, switched capacitor circuits. Give a complete schematic with the capacitor ratios and switch phasing identified.

Solution

All of the stages can be represented by the following block diagram.

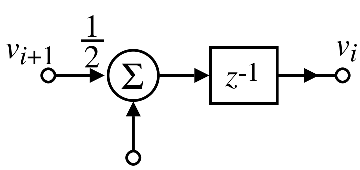


Fig. S10.4-05A

$$v_i = (0.5v_{i+1} \pm b_iV_{REF})z^{-1}$$

which is a summing sample and hold with weighted inputs. A possible switched-capacitor realization of the *i*-th stage (and all stages) is shown below.

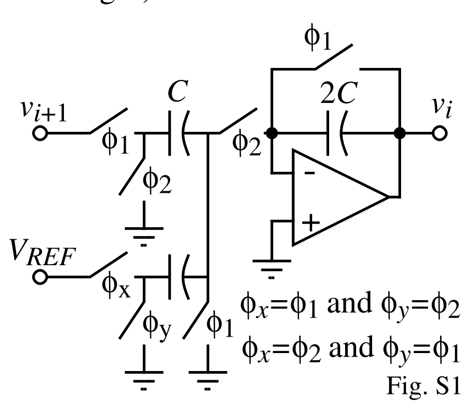
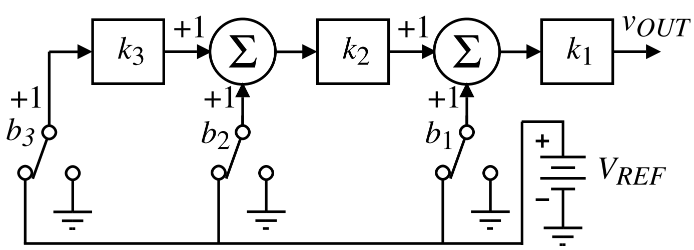
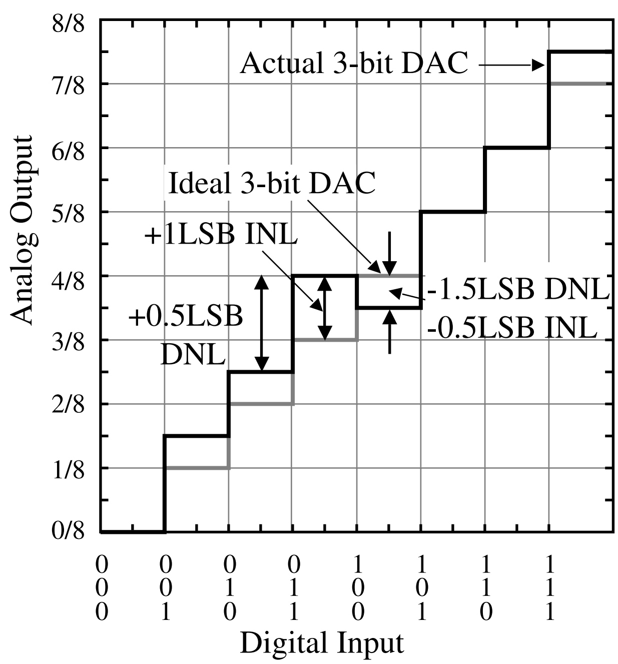


Fig. S10.4-5B

Problem 10.4-06

A pipeline DAC is shown. If k_1 = 7/16, k_2 = 5/7, and k_3 = 3/5 write an expression for v_{OUT} in terms of b_i (i = 1, 2, 3) and V_{REF}. Plot the input-output characteristic on the curve shown below and find the largest ±INL and largest ±DNL. Is the DAC monotonic or not?





Digital Word	v_{OUT}
000	0/16
001	3/16
010	5/16
011	8/16
100	7/16
101	10/16
110	12/16
111	15/16

Solution

The output can be written as

$$v_{OUT} = k_1(b_1+k_2(b_2+k_3b_3))V_{REF} = [k_1b_1 + k_1k_2b_2 + k_1k_2k_3b_3]V_{REF}$$

Using the values given gives

$$v_{OUT} = \left[\left(\frac{7}{16}\right)b_1 + \left(\frac{7}{16}\right)\left(\frac{5}{7}\right)b_2 + \left(\frac{7}{16}\right)\left(\frac{5}{7}\right)\left(\frac{3}{5}\right)b_3\right]V_{REF} = \left[\frac{7}{16}b_1 + \frac{5}{16}b_2 + \frac{3}{16}b_3\right]V_{\mathrm{REF}}$$

The values for v_{OUT} for this DAC are shown beside the plot and have been plotted on the output-input characteristic curve. A summary of the performance is given below.

$$\boxed{\text{INL: +1LSB, -0.5LSB} \qquad \text{DNL: +0.5LSB, -1.5LSB} \quad \text{DAC is nonmonotonic}}$$

Problem 10.4-07

A pipeline digital-analog converter is shown. When b_i is 1, the switch is connected to V_{REF}, otherwise it is connected to ground. Two of the 0.5 gains on the summing junctions are in error. Carefully sketch the resulting digital-analog transfer characteristic on the plot on the next page and identify the INL with respect to the infinite resolution characteristic shown and DNL. The INL and DNL should be measured on the analog axis.

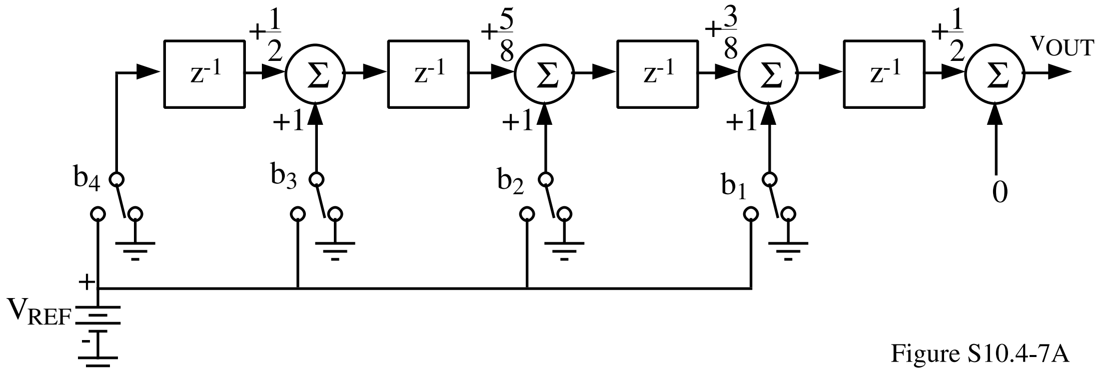


Figure S10.4-7A

Solution

Ignoring the delay terms, we can write the output voltage as,

$$\frac{v_{OUT}}{V_{REF}} = \left(\left(\left(\frac{b_4}{2} + b_3\right)\frac{5}{8} + b_2\right)\frac{3}{8} + b_1\right)\frac{1}{2} = \frac{1}{2}b_1 + \frac{3}{16}b_2 + \frac{30}{256}b_3 + \frac{15}{256}b_3$$

$$= \frac{128}{256}b_1 + \frac{48}{256}b_2 + \frac{30}{256}b_3 + \frac{15}{256}b_3$$

The performance is summarized in the table below (a plot can be made from the table).

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.05859	0.00000	-0.06250	0.00000	-0.06250
0	0	1	0	0.12500	0.11719	0.00000	-0.06250	0.00000	-0.12500
0	0	1	1	0.18750	0.17578	0.00000	-0.06250	0.00000	-0.18750
0	1	0	0	0.25000	0.18750	0.00000	-0.81250	0.00000	-1.00000
0	1	0	1	0.31250	0.24609	0.00000	-0.06250	0.00000	-1.06250
0	1	1	0	0.37500	0.30469	0.00000	-0.06250	0.00000	-1.12500
0	1	1	1	0.43750	0.36328	0.00000	-0.06250	0.00000	-1.18750
1	0	0	0	0.50000	0.50000	0.00000	1.18750	0.00000	0.00000
1	0	0	1	0.56250	0.55859	0.00000	-0.06250	0.00000	-0.06250
1	0	1	0	0.62500	0.61719	0.00000	-0.06250	0.00000	-0.12500
1	0	1	1	0.68750	0.67578	0.00000	-0.06250	0.00000	-0.18750
1	1	0	0	0.75000	0.68750	0.00000	-0.81250	0.00000	-1.00000
1	1	0	1	0.81250	0.74609	0.00000	-0.06250	0.00000	-1.06250
1	1	1	0	0.87500	0.80469	0.00000	-0.06250	0.00000	-1.12500
1	1	1	1	0.93750	0.86328	0.00000	-0.06250	0.00000	-1.18750

$\therefore$ $\underline{\underline{INL = +0\ LSBs,\ -1.1875 LSBs \text{ and } DNL = +1.1875 LSBs,\ -0.8125 LSBs}}$

Problem 10.4-08

Show how Eq. (10.4-2) can be derived from Eq. (10.4-1). Also show in the block diagram of Fig. 10.4-4 how the initial zeroing of the output can be accomplished.

Solution

Eq. (10.4-1) can be written as

$$V_{out} = \sum_{i=1}^{N} \frac{b_{i-1} z^{-i}}{2^{i-1}} = \sum_{i=1}^{N} \frac{b_{i-1} z^{-i}}{2^{i-1}} \frac{z}{z} = \frac{1}{z} \sum_{i=1}^{N} \frac{b_{i-1}}{2^{i-1} z^{i-1}} = \frac{1}{z} \sum_{i=1}^{N} \frac{b_{i-1}}{2^{i-1} z^{i-1}}$$

$$= \frac{1}{z} \sum_{i=0}^{N} \frac{b_i}{2^i z^i} = \frac{b_i}{z} \sum_{i=0}^{N} \frac{1}{2^i z^i}$$

where all b_i have assumed to be identical as stated in the text.

The summation can be recognized as a geometric series (assuming $N \rightarrow \infty$) to give

$$V_{out} = \frac{b_i}{z} \left[\frac{1}{1-\frac{1}{2z}} \right] = \frac{b_i z^{-1}}{1-0.5z^{-1}}$$

The output can initially be zeroed by adding a third switch to ground at the summing junction. The S/H will sample the 0V and produce $V_{out} = 0$.

Problem 10.4-09

Assume that the amplifier with a gain of 0.5 in Fig. 10.4-4 has a gain error of ΔA. What is the maximum value ΔA can be in Example 10.4-2 without causing the conversion to be in error?

Solution

Let the amplifier gain be A. Therefore, we can write the output in general as follows.

Bit from LSB to MSB	V_{out}
1	1
0	A-1
0	$A(A-1) + 1 = A^2 - A - 1$
1	$A[A(A-1) - 1] + 1 = A^3 - A^2 - A + 1$
1	$A\{A[A(A-1) - 1] + 1\} + 1 = A^4 - A^3 - A^2 + A + 1$

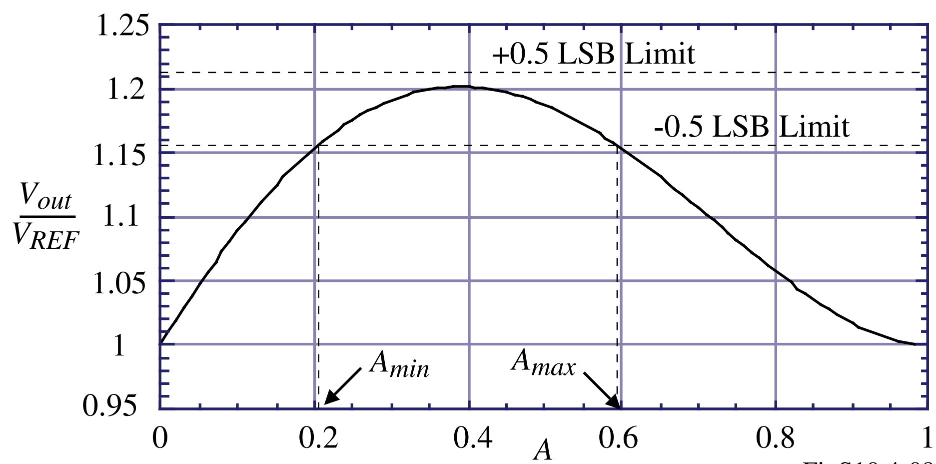
The ideal output is $V_{out} = \frac{19}{16} \pm 0.5LSB$ $\qquad LSB = \frac{2V_{REF}}{2^6} = \frac{V_{REF}}{2^5} = \frac{V_{REF}}{32}$

Assume V_{REF} = 1V, therefore

$$A^4 - A^3 - A^2 + A + 1 \le \frac{19}{16} \pm \frac{1}{32} = \frac{38}{32} \pm \frac{1}{32}$$

∴ The ideal output is 1.18750 and must be between 1.15625 and 1.21875.

Below is a plot of the output as a function of A.



FigS10.4-09

From this plot, we see that A must lie between 0.205 and 0.590 in order to avoid a ±0.5LSB error.

∴ $\boxed{0.205 \le A \le 0.590}$

Problem 10.4-10

Repeat Example 10.4-2 for the digital word 10101.

Solution

Let the amplifier gain be *A*. Therefore, we can write the output in general as follows.

Bit from LSB to MSB	V_{out}
1	1
0	A-1
1	$A(A\text{-}1) + 1 = A^2 - A + 1$
0	$A[A(A\text{-}1) + 1] - 1 = A^3 - A^2 + A - 1$
1	$A\{A[A(A\text{-}1) + 1] - 1\} + 1 = A^4 - A^3 + A^2 - A + 1$

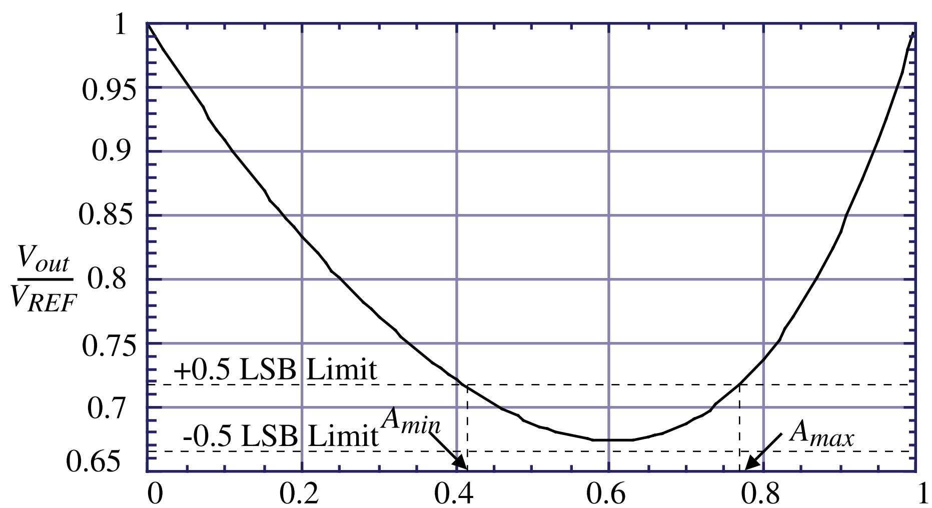
The ideal output is $V_{out} = \frac{11}{16} \pm 0.5LSB$ $\qquad LSB = \frac{2V_{REF}}{2^6} = \frac{V_{REF}}{2^5} = \frac{V_{REF}}{32}$

Assume V_{REF} = 1V, therefore

$$A^4 - A^3 - A^2 + A + 1 \le \frac{12}{16} \pm \frac{1}{32} = \frac{22}{32} \pm \frac{1}{32}$$

∴ The ideal output is 0.6875 and must be between 0.65625 and 0.71875.

Below is a plot of the output as a function of *A*.



FigS10.4-09

From this plot, we see that *A* must lie between 0.41 and 0.77 in order to avoid a ±0.5*LSB* error.

∴ $\boxed{0.41 \le A \le 0.77}$

Problem 10.4-11

Assume that the iterative algorithmic DAC of Fig. 10.4-4 is to convert the digital word 11001. If the gain of the 0.5 amplifier is 0.7, at which bit conversion is an error made?

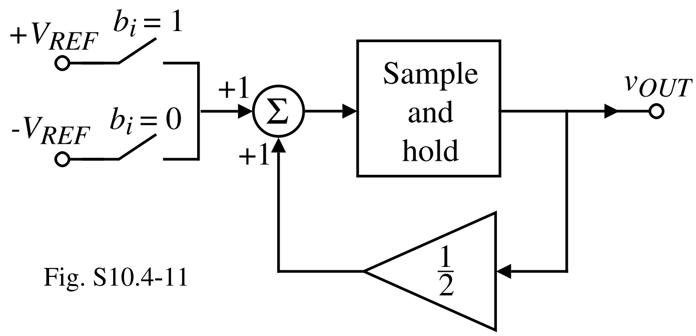


Fig. S10.4-11

Solution

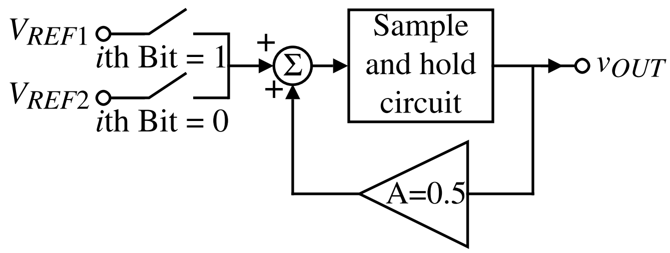
Conversion No.	Bit Converted	Ideal Result	Max. Ideal	Min. Ideal	Result for Gain = 0.7
1	1(LSB)	1	1.5	0.5	1 (OK)
2	0	-(1/2)	-0.25	-0.75	-0.30 (OK)
3	0	-(5/4)	-1.1250	-1.375	-1.210 (OK)
4	1	(3/8)	0.4375	0.3125	0.1530 (Error)
5	1 (MSB)	(19/16)	0.9062	0.8437	-

The max. and min. ideal are found by taking the ideal result and adding and substracting half of the ideal bit for that conversion number.

We note from the table that the error occurs in the 4th bit conversion.

Problem 10.4-12

An iterative, algorithmic DAC is shown in Fig. P10.4-12. Assume that the digital word to be converted is 10011. If $V_{REF1} = 0.9V_{REF}$ and $V_{REF2} = -0.8V_{REF}$, at which bit does an error occur in the conversion of the digital word to an analog output?



Solution

Ideally, the output of the *i*-th stage should be,

$$v_{OUT}(i) = 0.5\ v_{OUT}(i\text{-}1) \pm b_i V_{REF}$$

The *i*-th *LSB* is given as $\dfrac{V_{REF}}{2^{i-1}}$.

In this problem, the output of *i*-th stage is given as,

$$v_{OUT}(i) = 0.5\ v_{OUT}(i\text{-}1) + 0.9V_{REF} \quad \text{if } b_i = 1$$

and

$$v_{OUT}(i) = 0.5\ v_{OUT}(i\text{-}1) - 0.8V_{REF} \quad \text{if } b_i = 0$$

The performance is summarized in the following table where $v_{OUT}(i)$ is normalized to V_{REF}.

Conversion No.	0.5 *LSB*	Bit Converted	$v_{OUT}(i)$ Ideal	Max. Ideal $v_{OUT}(i)$	Min. Ideal $v_{OUT}(i)$	Actual $v_{OUT}(i)$
1	0.5	1	1	1.5	0.5	0.9
2	0.25	1	1.5	1.75	1.25	1.35
3	0.125	0	-0.25	-0.125	-0.375	-0.125
4	0.0625	0	-1.125	-1.0625	-1.1875	-0.8625
5	0.03125	1	0.4375	0.46875	0.40625	0.46875

An error occurs in the 4th bit conversion since it lies outside the maximum-minimum ideal $v_{OUT}(i)$. Note the 5th bit is okay.

Problem 10.5-01

Plot the transfer characteristic of a 3-bit ADC that has the largest possible differential nonlinearity when the integral nonlinearity is limited to $\pm 1LSB$. What is the maximum value of the differential nonlinearity for this case?)

Solution

A plot is given below showing the upper and lower limits for ±1 LSB INL. The dark line on the plot shows part of the ADC characteristics that illustrates that the maximum DNL is ±2 LSB.

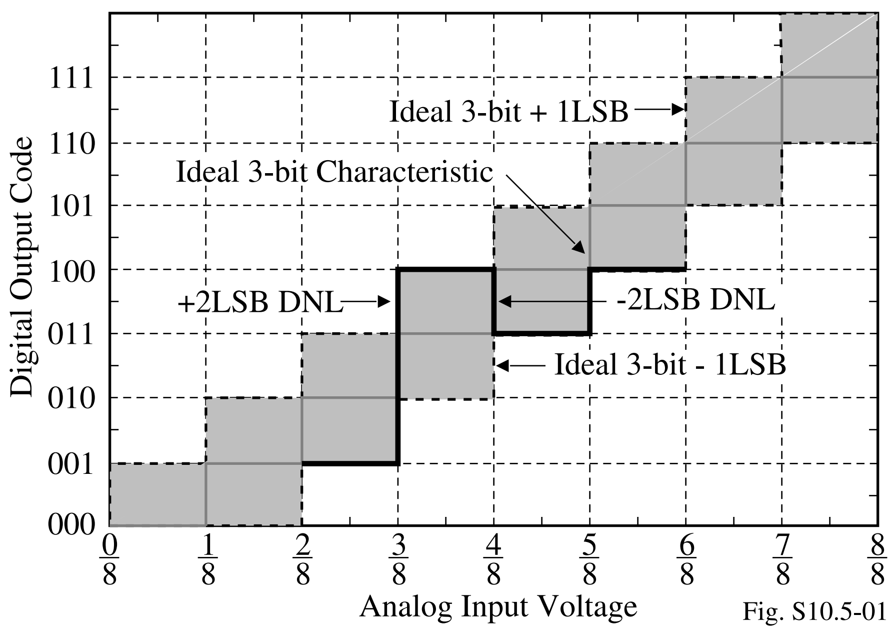


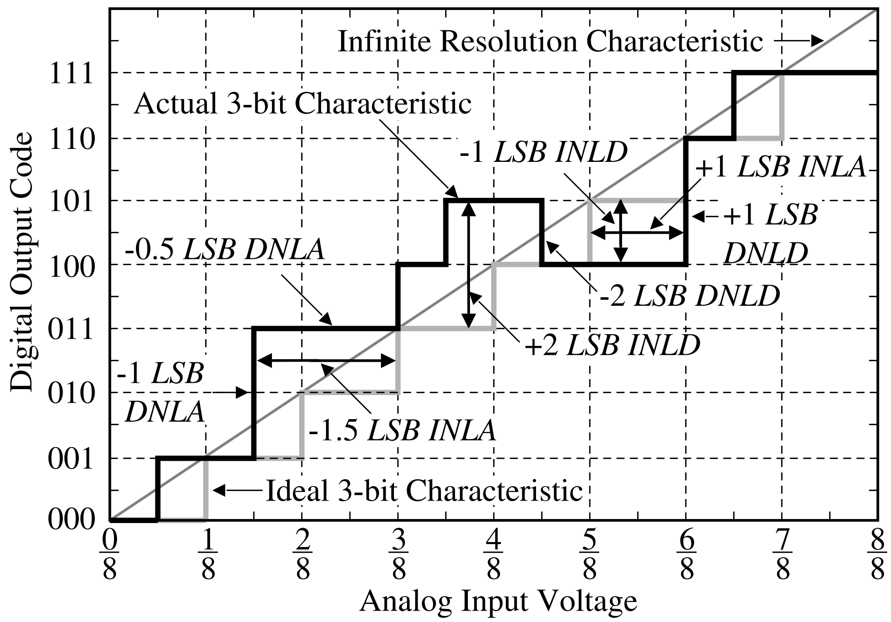
Fig. S10.5-01

Problem 10.5-2

(a.) Find the ±*INL* and ±*DNL* for the 3-bit ADC shown where the *INL* and *DNL* is referenced to the analog input voltage. (Use the terminology: *INLA* and *DNLA*.)

(b.) Find the ±*INL* and ±*DNL* for the 3-bit ADC shown where the *INL* and *DNL* is referenced to the digital output code. (Use the terminology: *INLD* and *DNLD*.)

(c.) Is this ADC monotonic or not?



Solutions

(a.) Refer to the characteristics above:

$+INLA = 1LSB$ $-INLA = -1.5LSB$

$+DNLA = +0.5LSB$ $-DNLA = -1LSB$

(b.) Refer to the characteristics above:

$+INLD = 2LSB$ $-INLD = -1LSB$

$+DNLD = +1LSB$ $-DNLD = -2LSB$

(c.) This ADC is not monotonic.

Problem 10.5-03

Assume that the step response of a sample-and-hold circuit is

$$v_{OUT}(t) = V_I(1 - e^{-tÆBW})$$

where V_I is the magnitude of the input step to the sample-and-hold and BW is the bandwidth of the sample-and-hold circuit in radians/sec. and is equal to 2πMradians/sec. Assume a worst case analysis and find the maximum number of bits this sample-and-hold circuit can resolve if the sampling frequency is 1MHz. (Assume that the sample-and-hold circuit has the entire period to acquire the sample.)

Solution

To avoid an error, the value of $v_{OUT}(t)$ should be within ±0.5*LSB* of V_I. Since v_{OUT} is always less than V_I let us state the requirements as

$$V_I - v_{OUT}(T) \le \frac{V_{REF}}{2^{N+1}}$$

$$\therefore\ V_I - V_I(1-e^{-T\cdot BW}) \le \frac{V_{REF}}{2^{N+1}} \rightarrow V_I e^{-T\cdot BW} \le \frac{V_{REF}}{2^{N+1}} \rightarrow 2^{N+1} \le \frac{V_I}{V_{REF}} e^{T\cdot BW}$$

The worst case value is when $V_I = V_{REF}$. Thus,

$$2^{N+1} \le e^{2\pi} = 535.49 \quad \rightarrow \quad 2^N \le \frac{535.49}{2} = 267.74$$

$$\therefore\ \boxed{N \ = \ 8}$$

Problem 10.5-04

If the aperture jitter of the clock in an ADC is 200ps and the input signal is a 1MHz sinusoid with a peak-to-peak value of V_{REF}, what is the number of bits that this ADC can resolve?

Solution

Eq. (10.8-1) gives $\Delta t \le \frac{V_{REF}}{2^{N+1}} \frac{2}{2\pi f V_{REF}} = \frac{1}{2^{N+1}\pi f} = 200\text{ps}$

$$2^N = \frac{1}{2\cdot 200\text{ps}\cdot \pi\text{MHz}} = \frac{10^6}{400\pi} = 756$$

$$ln(2^N) = ln(756) \quad \rightarrow \quad N = \frac{ln(756)}{ln(2)} = 9.63$$

$\therefore\ \underline{\underline{N = 9\text{bits}}}$

Problem 10.6-01

What is the conversion time in clock periods if the input to Fig. 10.6-2 is 0.25 V_{REF}? Repeat if $v_{in}^* = 0.7V_{REF}$.

Solution

$v_{in}^* = 0.25V_{REF}$:

$$N_{out} = N_{REF} \text{x} 0.25 = 0.25N_{REF}$$

$\therefore$ Clock periods = $N_{REF} + 0.25N_{REF} = \underline{\underline{1.25N_{REF}}}$

$v_{in}^* = 0.7V_{REF}$:

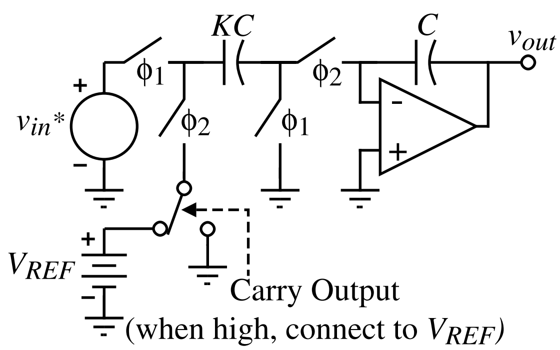
$$N_{out} = N_{REF} \text{x} 0.7 = 0.7N_{REF}$$

$\therefore$ Clock periods = $N_{REF} + 0.7N_{REF} = \underline{\underline{1.7N_{REF}}}$

Problem 10.6-02

Give a switched capacitor implementation of the positive integrator and the connection of the input and reference voltage to the integrator via switches 1 and 2 using a two-phase clock.

Solution



FS10.6-02

From Chapter 9, it can be shown that,

$$v_{out}(t) \approx K\int v_{in}^* \, dt \;\; \text{or} \; -K\int V_{REF} \, dt$$

depending on the carrier output.

Problem 10.7-01

If the sampled, analog input applied to an 8-bit successive-approximation converter is $0.7V_{REF}$, find the output digital word.

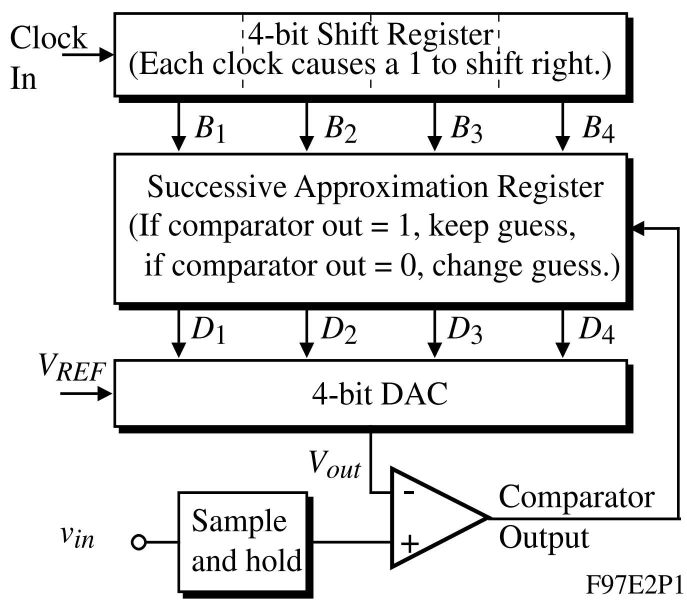
Solution

Bit	Trial Digital Word $b_0b_1b_2b_3b_4b_5b_6b_7$	$DV_{REF} = \left(\frac{b_0}{2}+\frac{b_1}{4}+\frac{b_2}{8}+\frac{b_3}{16}+\frac{b_4}{32}+\frac{b_5}{64}+\frac{b_6}{128}+\frac{b_7}{256}\right)V_{REF}$	$0.7V_{REF} > DV_{REF}$?	Decoded Bit
1	1 0 0 0 0 0 0 0	$0.5V_{REF}$	Yes	1
2	1 1 0 0 0 0 0 0	$0.75V_{REF}$	No	0
3	1 0 1 0 0 0 0 0	$0.625V_{REF}$	Yes	1
4	1 0 1 1 0 0 0 0	$0.6875V_{REF}$	Yes	1
5	1 0 1 1 1 0 0 0	$0.71875V_{REF}$	No	0
6	1 0 1 1 0 1 0 0	$0.703125V_{REF}$	No	0
7	1 0 1 1 0 0 1 0	$0.6953125V_{REF}$	Yes	1
8	1 0 1 1 0 0 1 1	$0.69921875V_{REF}$	Yes	1

The digital word is 1 0 1 1 0 0 1 1

Problem 10.7-02

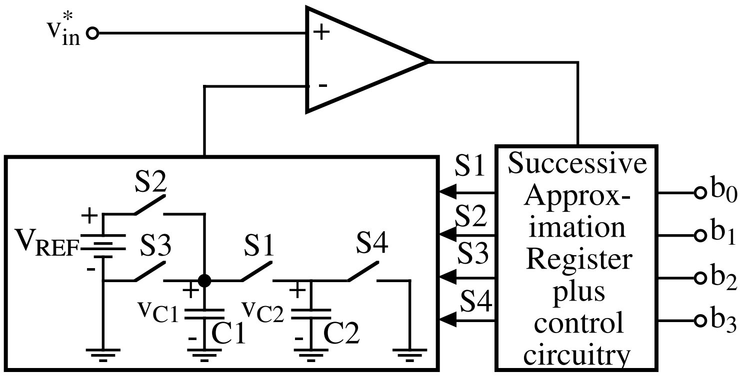
A 4-bit, successive approximation ADC is shown. Assume that V_{REF} = 5V. Fill in the table below when v_{in} = 3V.



Clock Period	$B_1B_2B_3B_4$	Guessed $D_1D_2D_3D_4$	V_{out}	Comparator Output	Actual $D_1D_2D_3D_4$
1	1 0 0 0	1 0 0 0	2.5V	1	1 0 0 0
2	0 1 0 0	1 1 0 0	3.75V	0	1 0 0 0
3	0 0 1 0	1 0 1 0	3.125V	0	1 0 0 0
4	0 0 0 1	1 0 0 1	2.8125V	1	1 0 0 1

Problem 10.7-03

For the successive approximation ADC shown in Fig. 10.7-7, sketch the voltage across capacitor C_1 (v_{C1}) and C_2 (v_{C2}) of Fig. 10.4-1 if the sampled analog input voltage is $0.6V_{REF}$. Assume that $S2$ and $S3$ closes in one clock period and $S1$ closes in the following clock period. Also, assume that one clock period exists between each successive iteration. What is the digital word out?



Actual digital word is 1001.

i	Guess	v_{Guess}	Actual
0	1	0.5	1
1	11	0.75	1.0
2	101	0.625	100
3	1001	0.5625	1001

Solution

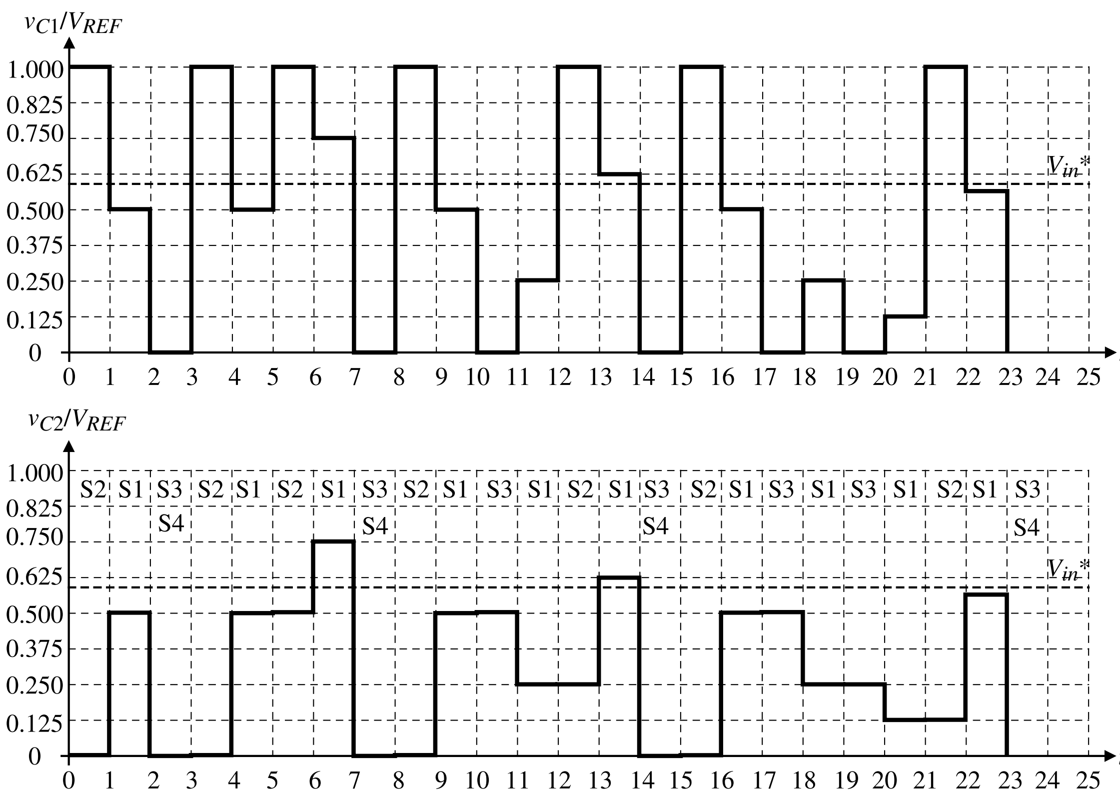


Fig. 10.7-03

Problem 10.7-04

Assume that the input of Example 10.7-1 is $0.8V_{\mathrm{REF}}$ and find the digital output word to 6 bits.

Solution

b_0: $V_{in}(0) = 0.8V_{REF}$ $\rightarrow$ $b_0 = 1$

b_1: $V_{in}(1) = 2(0.8V_{REF}) - V_{REF} = +0.6V_{REF}$ $\rightarrow$ $b_1 = 1$

b_2: $V_{in}(2) = 2(0.6V_{REF}) - V_{REF} = +0.2V_{REF}$ $\rightarrow$ $b_2 = 1$

b_3: $V_{in}(3) = 2(0.2V_{REF}) - V_{REF} = -0.6V_{REF}$ $\rightarrow$ $b_3 = 0$

b_4: $V_{in}(4) = 2(-0.6V_{REF}) + V_{REF} = -0.2V_{REF}$ $\rightarrow$ $b_4 = 0$

b_5: $V_{in}(5) = 2(-0.2V_{REF}) + V_{REF} = +0.6V_{REF}$ $\rightarrow$ $b_5 = 1$

$\therefore$ Digital output word = 1 1 1 0 0 1

Problem 10.7-05

Assume that the input of Example 10.7-1 is $0.3215V_{\mathrm{REF}}$ and find the digital output word to 8 bits.

Solution

b_0: $V_{in}(0) = 0.3215V_{REF}$ $\rightarrow$ $b_0 = 1$

b_1: $V_{in}(1) = 2(0.3125V_{REF}) - V_{REF} = -0.357V_{REF}$ $\rightarrow$ $b_1 = 0$

b_2: $V_{in}(2) = 2(-0.357V_{REF}) + V_{REF} = +0.286V_{REF}$ $\rightarrow$ $b_2 = 1$

b_3: $V_{in}(3) = 2(0.286V_{REF}) - V_{REF} = -0.428V_{REF}$ $\rightarrow$ $b_3 = 0$

b_4: $V_{in}(4) = 2(-0.428V_{REF}) + V_{REF} = +0.144V_{REF}$ $\rightarrow$ $b_4 = 1$

b_5: $V_{in}(5) = 2(0.144V_{REF}) - V_{REF} = -0.712V_{REF}$ $\rightarrow$ $b_5 = 0$

b_6: $V_{in}(6) = 2(-0.712V_{REF}) + V_{REF} = -0.424V_{REF}$ $\rightarrow$ $b_4 = 0$

b_7: $V_{in}(7) = 2(-0.424V_{REF}) + V_{REF} = +0.152V_{REF}$ $\rightarrow$ $b_4 = 1$

$\therefore$ Digital output word = 1 0 1 0 1 0 0 1

Problem 10.7-06

Repeat Example 10.7-1 for 8 bits if the gain of two amplifiers actually have a gain of 2.1.

Solution

$v_{in}^* = \frac{1.50}{5.00} V_{REF} = 0.3V_{REF}$

b_0: $V_{in}(0) = 0.3V_{REF}$ $\rightarrow$ $b_0 = 1$

b_1: $V_{in}(1) = 2.1(0.3V_{REF}) - V_{REF} = -0.37V_{REF}$ $\rightarrow$ $b_1 = 0$

b_2: $V_{in}(2) = 2.1(-0.37V_{REF}) + V_{REF} = +0.223V_{REF}$ $\rightarrow$ $b_2 = 1$

b_3: $V_{in}(3) = 2.1(+0.223V_{REF}) - V_{REF} = -0.5317V_{REF}$ $\rightarrow$ $b_3 = 0$

b_4: $V_{in}(4) = 2.1(-0.5317V_{REF}) + V_{REF} = -0.0634V_{REF}$ $\rightarrow$ $b_4 = 0$

b_5: $V_{in}(5) = 2.1(-0.0634V_{REF}) + V_{REF} = +0.86686V_{REF}$ $\rightarrow$ $b_5 = 1$

b_6: $V_{in}(6) = 2.1(+0.86686V_{REF}) - V_{REF} = +0.820406V_{REF}$ $\rightarrow$ $b_6 = 1$

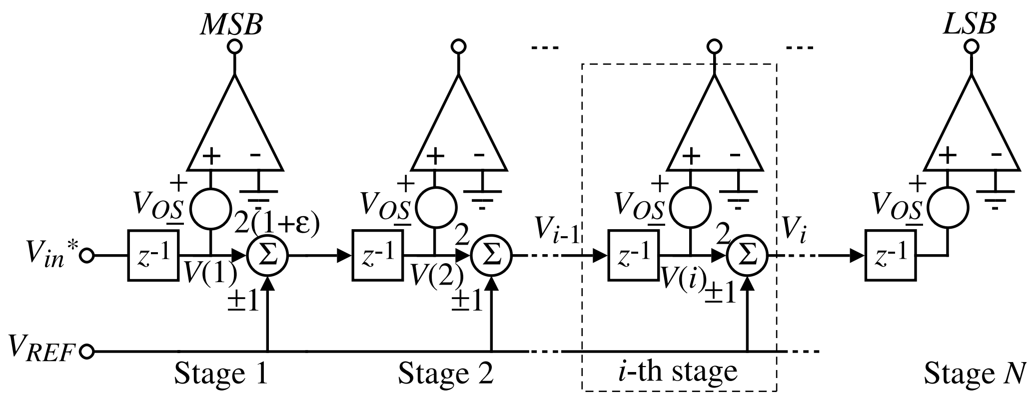
b_7: $V_{in}(7) = 2.1(+0.820406V_{REF}) - V_{REF} = +0.820406V_{REF}$ $\rightarrow$ $b_6 = 1$

The ideal digital word for Ex. 10.7-1 is 1 0 1 0 0 1 1 0

We see that the amplifier with a gain of 2.1 causes an error in the 8th bit.

Problem 10.7-07

Assume that $V_{in}^* = 0.7V_{REF}$ is applied to the pipeline algorithmic ADC of Fig. 10.7-9 with 5 stages. All elements of the converter are ideal except for the multiplier of 2 of the first stage, given as 2(1+ε). (a.) What is the smallest magnitude of ε that causes an error, assuming that the comparator offsets, V_{OS} , are all zero? (b.) Next, assume that the comparator offsets are all equal and nonzero. What is the smallest magnitude of the comparator offsets, V_{OS}, that causes an error, assuming that ε is zero?



Solution

Use the following table to solve this problem.

Stage No.	Bit Converted ($MSB \to LSB$)	$V(i)$	$V(i)$ with $\varepsilon(\iota)\neq 0$	$\varepsilon(i)$*	$V(i)$ with V_{OS}=0
1	1	0.7	0.7	-	0.7
2	1	0.4	$1.4(1+\varepsilon)-1 = 0.4+1.4\varepsilon$	-0.286	0.4
3	0	-0.2	$2(0.4+1.4\varepsilon)-1 = -0.2+2.8\varepsilon$	0.0714	-0.2
4	1	0.6	$2(-0.2+2.8\varepsilon)+1 = 0.6+5.6\varepsilon$	-0.107	0.6
5	1	0.2	$2(0.6+5.6\varepsilon)-1 = 0.2+11.2\varepsilon$	-0.0178	0.2

*$\varepsilon(i)$ is calculated by setting $V(i)$ with $\varepsilon \neq 0$ to zero.

From the above table we get the following results:

∴ From the fifth column, we see that the minimum $|\varepsilon|$ is 0.0178

(b.) The minimum V_{OS} = ±0.2V.

Problem 10.7-08

The input to a pipeline algorithmic ADC is 1.5V. If the ADC is ideal and V_{REF} = 5V, find the digital output word up to 8 bits in order of *MSB* to *LSB*. If V_{REF} = 5.2 and the input is still 1.5V, at what bit does an error occur?

Solution

The iterative relationship of an algorithmic ADC is,

$v(i+1) = 2v(i) - b_iV_{REF}$ where $b_i = 1$ if b_i = "1" and –1 if b_i = "0".

Ideal case (V_{REF}=5V):

i	$v(i)$	b_i	$2v(i) - b_iV_{REF}$
1	1.5	1	3 - 5 = -2
2	-2	0	-4 + 5 = 1
3	1	1	2 – 5 = -3
4	-3	0	-6 + 5 = -1
5	-1	0	-2 + 5 = 3
6	3	1	6 – 5 = 1
7	1	1	2 – 5 = -3
8	-3	0	

Actual case (V_{REF}=5.2V):

i	$v(i)$	b_i	$2v(i) - b_iV_{REF}$
1	1.5	1	3 – 5.2 = -2.2
2	-2.2	0	-4.4 + 5.2 = 0.8
3	0.8	1	1.6 – 5.2 = -3.6
4	-3.6	0	-7.2 + 5.2 = -2.0
5	-2.0	0	-4 + 5.2 = 1.2
6	1.2	1	2.4 – 5.2 = -2.8
7	-2.8	0	-5.6 + 5.2 = -0.6
8	-0.6	0	

The error occurs at the 7th bit.

Problem 10.7-09

If $V_{in}^* = 0.1V_{REF}$, find the digital output of an ideal, 4-stage, algorithmic pipeline ADC. Repeat if the comparators of each stage have a dc voltage offset of 0.1V.

Solution

Ideal:

Stage i	$V_{i\text{-}1}$	$V_{i\text{-}1} > 0$?	Bit i
1	0.1	Yes	1
2	0.1x2-1.0 = -0.8	No	0
3	-0.8x2+1.0 = -0.6	No	0
4	-0.6x2+1.0 = -0.2	No	0

Offset = 0.1V:

$$V_i = 2V_{i\text{-}1} - b_i\, V_{REF} + 0.1$$

Stage i	$V_{i\text{-}1}$	$V_{i\text{-}1} > 0$?	Bit i
1	0.1	Yes	1
2	0.1x2-1.0+0.1 = -0.7	No	0
3	-0.7x2+1.0+0.1 = -0.3	No	0
4	-0.3x2+1.0+0.1 = +0.5	Yes	1

An error will occur in the 4th bit when $V_{in}^* = 0.1V_{REF}$ and the offset voltage is 0.1V.

Problem 10.7-10

Continue Example 10.7-3 out to the 10th bit and find the equivalent analog voltage.

Solution

$v_{in}^* = 0.8V_{REF}$

$V_a(0) = 2(0.8V_{REF}) = 1.6V_{REF}$, $\quad 1.6\ V_{REF} > V_{REF} \quad \Rightarrow \quad b_0 = 1$

$V_a(1) = 2(1.6V_{REF} - V_{REF}) = 1.2V_{REF}$, $\quad 1.2\ V_{REF} > V_{REF} \quad \Rightarrow \quad b_1 = 1$

$V_a(2) = 2(1.2V_{REF} - V_{REF}) = 0.4V_{REF}$, $\quad 0.4\ V_{REF} < V_{REF} \quad \Rightarrow \quad b_2 = 0$

$V_a(3) = 2(0.4V_{REF} + 0) = 0.8V_{REF}$, $\quad 0.8\ V_{REF} < V_{REF} \quad \Rightarrow \quad b_3 = 0$

(Note the ADC repeats at every 4 bits)

$V_a(4) = 2(0.8V_{REF} + 0) = 1.6V_{REF}$, $\quad 1.6\ V_{REF} > V_{REF} \quad \Rightarrow \quad b_4 = 1$

$V_a(5) = 2(1.6V_{REF} - V_{REF}) = 1.2V_{REF}$, $\quad 1.2\ V_{REF} > V_{REF} \quad \Rightarrow \quad b_5 = 1$

$V_a(6) = 2(1.2V_{REF} - V_{REF}) = 0.4V_{REF}$, $\quad 0.4\ V_{REF} < V_{REF} \quad \Rightarrow \quad b_6 = 0$

$V_a(7) = 2(0.4V_{REF} + 0) = 0.8V_{REF}$, $\quad 0.8\ V_{REF} < V_{REF} \quad \Rightarrow \quad b_7 = 0$

Repeats again.

$\therefore$ The digital output word is 1 1 0 0 1 1 0 0 1 1 0 0 ……..

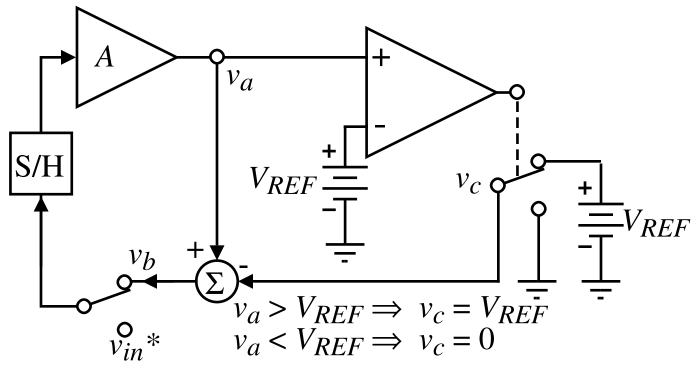
The analog equivalent is

$$V_{REF}\left(\frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{0}{16} + \frac{1}{32} + \frac{1}{64} + \frac{0}{128} + \frac{0}{256} + \frac{1}{512} + \frac{1}{1024} + \cdots\right)$$

$$= 0.79980469V_{REF}$$

Problem 10.7-11

Repeat Example 10.7-3 if the gain of two amplifier actually has a gain of 2.1.



Solution

(a.) A = 2.0. Assume V_{REF} = 1V.

i	$v_a(i)$	$v_a(i) > V_{REF}$?	b_i	$v_b(i)$
1	2(0.8)=1.6	Yes	1	0.6
2	2(0.6)=1.2	Yes	1	0.2
3	2(0.2)=0.4	No	0	0.4
4	2(0.4)=0.8	No	0	0.8
5	2(0.8)=1.6	Yes	1	0.6

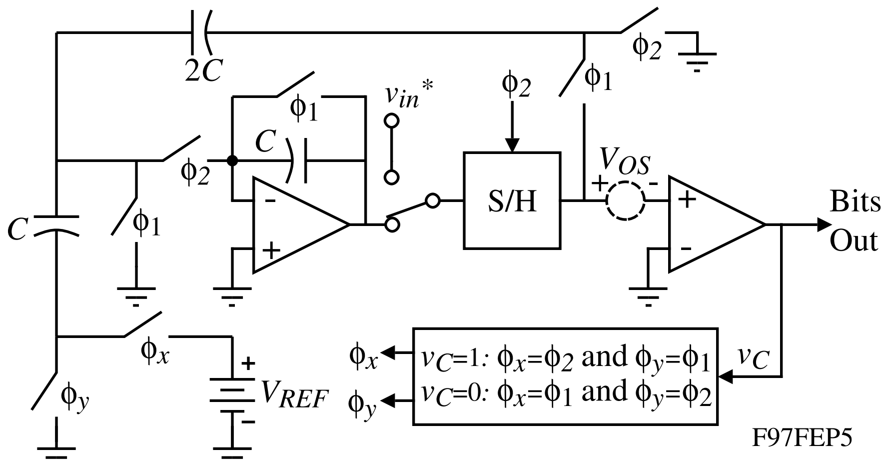
(b.) A = 2.1. Assume V_{REF} = 1V.

i	$v_a(i)$	$v_a(i) > V_{REF}$?	b_i	$v_b(i)$
1	2.1(0.8)=1.68	Yes	1	0.68
2	2.1(0.68)=1.428	Yes	1	0.428
3	2.1(0.428)=0.8988	No	0	0.8988
4	2.1(0.8988)=1.88748	Yes	1	0.88748
5	2.1(0.88748)=1.886371	Yes	1	0.886371

An error occurs in the 4th bit.

Problem 10.7-12

An algorithmic ADC is shown below where ϕ_1 and ϕ_2 are nonoverlapping clocks. Note that the conversion begins by connecting v_{in}^* to the input of the sample and hold during a ϕ_2 phase. The actual conversion begins with the next phase period, ϕ_1. The output bit is taken at each successive ϕ_2 phase. (a.) What is the 8-bit digital output word if $v_{in}^* = 0.3V_{REF}$? (b.) What is the equivalent analog of the digital output word? (c.) What is the largest value of comparator offset, V_{OS}, before an error is caused in part (a.) if V_{REF} = 1V?



F97FEP5

Solution

(a.)

Clock Period	Output of S/H (Normalized to V_{REF})	$v_C > 0$?	Digital Output
Start	0.3V	Yes	-
1	(0.3·2) - 1 = -0.4V	No	0
2	(-0.4·2) + 1 = 0.2V	Yes	1
3	(0.2·2) - 1 = -0.6V	No	0
4	(-0.6·2) + 1 = -0.2V	No	0
5	(-0.2·2) + 1 = 0.6V	Yes	1
6	(0.6·2) -1 = 0.2V	Yes	1
7	(0.2·2) - 1 = -0.6V	No	0
8	(-0.6·2) + 1 = -0.2V	No	0

(b.) $$\boxed{V_{analog} = \left(\frac{1}{4} + \frac{1}{32} + \frac{1}{64}\right) V_{REF} = 0.296875 V_{REF}}$$

(c.) In part (a.) the output of the S/H never got smaller than $\pm 0.2V_{REF} = \pm 0.2$V.

Problem 10.8-01

Why are only 2^N-1 comparators required for a N-bit flash A/D converter? Give a logic diagram for the digital decoding network of Fig. 10.8-1 which will provide the correct digital output word.

Solution

(See the solution for Problem 10.22 of the first edition)

Problem 10.8-02

What are the comparator outputs in order of the upper to lower if V^*_{in} is $0.6V_{REF}$ for the A/D converter of Fig. 10.8-1?

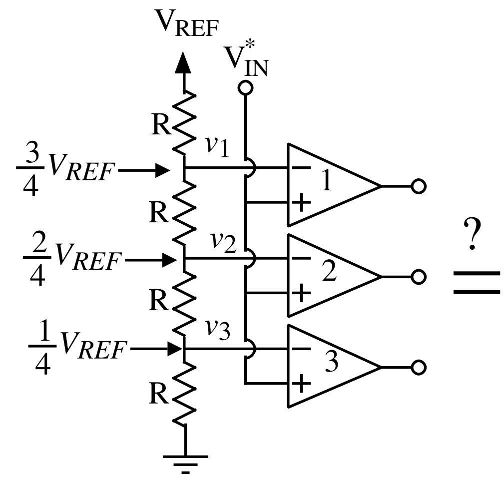
Solution

The comparator outputs in order from the upper to lower of Fig. 10.8-1 for $V^*_{in} = 0.6V_{REF}$ is

1 1 1 0 0 0 0.

Problem 10.8-03

Figure P10.8-3 shows a proposed implementation of the conventional 2-bit flash analog-to-digital converter (digital encoding circuitry not shown) shown on the left with the circuit on the right. Find the values of C_1, C_2, and C_3 in terms of C that will accomplish the function of the conventional 2-bit flash analog-to-digital. Compare the performance of the two approaches from the viewpoints of comparator offset, speed of conversion, and accuracy of conversion assuming a CMOS integrated circuit implementation.



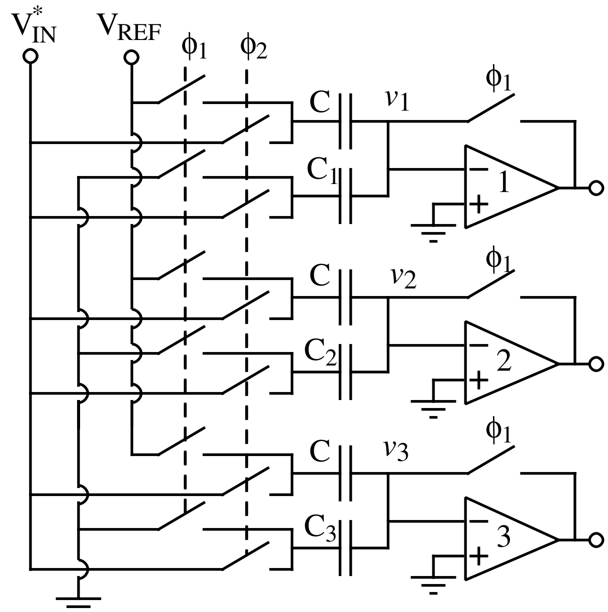


Figure S10.8-3A

Solution

Operation:

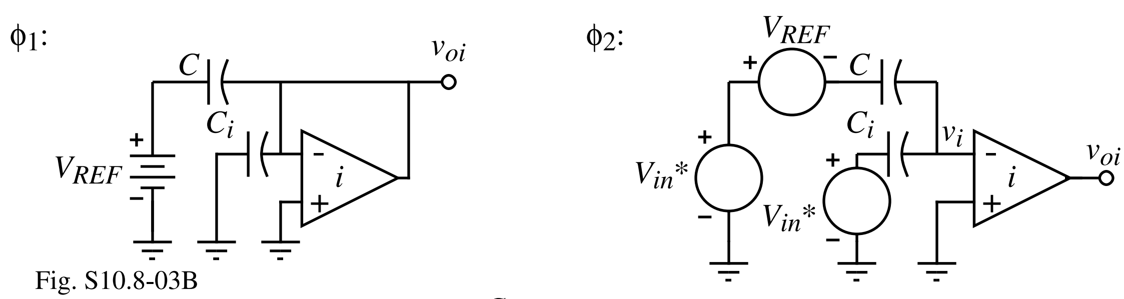


Fig. S10.8-03B

$$v_i(\phi_2) = (V_{in}^*\text{-}V_{REF})\left(\frac{C}{C+C_i}\right) + \left(\frac{C_i}{C+C_i}\right)V_{in}^* = V_{in}^* - V_{REF}\left(\frac{C}{C+C_i}\right)$$

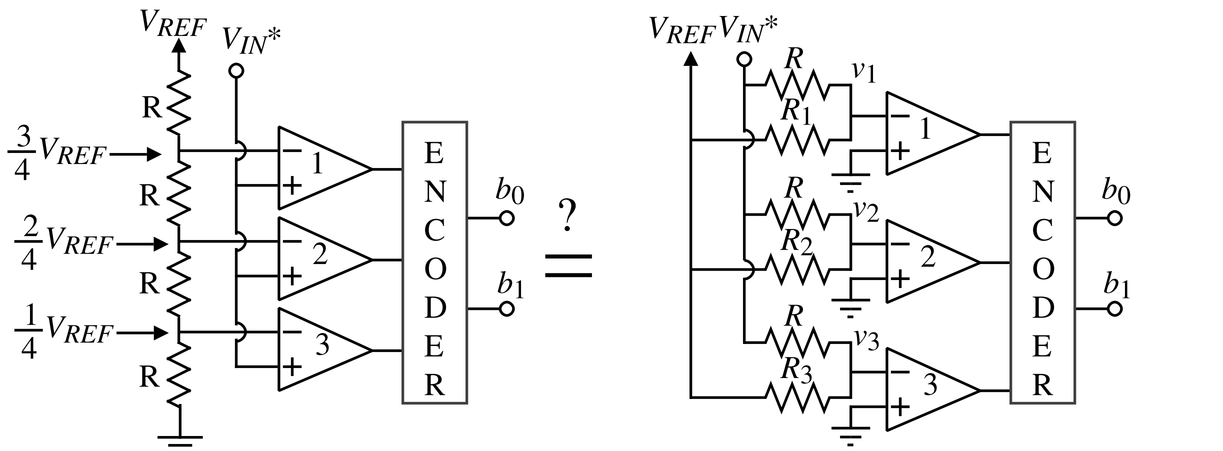
For the conventional flash ADC, $v_i = V_{in}^* - \frac{2^N\text{-}i}{2^N}V_{REF}$. For $N = 2$, we get

$$\therefore \ \frac{2^N\text{-}i}{2^N} = \frac{C}{C+C_i} \quad \rightarrow \ C_i = \left(\frac{i}{2^N\text{-}i}\right)C \quad \text{For } N = 2\text{, we get } \underline{\underline{C_1 = C/3,\ C_2 = C,\ \text{and } C_3 = 3C}}$$

ADC	Comp. Offset	Conv. Speed	Accuracy	Other Aspects
Conv. Flash ADC	≤ ±0.5*LSB*	Fast	Poor	Equal R's
Proposed ADC	Autozeroed	Faster, comp. is simpler	Better	Unequal C's, No CMRR problems

Problem 10.8-04

Two versions of a 2-bit, flash A-D converter are shown in Fig. P10.8-5. Design R_1, R_2, and R_3 to make the right-hand version be equivalent to the left-hand version of the 2-bit flash A-D converter. Compare the performance advantages and disadvantages between the two A-D converters.



Conventional Flash ADC Proposed Flash ADC

Figure S10.8-04

Solution

For the proposed ADC, the comparators must switch at $V_{in}* = 0.75V_{REF}$, $0.5V_{REF}$ and $0.25V_{REF}$ for comparators, 1,2, and 3, respectively.

$$\therefore\ v_1 = \left(\frac{R_1}{R+R_1}\right)V_{in}* - \left(\frac{R}{R+R_1}\right)V_{REF} = 0 \quad\rightarrow\quad V_{in}* = \left(\frac{R}{R_1}\right)V_{REF} \quad\rightarrow\quad R_1 = (4/3)R$$

$$v_2 = \left(\frac{R_2}{R+R_2}\right)V_{in}* - \left(\frac{R}{R+R_1}\right)V_{REF} = 0 \quad\rightarrow\quad V_{in}* = \left(\frac{R}{R_2}\right)V_{REF} \quad\rightarrow\quad R_2 = 2R$$

and

$$v_3 = \left(\frac{R_3}{R+R_3}\right)V_{in}* - \left(\frac{R}{R+R_3}\right)V_{REF} = 0 \quad\rightarrow\quad V_{in}* = \left(\frac{R}{R_3}\right)V_{REF} \quad\rightarrow\quad R_3 = 4R$$

Comparison:

	Conventional Flash ADC	Proposed Flash ADC
Advantages	Less resistor area Guaranteed monotonic All resistors are equal $V_{in}*$ does not supply current Faster- $V_{in}*$ directly connected	Insensitive to CM effects Positive input grounded No high impedance nodes, fast
Disadvantages	Sensitive to CM effects High impedances nodes-only a disadvantage if V_{REF} changes.	More resistor area Can be nonmonotonic Resistor spread of 2^N $V_{in}*$ must supply current More noise because more resistors

Problem 10.8-05

Part of a 6-bit, flash ADC is shown. The comparators have a dominant pole at 10^3 radians/sec, a dc gain of 10^4 a slew rate of 3V/µs, and a binary output voltage of 1V and 0V. Assume that the conversion time is the time required for the comparator to go from its initial state to halfway to is final state. What is the maximum conversion rate of this ADC if V_{REF} = 5V? Assume the resistor ladder is ideal.

Solution:

The output of the *i*-th comparator can be found by taking the inverse Laplace transform of,

$$V_{out}(s) = \left(\frac{A_o}{(s/10^3) + 1}\right)\cdot\left(\frac{v_{in}^*-V_{Ri}}{s}\right)$$

to get,

$$v_{out}(t) = A_o(1 - e^{-10^3 t})(v_{in}^* - V_{Ri}).$$

The worst case occurs when

$$v_{in}^*-V_{Ri} = 0.5V_{LSB} = \frac{V_{REF}}{2^7} = \frac{5}{128}$$

$\therefore$ $0.5\text{V} = 10^4(1 - e^{-10^3 T})(5/128) \rightarrow \dfrac{64}{5\cdot 10^4} = 1- e^{-10^3 T}$

or, $e^{-10^3 T} = 1 - \dfrac{64}{50{,}000} = 0.99872 \quad \rightarrow \quad T = 10^{-3} \ln(1.00128) = 2.806\mu\text{s}$

$$\therefore \boxed{\text{Maximum conversion rate} = \frac{1}{2.806\mu\text{s}} = 0.356\text{x}10^6 \text{ samples/second}}$$

Check the influence of the slew rate on this answer.

$\text{SR} = 3\text{V}/\mu\text{s} \rightarrow \quad \dfrac{\Delta V}{\Delta T} = 3\text{V}/\mu\text{s} \quad \rightarrow \quad \Delta V = 3\text{V}/\mu\text{s}(2.806\mu\text{s}) = 8.42\text{V} > 1\text{V}$

Therefore, slew rate does not influence the maximum conversion rate.

Problem 10.8-06

A flash ADC uses op amps as comparators. The power supply to the op amps is +5V and ground. Assume that the output swing of the op amp is from ground to +5V. The range of the analog input signal is from 1V to 4V (V_{REF} = 3V). The op amps are ideal except that the output voltage is given as

$$v_o = 1000\,(v_{id} + V_{OS}) + A_{cm}\,v_{cm}$$

where v_{id} is the differential input voltage to the op amp, A_{cm} is the common mode gain of the op amp, v_{cm} is the common mode input voltage to the op amp, and V_{OS} is the dc input offset voltage of the op amp. (a.) If A_{cm} = 1V/V and V_{OS} = 0V, what is the maximum number of bits that can be converted by the flash ADC assuming everything else is ideal. Use a worst case approach. (b.) If A_{cm} = 0 and V_{OS} = 40mV, what is the maximum number of bits that can be converted by the flash ADC assuming everything else is ideal. Use a worst case approach.

Solution

(a.) $\Delta v_o = 5\text{V} = 1000\Delta v_{id} \pm 1 v_{cm}$

Choose v_{cm} = 4V as the worst case.

$$\therefore \qquad \Delta v_{id} = \frac{5+4}{1000} = \frac{9}{1000} \le \frac{V_{REF}}{2^{N+1}} = \frac{3}{2^{N+1}}$$

$$2^{N+1} \le \frac{1000\cdot 3}{9} \quad \rightarrow \quad 2^N \le \frac{500\cdot 3}{9} = 167 \quad \rightarrow \quad \underline{\underline{N = 7}}$$

(b.) $\Delta v_o = 5\text{V} = 1000\Delta v_{id} \pm 1000\cdot 40\text{mV}$

$$\Delta v_{id} = \frac{5\text{-}(\pm 1000\cdot 40\text{mV})}{1000} = 5\text{mV} - (\pm 40\text{mV}) = 45\text{mV (worst case)}$$

$$\therefore \qquad 45\text{mV} \le \frac{3}{2^{N+1}} \quad \rightarrow \quad 2^N \le \frac{3}{45\text{mV}} \quad \rightarrow \quad 2^N \le \frac{3000}{2\cdot 45} = 33.33$$

$$\therefore \qquad \underline{\underline{N = 5}}$$

Problem 10.8-07

For the interpolating ADC of Fig. 10.8-3, find the accuracy required for the resistors connected between V_{REF} and ground using a worst case approach. Repeat this analysis for the eight series interpolating resistors using a worst case approach.

Solution

All of the resistors must have the accuracy of ±0.5*LSB*. This accuracy is found as

$$INL = 2^{N\text{-}1}\frac{\Delta R}{R} < 0.5$$

If N = 3, then

$$2^2\frac{\Delta R}{R} < 0.5 \quad \rightarrow \quad \frac{\Delta R}{R} < \frac{1}{8} = \underline{\underline{12.5\%}}$$

Problem 10.8-08

Assume that the input capacitance to the 8 comparators of Fig. 10.8-6 are equal. Calculate the relative delays from the output of amplifiers A_1 and A_2 to each of the 8 comparator inputs.

Solution

Solve by finding the equivalent resistance seen from each comparator, $R_{eq.}(i)$ This resistance times the input capacitance, C, to each comparator will be proportional to the delay.

$R_{eq.}(1) = 0.25R + R||3R = 0.25R + 0.75R = R$

$R_{eq.}(2) = 2R||2R = R$

$R_{eq.}(3) = 0.25R + R||3R = 0.25R + 0.75R = R$

$R_{eq.}(4) = R$

Similarly,

$R_{eq.}(5) = R$

$R_{eq.}(6) = R$

$R_{eq.}(7) = R$

$R_{eq.}(8) = R$

Therefore, $\tau = R_{eq.}(i)C$ are all equal and all delays are equal.

Problem 10.8-09

What number of comparators are needed for a folding and interpolating ADC that has the number of coarse bits as $n1 = 3$ and the number of fine bits as $n2 = 4$ and uses an interpolation of 4 on the fine bits? How many comparators would be needed for an equivalent 7-bit flash ADC?

Solution

$n1 = 3 \Rightarrow \quad 2^3\text{-}1 = 7$

$n2 = 4 \Rightarrow \quad 2^4\text{-}1 = 15$

Therefore, 21 comparators are needed compared with 2^7-1 = 127 for a 7-bit flash.

Problem 10.8-10

Give a schematic for a folder having a single-ended output that varies between 1V and 3V, starts at 1V, ends at 1V and passes through 2V six times.

Solution

See the circuit schematic below.

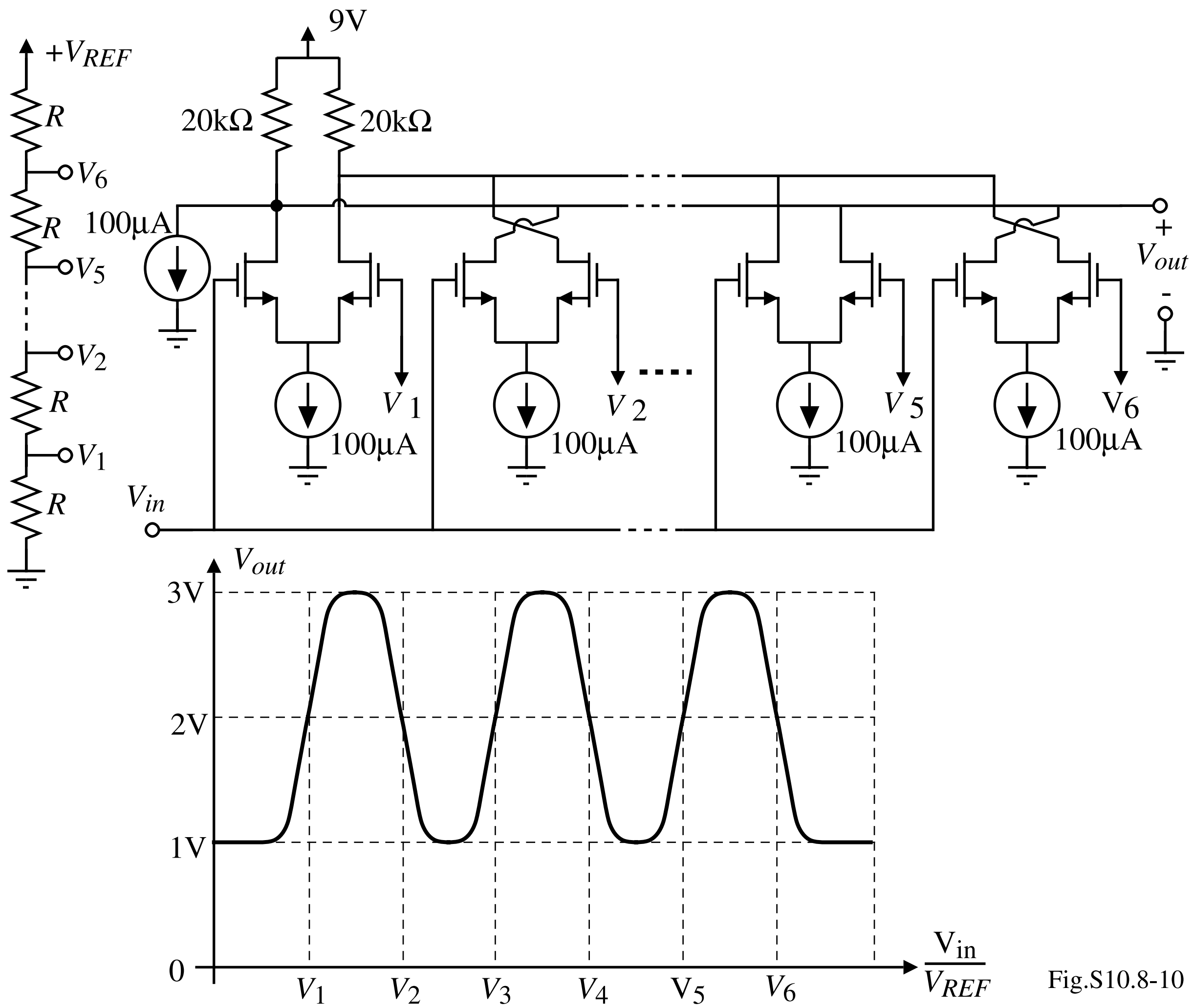
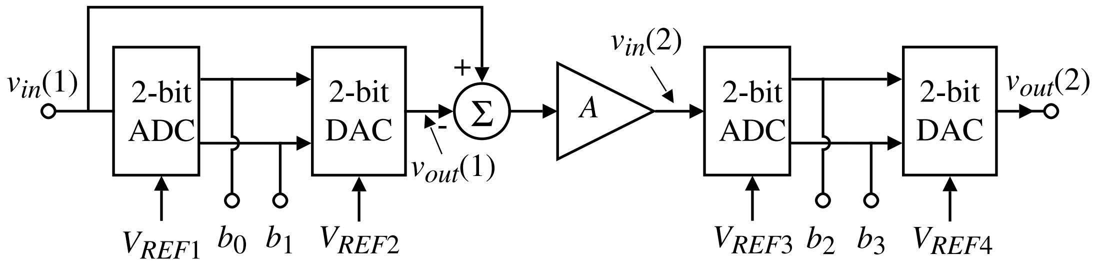


Fig.S10.8-10

Problem 10.8-11

A pipeline, ADC is shown in Fig. P10.8-11. Plot the output-input characteristic of this ADC if V_{REF1} = $0.75V_{REF}$, $V_{REF2} = V_{REF}$, $V_{REF3} = 0.75V_{REF}$, $V_{REF4} = 1.25V_{REF}$, and $A = 4$. Express the *INL* and the *DNL* in terms of a +*LSB* and a -*LSB* value and determine whether the converter is monotonic or not. (F93E2P2)



Solution

Observations:

∴ First stage changes at $v_{in}(1) = (3/16)V_{REF}$, $(6/16)V_{REF}$, $(9/16)V_{REF}$ and $(12/16)V_{REF}$.

∴ $v_{out}(1) = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)V_{REF}$

3.) Second stage changes at $v_{in}(2) = (3/16)V_{REF}$, $(6/16)V_{REF}$, $(9/16)V_{REF}$ and $(12/16)V_{REF}$.

4.) $v_{in}(2) = 4[v_{in}(1) - v_{out}(1)]$ or $v_{in}(1) = (1/4)\ v_{in}(2) + v_{out}(1)$

Value of $v_{in}(1)$ where a change occurs	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3	Comments
0	0	0	0	0	0	0	Starting point
(1/4)x(3/16)=0.75/16	0	0	0	3/16	0	1	
(1/4)x(6/16)=1.50/16	0	0	0	6/16	1	0	
(1/4)x(9/16)=2.25/16	0	0	0	9/16	1	1	
3/16	0	1	4/16	-4/16	0	0	Stage 1 switches
(1/4)x(3/16)+(4/16)=4.75/16	0	1	4/16	3/16	0	1	
(1/4)x(6/16)+(4/16)=5.50/16	0	1	4/16	6/16	1	0	
6/16	1	0	8/16	-8/16	0	0	Stage 1 switches
(1/4)x(3/16)+(8/16)=8.75/16	1	0	8/16	3/16	0	1	
9/16	1	1	12/16	-12/16	0	0	Stage 1 switches
(1/4)x(3/16)+(12/16)=12.75/16	1	1	12/16	3/16	0	1	
(1/4)x(6/16)+(12/16)=13.50/16	1	1	12/16	6/16	1	0	
(1/4)x(9/16)+(12/16)=14.25/16	1	1	12/16	9/16	1	1	

Plot is on the next page.

Problem 10.8-11- Continued

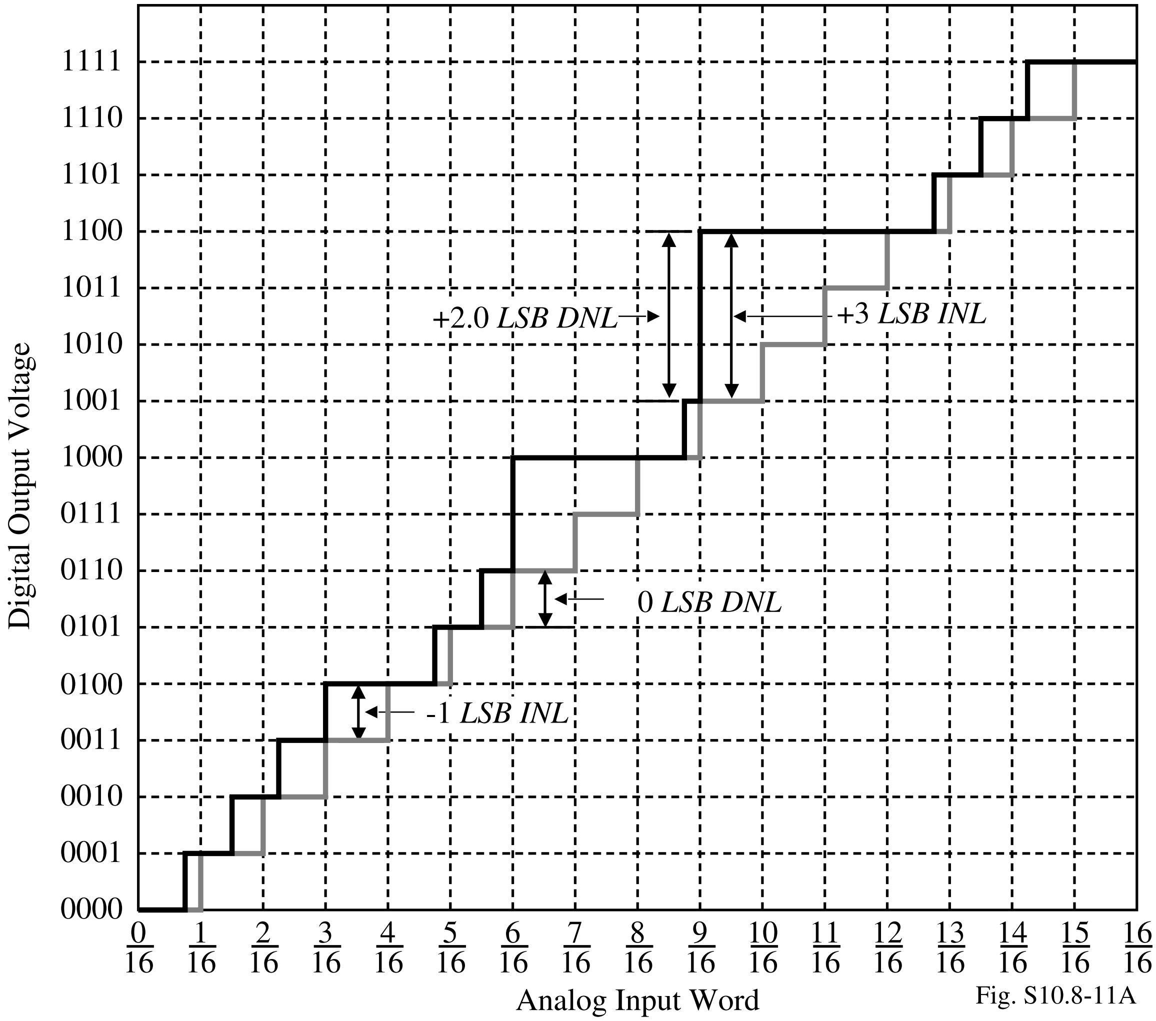
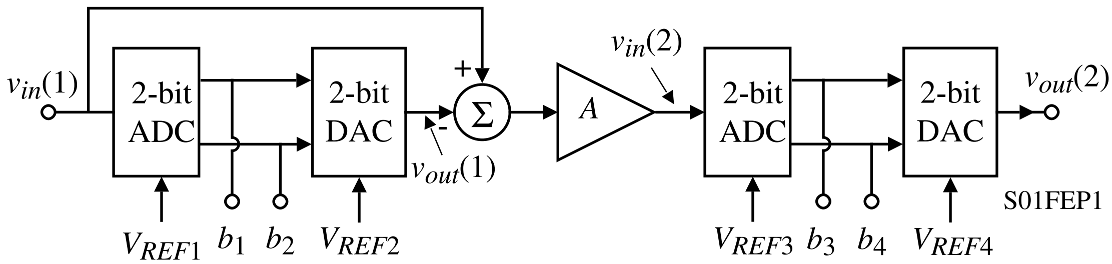


Fig. S10.8-11A

INL: +3*LSB* and –1 *LSB*
DNL: +2*LSB* and 0*LSB*
The ADC is monotonic
The ADC has missing codes which are 0111, 1010, and 1011

Problem 10.8-12

A pipeline, ADC is shown below. Plot the output-input characteristic of this ADC if V_{REF1} = V_{REF2} = $0.75V_{REF}$ and all else is ideal ($V_{REF3} = V_{REF4} = V_{REF}$ and A = 4). Express the *INL* and the *DNL* in terms of a +*LSB* and a -*LSB* value and determine whether the converter is monotonic or not.



Solution

The first stage changes when $v_{in}(1) = \frac{3}{16}V_{REF}, \frac{6}{16}V_{REF}, \frac{9}{16}V_{REF}$, and $\frac{12}{16}V_{REF}$.

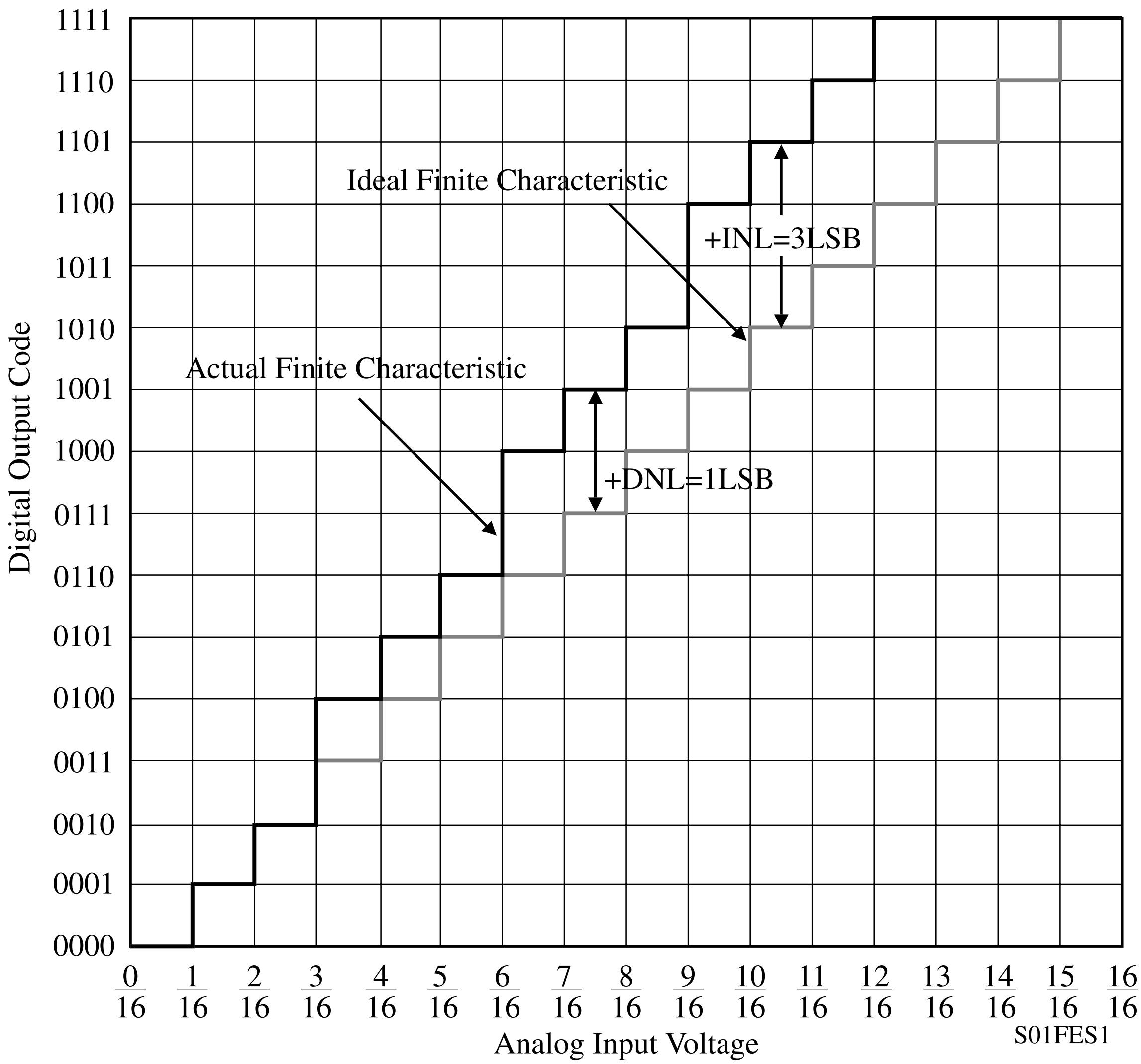
The second stage changes when $v_{in}(2) = \frac{4}{16}V_{REF}, \frac{8}{16}V_{REF}, \frac{12}{16}V_{REF}$, and $\frac{16}{16}V_{REF}$.

Therefore,

$v_{in}(1)$	b_1	b_2	$v_{out}(1)$	$v_{in}(2) = 4v_{in}(1)–4v_{out}(1)$	b_3	b_4
0	0	0	0	0	0	0
1/16	0	0	0	4/16 = 1/4	0	1
2/16	0	0	0	8/16 = 2/4	1	0
3/16	0	1	3/16	12/16-12/16 = 0	0	0
4/16	0	1	3/16	16/16-12/16 = 4/16	0	1
5/16	0	1	3/16	20/16-12/16 = 8/16	1	0
6/16	1	0	6/16	24/16-24/16 = 0	0	0
7/16	1	0	6/16	28/16-24/16 = 4/16	0	1
8/16	1	0	6/16	32/16-24/16= 8/16	1	0
9/16	1	1	9/16	36/16-36/16	0	0
10/16	1	1	9/16	40/16-36/16 = 4/16	0	1
11/16	1	1	9/16	44/16-36/16 = 8/16	1	0
12/16	1	1	9/16	48/16-36/16 12/16	1	1
13/16	1	1	9/16	52/16-36/16 = 16/16	1	1
14/16	1	1	9/16	56/16-36/16 = 20/16	1	1
15/16	1	1	9/16	60/16-36/16 = 24/16	1	1

Problem 10.8-12 - Continued

ADC Characteristic Plot:



From the above plot we see that:

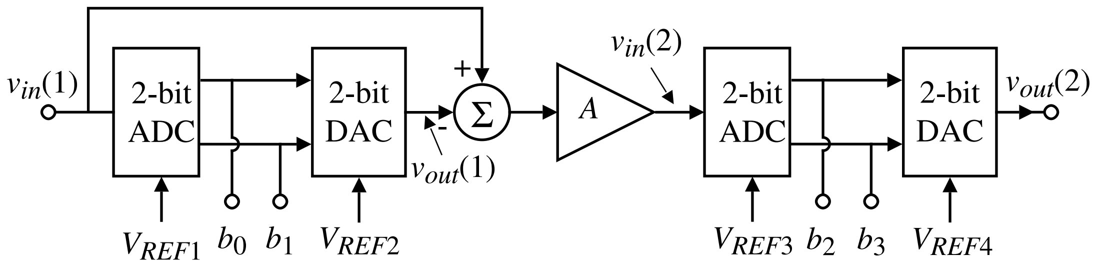
$+INL$ = 3LSB, $-INL$ = 0LSB, $+DNL$ = 1LSB and $-DNL$ = 0LSB

(Note that we cannot say that the ADC has –1LSB for –*DNL* when the ADC saturates.)

The ADC is monotonic.

Problem 10.8-13

Repeat Problem 11 if (a.) $A = 2$ and (b.) $A = 6$ and all other values of the ADC are ideal.



Solution

(a.) $A = 2$. Observations:

∴ First stage changes at $v_{in}(1) = (4/16)V_{REF}$, $(8/16)V_{REF}$, and $(12/16)V_{REF}$.

∴ $$v_{out}(1) = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)V_{REF}$$

3.) 2nd stage changes at $v_{in}(2) = (4/16)V_{REF}$, $(8/16)V_{REF}$, and $(12/16)V_{REF}$.

4.) $v_{in}(2) = 2[v_{in}(1) - v_{out}(1)]$ or $v_{in}(1) = (1/2)\ v_{in}(2) + v_{out}(1)$

Value of $v_{in}(1)$ where a change occurs	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3	Comments
0	0	0	0	0	0	0	Starting point
(1/2)x(4/16)=2/16	0	0	0	4/16	0	1	
(1/2)x(8/16)=4/16	0	1	4/16	0	0	0	Stage 1 switches
(1/2)x(4/16)+(4/16)=6/16	0	1	4/16	4/16	0	1	
(1/2)x(8/16)+(4/16)=8/16	1	0	8/16	0	0	0	Stage 1 switches
(1/2)x(4/16)+(8/16)=10/16	1	0	8/16	4/16	0	1	
(1/2)x(8/16)+(8/16)=12/16	1	1	12/16	0	0	0	Stage 1 switches
(1/2)x(4/16)+(12/16)=14/16	1	1	12/16	4/16	0	1	

With a gain of 2, the second stage sees $v_{in}(2) = 2[v_{in}(1) - v_{out}(1)]$. $v_{in}(2)$ will never exceed $0.25V_{REF}$ before the first stage output brings $v_{in}(2)$ back to zero. As a consequence, b_2 is stuck at zero. The plot is on the next page. It can seen from the plot that *INL* =+0*LSB* and –2*LSB* , *DNL* = +2*LSB* and –0*LSB*. The ADC is monotonic.

(b.) $A = 6$. $v_{in}(2) = 6[v_{in}(1) - v_{out}(1)]$ or $v_{in}(1) = (1/6)\ v_{in}(2) + v_{out}(1)$

Value of $v_{in}(1)$ where a change occurs	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3	Comments
0	0	0	0	0	0	0	Starting point
(1/6)x(4/16)=0.667/16	0	0	0	4/16	0	1	
(1/6)x(8/16) = 1.333/16	0	0	0	8/16	1	0	
(1/6)x(12/16)=2/16	0	0	0	12/16	1	1	
4/16	0	1	4/16	0	0	0	Stage 1 switches
(1/6)x(4/16)+(4/16)=4.667/16	0	1	4/16	4/16	0	1	

Problem 10.8-13 – Continued

Value of $v_{in}(1)$ where a change occurs	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3	Comments
(1/6)x(8/16)+(4/16)=5.333/16	0	1	4/16	8/16	1	0	
(1/6)x(12/16)+(4/16)=6/16	0	1	4/16	12/16	1	1	
8/16	1	0	8/16	0	0	0	Stage 1 switches
(1/6)x(4/16)+(8/16)=8.667/16	1	0	8/16	4/16	0	1	
(1/6)x(8/16)+(8/16)=9.333/16	1	0	8/16	8/16	1	0	
(1/6)x(12/16)+(8/16)=10/16	1	0	8/16	12/16	1	1	
12/16	1	1	12/16	0	0	0	Stage 1 switches
(1/6)x(4/16)+(12/16)=12.667/16	1	1	12/16	4/16	0	1	
(1/6)x(8/16)+(12/16)=13.333/16	1	1	12/16	8/16	1	0	
(1/6)x(12/16)+(12/16)=14/16	1	1	12/16	12/16	1	1	

It can seen from the plot below that *INL* =+1*LSB* and –0*LSB*, *DNL* = ±0*LSB*. The ADC is monotonic.

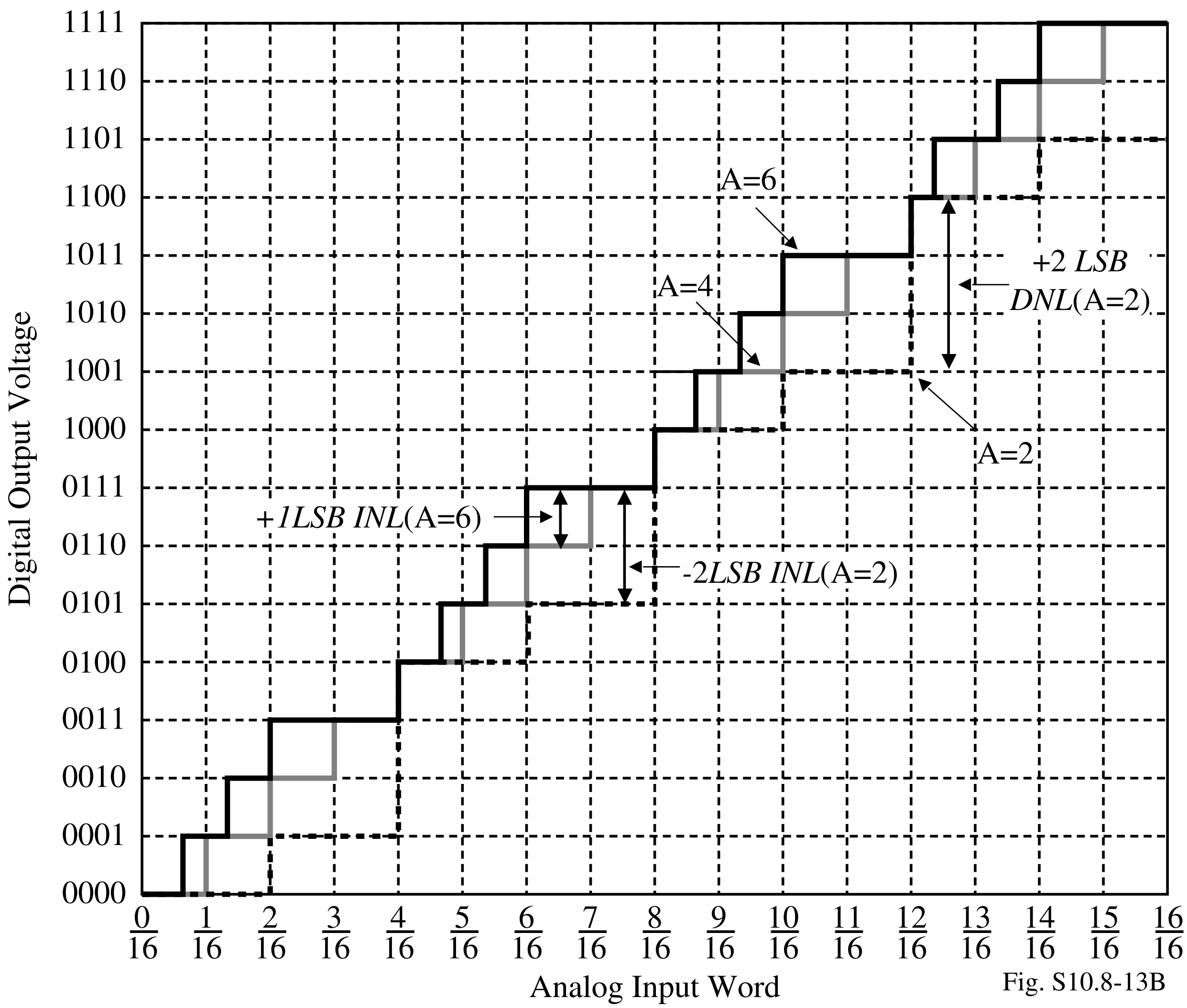
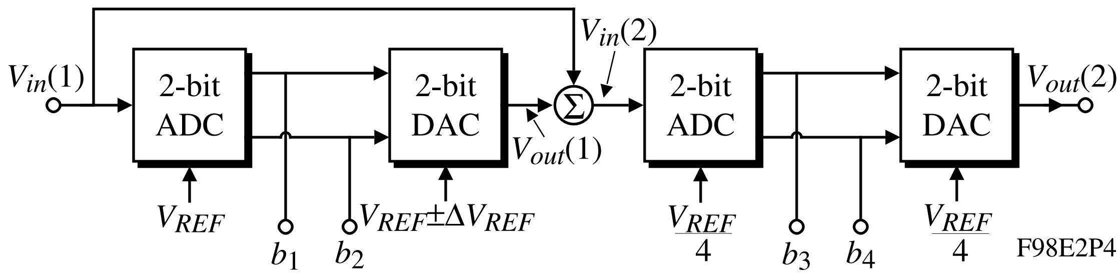


Fig. S10.8-13B

Problem 10.8-14

For the pipeline ADC shown, the reference voltage to the DAC of the first stage is $V_{REF} \pm \Delta V_{REF}$. If all else is ideal, what is the smallest value of ΔV_{REF} that will keep the *INLA* to within (a.) ±0.5*LSB* and (b.) ±1*LSB*?



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Solution

$$V_{out}(1) = \text{Ideal} \pm \text{Error} = \left(\frac{b_1}{2} + \frac{b_2}{4}\right)V_{REF} \pm \left(\frac{b_1}{2} + \frac{b_2}{4}\right)\Delta V_{REF}$$

$$V_{out}(2) = V_{in}(1) - V_{out}(1) = V_{in}(1) - \left(\frac{b_1}{2} + \frac{b_2}{4}\right)V_{REF} \pm \left(\frac{b_1}{2} + \frac{b_2}{4}\right)\Delta V_{REF}$$

The second stage switches at $V_{REF}/16$, $2V_{REF}/16$, $3V_{REF}/16$, and $4V_{REF}/16$.

Therefore the *LSB* is $V_{REF}/16$.

(a.) $INLA = \pm 0.5LSB$

$$\left(\frac{b_1}{2} + \frac{b_2}{4}\right)\Delta V_{REF} \le \frac{\pm V_{REF}}{32}$$

When b_1 and b_2 are both 1 corresponds to the worst case.

$$\therefore \boxed{\Delta V_{REF} \le \frac{4}{3}\frac{\pm V_{REF}}{32} = \frac{\pm V_{REF}}{24}}$$

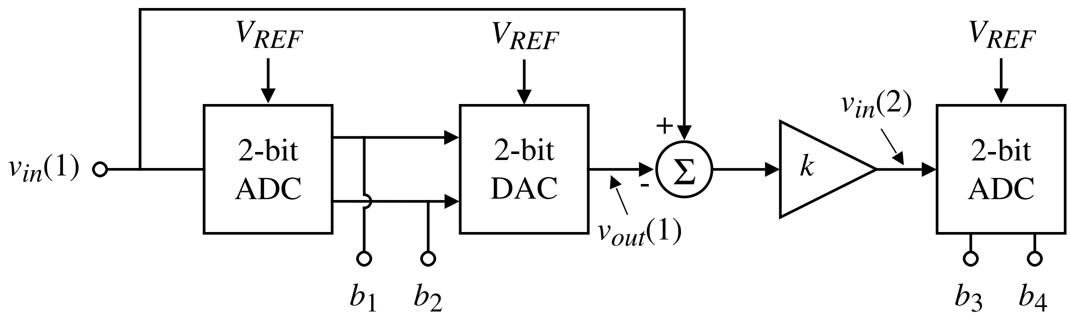
(b.) $INLA = \pm 0.5LSB$

$$\left(\frac{b_1}{2} + \frac{b_2}{4}\right)\Delta V_{REF} \le \frac{\pm V_{REF}}{16}$$

$$\therefore \boxed{\Delta V_{REF} \le \frac{4}{3}\frac{\pm V_{REF}}{16} = \frac{\pm V_{REF}}{12}}$$

Problem 10.8-15

A 4-bit ADC consisting of two, 2-bit stages (pipes) is shown. Assume that the 2-bit ADC's and the 2-bit DAC function ideally. Also, assume that V_{REF} = 1V. The ideal value of the scaling factor, k, is 4. Find the maximum and minimum value of k that will not cause an error in the 4-bit ADC. Express the tolerance of k in terms of a plus and minus percentage.



Solutions

The input to the second ADC is $v_{in}(2) = k\left[v_{in}(1) - \left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right]$.

If we designate this voltage as $v'_{in}(2)$ when $k = 4$, then the difference between $v_{in}(2)$ and $v'_{in}(2)$ must be less than ±1/8 or the *LSB* bits will be in error.

Therefore:

$$\left|v_{in}(2) - v'_{in}(2)\right| = \left|k\ v_{in}(1) - k\left(\frac{b_1}{2} + \frac{b_2}{4}\right) - 4\ v_{in}(1) + 4\left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right| \leq \frac{1}{8}$$

If $k = 4 + \Delta k$, then

$$\left|4\ v_{in}(1) + \Delta k\ v_{in}(1) - 4\left(\frac{b_1}{2}+\frac{b_2}{4}\right) - \Delta k\left(\frac{b_1}{2}+\frac{b_2}{4}\right) - 4\ v_{in}(1) + 4\left(\frac{b_1}{2}+\frac{b_2}{4}\right)\right| \leq \frac{1}{8}$$

or

$$\Delta k\left|v_{in}(1) - \left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right| \leq \frac{1}{8}\ .$$

The largest value of $\left|v_{in}(1) - \left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right|$ is 1/4 for any value of $v_{in}(1)$ from 0 to V_{REF}. Therefore,

$$\frac{\Delta k}{4} \leq \frac{1}{8} \quad \Rightarrow \quad \Delta k \leq 1/2.$$

Therefore the tolerance of k is $\boxed{\frac{\Delta k}{k} = \frac{\pm 1}{2\cdot 4} = \frac{\pm 1}{8} \Rightarrow \pm 12.5\%}$

Problem 10.8-16

The pipeline, analog-to-digital converter shown in Fig. P10.8-16 uses two identical, ideal, two-bit stages to achieve a 4-bit analog-to-digital converter. Assume that the bits, b_2 and b_3, have been mistakenly interchanged inside the second-stage ADC. Plot the output-input characteristics of the converter, express the INL and DNL in terms of a +LSB and a -LSB, and determine whether the converter is monotonic or not.

Solution

$v_{in}(1)$	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3
0	0	0	0	0	0	0
1/16	0	0	0	1/16	1	0
2/16	0	0	0	2/16	0	1
3/16	0	0	0	3/16	1	1
4/16	0	1	4/16	0	0	0
5/16	0	1	4/16	1/16	1	0
6/16	0	1	4/16	2/16	0	1
7/16	0	1	4/16	3/16	1	1
8/16	1	0	8/16	0	0	0
9/16	1	0	8/16	1/16	1	0
10/16	1	0	8/16	2/16	0	1
11/16	1	0	8/16	3/16	1	1
12/16	1	1	12/16	0	0	0
12/16	1	1	12/16	1/16	1	0
13/16	1	1	12/16	2/16	0	1
14/16	1	1	12/16	3/16	1	1

The plot on the next page shows that the $INL = \pm 1LSB$ and $DNL = +1LSB$ and $-2LSB$. The ADC is not monotonic.

Problem 10.8-16 – Continued

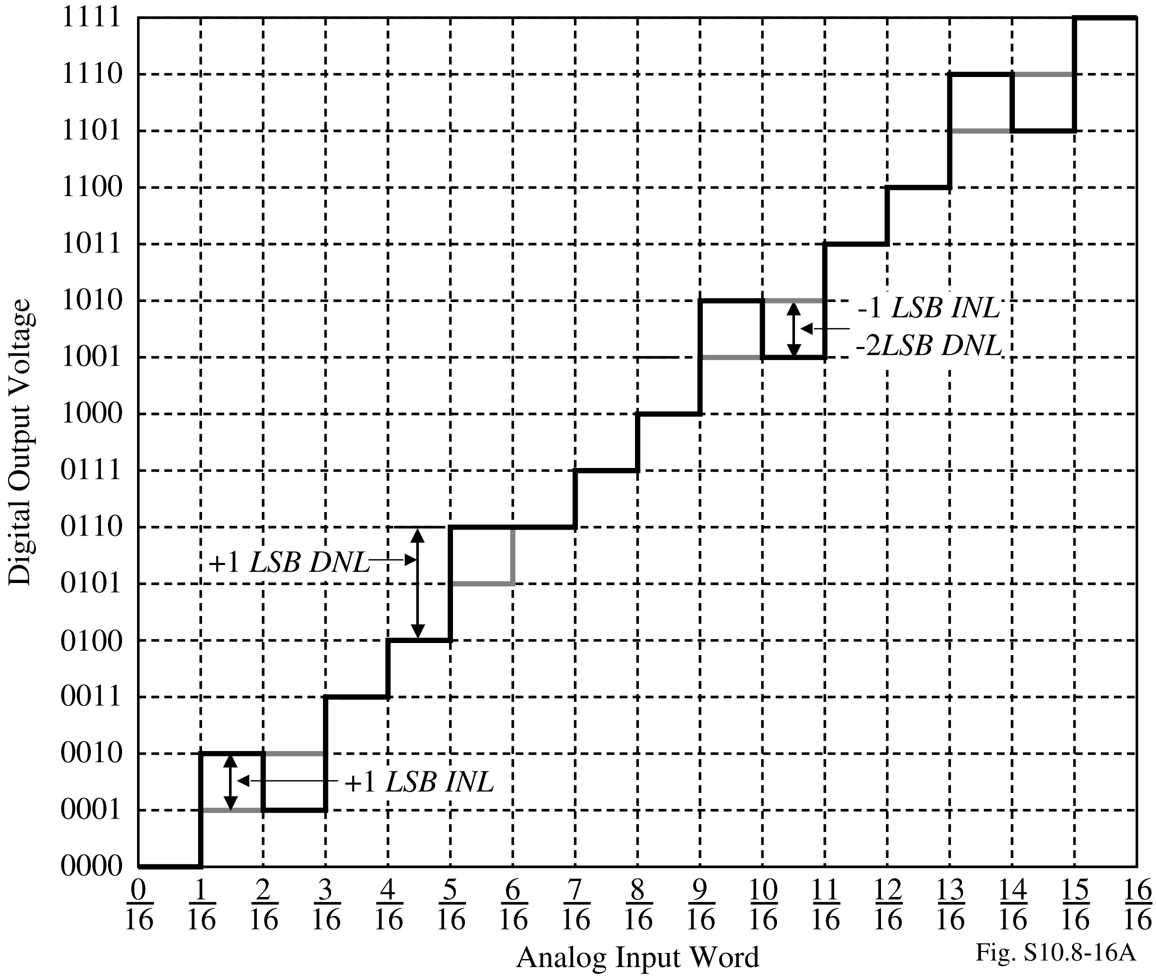


Fig. S10.8-16A

Problem 10.9-01

A first-order, delta-sigma modulator is shown in Fig. P10.9-1. Find the magnitude of the output spectral noise with $V_{in}(z) = 0$ and determine the bandwidth of a 10-bit analog-to-digital converter if the sampling frequency, f_s, is 10 MHz and k = 1. Repeat for k = 0.5.

Solution

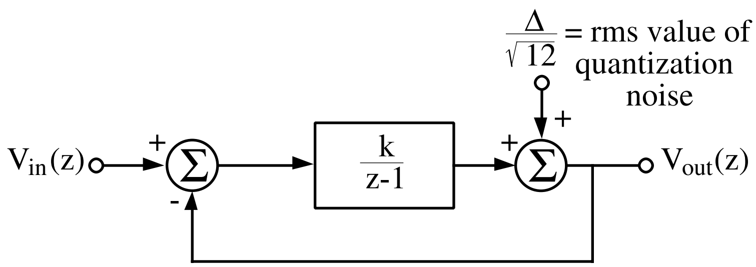


Figure P10.9-1

From the block diagram, we can write,

$$V_{out}(z) = \frac{\Delta}{\sqrt{12}} + \frac{k}{z-1}[V_{in}(z) - V_{out}(z)]$$

Solving for $V_{out}(z)$ gives,

$$V_{out}(z) = \left(\frac{z-1}{z-1+k}\right)\left[\frac{\Delta}{\sqrt{12}} + \frac{kV_{in}(z)}{z-1}\right] = \left(\frac{z-1}{z-1+k}\right)\frac{\Delta}{\sqrt{12}} \quad \text{if } V_{in}(z) = 0$$

$$\therefore \quad H(z) = \left(\frac{z-1}{z-1+k}\right) \quad \rightarrow \quad H(e^{j\omega T}) = \frac{e^{j\omega T} - 1}{e^{j\omega T} - 1 + k} = \frac{e^{j\omega T/2} - e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2} + ke^{-j\omega T/2}}$$

$$H(e^{j\omega T}) = \frac{2j\sin(\omega T/2)}{2j\sin(\omega T/2) + k[\cos(\omega T/2) - j\cos(\omega T/2)]} = \frac{2\tan(\omega T/2)}{(2-k)\tan(\omega T/2) - jk}$$

Find the bandwidth by setting $|H(e^{j\omega T})|^2 = 0.5$.

$$|H(e^{j\omega T})|^2 = \frac{4\tan^2(\omega T/2)}{(2-k)^2\tan^2(\omega T/2) + k^2} = 0.5 \rightarrow 8\tan^2(\omega T/2) = (2-k)^2\tan^2(\omega T/2) + k^2$$

$$\tan^2(\omega T/2)[8 - (2-k)^2] = k^2 \quad \rightarrow \quad \omega T/2 = \tan^{-1}\left[\sqrt{\frac{k^2}{8 - (2-k)^2}}\right]$$

$$\omega = \frac{2}{T}\tan^{-1}\left[\frac{k}{\sqrt{8 - (2-k)^2}}\right] = 2f_s\tan^{-1}\left[\frac{k}{\sqrt{8 - (2-k)^2}}\right]$$

For $k = 1$,

$$\omega_{-3dB} = 2f_s\tan^{-1}\left[\frac{1}{\sqrt{4}}\right] = \underline{\underline{0.927\text{x}10^7 \text{ rads/sec} \rightarrow 1.476 \text{ MHz}}}$$

For $k = 0.5$,

$$\omega_{-3dB} = 2f_s\tan^{-1}\left[\frac{0.5}{\sqrt{8 - \frac{9}{4}}}\right] = \underline{\underline{0.411\text{x}10^7 \text{ rads/sec} \rightarrow 0.654 \text{ MHz}}}$$

Note that the results are independent of the number of bits because *H* is the noise transfer function.

Problem 10.9-02

The specification for an oversampled analog-to-digital converter is 16-bits with a bandwidth of 100kHz and a sampling frequency of 10MHz. (a.) What is the minimum number of loops in a Sodini modulator using a 1-bit quantizer ($\Delta = V_{REF}/2$) that will meet this specification? (b.) If the Sodini modulator has two loops, what is the minimum number of bits for the quantizer to meet the specification?

Solution

The general formula for the *L*-th order Sodini loop is,

$$n_o = \frac{\Delta}{\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{2f_B}{f_s}\right)^{L+0.5}$$

(a.) Δ(quantizer) = $0.5V_{REF}$ and an $LSB = \frac{V_{REF}}{2^{16}}$

$$\therefore \qquad n_o = \leq LSB \quad \Rightarrow \quad \frac{V_{REF}}{2\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{200}{10{,}000}\right)^{L+0.5} \leq \frac{V_{REF}}{2^{16}}$$

or

$$\frac{2^{15}}{\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{1}{50}\right)^{L+0.5} \leq 1 \quad \Rightarrow \quad \underline{\underline{L \geq 3}}$$

(b.) Δ(quantizer) = $\frac{V_{REF}}{2^b}$, where b = no. of bits

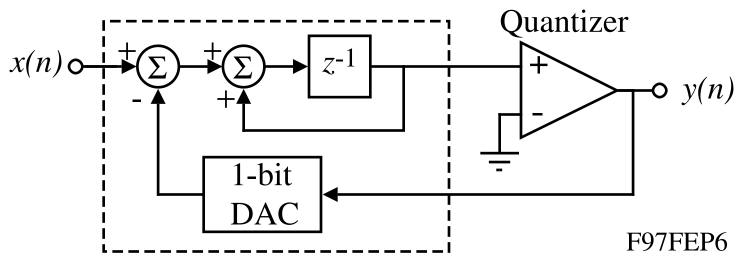
$$\therefore \qquad n_o = \frac{V_{REF}}{2^b} \frac{\pi^2}{\sqrt{12}\sqrt{5}} \left(\frac{1}{50}\right)^{2.5} \leq \frac{V_{REF}}{2^{16}}$$

$$2^b \geq \frac{2^{16}\pi^2}{\sqrt{12}\sqrt{5}} \left(\frac{1}{50}\right)^{2.5} = 4.7237$$

$$\therefore \qquad \underline{\underline{b = 3}}$$

Problem 10.9-03

Draw a single-ended switched capacitor realization of everything within the dashed box of the delta-sigma modulator. Assume that the output of the 1-bit DAC is $\pm 0.5V_{REF}$. Be sure to show the phases of the switches (ϕ_1 and ϕ_2).



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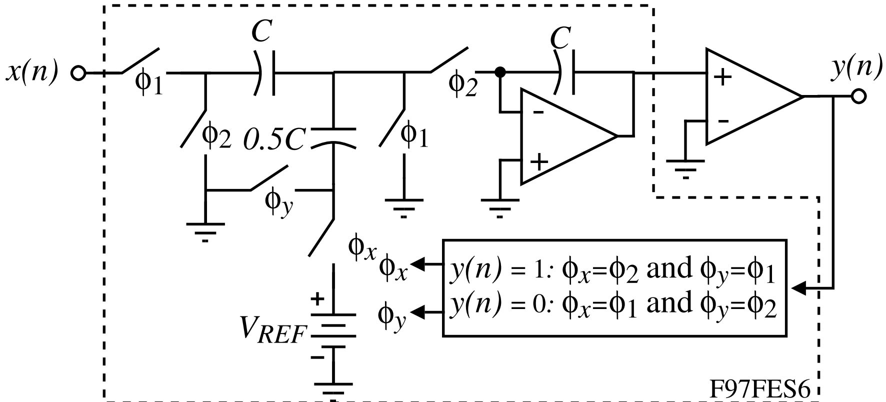
Solution

Note that the inner loop is equal to $\dfrac{z^{-1}}{1-z^{-1}}$ which is a switched capacitor noninverting integrator. Therefore a possible realization of the dashed box is shown below.



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Problem 10.9-04

The modulation noise spectral density of a second-order, 1-bit ΣΔ modulator is given as

$$|N(f)| = \frac{4\Delta}{\sqrt{12}}\sqrt{\frac{2}{f_s}}\ \sin^2\left(\frac{\omega\tau}{4}\right)$$

where Δ is the signal level out of the 1-bit quantizer and $f_s = (1/\tau)$ = the sampling frequency and is 10MHz. Find the signal bandwidth, f_B, in Hz if the modulator is to be used in an 18 bit oversampled ADC. Be sure to state any assumption you use in working this problem.

Solution

The rms noise in the band 0 to f_B can be found as,

$$n_o^2 = \int_0^{f_B} |N(f)|^2 df = \frac{16\Delta^2}{12}\frac{2}{f_s}\int_0^{f_B} \sin^4\left(\frac{\omega}{4f_s}\right) df$$

Assume that $\frac{\omega}{4f_s} = \frac{2\pi f}{4f_s} = \frac{\pi f}{2f_s} << 1$ so that $\sin^4\left(\frac{\omega}{4f_s}\right) \approx \frac{\omega}{4f_s}$

$$\therefore \qquad n_o^2 = \frac{8}{3}\frac{\Delta^2}{f_s}\int_0^{f_B}\left(\frac{2\pi f}{4f_s}\right)^4 df = = \frac{8}{3}\frac{\Delta^2}{f_s}\left(\frac{\pi^4}{16 f_s{}^4}\right)\int_0^{f_B} f^4\ df$$

$$= \frac{8}{3}\frac{\Delta^2\pi^4}{16}\frac{1}{5}\left(\frac{f_B}{f_s}\right)^5 = \frac{8}{15}\frac{\Delta^2\pi^4}{16}\left(\frac{f_B}{f_s}\right)^5$$

$$n_o = \sqrt{\frac{8}{15}}\frac{\Delta\pi^2}{4}\left(\frac{f_B}{f_s}\right)^{5/2}$$

Assume that $\Delta \approx V_{REF}$. For an 18-bit converter, we get

$$n_o \le \frac{V_{REF}}{2^{18}} = \frac{\Delta}{2^{18}} \quad \rightarrow \quad \sqrt{\frac{8}{15}}\frac{\Delta\pi^2}{4}\left(\frac{f_B}{f_s}\right)^{5/2} \le \frac{\Delta}{2^{18}}$$

$$\left(\frac{f_B}{f_s}\right)^{5/2} \le \sqrt{\frac{15}{8}}\frac{4}{\Delta\pi^2}\frac{1}{2^{18}} = \frac{0.555}{2^{18}} = 2.117\text{x}10^{-6}$$

$$\frac{f_B}{f_s} \le 0.005373 \quad \rightarrow \quad \underline{\underline{f_B = 53.74\text{ kHz}}}$$

Problem 10.9-05

The noise power in the signal band of zero to f_B of a L-th order, oversampling ADC is given as

$$n_o = \frac{\Delta}{\sqrt{12}}\frac{\pi^L}{\sqrt{2L+1}}\left(\frac{2f_B}{f_s}\right)^{L+0.5}$$

where f_s is the sampling frequency.

$$\Delta = \frac{V_{REF}}{2^b}$$

and b is the number of bits of the quantizer. Find the minimum oversampling ratio, OSR ($=f_s/f_B$), for the following cases:

(a.) A 1-bit quantizer, third-order loop, 16 bit oversampled ADC.

(b.) A 2-bit quantizer, third-order loop, 16 bit oversampled ADC.

(c.) A 3-bit quantizer, second-order loop, 16 bit oversampled ADC.

Solution

(a.) $$n_o = \frac{V_{REF}}{2\sqrt{12}}\frac{\pi^3}{\sqrt{7}}\left(\frac{2f_B}{f_s}\right)^{3.5} \le \frac{V_{REF}}{2^{16}} \rightarrow \left(\frac{f_B}{f_s}\right)^{3.5} \le \frac{\sqrt{42}}{\pi^3 2^{18}} = 7.9732\text{x}10^{-7} \rightarrow \frac{f_B}{f_s} \le 0.0181$$

$$\therefore \quad \boxed{\frac{f_s}{f_B} = \text{OSR} \ge 55.26}$$

(b.) $$n_o = \frac{V_{REF}}{2^2\sqrt{12}}\frac{\pi^3}{\sqrt{7}}\left(\frac{2f_B}{f_s}\right)^{3.5} \le \frac{V_{REF}}{2^{16}} \rightarrow \left(\frac{f_B}{f_s}\right)^{3.5} \le \frac{\sqrt{42}}{\pi^3 2^{17}} = 1.5946\text{x}10^{-6} \rightarrow \frac{f_B}{f_s} \le 0.0221$$

$$\therefore \quad \boxed{\frac{f_s}{f_B} = \text{OSR} \ge 45.33}$$

(c.) $$n_o = \frac{V_{REF}}{2^3\sqrt{12}}\frac{\pi^3}{\sqrt{5}}\left(\frac{2f_B}{f_s}\right)^{2.5} \le \frac{V_{REF}}{2^{16}} \rightarrow \left(\frac{f_B}{f_s}\right)^{2.5} \le \frac{\sqrt{30}}{\pi^2 2^{15}} = 1.6936\text{x}10^{-5} \rightarrow \frac{f_B}{f_s} \le 0.0123$$

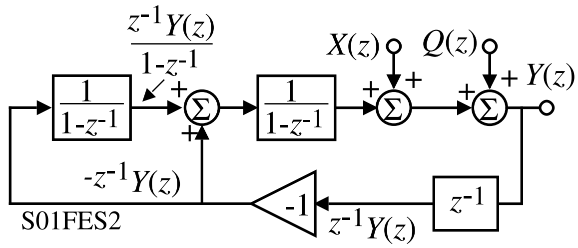
$$\therefore \quad \boxed{\frac{f_s}{f_B} = \text{OSR} \ge 81.00}$$

Problem 10.9-06

A second-order oversampled modulator is shown below. (a.) Find the noise transfer function, $Y(z)/Q(z)$. (b.) Assume that the quantizer noise spectral density of a 1-bit Σ-Δ modulator (not necessarily the one shown below) is

$$|N(f)| = \frac{2V_{REF}}{\sqrt{12}}\sqrt{\frac{2}{f_s}}\ \sin^2\left(\frac{\omega}{2f_s}\right)$$

where f_s = 10MHz and is the sampling frequency. Find the maximum signal bandwidth, f_B, in Hz if the Σ-Δ modulator is used in a 16-bit oversampled analog-to-digital converter.



Solution

(a.) $$Y(z) = Q(z) + X(z) + z^{-1}Y(z) + \left(\frac{1}{1-z^{-1}}\right)\left[-z^{-1}Y(z) - \frac{z^{-1}Y(z)}{1-z^{-1}}\right]$$

$$Y(z) = Q(z) + X(z) + z^{-1}Y(z) - \frac{z^{-1}}{1-z^{-1}}Y(z) - \frac{z^{-1}}{(1-z^{-1})^2}Y(z)$$

$$Y(z)\left[1-z^{-1}+\frac{z^{-1}}{1-z^{-1}}+\frac{z^{-1}}{(1-z^{-1})^2}\right] = Y(z)\left[\frac{1-2z^{-1}+z^{-2}+z^{-1}-z^{-2}+z^{-1}}{(1-z^{-1})^2}\right] = Q(z) + X(z)$$

∴ $$Y(z) = (1-z^{-1})^2[Q(z) + X(z)] \quad \Rightarrow \quad \boxed{\frac{Y(z)}{Q(z)} = (1-z^{-1})^2}$$

(b.) $$n_o^2 = \int_0^{f_B}|N(f)|^2 df = \frac{4V_{REF}^2}{12}\frac{2}{f_s}\int_0^{f_B} sin^4\left(\frac{\pi f}{f_s}\right)df \approx \frac{2V_{REF}^2}{3f_s}\int_0^{f_B}\left(\frac{\pi f}{f_s}\right)^4 df$$

$$n_o^2 = \frac{2\pi^4V_{REF}^2}{3f_s^5}\int_0^{f_B} f^4 df = \frac{2\pi^4V_{REF}^2}{15f_s^5}f_B^5 = \frac{2\pi^4V_{REF}^2}{15}\left(\frac{f_B}{f_s}\right)^5$$

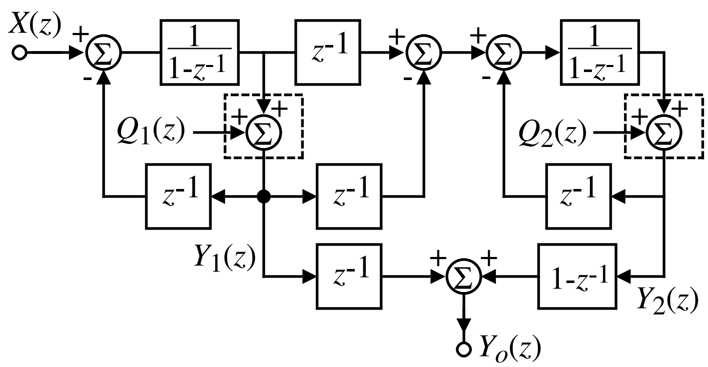
$$n_o = \sqrt{\frac{2}{15}}\,V_{REF}\pi^2\left(\frac{f_B}{f_s}\right)^5 \le \frac{V_{REF}}{2^{16}}$$

∴ $$\left(\frac{f_B}{f_s}\right)^{5/2} \le \sqrt{\frac{15}{2}}\frac{1}{\pi^2}\frac{1}{2^{16}} = \frac{0.2775}{2^{16}} = 4.234\text{x}10^{-6}$$

$$\left(\frac{f_B}{f_s}\right) \le (4.234\text{x}10^{-6})^{2/5} = 0.0072 \quad \Rightarrow \quad f_B \le \underline{\underline{70.909\text{kHz}}}$$

Problem 10.9-07

Find an expression for the output, $Y_o(z)$, in terms of the input, $X(z)$, and the quantization noise sources, $Q_1(z)$ and $Q_2(z)$, for the multi-stage Σ-Δ modulator shown in Fig. P10.9-7. What is the order of this modulator?



Solution

First, find $Y_1(z)$ and $Y_2(z)$.

$$Y_1(z) = Q_1(z) + \frac{1}{1-z^{-1}}[X(z) - z^{-1}Y_1(z)] = Q_1(z) + \frac{X(z)}{1-z^{-1}} - \frac{z^{-1}Y_1(z)}{1-z^{-1}}$$

$$Y_1(z)\left[1 + \frac{z^{-1}}{1-z^{-1}}\right] = Q_1(z) + \frac{X(z)}{1-z^{-1}} \quad \Rightarrow \qquad Y_1(z) = (1-z^{-1})Q_1(z) + X(z)$$

$$Y_2(z) = Q_1(z) + \frac{1}{1-z^{-1}}\left[-z^{-1}Y_2(z) - z^{-1}Y_1(z) + \frac{z^{-1}}{1-z^{-1}}[X(z) - z^{-1}Y_1(z)]\right]$$

$$Y_2(z)\left[1 + \frac{z^{-1}}{1-z^{-1}}\right] = Q_2(z) + \frac{z^{-1}X(z)}{(1-z^{-1})^2} - \frac{z^{-2}Y_1(z)}{(1-z^{-1})^2} - \frac{z^{-1}Y_1(z)}{1-z^{-1}}$$

$$Y_2(z) = (1-z^{-1})Q_2(z) + \frac{z^{-1}X(z)}{1-z^{-1}} - Y_1(z)\left[z^{-1} + \frac{z^{-2}}{1-z^{-1}}\right]$$

$$Y_2(z) = (1-z^{-1})Q_2(z) + \frac{z^{-1}X(z)}{1-z^{-1}} - \frac{z^{-1}Y_1(z)}{1-z^{-1}}$$

$\therefore \qquad Y_o(z) = z^{-1}Y_1(z) + (1-z^{-1})Y_2(z)$

$$= z^{-1}(1-z^{-1})Q_1(z) + z^{-1}X(z) + (1-z^{-1})^2Q_2(z) + z^{-1}X(z) - z^{-1}Y_1(z)$$

$$= z^{-1}(1-z^{-1})Q_1(z) + z^{-1}X(z) + (1-z^{-1})^2Q_2(z) + z^{-1}X(z) - z^{-1}(1-z^{-1})Q_1(z) - z^{-1}X(z)$$

$$\boxed{Y_o(z) = z^{-1}X(z) + (1-z^{-1})^2Q_2(z)}$$

Therefore, the modulator is second-order.

Problem 10.9-08

Two $\Delta\Sigma$ first-order modulators are multiplexed as shown below. $\Delta\Sigma_1$ provides its 1-bit quantizer output during clock phase ϕ_1 and $\Delta\Sigma_2$ provides its 1-bit quantizer output during clock phase ϕ_2 where ϕ_1 and ϕ_2 are nonoverlapping clocks. The noise, n_o, of a general L-loop $\Delta\Sigma$ modulator is

$$n_o = \frac{\Delta}{\sqrt{12}}\frac{\pi^L}{\sqrt{2L+1}}\left(\frac{2f_B}{f_S}\right)^{L+0.5}$$

(a.) Assume that the quantization level for each quantizer is $\Delta = 0.5V_{REF}$ and find the dynamic range in dB that would result if the clock frequency is 100MHz and the bandwidth of the resulting ADC is 1MHz.

(b.) What would the dynamic range be in dB if the quantizers are 2-bit?

Solution:

(a.) If the $\Delta\Sigma_1$ modulator outputs a pulse during ϕ_1 and the $\Delta\Sigma_2$ modulator outputs a pulse during ϕ_2, then two samples occur in 10 ns which is effectively an output pulse rate of 200x10^6 pulses/sec which corresponds to a sampling rate of 200MHz. Therefore,

$$n_o = \frac{V_{REF}}{2\sqrt{12}}\frac{\pi}{\sqrt{3}}\left(\frac{2\cdot 100\text{MHz}}{200\text{MHz}}\right)^{1.5} = 261.8\text{x}10^{-6}V_{REF}$$

$$\therefore \quad \frac{V_{REF}}{n_o} = \frac{10^6}{261.8} = 3819.72 \quad \Rightarrow \quad \boxed{\text{Dynamic Range} = 71.64\text{ dB (11.94bits)}}$$

(b.) A two-bit quantizer gives $\Delta = V_{REF}/4$.

$$\therefore \quad n_o = \frac{V_{REF}}{4\sqrt{12}}\frac{\pi}{\sqrt{3}}\left(\frac{2\cdot 100\text{MHz}}{200\text{MHz}}\right)^{1.5} = 130.9\text{x}10^{-6}V_{REF}$$

$$\frac{V_{REF}}{n_o} = \frac{10^6}{130.9} = 7{,}639.4 \quad \Rightarrow \quad \boxed{\text{Dynamic Range} = 77.64\text{ dB (12.94bits)}}$$

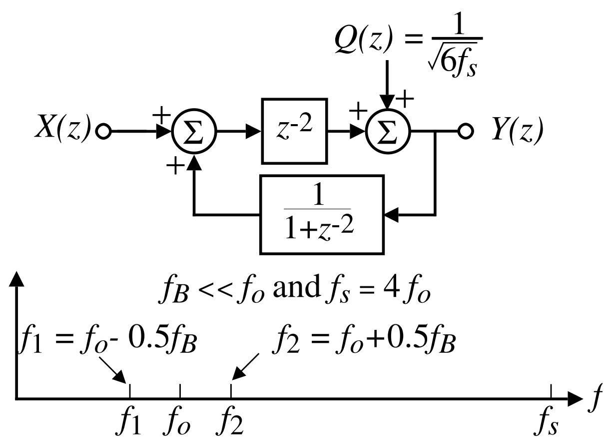
Because n_o is in rms volts, it is consistent to divide V_{REF} by $2\sqrt{2}$ to get

(a.) $$\frac{V_{REF}/2\sqrt{2}}{n_o} = \frac{3819.72}{2\sqrt{2}} = 1350.47 \rightarrow 62.61\text{ dB}$$

(b.) $$\frac{V_{REF}/2\sqrt{2}}{n_o} = \frac{7639.4}{2\sqrt{2}} = 2700.9 \rightarrow 68.61\text{ dB}$$

Problem 10.9-09

A first-order, 1-bit, bandpass, ΔΣ modulator is shown in Fig. P10.9-9. Find the modulation noise spectral density, N(f), and integrate the square of the magnitude of N(f) over the bandwidth of interest (f_1 to f_2) and find an expression for the noise power, $n_o(f)$, in the bandwidth of interest in terms of Δ and the oversampling factor M where M = $f_s/(2f_B)$. What is the value of f_B for a 14 bit analog-to-digital converter using this modulator if the sampling frequency, f_s, is 10MHz?



Solution

$$Y(z) = Q(z) + \frac{1}{1+z^{-2}}[X(z) + z^{-2}Y(z)] = Q(z) + \frac{X(z)}{1+z^{-2}} + \frac{z^{-2}Y(z)}{1+z^{-2}} \rightarrow Y(z) = (1+z^{-2})Q(z) + X(z)$$

$$N(z) = Y(z)\Big|_{X(z)=0} = (1+z^{-2})Q(z) \qquad \rightarrow \qquad N(f) = N(e^{j\omega T}) = (1 + e^{-2\omega T})Q(f)$$

$$N(f) = \frac{e^{j\omega T}}{e^{j\omega T}}(1 + e^{-2\omega T})Q(f) = \frac{e^{j\omega T} + e^{-j\omega T}}{e^{j\omega T}}Q(f) = \frac{2\cos(\omega T)}{e^{j\omega T}}\frac{\Delta}{\sqrt{6f_s}} = \frac{4\Delta}{\sqrt{6f_s}}\cos(\omega T)\, e^{-j\omega T}$$

$$n_o^2(f) = \int_{f_1}^{f_2}|N(f)|^2 df = \int_{f_1}^{f_2}\frac{4\Delta^2}{6f_s}\cos^2(\omega T)df = \frac{\Delta^2}{3f_s}\int_{f_1}^{f_2}[1+\cos(2\omega T)]df$$

$$= \frac{\Delta^2}{3f_s}\int_{f_1}^{f_2} df + \frac{\Delta^2}{3f_s}\int_{f_1}^{f_2}\cos\left(\frac{4\pi f}{f_s}\right)df = \frac{\Delta^2}{3f_s}(f_2-f_1) + \frac{\Delta^2}{3f_s}\left[\frac{f_s}{4\pi}\sin\left(\frac{4\pi f}{f_s}\right)\right]_{f_1}^{f_2}$$

$$= \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[\sin\left(\frac{4\pi f_2}{f_s}\right) - \sin\left(\frac{4\pi f_1}{f_s}\right)\right]$$

$$= \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[2\cos\left(\frac{2\pi}{f_s}(f_2+f_1)\right)\sin\left(\frac{2\pi}{f_s}(f_2-f_1)\right)\right] = \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[\cos\left(\frac{4\pi f_o}{f_s}\right)\sin\left(\frac{2\pi f_B}{f_s}\right)\right]$$

$$= \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[\cos(\pi)\sin\left(\frac{2\pi f_B}{f_s}\right)\right] = \frac{\Delta^2}{3f_s}f_B - \frac{\Delta^2}{12\pi}\left[\sin\left(\frac{2\pi f_B}{f_s}\right)\right]$$

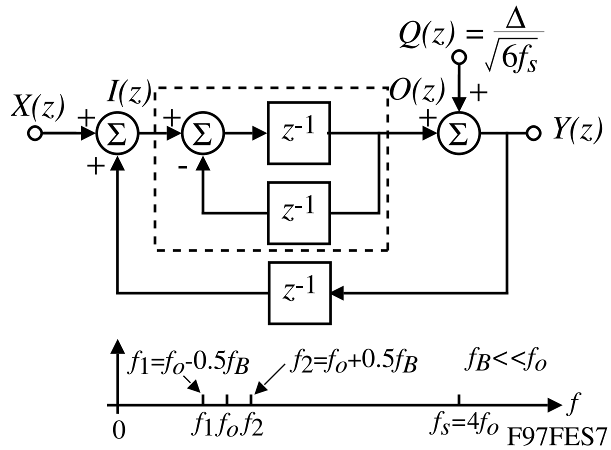
$$n_o^2(f) \approx \frac{\Delta^2}{3f_s}f_B - \frac{\Delta^2}{12\pi}\left[\frac{2\pi f_B}{f_s} - \frac{1}{6}\left(\frac{2\pi f_B}{f_s}\right)^2 + \cdots\right] \approx \frac{\Delta^2}{3f_s}f_B - \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2\pi}{36}\left(\frac{2f_B}{f_s}\right)^2$$

$$n_o^2(f) = \frac{\Delta^2\pi}{36}\left(\frac{2f_B}{f_s}\right)^2 \rightarrow n_o(f) = \frac{\Delta\sqrt{\pi}}{6}\left(\frac{2f_B}{f_s}\right) \le \frac{\Delta}{2^{14}}$$

$$\therefore \quad \frac{2f_B}{f_s} \le \left(\frac{6}{2^{14}\sqrt{\pi}}\right)^{2/3} = 0.003095 \quad \Rightarrow \quad f_B \le \frac{0.003095}{2}\text{x10MHz} = \underline{\underline{15.47\text{kHz}}}$$

Problem 10.9-10

A first-order, 1-bit, bandpass, delta-sigma modulator is shown. Find the modulation noise spectral density, $N(f)$, and integrate the square of the magnitude of $N(f)$ over the bandwidth of interest (f_1 to f_2) and find an expression for the noise power, $n_o(f)$, in the bandwidth of interest in terms of Δ and the oversampling factor M where $M = f_s/(2f_B)$. What is the value of f_B for a 12 bit analog-to-digital converter using this modulator if the sampling frequency, f_s, is 100MHz? Assume that f_s=4f_o and f_B<<f_o.



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Solution

To find the noise transfer function, set $X(z) = 0$ and solve for $Y(z)$. The transfer function for the dashed box is

$$O(z) = z^{-1}[I(z) - z^{-1}O(z)] \;\rightarrow\; \frac{O(z)}{I(z)} = \frac{z^{-1}}{1-z^{-2}} \qquad \therefore\; Y(z) = Q(z) + \frac{z^{-2}}{1+z^{-2}}Y(z)$$

or $$Y(z)\left[1 - \frac{z^{-2}}{1+z^{-2}}\right] = Q(z) \;\Rightarrow\; Y(z)[1+z^{-2}-z^{-2}] = [1+z^{-2}]Q(z) \;\Rightarrow\; Y(z) = [1+z^{-2}]Q(z)$$

$$\therefore \qquad N(z) = (1+z^{-2})Q(z) \;\rightarrow\; N(\varepsilon^{j\omega T}) = (1+e^{-j2\omega T})Q(f) = \frac{e^{j\omega T}+e^{-j\omega T}}{e^{j\omega T}}Q(f)$$

Substituting for $Q(f)$ gives $N(f) = \frac{2\Delta}{\sqrt{6f_s}}cos(\omega T)\,e^{-j\omega T}$

$$n_o^2(f) = \int_{f_2}^{f_1}|N(f)|^2 df = \int_{f_2}^{f_1}\frac{4\Delta}{6f_s}cos^2(\omega T)\,e^{-j\omega T}\,df = \frac{\Delta^2}{3f_s}\int_{f_2}^{f_1}[1+cos2\omega T]df$$

$$= \frac{\Delta^2}{3f_s}\int_{f_2}^{f_1}df + \frac{\Delta^2}{3f_s}\int_{f_2}^{f_1}cos\left(\frac{4\pi f}{f_s}\right)df = \frac{\Delta^2}{3f_s}(f_2-f_1) + \frac{\Delta^2}{12\pi}\left[sin\left(\frac{4\pi f_2}{f_s}\right) - sin\left(\frac{4\pi f_1}{f_s}\right)\right]$$

$$= \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[2cos\left(\frac{4\pi}{f_s}\right)\left(\frac{f_2+f_1}{2}\right)sin\left(\frac{2\pi}{f_s}\right)(f_2-f_1)\right] = \frac{\Delta^2 f_B}{3f_s} + \frac{\Delta^2}{6\pi}\left[cos\left(\frac{4\pi f_o}{f_s}\right)sin\left(\frac{2\pi f_B}{f_s}\right)\right]$$

$$\therefore\; n_o^2(f) \approx \frac{\Delta^2 f_B}{3f_s} - \frac{\Delta^2}{6\pi}\left[\frac{2\pi f_B}{f_s} - \frac{1}{6}\left(\frac{2\pi f_B}{f_s}\right) + \cdots\right] \Rightarrow \boxed{n_o^2(f) = \frac{\Delta^2\pi^2}{36}\left(\frac{2f_B}{f_s}\right)^3 = \left(\frac{\Delta\pi}{6}\right)^2\frac{1}{M^3}}$$

$$n_o(f) = \frac{\Delta\pi}{6}\frac{1}{M^{3/2}} \le \frac{\Delta}{2^{13}} \;\rightarrow\; \frac{2f_B}{f_s} \le \left(\frac{6}{2^{13}\pi}\right)^{2/3} = 0.006013 \;\rightarrow\; \boxed{f_B \le 189\text{kHz}}$$