ELE 704 / EE8502
Analog CMOS Integrated Circuits

Laboratory 4 - Differential Voltage Comparator with Hysteresis

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September 2009

1 Pre-Laboratory

1.1 Background

Voltage comparators are essential components of electronic systems. They have found applications in virtually every electronic systems, such as relaxation oscillators, analog-to-digital converters, and clock and data recovery circuits, to name a few. Differential voltage comparators are essentially differential amplifiers but with fast transitions. Positive feedback is required to achieve fast transitions. Comparators with hysteresis are advantageous compared with those without hysteresis when used in applications where the inputs of the comparators contains high-frequency disturbances, as shown in Fig.1. Comparators with hysteresis are also called Smith triggers, in attribution to the great engineer and scientist Otto Herbert Schmitt (1913-1998) [1]. The original idea of Schmitt trigger was published in the Journal of Scientific Instrument (1938) by Otto when he was a graduate student [2].

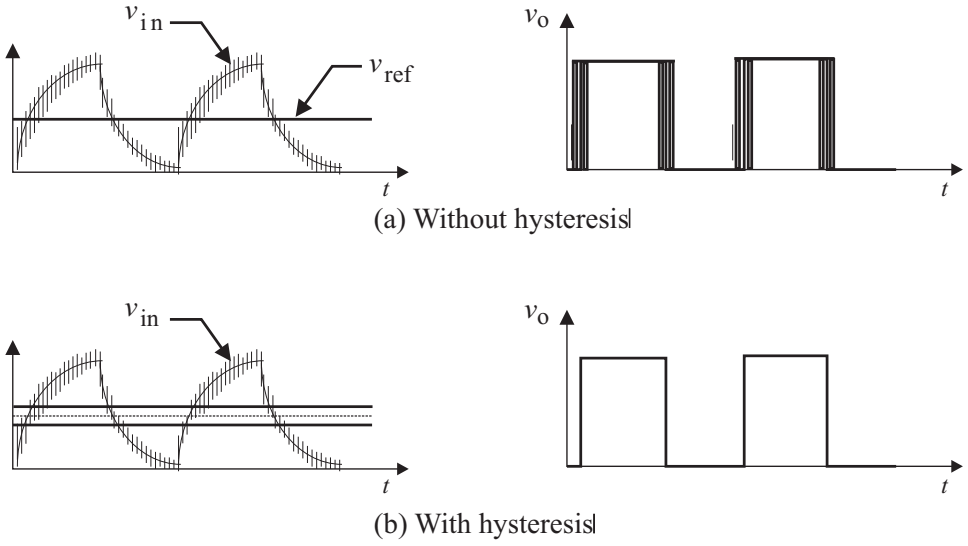

Figure 1: Performance of comparators with and without hysteresis.

In this laboratory, you are required to design, analyze, and simulate All-

stot differential-input single-ended output voltage comparator with a dc biasing network.

1.2 Allstot Voltage Comparator

Perhaps the most widely used Schmitt trigger with hysteresis is the one proposed by Allstot [3]. Fig.2 shows the simplified schematic of the comparator. All transistors are biased in the saturation.

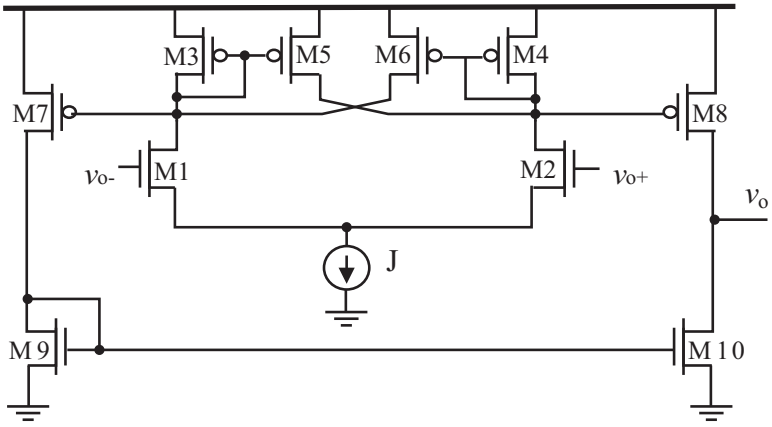

Figure 2: Comparator with hysteresis proposed by A. Allstot.

Transistors M5 and M6 form the positive feedback to provide additional paths to charge the output node. It can be shown that when the positive feedback is absent, i.e. M5 and M6 do not exist (in this case the load of M1 and M2 are diode-connected M3 and M4, which behave as resistors with resistance $1/g_{m3,4}$), we have

$$v_{in}^{+} = v_{in}^{-} + \sqrt{\frac{k_{3,4}}{k_{1,2}}}(v_o^{+} - v_o^{-}), \tag{1}$$

where $k_{1,2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2}$ and $k_{3,4} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{3,4}$. Assume the state transition of the Schmitt trigger takes place when $v_o^{+} = v_o^{-}$. It is evident from (1) that this occurs when $v_{in}^{+} = v_{in}^{-}$.

Now consider the case where positive feedback is present. It can be shown that

$$
\begin{aligned}
v_{in}^{+} &\approx (V_{ss}+V_T)+\sqrt{\frac{k_3}{k_1}}\left(V_{DD}-v_o^{-}-V_T\right)\left(1+\frac{1}{2}\frac{I_{D6}}{I_{D3}}\right), \\
v_{in}^{-} &\approx (V_{ss}+V_T)+\sqrt{\frac{k_4}{k_2}}\left(V_{DD}-v_o^{-}V_T\right)\left(1+\frac{1}{2}\frac{I_{D5}}{I_{D4}}\right),
\end{aligned}
\tag{2}
$$

Note that we have assumed that $\frac{I_{D6}}{I_{D3}}, \frac{I_{D5}}{I_{D4}} \ll 1$ and utilized $\sqrt{1+x} \approx 1+\frac{1}{2}x$ in derivation of (2). It follows from (2) that

$$
v_{in}^{+} \;=\; v_{in}^{-}+\sqrt{\frac{k_{3,4}}{k_{1,2}}}\left(v_o^{+}-v_o^{-}\right)+\frac{I_{D5,6}}{I_{D3,4}}\sqrt{\frac{k_{3,4}}{k_{1,2}}}(\Delta v_o), \tag{3}
$$

where Δv_o is the variation of the output voltage and is defined from $v_o^{+} = v_o + \Delta v_o$ and $v_o^{-} = v_o - \Delta v_o$. A comparison of (1) and (3) reveals that the switching point of the comparator has been shifted by the amount quantified by the second term on the right hand side of (3). It also becomes apparent that by varying the width of M5 and M6, which change I_{D5} and I_{D6}, the switching voltages, i.e., the triggering voltage of the comparator, can be adjusted.

1.3 Pre-Lab Requirements

In your pre-laboratory, you are required to derived the preceding expressions.

2 Laboratory Work

You need to complete the followings:

1. Create the schematic view and symbol view of the comparator with a dc biasing network.

2. Create a test fixture for testing the comparator. A capacitive load of 0.1 pF should be used in testing.

3. Connect an ideal voltage source of 0.9 V to v_{in-}. Disable the positive feedback by removing M5 and M6 (You do not need to remove the transistors. All you need to do is to cut wires connecting these transistors to the output node. Warning messages will appear when recompiling. Just ignore them as you know where they come from). Perform DC sweeping of $v_{in}+$ from 0 to 1.8V and from 1.8 to 0V to find the triggering voltages of the comparator. Plot the output voltage versus the input voltage. Identify the triggering voltages in your plots.

4. Connect an ideal voltage source of 0.9 V to v_{in-}. Enable the positive feedback by re-connecting M5 and M6 to the output nodes (Warning messages should disappear). Perform DC sweeping of $v_{in}+$ from 0 to 1.8V and from 1.8 to 0V to find the triggering voltages of the comparator. Plot the output voltage versus the input voltage. Identify the triggering voltages in your plots. Repeat this step by increase and decrease the width of M5 and M6. This will change the strength of the positive feedback subsequently the triggering voltages. Plot the output voltage versus the input voltage for both cases.

5. Connect an ideal square-wave voltage source to v_{in+} and keep the 0.9 V ideal voltage source connected to v_{in-}. The square-wave voltage source should have voltage swing 0-1.8V and 50% duty cycle. You can choose the oscillation period between kHz and MHz. Enable the positive feedback by re-connecting M5 and M6 to the output nodes. Perform transient analysis over several periods. Note that you should choose more cycles and discard the initial few cycles, which correspond to the initial conditions of your simulation. Plot the waveform of both v_{in+} and v_o in the steady state. Identify the triggering voltages for 0-¿1.8V transitions and 1.8V-¿0 transitions.

3 Post-Laboratory Report

The followings must be included in your Post-Lab Report

1. The schematic of the voltage comparator with an appropriate border. Your name and student ID must be shown in the border area.

2. A table documenting the exact dimension of all transistors used in your design.

3. Simulated voltage transfer characteristic curve with $v_{in-} = 0.9$ V when the positive feedback is removed.

4. Simulated voltage transfer characteristic curve with $v_{in-} = 0.9$ V when the positive feedback is enabled.

5. Simulated voltage transfer characteristic curve with $v_{in-} = 0.9$ V when the positive feedback is enabled and the width of M5 and that of M6 are increased and decreased.

6. Simulated transient response of the output voltage with $v_{in-} = 0.9$ V when the positive feedback is enabled.

Bibliography

[1] J. Harkness, "An idea man," *IEEE Engineering in Medicine and Biology Maganize*, pp.20-41, Nov./Dec. 2004.

[2] O. Schmitt, "A thermionic trigger," *J. Scientific Instruments*, vol.15, pp. 24-26, Jan. 1938.

[3] A. Allstot, "A precision variable-supply CMOS comparator," *IEEE J. Solid-State Circuits*, Vol. 17, No. 6, pp. 1080-1087, Dec. 1982.