

**OBJECTIVE:** To design, simulate and layout a CMOS Comparator with the given specifications.

**Design Specifications:**

- 1) Gain > 2000
- 2) Propagation Delay < 0.75 $\mu$ s
- 3) CMR >  $\pm 3$ V
- 4) Slew Rate >  $\pm 2$ V/ $\mu$ s
- 5) Output Dynamic Range >  $\pm 3$ V
- 6) Power Supply =  $\pm 5$ V
- 7) Load Capacitance  $C_L = 5$ pF

**Spice Parameters for the AMI 1.5 $\mu$  technology:**

**NMOS:**

$$K_N' = 7.55 \times 10^{-5} A/V^2$$

$$\lambda_N = 0.07 V^{-1}$$

$$|V_{TN}| = 0.68 V$$

**PMOS:**

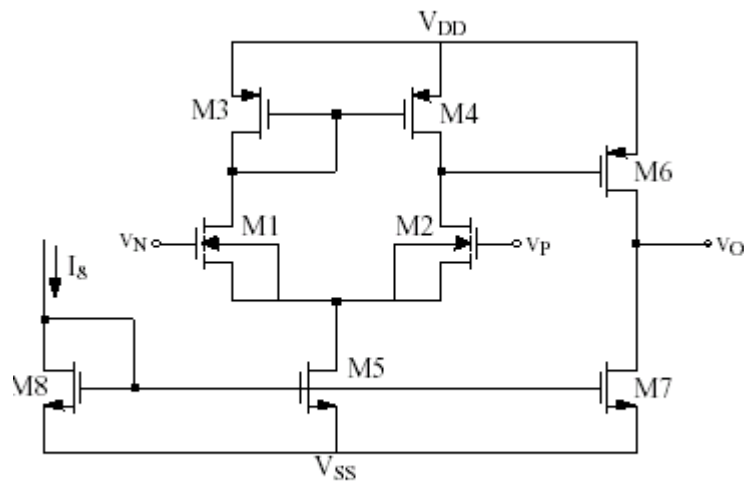
$$K_P' = 2.15 \times 10^{-5} A/V^2$$

$$\lambda_P = 0.12 V^{-1}$$

$$|V_{TP}| = 0.75 V$$

**INTRODUCTION:**

In this project, a simple CMOS comparator was designed, simulated using Cadence tool kit and finally a layout was done using L-Edit Layout Tool. The design was based on a +/-5V power supply, AMI 1.5-micron technology. To meet the given specifications, a two-stage open loop comparator design was used. This design is very similar to the one of a differential op amp without compensation. However the output of the comparator will only take on two values, either the logic high (when it goes up to  $V_{OH}$ ) or logic low, (output drops to  $V_{OL}$ ) depending on the difference between two analog inputs.



*Schematic of a two stage open loop comparator*

**DESIGN METHODOLOGY:**

As a starting point for the hand design the specifications are considered. Out of all the given specifications the most difficult to achieve was the propagation delay  $t_p$  and gain. So, as the first step the propagation delay was assumed to be 0.60  $\mu$ s.

Now in a CMOS comparator the propagation delay  $t_p$  is expressed as

$$t_p = RC \ln\left(\frac{2k}{2k-1}\right) \dots\dots\dots(1)$$

where R is the total equivalent resistance and C is the total equivalent capacitance in the output stage of the comparator. Here the factor k is given as

$$k = \frac{V_{in}}{V_{in}(\min)} \dots\dots\dots(2)$$

In this case the value of  $k$  is unity. Thus the expression for  $t_p$  as shown in equation (1) modifies to

$$t_p = RC \ln 2$$

$$t_p = 0.693RC$$

Now here the value of  $C$  is the value of the load capacitance i.e. 5pF. Thus our assumption of  $t_p$  to be 0.60μs leads us to the relation

$$0.60\mu s = 0.693 * R * 5pF$$

$$\therefore R = 174.3k\Omega$$

This  $R$  in our circuit topology corresponds to  $(r_{ds6} || r_{ds7})$ .

Thus have,

$$(r_{ds6} || r_{ds7}) = 174.3K\Omega$$

$$\therefore \left( \frac{1}{\lambda_n I_{d7}} || \frac{1}{\lambda_p I_{d6}} \right) = 174.3K\Omega$$

But from the topology  $I_{d6} = I_{d7} = I_d$ . Thus,

$$\lambda_n I_d + \lambda_p I_d = \frac{1}{174.3k\Omega}$$

$$\therefore I_{d6} = I_{d7} = I_d = 43\mu A.$$

But to be have some margin the value is assumed somewhat larger than the obtained value. Thus the value is assumed is

$$\boxed{\therefore I_{d6} = I_{d7} = I_d = 50\mu A.}$$

Now, the value of  $I_{d5}$  is taken to be one-fifth of the  $I_{d7}$ . Thus the value is

$$\boxed{\therefore I_{d5} = \left( \frac{I_{d7}}{5} \right) = 10\mu A.}$$

Now assuming that the transistor pairs M1, M2 & M3, M4 are matched, ideally

$$\boxed{I_{d1} = I_{d2} = I_{d3} = I_{d4} = \frac{I_{d5}}{2} = 5\mu A.}$$

Gain is the most important parameter to be achieved in a comparator design. The design is to done in such a way that the desired gain is obtained. Here gain ( $A_v$ ) of more than 2000 is required .

Hence assuming a gain of 2500 to be achieved.

Now the total gain  $A_v$  is given by

$$A_v(tot) = A_{v1} * A_{v2}$$

A gain of 25 is desired to be obtained from the second stage.

Here  $V_{dssat}$  can be upto 2 V for M6. For this  $V_{dssat}$  we got W/L to be unity. Although this W/L is fine the required amount of gain is not obtained using this W/L. So to obtain the required gain we need to change the W/L. For  $V_{dssat} = 0.5$  V we get W/L = 18. Using this value the transconductance of M6 can be evaluated by the following expression

$$g_{m6} = \sqrt{2k_p' \left(\frac{W}{L}\right)_6 I_{d6}}$$

This gives us  $g_{m6} = 207.2 \mu A/V$

This also gives us a gain of 25 from the second stage which is as desired.

Thus

$$\boxed{\left(\frac{W}{L}\right)_6 = 20}$$

Now the gain required from the first stage is 100.

$$A_{v1} = g_{m2}(rds_2 \parallel rds_4) = 100$$

From the current values we get

$$rds_2 = \left(\frac{1}{\lambda_N I_{d2}}\right) = 2.85 M\Omega$$

$$rds_4 = \left(\frac{1}{\lambda_P I_{d4}}\right) = 1.66 M\Omega$$

$$\therefore rds_2 \parallel rds_3 = 1.05 M\Omega$$

This gives the transconductance of M2 by the formula given above

$$\therefore g_{m2} = 95.2 \mu A/V$$

Thus the size of M2 was calculated by the relation

$$g_{m2} = \sqrt{2k_n' \left(\frac{W}{L}\right)_2 I_{d2}}$$

$$\boxed{\therefore \left(\frac{W}{L}\right)_2 = 12.02 \cong 12}$$

Now as the M1 and M2 are matched, their sizes should be the same.

$$\therefore \left(\frac{W}{L}\right)_2 = 12$$

The basic rule for the proper operation of the comparator is that

$$V_{ds3} = V_{gs6}$$

From the current equation  $V_{gs6} = V_{ds3} = 1.237 \text{ V}$

But we have  $V_{ds4} = V_{ds3}$  and  $V_{ds3} = V_{gs3} = V_{gs4}$ .

Hence  $V_{gs4} = 1.237 \text{ V}$ .

Now with this knowledge the sizes of M3 & M4 are computed using the current expressions to get

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 3$$

Now the size of M5 is decided using the CMR requirements. The transistor M5 has to remain in saturation.

For M5 to remain in saturation :  $V_{ds5} = V_{gs5} - V_{T5}$ .

$$\therefore V_{in(cm^-)} - V_{gs1} - (-V_{ss}) = V_{gs5} - V_{T5}$$

Take  $V_{in(cm^-)} = 3V$  and from the current equation for  $I_{d1}$  we get  $V_{gs1} = 0.785 \text{ V}$

$$\therefore V_{gs5} - V_{T5} = 1.21V$$

Thus using the current equation we get

$$\left(\frac{W}{L}\right)_5 = 1$$

The current in both the stages is provided by using current mirrors. The current  $I_{d5}$  is  $10\mu\text{A}$ . So to keep the amount of current as minimum as possible, a reference current of  $10\mu\text{A}$  is assumed in the transistor M8. This leads to the sizes of M8 and M5 to be equal as  $V_{gs}$  of both transistors are equal.

Hence

$$\left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_5 = 1$$

The current in M7 being five times that in M8 gives the size of M7 to be five times that of M8.

$$\therefore \left(\frac{W}{L}\right)_7 = 5$$

Thus the dimensions of all the transistors are obtained.

These are specified in the table below:

<b>TRANSISTOR</b>	<b>W(<math>\mu\text{m}</math>)</b>	<b>L(<math>\mu\text{m}</math>)</b>
M1	18	1.5
M2	18	1.5
M3	3	1.5
M4	3	3
M5	1.5	1.5
M6	30	1.5
M7	7.5	1.5
M8	1.5	1.5

## **SIMULATION RESULTS AND CHANGES MADE IN THE DESIGN**

The proposed design was simulated using Cadence tool. The simulation was performed using the AMI 1.5 $\mu$  technology parameters.

Initially the designed values were used to simulate the circuit, the output that was expected was not achieved. The gain was very small and the propagation delay was higher than what was required. Hence the design was modified to achieve the specifications. The main aim again was to keep transistors to the minimum possible sizes. But this time the saturation voltages of the transistors were reduced. Initially as mentioned in the design methodology the saturation voltages of the output state transistors was taken to be  $V_{DD}-V_{OH}$  and  $V_{SS}-V_{OL}$ . But as this did not give desired results the saturation voltages were taken to be 0.5 V and the design was accordingly modified. This gave the desired results. The original results and the changes made are described below:

### ***Resolution:***

On simulating the design with the obtained parameters it was found that the circuit works as a comparator for input voltage values larger than 2.6 mV. This voltage gives us the resolution of the comparator as 2.6 mV. This is minimum value of the voltage that should be applied to the circuit for it to act as a comparator.

### ***Gain:***

The Gain of the comparator was found out to be 865. This is quite less than what the specifications are. It was found out that the first stage provided less amount of gain than required. So the sizes of the input stage transistors were modified to obtain the required gain.

It is known that gain of the system is directly proportional to the  $r_{ds}$  of the transistors. Also  $r_{ds}$  of a transistor is inversely proportional to the  $\lambda$  and  $\lambda$  is inversely proportional to the channel length. So  $r_{ds}$  is directly proportional to the channel length. Hence to increase the gain of the first stage the lengths and widths of all the transistors were doubled keeping the W/L ratio same. As L is doubled  $\lambda$  is halved and hence the  $r_{ds}$  is doubled thereby increasing the gain of the system. After doubling the lengths and the width the gain was obtained as per the requirements.

### ***Propagation delay:***

The propagation delay observed was 0.314  $\mu$ s for the fall time and 0.02  $\mu$ s for the rise time at an input of 3V. Now for an input of  $\pm 1.295$  mV (i.e.  $V_{in(min)}$ ) the propagation delay is found to be 0.325  $\mu$ s for the fall time 0.03  $\mu$ s for the rise time. The propagation delay obtained for the minimum value of input is the worst propagation delay.

### ***Slew rate:***

The slew rate was observed to be 13.8 V/ $\mu$ s.

### ***Output dynamic range:***

The output dynamic range was obtained to be  $\pm 4.9$  V.

### ***Common Mode range:***

The common mode range is + 4.5 V to - 3.7 V. For positive value it was check that M1 remains in saturation and for the negative value it was verified that M5 remains in saturation.

### **Final Dimensions of the Transistors after Simulation**

TRANSISTOR	W( $\mu\text{m}$ )	L( $\mu\text{m}$ )
M1	36	3
M2	36	3
M3	6	3
M4	6	3
M5	1.5	1.5
M6	30	1.5
M7	7.5	1.5
M8	1.5	1.5

### **Comparison of the hand calculated and the simulated values**

Parameters	Calculated Values	Simulated Values
Gain $A_v$	2500	3384
Propagation Delay $t_p$	0.40 $\mu\text{s}$	0.324 $\mu\text{s}$
Slew Rate SR	10V/ $\mu\text{s}$	13.8 V/ $\mu\text{s}$
Output Dynamic range	$\pm 4.5$ V	$\pm 4.9$ V
Common Mode range	$\pm 3.5$ V	+ 4.9 V to - 3.7 V
Resolution	2.4 mV	2.6 mV

As the table shows, there are still some differences between the designed values and the ones that were finally obtained in simulation. This is because several simplifications were assumed in the design and the parasitic capacitances not considered at all.

## **LAYOUT OF THE COMPARATOR**

Once the simulation of the designed circuit was completed, the layout of the circuit was done using **Tanner L-Edit Pro V9.0 tool kit**. Various considerations are to be taken in to account while doing the layout. The first and the foremost thing is the proper matching of the transistors of the differential input stage and the active loads. This is necessary because even a small mismatch at the input stage will show up at the output as a larger mismatch and affect the performance of the circuit. Proper matching is achieved by splitting up the large transistors into smaller sized ones and using the centroid layout technique.

For matching the differential input pair same source was used for both transistors M1 and M2. The entire transistors were split up into smaller ones and were connected in parallel using the centroid layout techniques. Similarly transistors M3 and M4 were also split up into smaller ones. Finally the current mirrors M5, M6 and M7 were made in the same substrate to provide suitable matching. This is necessary because these are the transistors that provide the current to various branches of the comparator and hence must be matched. Here M7 had a bigger size and hence it was split up in to smaller ones of the size of M5 and M6 and connected in parallel.

Body contacts were provided to avoid body effect for each of the substrate. During the entire layout various rules regarding the dimensions, spacing and connections were followed as per the standards. Also care was taken to consume minimum area and power during the layout by reducing the interconnects.

### **CONCLUSION:**

The comparator design meets the required specifications. Although there are many factors that need to be taken into account while designing a good comparator. The major factor that affects the performance is the DC offset voltage due to mismatch in the input stage. This can show up at the output as a considerable voltage. This has to be taken care of by proper matching of the input transistors. Also another factor affecting the performance is the speed or the propagation delay of the delay. To get a high-speed comparator a cascaded comparator can be used. Also if the comparator is to be placed in a noisy environment then the output will also be noisy in response to a noisy input. In this case the transfer characteristic of the comparator is to be modified. A comparator with hysteresis can be used which basically forces the transition from low to high to occur at a different time than the transition from high to low. If we need to drive large capacitive loads then we can put push-pull inverters in cascade with the output stage of our design. Finally the layout was done so as to achieve maximum matching and minimum interconnects so as to reduce the parasitic capacitances.

Here is the layout the comparator:

