

A CMOS CAPACITOR-LESS LOW DROP-OUT VOLTAGE REGULATOR

Vincent Lixiang Bu

Department of Computer and Electrical Engineering
Tufts University, Medford, MA02155, USA
Email: Lixiang.Bu@tufts.edu

Abstract—A 3-5V 50mA CMOS low Drop-out (LDO) linear regulator with a single compensation capacitor of 1pF is presented. The circuit realization is well-studied and developed with respect to the loop-gain response, the transient response, the output noise, the output accuracy, as well as the standby power consumption. The proposed LDO regulator is implemented in the AMI 0.6 μ m CMOS process, the active layout area is 541 x 320 μ m. The experimental results show that the maximum output load current is 50mA and the regulated output voltage is 2.8V. The regulator provides a full load transient response less than 5mV overshoots and undershoots. Moreover, it provides a power supply reject rate better than -65dB and an output noise of 0.02 μ V/sqrt Hz at 100 kHz.

Index Terms—Low drop-out, low-voltage regulators, CMOS, linear regulator, Miller compensation, power supply circuits, regulators.

I. INTRODUCTION

The demand for the low-voltage, low drop-out (LDO) regulators is increasing because of the growing demand of portable electronics, i.e., phones, pagers, laptops, etc. Meanwhile low-dropout regulator has demonstrated its low noise high-accuracy and fast-response performance, and thereby is widely utilized to power up advanced analogue and radio-frequency integrated circuits. The required regulator also has to have a small active area, a small dip at the output voltage.

Recently, LDO design has become more and more challenging due to the increasing demand of high-performance LDOs, of which low-voltage fast-transient LDOs are especially important [3]. Methods to improve the classical LDO structure have been proposed. [3]—[5]. However, structural limitation, which is the main obstacle to simultaneously achieving stability, high output-voltage accuracy and short response time, still cannot be overcome.

For the sake of good understanding theoretical knowledge, gaining hand-on experience for whole processes of analog IC custom design and academic interests, the LDO regulator has been chosen as the final project for the course of *Analog and Mixed – Signal IC Design*. The design is based on variety of the state-of-the-art published structures [3]-[15], and designed experimental result can achieve proposed specifications.

Through theory studying and models comparison, the limitation of the classical LDOs is mainly due to the associated single pole-zero cancellation scheme, in which an off-chip capacitor with a high equivalent series resistance (ESR) is required to achieve low-frequency pole-zero cancellation. [3]—[10]. The resultant loop gain is not sufficiently high to achieve good line and load regulations and the loop-gain bandwidth is also not sufficiently wide for short response time [3], [11], [12]. In addition, the required high ESR introduces undesirable large overshoots and undershoots during load transient response [3], [11], [12]. Further improvement on the classical structure is difficult and hard to implement as a course final project. Therefore, to achieve good specifications, a novel LDO with a very simple circuit structure is employed in this project—the structure, which a double pole-zero cancellation scheme and a linearly operated power PMOS transistor at dropout to enhance the loop-gain response. The design provides good performances but the key feature settling time, which are an expensive trade-off and also an interesting topic left to be explored further in the future.

II. PROPOSED LOW-DROPOUT REGULATOR

A. Structure and schematic design

The structure of the proposed LDO is shown in Fig. 1. It is composed of two stages OTA. The first stage, as in the classical LDO, is the error amplifier to provide error signal for voltage regulation. And the second stage is a common source amplifier which has a high output swing. Due to the cascade

This work is the final project of course EE147: Analog and Mixed-Signal IC Design, Prof S. Sonkusale, ECE Dept, Tufts Univ., spring, 2007.

architecture, the loop gain depends on the products of the voltage gains of the two gain stages. The high loop gain provides good line and load regulations [4], [11], [12].

The circuit structures of the error amplifier and the second gain stage are very typical two stages OTA. The circuit schematic in Fig. 2 shows that the error amplifier is a differential pair (M2 and M3) with active load (M4 and M5), while the second gain stage is a common source stage (M6) with a bias-current source (M7). The output swing of the second stage is much better than the source follower in turning on or off the power transistor, and therefore this configuration is suitable for low-voltage LDO designs. The current mirrors (M1, M7 and M8) provide current sources for both stages.

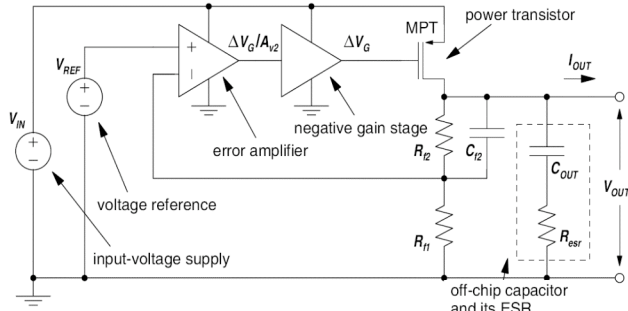


Fig. 1 Structure and circuit diagram of the proposed LDO

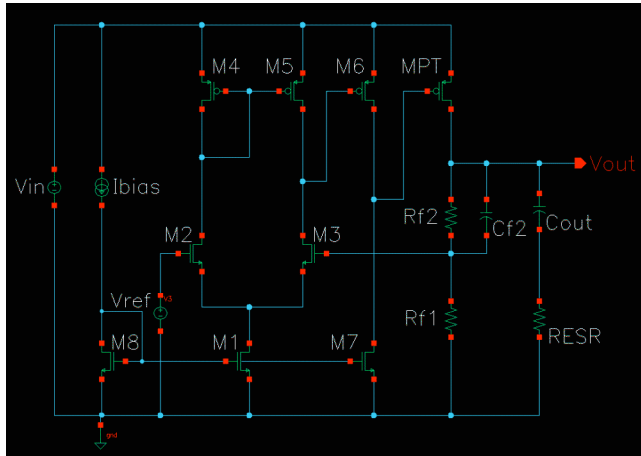


Fig. 2 Schematic View of the proposed LDO

The power transistor (MPT) is design to operate in linear region at dropout. Although the voltage gain of the power transistor is less than unity, the loop gain is not degraded due to the error amplifier and the second gain stage. A loop gain of more than 60dB can be easily achieved in the proposed design and is already sufficient for good line and load regulations [12]. In the proposed design, for the good transient response performance reason, the transistor size reaches millimeter or even centi-meter orders, which generate a bigger gate capacitance. The slew rate at the gate of the power transistor and the frequency response of the LDO are disadvantages for the proposed LDO, which is a trade off for good line and load regulation performance.

In Fig. 1 and 2, the voltage reference is chosen the widely-used bandgap references voltage value. I_{bias} is chosen so that the two-stage OTA and MPT work properly. And V_{in} works from 3V to 5V, which is the proposed LDO's regulating range.

B. Stability and loop-gain compensation analysis

The proposed LDO has three LHP poles which are created at the LDO output (p_1), the second-stage output (p_2) and the error-amplifier output (p_3), respectively. The corresponding pole frequencies can be expressed by

$$p_1 = \frac{1}{C_{out} r_{op}} = \frac{\lambda I_{out}}{C_{out}} \quad (1)$$

$$p_2 = \frac{1}{C_g R_{oa}} \quad (2)$$

$$p_3 = \frac{1}{C_a R_{oea}} \quad (3)$$

where R_{oea} and R_{oa} are the output resistance of the first and second gain stage, respectively, while C_a and C_g is the gain capacitances of the second stage and the power transistor operating in linear region, respectively. Since there are two cascade gain stages to ensure a high loop gain, the gain of each stage needs not be too high. As a result, both R_{oea} and R_{oa} are relatively smaller than the output resistance of the error amplifier in the classical LDOs.

The frequency compensation can be achieved by two pole-zero cancellations. One LHP zero (z_{esr}) is generated by C_{out} and R_{esr} as given by

$$z_{esr} = \frac{1}{C_{out} R_{esr}} \quad (4)$$

while another LHP zero (z_f) is created by the feedback resistors and C_{f2} as give by

$$z_f = \frac{1}{C_{f2} R_{f2}} \quad (5)$$

This method makes use of the feedback resistor that must be present in any LDO design to create the zero, and therefore the additional chip area is only due to C_{f2} . As the feedback resistors are generally large to minimize the power loss at the feedback resistors, the required C_{f2} is very small. In the proposed design, a C_{f2} of about 1pF is needed. The coupling noise by the small C_{f2} is therefore negligible. Moreover, the transient response is not affected as C_{f2} is connected to the LDO output. In fact, a LHP pole (p_2) is created simultaneously with z_f , and its position is given by

$$p_f = \frac{1}{C_{f2} (R_{f1} \parallel R_{f2})} \quad (6)$$

From (5) and (6), $z_f \ll p_f$ when $R_{f1} \ll R_{f2}$. This can be achieved by using a small V_{REF} .

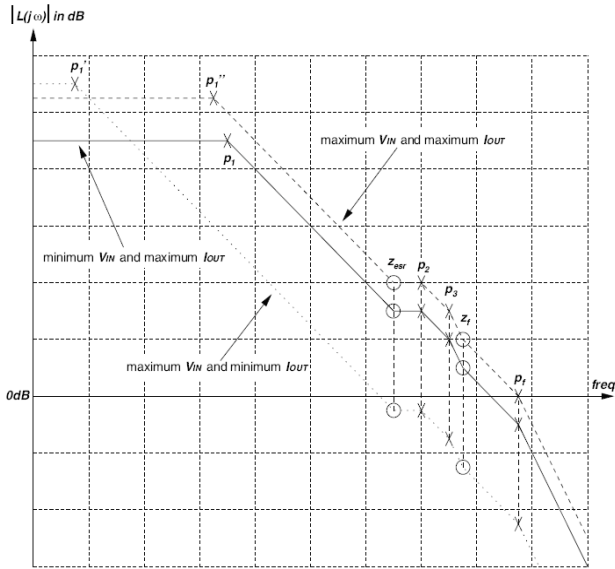


Fig. 3 Loop gains of the proposed LDO at different conditions

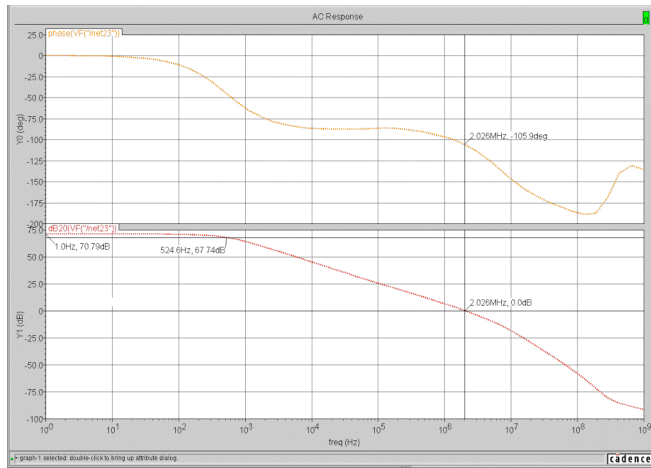


Fig. 4 Open-loop gains of the proposed LDO at maximum V_{in} and maximum I_{out}

Fig. 3 illustrated the stability of the proposed LDO at different V_{in} and I_{out} . At the minimum V_{in} (dropout condition) and the maximum I_{out} , the proposed LDO is stable and ensures that p_f is beyond the UGF. When V_{in} increases to the maximum, the power transistor operates from linear region to saturation region due to a larger drain-source voltage. The output resistance of the power transistor increases, and therefore the loop gain increases. The higher loop gain causes a higher UGF. Stability is maintained when $UGF \leq p_f$ is designed. For another extreme case, at the maximum V_{in} and the minimum I_{out} , the dominant pole p_1' is at a very low frequency and dominant-pole compensation is the most efficient method to provide a stable LDO. It is noted that the

frequencies of p_2, p_3, p_f, z_{sr} and z_f almost remain unchanged at the different V_{in} and I_{out} . From the above discussion, the proposed LDO should be stabilized at the designed maximum V_{in} and maximum I_{out} in order for the proposed LDO to be perfectly stable at any operating conditions. The open loop AC response simulation at maximum V_{in} and maximum I_{out} is shown on Fig. 4.

The output accuracy of the proposed LDO is high with regard to the effect of the offset voltage since there are only two pairs of devices that require good matching (M2–M3 and M4–M5). The offset voltage due to large variations at the error amplifier output, occurring in the classical LDOs, is reduced in the proposed LDO due to the gain stage formed by M6 and M7. As shown in Fig. 2, when there is a ΔV_G at the gate of the power transistor due to the change of I_{out} , the change at the error amplifier output is just a $\Delta V_G / A_{v2}$, where is the voltage gain of the second stage and is much larger than unity. The variation of V_{DS5} is much reduced and so is the offset voltage.

Due to the simple circuit structure, the output noise of the proposed LDO is low. Moreover, there is no embedded capacitor or resistor to create poles and zeros for stability purpose, and therefore no coupling noise is imposed on the error amplifier. Moreover, the output noise from the error amplifier can be minimized by large g_{m2} and g_{m3} .

III. EXPERIMENTAL RESULTS

The proposed LDO is designed in AMS (Austria Mikro System Group, Austria) 0.6- μm CMOS technology, and the threshold voltage is about 0.85V at room temperature. The whole chip layout view is shown in Fig. 5, and the area is only $541 \mu\text{m} \times 320 \mu\text{m}$. The LDO is capable of operating from 3V to 5V, which covers a wide range of the typical battery voltage. A dropout voltage of 200mV at a 50mA maximum load current is achieved. Moreover, the utilized off-chip capacitor is 100 μF with a RSR of about 30m Ω . Table I summarizes the LDO's performance.

Owing to the high loop gain provided by the design structure and extremely large size of power transistor, both line and load regulations are pretty good. The measured line and load regulation are 4mV/V and 2mV/mA, respectively. The worst case measurements are shown in Fig. 6 and Fig. 7. From the measurement, both overshoots and undershoots are smaller than 5mV. However, as discussed before, the trade off for the good line and load regulations is the settling time of full load changes. The huge width of power transistor, around tens of milli-meters, makes the dynamic response of LDO slow, effectively over 100 μs . This is a serious disadvantage for the proposed LDO, which restricts the usage in high speed area.

In addition to static-state and dynamic-state performances, the LDO provides low output noise. The measured output noise spectral density is 0.0239 $\mu\text{V}/\sqrt{\text{Hz}}$ at 100kHz with full load current. Moreover, the power supply rejection (PSRR) is -60dB when operating at 3V.

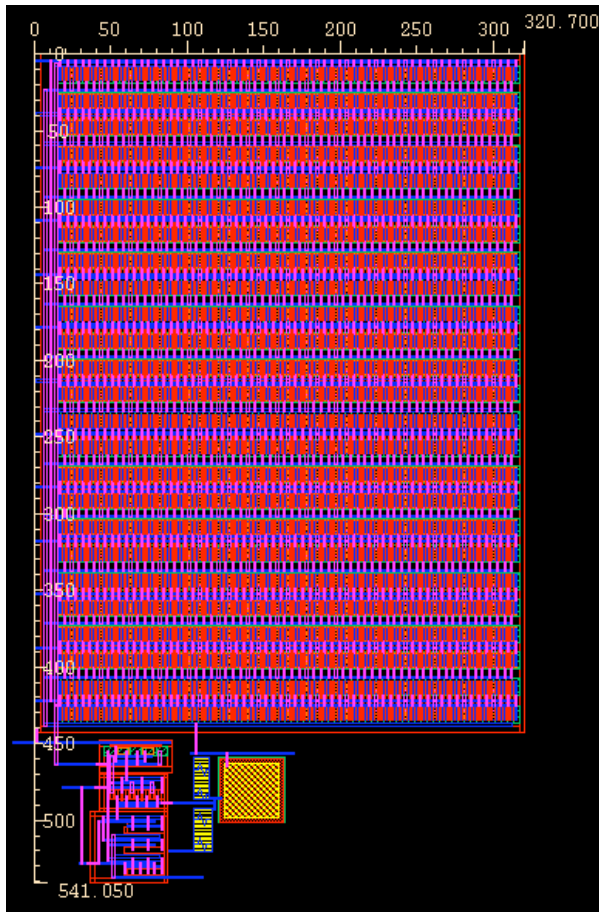


Fig. 5 Proposed LDO Full Chip Layout View

TABLE I. SUMMARY OF MEASURED PERFORMANCE

Technology	AMS 0.6- μm CMOS
Threshold Voltage	$\sim 0.85\text{V}$ @ $T=27^\circ\text{C}$
Chip Area	$541\ \mu\text{m} \times 320\ \mu\text{m}$
Supply Voltage	3V to 5V
Ground Current	$20\ \mu\text{A}$
Output Current	0 to 50mA
Dropout Voltage	200mV @ 50mA
Present Output Voltage	2.8V
Line Regulation	4mV/V
Load Regulation	2mV/mA
Full Load Transient Response	$150\ \mu\text{s}$
Output Noise	$0.0239\ \mu\text{V}/\sqrt{\text{Hz}}$ @ 100kHz
PSRR	-60dB @ $V_{in}=3\text{V}$

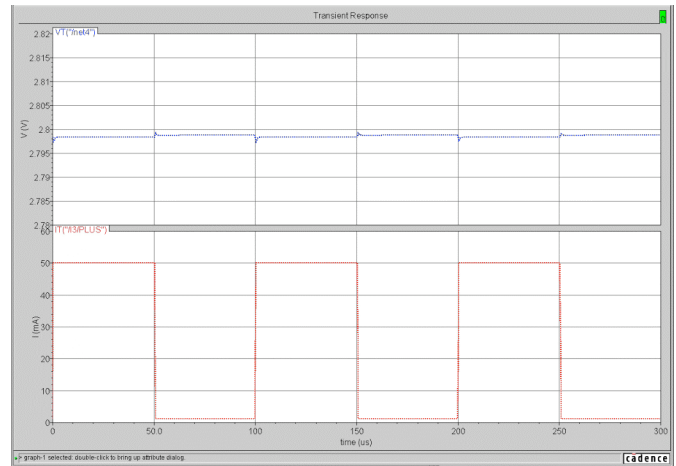


Fig. 6 Measured Load Transient Response at $V_{in} = 3\text{V}$ and $I_{out} = 1$ to 50mA

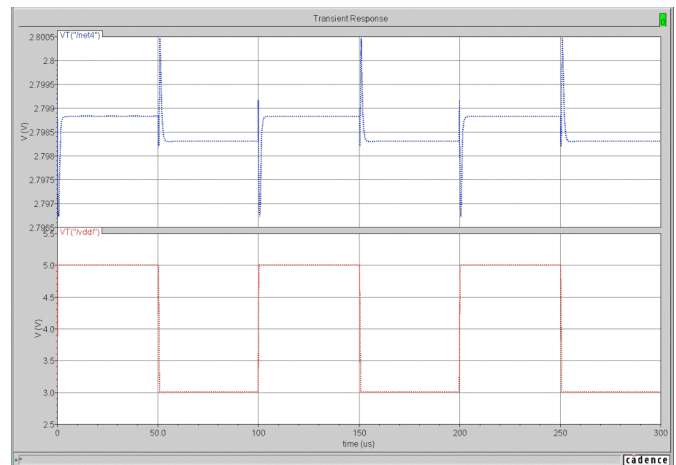


Fig. 7 Measured Line Response at $I_{out} = 50\text{mA}$ and $V_{in} = 3$ to 5V

CONCLUSION

A low dropout liner regulation with a compensation capacitor has been presented. The design is based on a simply but advanced structure and a proposed double pole-zero cancellation scheme. It achieves many published designs' specifications. Experimental results show that the proposed LDO has small overshoots and undershoot, excellent line and load regulations, as well as low-noise output. However, the proposed design has the disadvantage of slow load transient responses. The designed LDO is suitable for powering up low-voltage CMOS mixed-signal systems that require high-precision supply voltage as well as low recovery speed. This final design project is a great experience for learning theoretical knowledge and gaining hand-on skills for whole processes of custom analog and mixed-signal IC design.

ACKNOWLEDGMENT

I would like to first thank the instructor Prof. S. Sonkusale and teaching assistant Mr. S. Hwang for their expert knowledge and guidance throughout my entire program for this challenging but exciting course. I would also thank all of my colleagues and peers for their input and moral support. I would also like to extend my thanks to Prof. J. Noonan and Prof. J. Hopwood to whom I owe my acceptance and preparation towards achieving a Master of Science degree in electrical engineering. Finally, I would like to thank my dear family for all their love and support along my arduous journey in the electrical engineering profession. To my family, I owe them my current successes and the success that will follow in the future. Thank you!

REFERENCES

- [1] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill
- [2] S. Sokusale, EE147 *Analog and Mixed-Signal IC Design Notes*, ECE, Tufts Univ. Spring, 2007
- [3] G.A. Rincon-Mora and P.E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator," *IEEE Journal of Solid-State Circuits*, vol. 33, pp.36-44, Jan. 1998.
- [4] G.A. Rincon-Mora and P.E. Allen, "Study and Design of Low Drop-Out Regulators," 1996
- [5] Ka Nang Leung, Philip K.T. Mok and Sai Kit Lau, "A Low-Voltage CMOS Low-dropout Regulator with Enhanced Response," 2004 *International Symposium* on vol. 1, Issue , 23-26 May 2004 Page(s): I-385 - I-388 Vol.1
- [6] G.A. Rincon-Mora and P.E. Allen, "Optimized Frequency-Shaping Circuit Topologies for LDO's," *Transactopm pm Corciot amd Systems II*, vol. 45, pp.703-708, June. 1998.
- [7] K. Salmi, C. Scarabello, O. Chevalerias and F. Rodes, "4V 5mA Low Drop-out Regulator Using Series-Pass N-Channel MOSFET," *Electronics Letters*, vol. 35, pp.1214-1215, Jul. 1999.
- [8] C. Simpson, "Linear Regulators: Theory of Operation and Compensation," *National Semiconductor Application Note 1148s*, pp.1-12, May, 2000.
- [9] C. Simpson, "A User's Guide to Compensating Low-Dropout Regulators," *National Semiconductor Power Management Applications*, pp.1-14.
- [10] T.Kugelstadt, "Fundamental Theory of PMOS Low-dropout Voltage Regulator," *Texas Instrumnets Application Report*, Apr. 1999.
- [11] B.S. Lee, "Technical Review of Low Dropout Voltage. Regulator Operation and Performance," *Texas Instrumnets Application Report*, pp.1-25, Aug. 1999.
- [12] B.S. Lee, "Understanding the Terms and Definitions of LDO Voltage Regulator," *Texas Instrumnets Application Report*, pp.1-12, Oct. 1999.
- [13] R.J. Milliken, "A Capacitor-Less Low Drop-Out Regulator with Fast Transient Response," Thesis submitted to TAMU.
- [14] W.J. Huang, S.H.Lu and S.I. Liy, "CMOS Low Dropout Linear Regulator with Miller Capacitor," *Electronics Letters* Volume 42, Issue 4, 16 Feb. 2006 Page(s): 216 - 217
- [15] B.M. King, "Understanding the Load-Transient Response of LDO Voltage Regulator," *Texas Instrumnets Analog Application Journal*, pp.19-21, Nov. 2000.