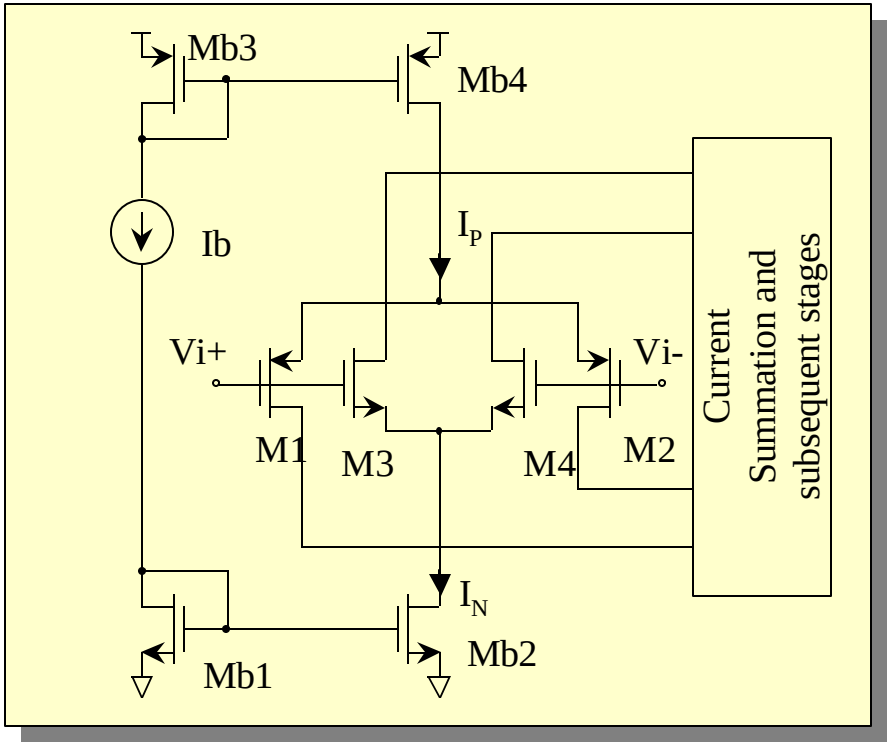
Rail-to-Rail Op Amps

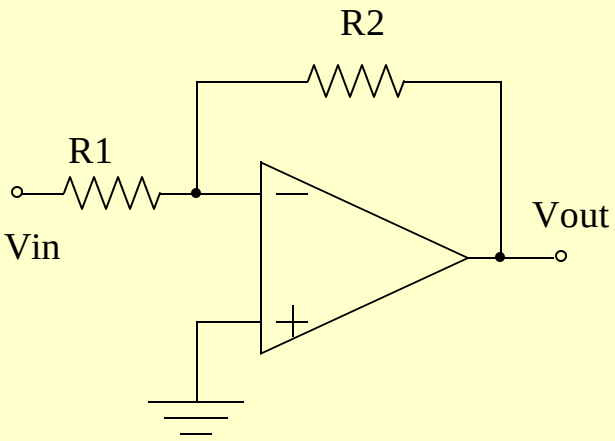


Edgar Sánchez-Sinencio TAMU, AMSC

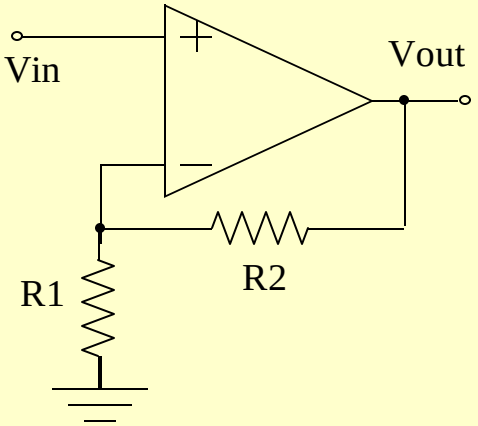
Thanks to Shouli Yan for his valuable input in helping in generating part of this material

Rail-to-Rail Op Amps

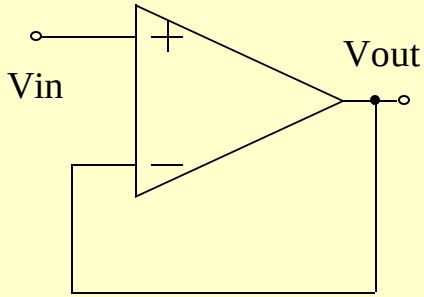
- There are 2 basic configurations for Op Amp applications:
  (a) inverting configuration, and,
  (b) non-inverting configuration.



(a) Inverting Configuration



(b) Non-Inverting Configuration



(c) Voltage Follower
(a special case of non-inverting configuration)

Why Rail-to-Rail Differential Input Stage?

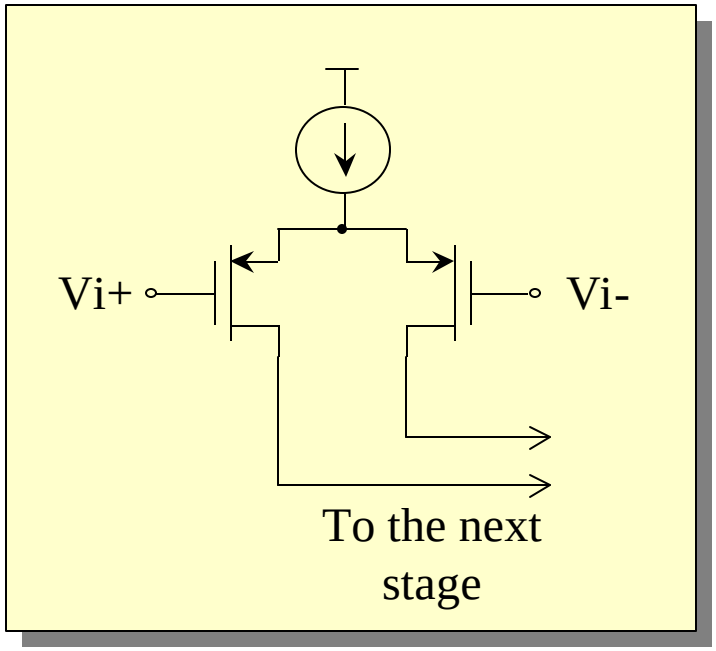
- The input and output swings of inverting and non-inverting configurations

Configuration	Input common mode voltage swing	Output voltage swing
Inverting	≈0	Rail-to-rail
Non-inverting	R1/(R1+R2) * Vsup	Rail-to-rail
Voltage follower	Rail-to-rail	Rail-to-rail

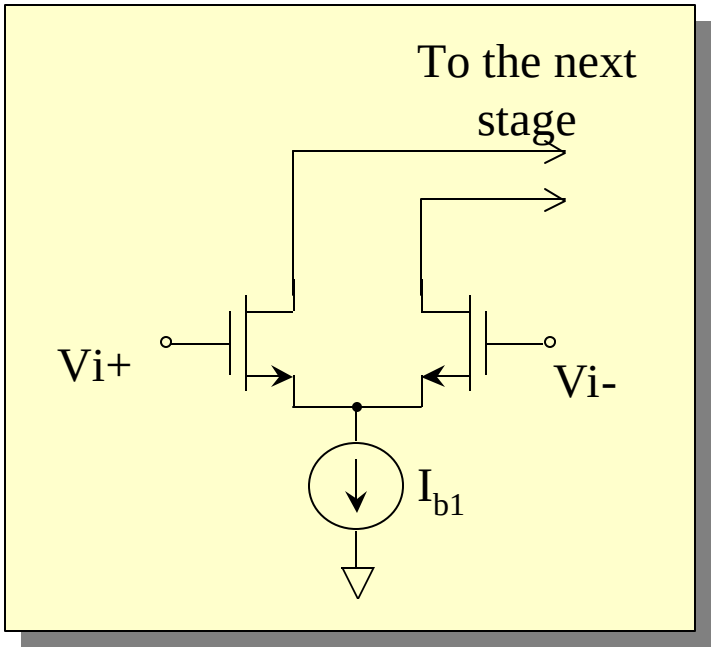
- From the table, we see that for inverting configuration, rail-to-rail input common mode range is not needed. But for non-inverting configuration, some input common mode voltage swing is required, especially for a voltage follower which usually works as an output buffer, we need a **rail-to-rail** input common mode voltage range! To make an Op Amp work under any circumstance, a differential input with **rail-to-rail** common mode range is needed.

How to Obtain a Rail-to-Rail Input Common Mode Range?

- We know that usually the input stage of an op amp consists of a differential pair. There are two types of differential pairs.



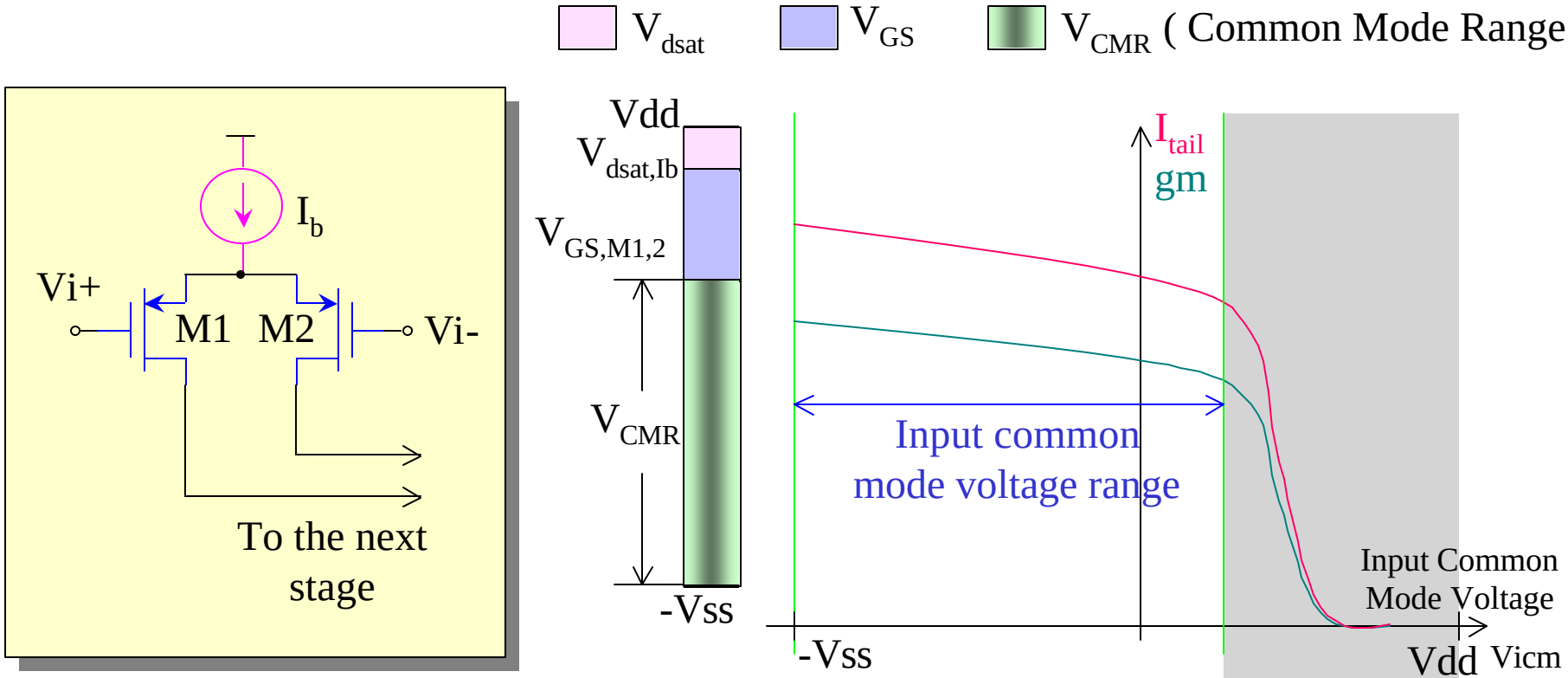
(a) P-type differential input stage



(b) N-type differential input stage

How to Obtain a Rail-to-Rail Input Common Mode Range? (cont'd)

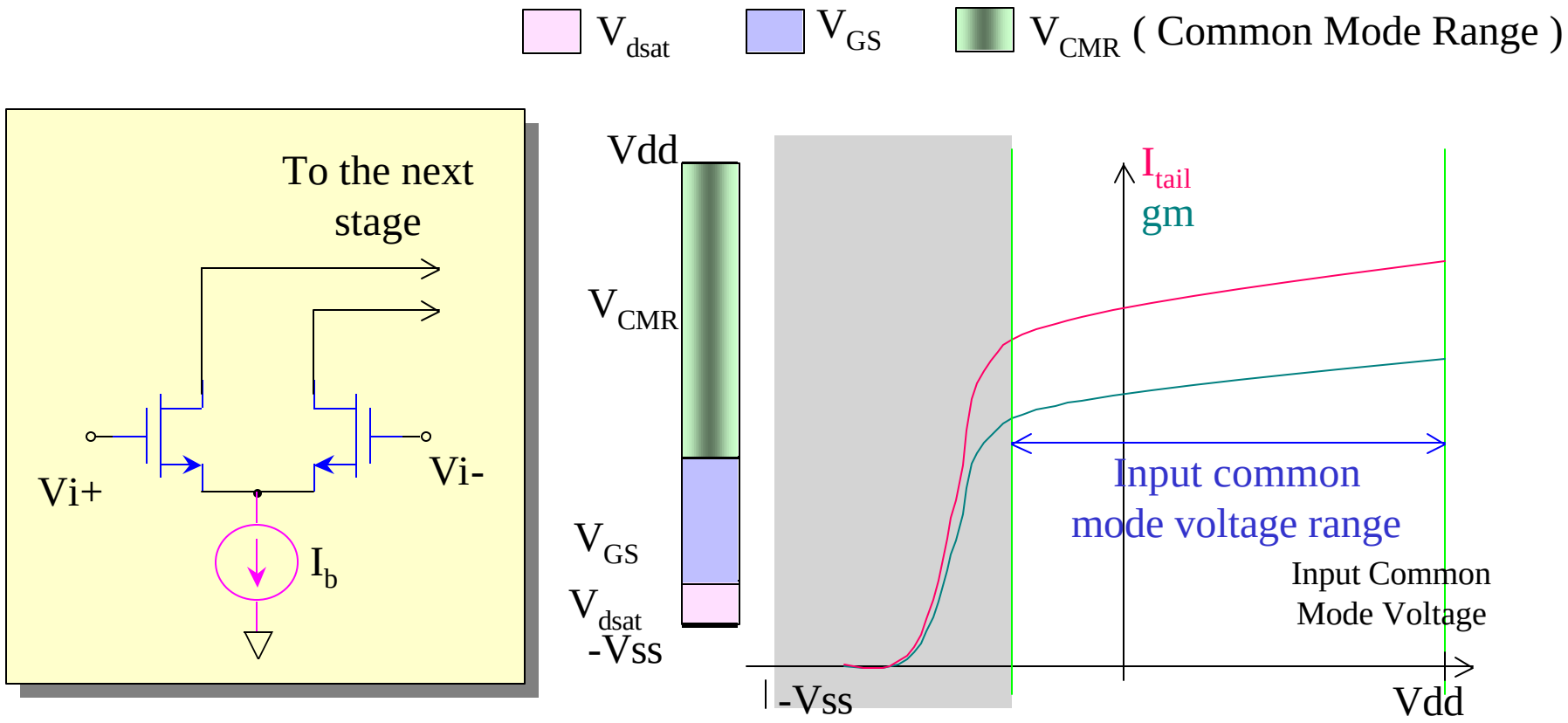
- First, let us observe how a differential pair works with different input common mode voltage
  - P-type input differential pair



Where $V_{GS}=V_{dsat}+V_T$

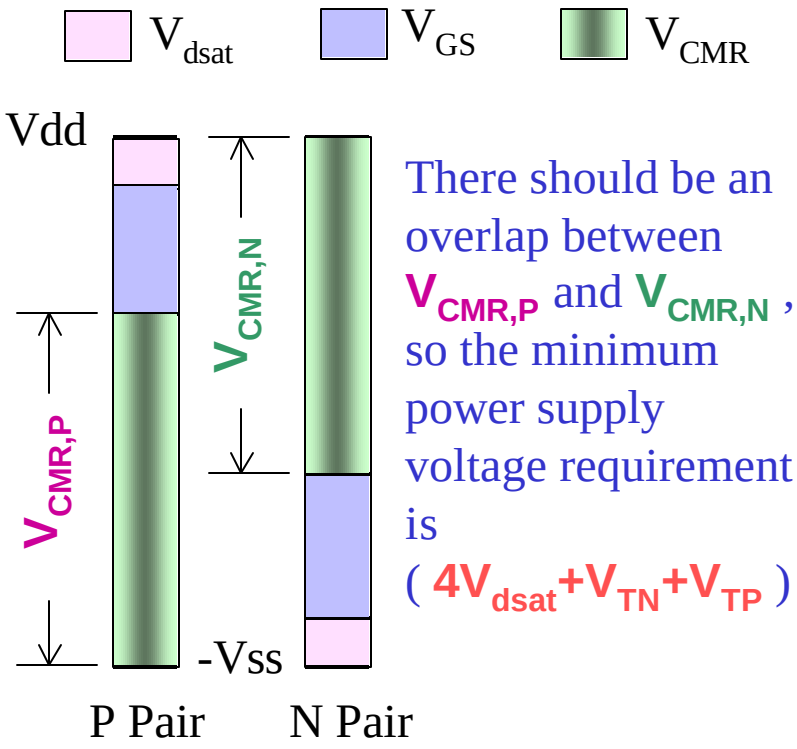
How to Obtain a Rail-to-Rail Input Common Mode Range? (cont'd)

– N-type differential input stage



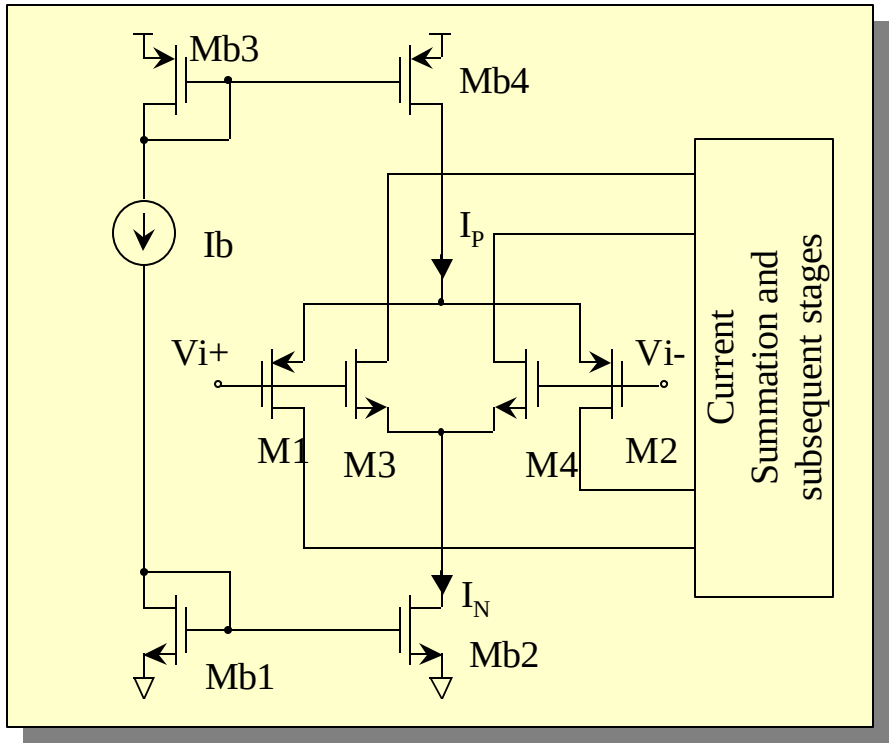
How to Obtain a Rail-to-Rail Input Common Mode Range? (cont'd)

- Why not connect these two pairs in parallel and try to get a full rail-to-rail range? Yes, this is one way!



There should be an overlap between $V_{CMR,P}$ and $V_{CMR,N}$, so the minimum power supply voltage requirement is ($4V_{dsat}+V_{TN}+V_{TP}$)

$V_{SUP} \geq 4V_{dsat}+V_{TN}+V_{TP}$

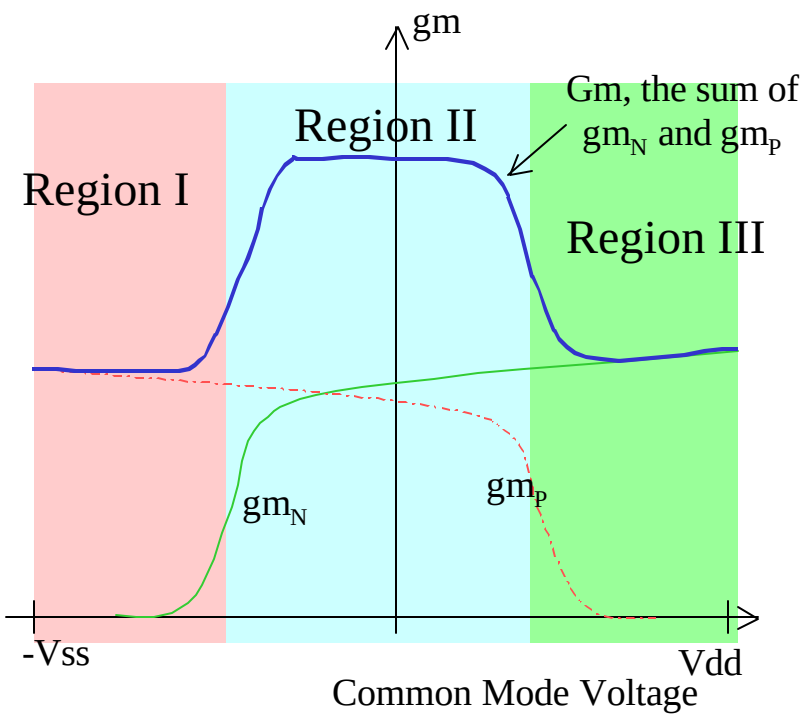


Simple N-P complementary input stage

Almost all of the rail-to-rail input stages are doing in this way by some variations! But how well does it work?

How to Obtain a Rail-to-Rail Input Common Mode Range? (cont'd)

- Transconductance vs. Vicm



The total transconductance of the input stage varies from gm to 2gm, the variation is **100%** !

- If $K = \frac{1}{2} KP_N (\frac{W}{L})_N = \frac{1}{2} KP_P (\frac{W}{L})_P$ and

  $I_N = I_P = I_{TAIL}$

  then $gm_N = gm_P = gm = \sqrt{2KI_{TAIL}}$.

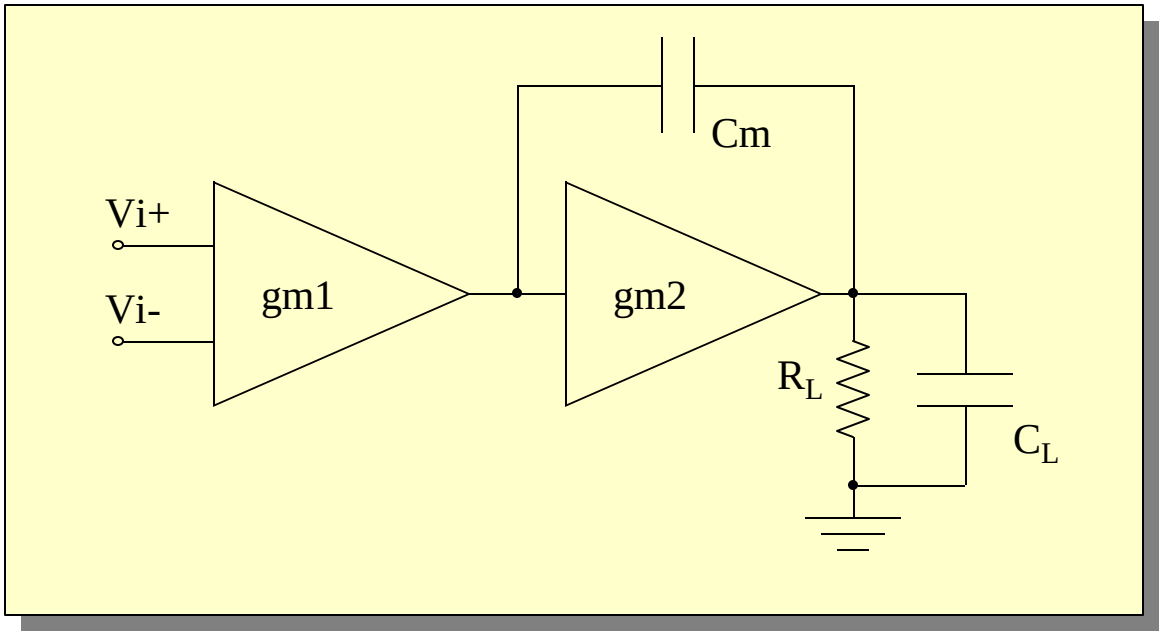
Region I. When Vicm is close to the negative rail, only P-channel pair operates.The N channel pair is off because its V_{GS} is less than V_T. The total transconductance of the differential pair is given by $gm_T = gm_P = gm$.

Region II. When Vicm is in the middle range, both of the P and N pairs operate. The total transconductance is given by $gm_T = gm_N + gm_P = 2gm$.

Region III. When Vicm is close to the positive rail, only N-channel pair operates. The total transconductance is given by $gm_T = gm_N = gm$.

Why is a Constant Gm needed ?

- The total transconductance, g_{mT}, of the input stage shown in the previous slide varies as much as twice for the common mode range!
- For an operational amplifier, constant transconductance of the input stage is very important for the functionality of the amplifier.
- As an example, we will analyze a simple 2-stage CMOS operational amplifier. The conceptual model of the amplifier is shown below.



Why is a Constant Gm needed ? (cont'd)

- The transfer function of the amplifier is given by

$$A(s) \approx \frac{g_{m1}g_{m2}(1-s\frac{C_m}{g_{m2}})}{s^2C_LC_m + sC_mg_{m2} + g_{o1}g_L} = A_0 \frac{1-s\frac{1}{z}}{s^2\frac{1}{p_1p_2} + s\frac{1}{p_1} + 1}$$

where $A_0 = \frac{g_{m1}g_{m2}}{g_{o1}g_L}$, which is the DC gain of the amplifier.

$p_1 = \frac{GBW}{A_0} = \frac{g_{m1}/C_m}{A_0}$, $p_2 = \frac{g_{m2}}{C_L}$, and $z = \frac{g_{m2}}{C_m}$,

p_1 and p_2 are the dominant pole and non-dominant pole of the amplifier respectively, and $p_1 << p_2$.

z is the zero generated by the direct high frequency path through C_m.

Why Should We Have a Constant Gm (cont'd)

GBW is the Gain BandWidth product, or the unity gain frequency of the amplifier, which is given by

$$GBW = \frac{g_{m1}}{C_m}.$$

We may notice that *GBW* changes with g_{m1}! If g_{m1} changes 2 times, the *GBW* also does so!

- To ensure the stability of the amplifier, we should maintain a sufficient phase margin. Usually, we let p_2 to be 2.5 times of GBW. Let's assume $C_m=C_L/2$, then $z=2p_2=5\times GBW$.
- If the total transconductance of the input stage, g_{m1}, varies 2 times as we have encountered in previous discussion, from *gm* to *2gm*, let us check what will happen…

Why is a Constant Gm needed ? (cont'd)

- We can change *gm* by varying some parameters of the input stage. Let us assume that we design an amplifier with sufficient phase margin when g_{m1} is low (which is now *gm*). That is

$$p_2 = \frac{g_{m2}}{C_L} = 2.5GBW_{LOW} = 2.5\frac{g_{m1,LOW}}{C_m} = 2.5\frac{gm}{C_m},$$

  - When g_{m1}=*gm*, we can get that the phase margin as **57**°, which is sufficient to ensure the stability of the amplifier.
  - When the g_{m1} is at its maximum value, *2gm*, the *GBW* doubles, at this point, the phase margin changes to **29**° ! It is not enough and the amplifier may be unstable and may become an oscillator!!

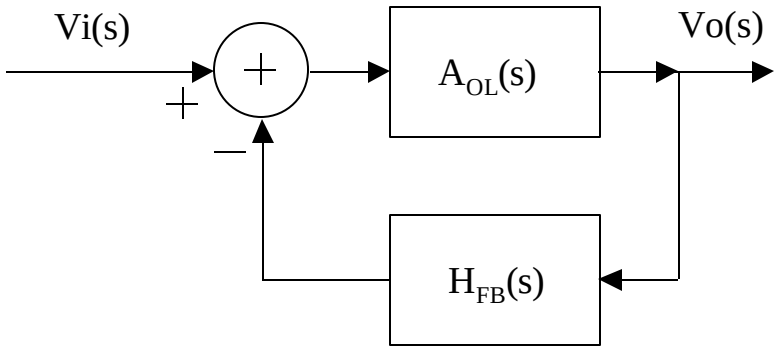
- Of course we can do in another way that, when g_{m1} is *2gm*, we design the amplifier with sufficient phase margin, which means,

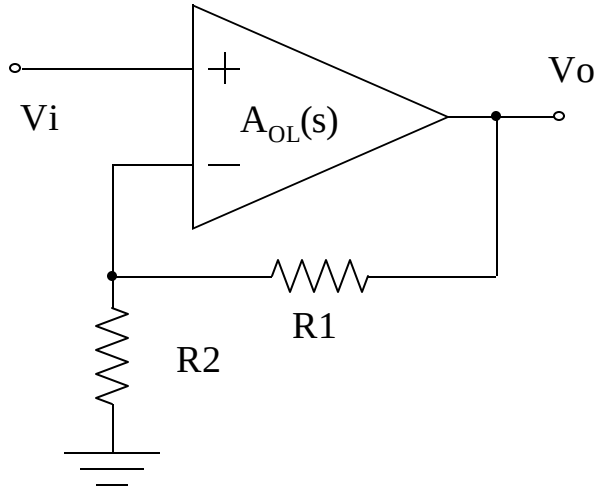
$$p_2 = \frac{g_{m2}}{C_L} = 2.5GBW_{HIGH} = 2.5\frac{g_{m1,HIGH}}{C_m} = 5\frac{gm}{C_m},$$

(cont'd)

We have to push g_{m2} to 2 times of its original value in previous case! It means **more power**, and may reach near the limitation of the process, that is we can only design an amplifier with **50% of the GBW** that a specific process permits. Of course, we do not want either of these two!

- So, transconductance variation of input stage is not desirable, it prevents the optimal frequency compensation of the amplifier. There are other negative effects of the changing transconductance. For instance, gm variation may introduce extra harmonic distortion because of the changing voltage gain.
  - Let us consider a feedback voltage amplifier with input gm variation. As shown in the next slide.
  - Assume the open loop gain of the Op Amp is $A_{OL}(s)$, and the transfer function of feedback branch is $H_{FB}(s)$. The close loop gain of the amplifier is defined by





$$A_{CL}(s) = \frac{1}{H_{FB}(s) + \frac{1}{A_{OL}(s)}}$$

- For the practical case, close loop gain of the amplifier in the right figure is given by

$$A_{CL}(s) = \frac{1}{H_{FB} + \frac{1}{A_{OL}(s)}}, \text{ where } H_{FB} = \frac{R_2}{R_1 + R_2},$$

- $A_{CL}(s)$ changes if $A_{OL}(s)$ varies with the input voltage, although to a less extent, which will introduce some nonlinear distortion at the output, especially at higher frequencies when $A_{OL}(s)$ is low.

- In summary, We need a **constant** transconductance for the input stage!

- In the following, we will study some structures of constant-gm N-P complementary input stage.

Techniques for N-P Complementary Rail-to-Rail Input Stage

There are several constant gm rail-to-rail input stage structures in literature, we will do a review from their implementation basic ideas

1. For input stages with input transistors working in weak-inversion region, using current complementary circuit to keep the sum of I_N and I_P constant [1][2][6];

2. Using square root circuit to keep $(\sqrt{I_p}+\sqrt{I_n})$ constant [3][13][16];

3. and 4. Using current switches to change the tail current of input differential pairs [3][4][5][6];

5. Using hex-pair structure to control the tail currents of backup pairs [7];

Techniques for N-P Complementary Rail-to-Rail Input Stage (cont'd)

6. Using maximum/minimum selection circuit to conduct the output current of the differential pair with larger current, as well as larger gm, to the next stage [8][9];

7. Using electronic zener diode to keep $V_{GSn} + |V_{GSp}|$ constant [10];

8. Using DC level shift circuit to change the input DC level [11].

   We will analyze them one by one in the following sections.

   There are still other techniques [12][14][15][17][18], interested readers may check these references.

Note: Unless explicitly stated in this notes, we assume that the square law characteristic of MOS transistors in strong inversion and saturation region. Please notice that for short channel transistors in sub-micron processes, square law is not exactly followed.

Rail-to-Rail Input Stage, Structure 1 [1][2][6]

- For input stages with input transistors working in weak-inversion region, using current complement circuit to keep the sum of I_N and I_P constant
- Basic idea
  - For CMOS transistors working in weak-inversion region,

$$I_{Dwi} = \frac{W}{L} I_{D0} \exp(\frac{V_{GS}}{nKT/q})$$

$$g_{mwi} = \frac{W}{L} \frac{I_{D0}}{nKT/q} \exp(\frac{V_{GS}}{nKT/q}) = \frac{I_{Dwi}}{nKT/q} = k \cdot I_{Dwi}$$

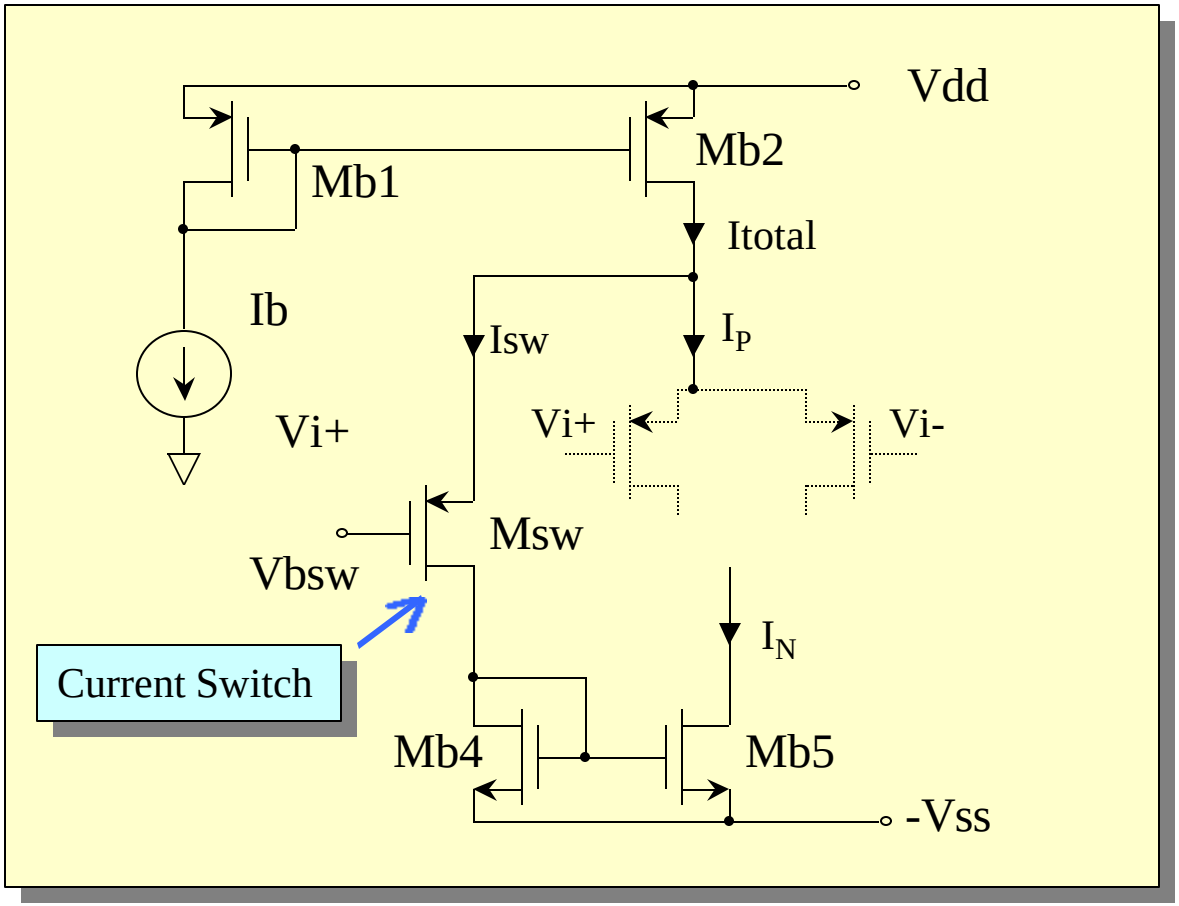
  - So, the total transconductance of the input stage is

$$g_{mT} = g_{mN} + g_{mP} = k(I_N + I_P)$$

Rail-to-Rail Input Stage, Structure 1 (cont'd)

- Thus the transconductance of the input stage is proportional to the sum of the tail currents of N and P pairs.

- The following circuit can keep (I_N+I_P) constant.



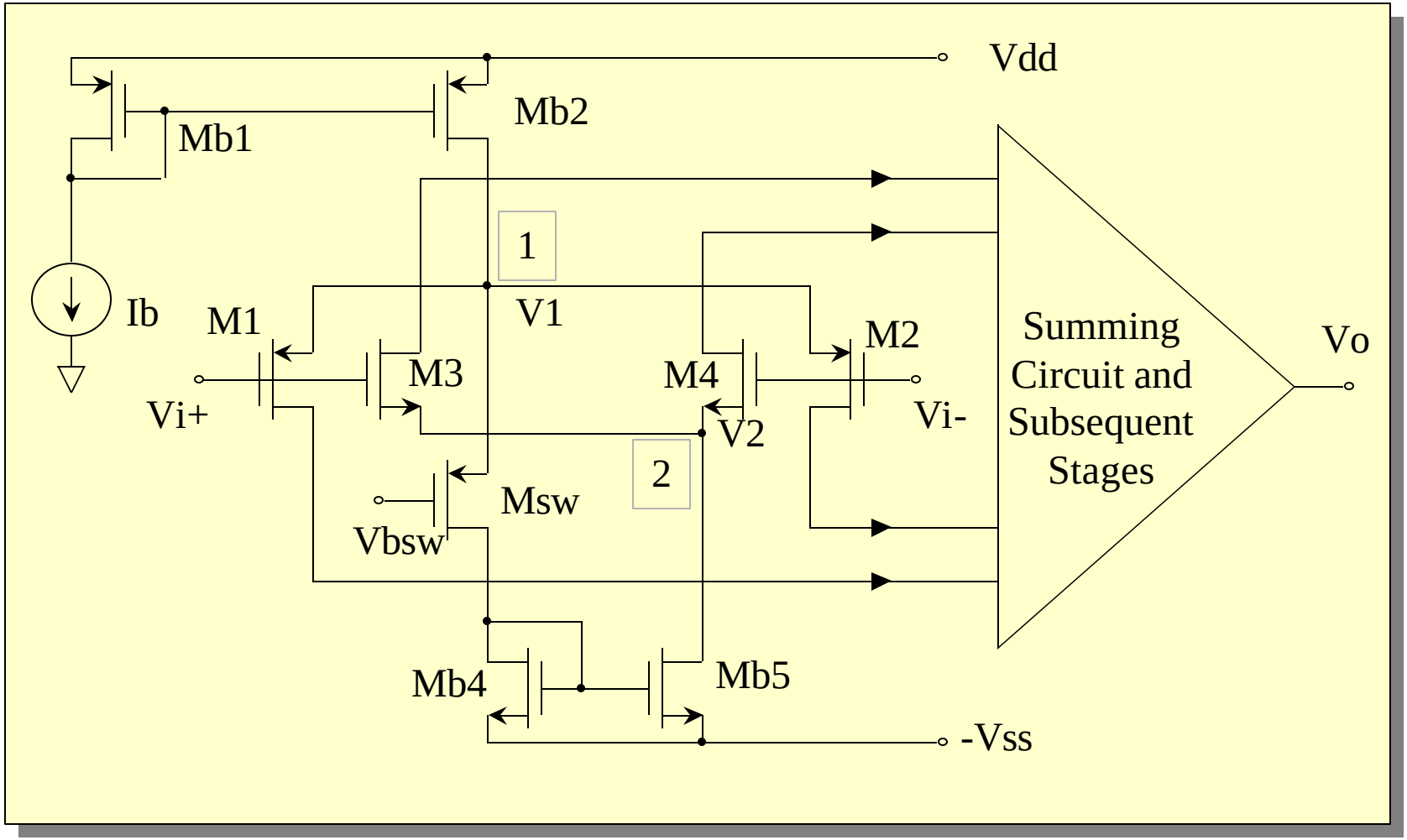
Rail-to-Rail Input Stage, Structure 1 (cont'd)

- Mb4 and Mb5 mirror the current through Msw, Isw, to provide the tail current of the N-channel input pair. Mb4 and Mb5 are with the same geometry.
- Mb2 always works in saturation region, and never to ohmic region, by properly selecting the gate biasing voltage Vbsw of Msw.
- Msw works as a current switch.
  - When the input common mode voltage, Vicm, is close to Vdd, the P input pair cuts off, the drain current of Mb2, I_{total} is diverted to Msw. And then mirrored through Mb4 and Mb5, to the source node of the N input pair.
  - When Vicm is close to -Vss, the switch Msw cuts off, I_{total} then flows to the P input pair.
  - In between, part of I_{tail} flows to P pair, and the rest to Msw, through current mirror Mb4 and Mb5, to the N pair.
- Using a first order approximation, the following equation stands,

$$I_p + I_n = I_{tail} = \text{const}$$

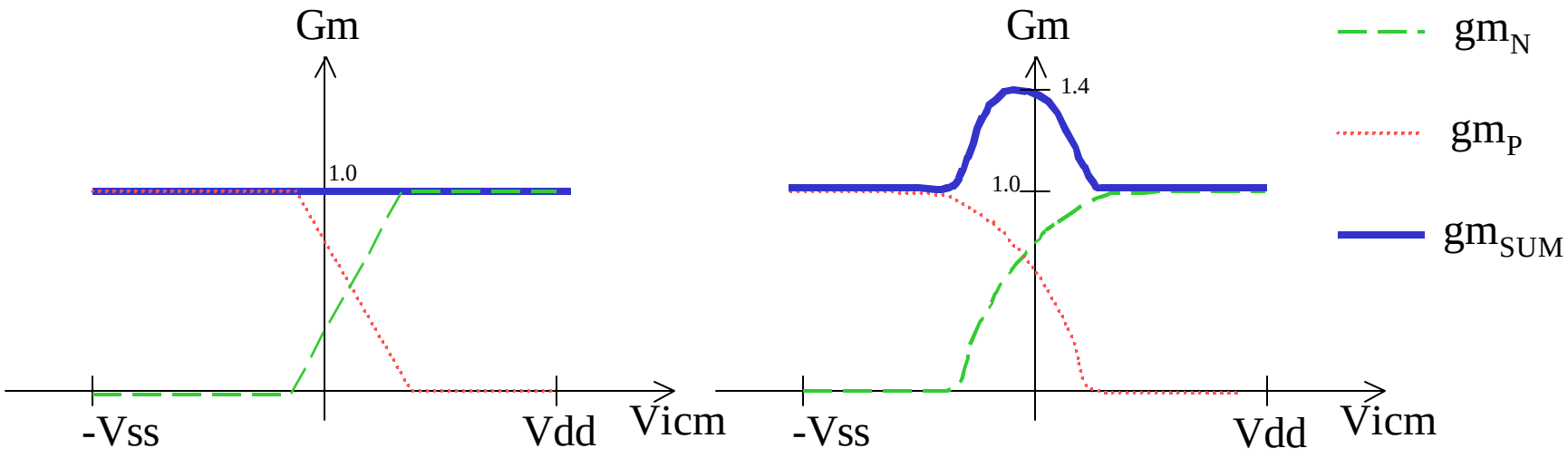
Rail-to-Rail Input Stage, Structure 1 (cont'd)

- The complete circuit



Rail-to-Rail Input Stage, Structure 1 (cont'd)

- Transconductance vs. input common mode voltage



(a) Input transistors working in weak inversion region

(b) Input transistors working in strong inversion region

Rail-to-Rail Input Stage, Structure 1 (cont'd)

- Discussion
  - This circuit is based on **bipolar** rail-to-rail input stage [1].
  - It has a rail-to-rail constant transconductance only when the input pairs work in **weak inversion** region [2].
  - If the input pairs are in **strong inversion** region, the transconductance will change by a factor of **1.4** ($\sqrt{2}$).
  - The **area is large**, which is necessary to make the input transistors work in weak inversion region.
  - As working in weak inversion region is a requirement to get a rail-to-rail constant transconductance, this structure only applies to amplifiers with **low GBW**.

Rail-to-Rail Input Stage, Structure 2 [3][13*][16]

- Using square root circuit to keep $(\sqrt{I_p}+\sqrt{I_n})$ constant
- Basic idea
  - For an input differential pair, using a 1st order approximation,

$$gm=\sqrt{2K_P(W/L)I_D}=\sqrt{K_P(W/L)I_{TAIL}}$$

Where the I_{TAIL} is the tail current of the differential pair. We can change gm by altering the tail current of the differential pair!

  - The total transconductance of the input stage is given by

$$gm_T=gm_N+gm_P=\sqrt{KP_N(W/L)_N I_N}+\sqrt{KP_P(W/L)_P I_P}$$

If $KP_N(W/L)_N = KP_P(W/L)_P=2K$

We can get

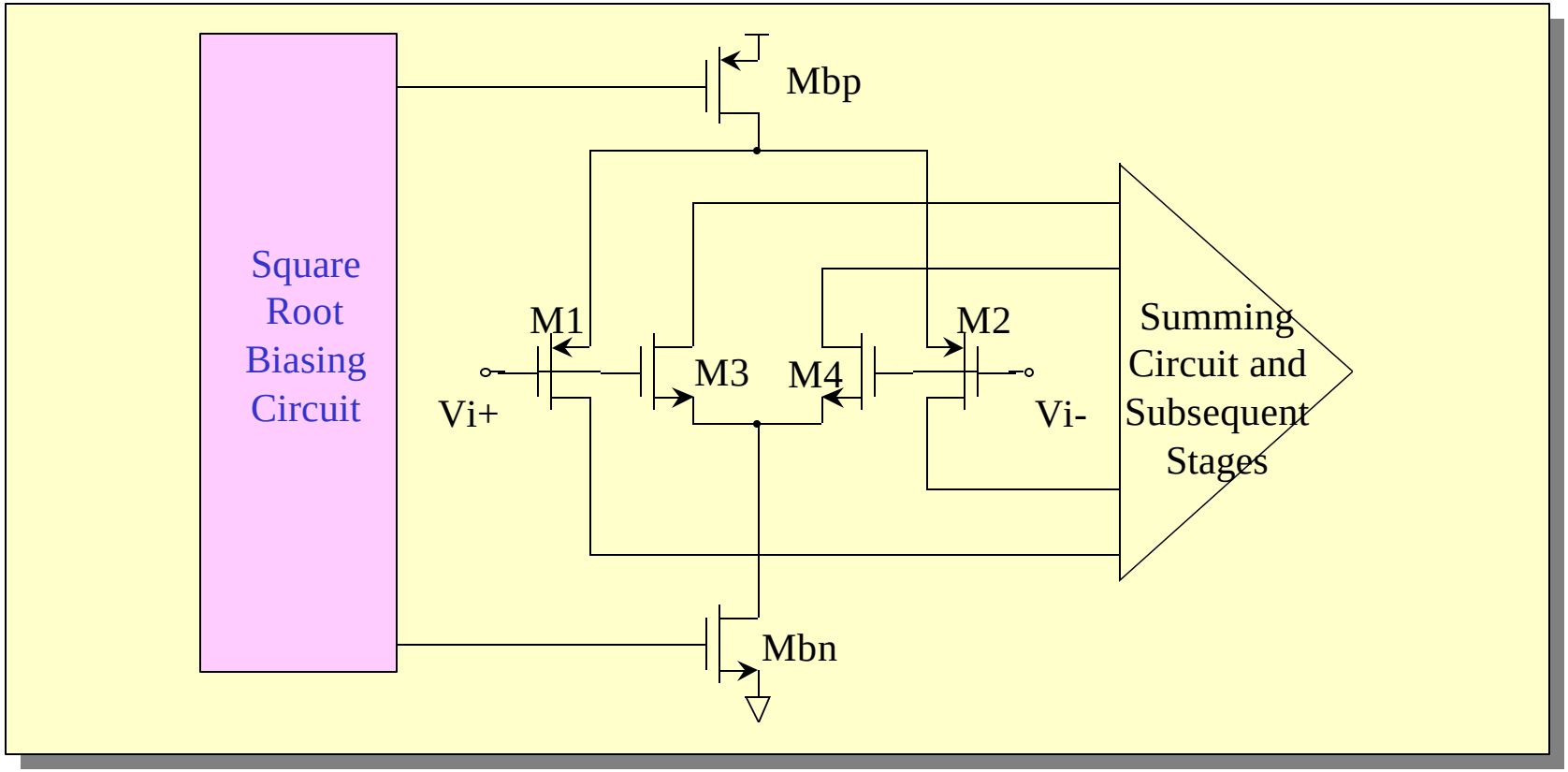
$$gm_T=gm_N+gm_P=\sqrt{2K}(\sqrt{I_N}+\sqrt{I_P})$$

  - To keep gm_T contant, we just need to keep $(\sqrt{I_N}+\sqrt{I_P})$ contant!

*:[13] is an improved version of this scheme, in [13] $KP_N(W/L)_N=KP_P(W/L)_P$ is not required. The authors presented techniques to compensate KP variations.

Rail-to-Rail Input Stage, Structure 2 (cont'd)

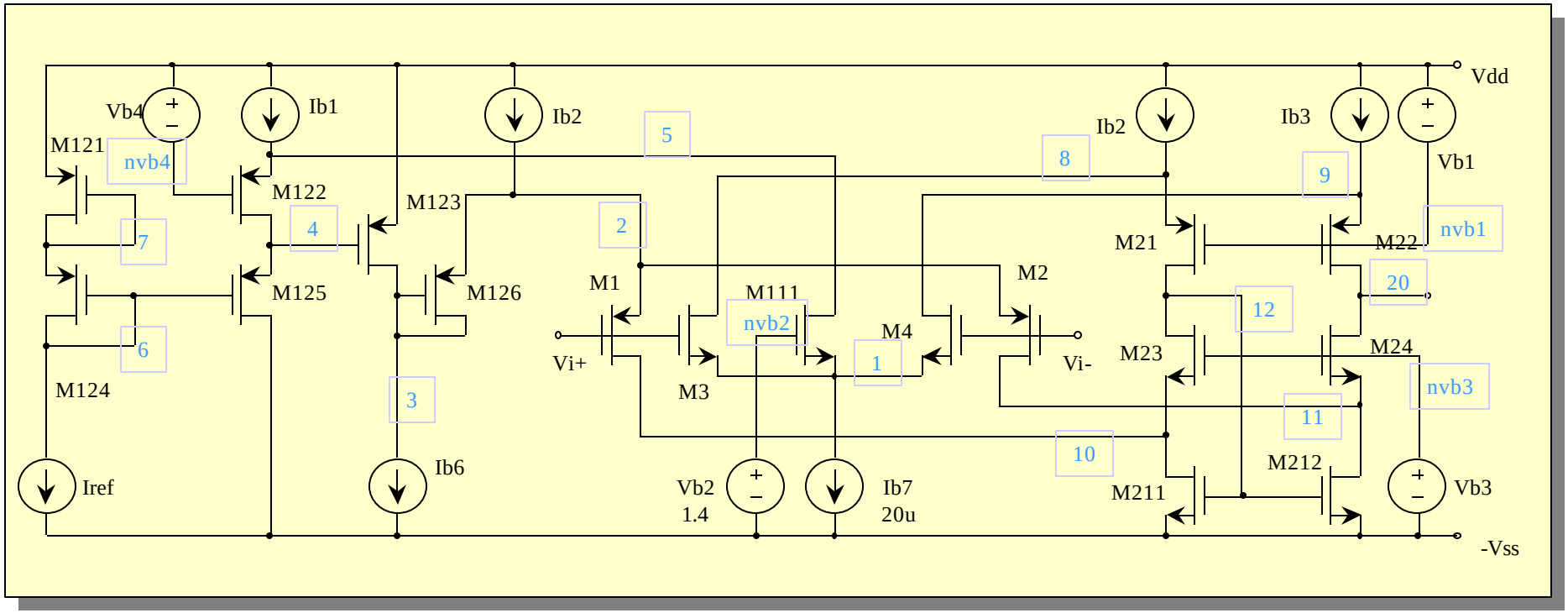
- Block diagram



- We can utilize the square law characteristic of MOS transistors to implement the square root biasing circuit.

Rail-to-Rail Input Stage, Structure 2 (cont'd)

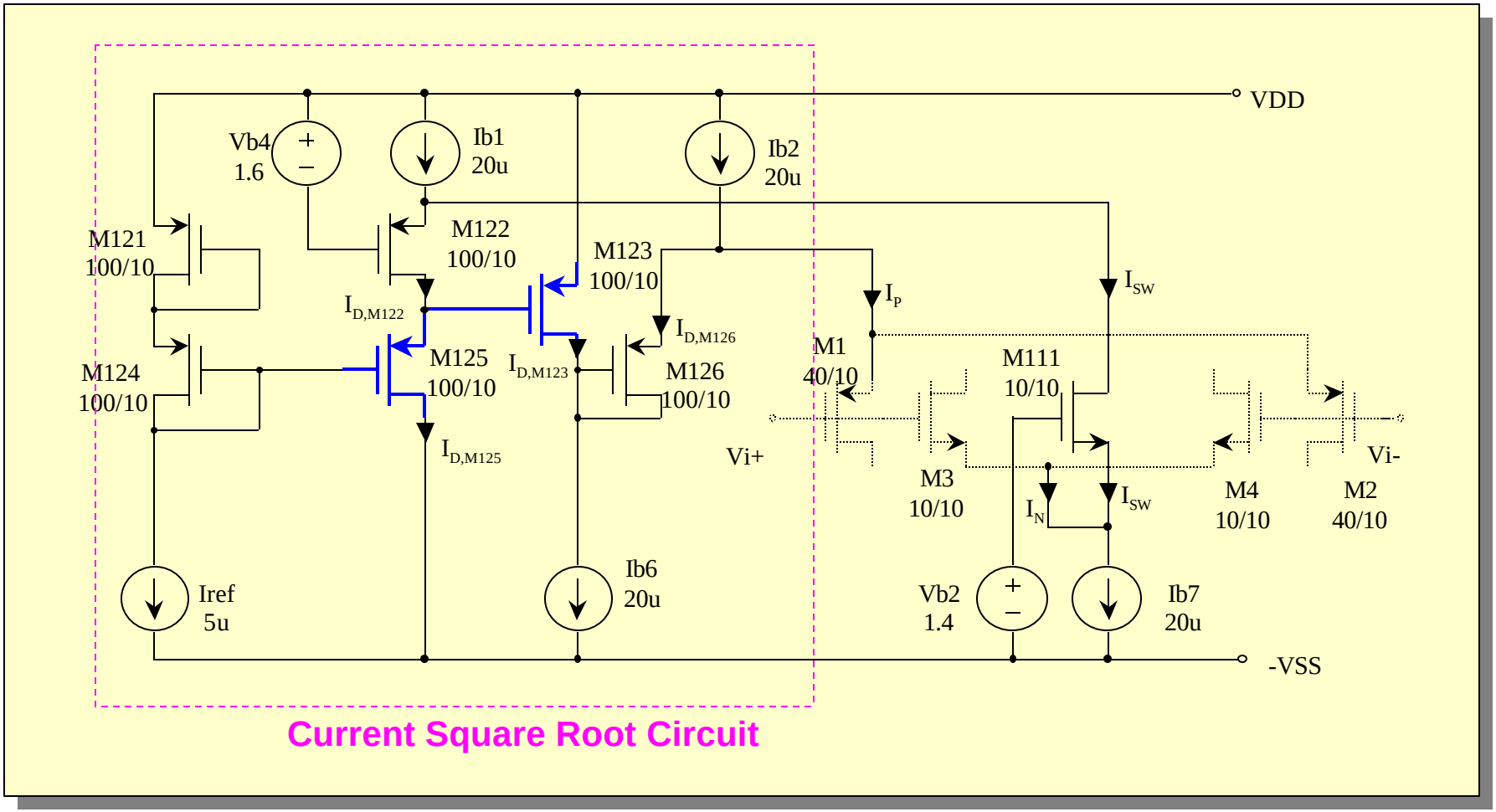
- The following is one implementation of the rail-to-rail input stage with square root biasing circuit [3].



N-P complementary input stage with square-root circuit

Rail-to-Rail Input Stage, Structure 2 (cont'd)

- Simplified Circuit



Rail-to-Rail Input Stage, Structure 2 (cont'd)

- Analysis

1. $V_{SG,M123} + V_{SG,M125} = V_{SG,M121} + V_{SG,M124} = const$,

   $V_{SG} = \sqrt{\frac{2I_D}{KP_P(W/L)}} + |V_{TP}|$, as $(W/L)_{M125}=(W/L)_{M123}=(W/L)_{M125,123}$,

   so $\sqrt{\frac{2I_{D,M123}}{KP_P(W/L)_{M123,125}}} + |V_{TP}| + \sqrt{\frac{2I_{D,M125}}{KP_P(W/L)_{M123,125}}} + |V_{TP}| = const$, that is $\sqrt{I_{D,M123}} + \sqrt{I_{D,M125}} = const_2$
2. $I_N+I_{SW}=I_{b7}=I_b$, $I_{D,M122}+ I_{SW}= I_{b1}=I_b$, and $I_{D,M122}= I_{D,M125}$ → $I_N= I_{D,M125}$
3. $I_{D,M123}+ I_{D,M126}= I_{b6}=I_b$, $I_{D,M126}+ I_P= I_{b2}=I_b$, → $I_P= I_{D,M123}$
4. From 1. to 3., we can obtain $\sqrt{I_N} + \sqrt{I_P} = const_2$
5. If M121~M124 are with the same geometry, further calculation yields

   $\sqrt{I_N} + \sqrt{I_P} = 2\sqrt{I_{D,M121,124}} = 2\sqrt{I_{ref}}$

Rail-to-Rail Input Stage, Structure 2 (cont'd)

- Working Principle
  - The input transistors work in strong inversion region.
  - The square-root circuit M121-M125 keeps the sum of the square-roots of the tail currents of the input pairs and then the gm constant.
  - The current switch, M111, compares the common-mode input voltage with Vb3 and decides which part of the current Ib7 should be diverted to the square-root circuit.
  - In the common-mode input voltage range from Vdd to -Vss+1.8V only the N channel pair operates. The current switch M111 is off and thus the tail current of the N channel input pair I_N equals Ib7=4Iref=20uA.
  - The sum of the gate-source voltages of M123 and M125 is equal to reference voltage which is realized by M121 and M124. Since the current through M125 equals I_N and the current through M123 equals the tail current of the P channel input pair I_P.

Rail-to-Rail Input Stage, Structure 2 (cont'd)

- It can be calculated that the square-root of Ip is given by

$$\sqrt{I_P} = 2\sqrt{I_{ref}} - \sqrt{I_N}$$

  Where it is assumed that M121 to M125 are matched.

- In the common-mode input range from -Vss+1.2V to Vss only the P channel input pair operates. In this range the current Ib7=4Iref=20uA flows through the current switch to the square-root circuit. Thus, the current through M125 is nearly zero which means that its gate-source voltage is smaller than its threshold voltage.
- If the current through M123 is larger than 4Iref=20uA, the current limiter M126 limits the current of M123 to 4Iref=20uA and directs it to the P channel input pair.
- It can be calculated that the transconductance of the input stage, and therefore the unity-gain frequency, is constant within the rail-to-rail input common mode range. The gm is defined by

$$gm = 2\sqrt{2KIref} \quad \text{where} \quad K = \frac{1}{2}KP_N\left(\frac{W}{L}\right)_N = \frac{1}{2}KP_P\left(\frac{W}{L}\right)_P$$

Rail-to-Rail Input Stage, Structure 2 (cont'd)

- The summing circuit M21-M24 adds the output signals of the complementary input stage, and forms the output voltage at node #20.

- Discussion
  - The circuit is somewhat complex and the functionality relies on the square law of MOS transistors. For current sub-micron processes, the square law is not closely followed, which may introduce large error for the total transconductance.

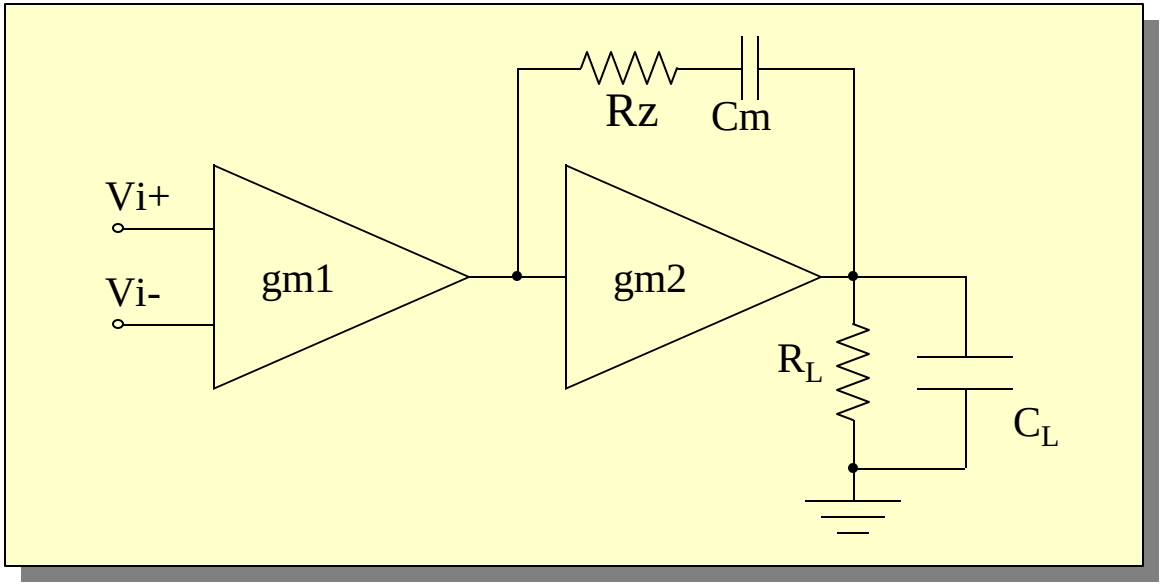
Rail-to-Rail Op Amp Design

Let us design a rail-to-rail input Op Amp with the following specifications utilizing rail-to-rail input stage Structure 2.

Process	MOSIS AMI 1.2u
Power Supply (Vsup)	±1.65V
Load Resistance (R_L)	20 KΩ
Load Capacitance (C_L)	20pF
Power Dissipation (P_D)	<1mW
DC Gain (Av_0)	≥80dB
Gain Bandwidth Product (GBW)	≥1MHz
Phase Margin (PM)	≥50°
Slew Rate (SR)	≥2V/μS
Input Common Mode Range (CMR)	rail-to-rail
Output Voltage Range	-1.45 ~ 1.45 V
Output Stage	Simple Class A

Rail-to-Rail Op Amp Design (cont'd)

- The block diagram of the 2-stage operational amplifier is shown in the following



  - We add Rz in this diagram compared with the figure in slide #8, which is used to cancel the zero generated by Cm. When Rz=1/gm2, the zero is cancelled.

Rail-to-Rail Op Amp Design (cont'd)

– When Rz=1/gm2, the transfer characteristics of the amplifier is given by

$$A(s) \approx \frac{g_{m1}g_{m2}}{s^2 C_L C_m + sC_m g_{m2} + g_{o1}g_L} = \frac{A_0}{s^2 \frac{1}{p_1 p_2} + s\frac{1}{p_1} + 1}$$

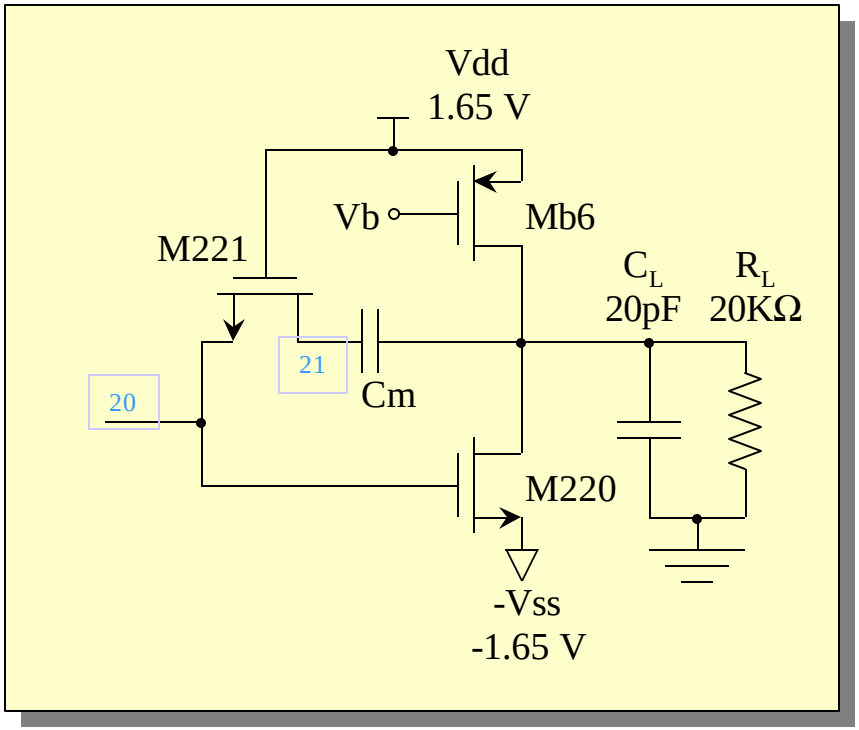
where $A_0 = \frac{g_{m1}g_{m2}}{g_{o1}g_L}$, $p_1 = \frac{GBW}{A_0} = \frac{g_{m1}/C_m}{A_0}$, $p_2 = \frac{g_{m2}}{C_L}$,

and $GBW = \frac{g_{m1}}{C_m}$.

- The rail-to-rail input stage of the amplifier is shown on slide #25.

Rail-to-Rail Op Amp Design (cont'd)

- The second stage, or output stage, of the amplifier (M220 and Mb6) is a simple inverter with Miller frequency compensation (Cm and M221).



M221 is a MOSFET which works in linear region, taking the role of Rz.
Mb6 works as a current source.

Rail-to-Rail Op Amp Design (cont'd)

- **Design procedure**

1) Tail current and input transistors

$GBW(rad/s) = \frac{g_{m1}}{C_m}$, Let $C_m = \frac{1}{2}C_L$, then we can get

$g_{m1} = GBW \times C_m = 2p \times 1MHz \times 10\,pF = 62.8mA/V$,

To leave some margin for the GBW, let g_{m1}=*80mA/V*.

$SR = \frac{I_{TAIL}}{C_m}$, so

$I_{TAIL} = SR \times C_m = 2V/mS \times 10\,pF = 20mA$, let $I_{TAIL} = 25mA$.

For P pair

$$(W/L)_{P-PAIR} = \frac{g_{m1}^{\ 2}}{2K_{PP}I_D} = \frac{g_{m1}^{\ 2}}{K_{PP}I_{TAIL}} = \frac{(80mA/V)^2}{1.9346 \times 10^{-5} A/V^2 \times 25mA} = 13.23$$

To make layout convenient, we choose $(W/L)_{P-PAIR} = 16$.

Rail-to-Rail Op Amp Design (cont'd)

To make layout convenient, we choose $(W/L)_{P-PAIR}=16$.

To make N pair and P pair be symmetrical, we should let

$$K_{PN}(\frac{W}{L})_{N-PAIR}=K_{PP}(\frac{W}{L})_{P-PAIR}\text{, so}$$

$$(\frac{W}{L})_{N-PAIR}=(\frac{W}{L})_{P-PAIR}\frac{K_{PP}}{K_{PN}}=16\times\frac{1.9346\times10^{-5}A/V^2}{7.3584\times10^{-5}A/V^2}=4.207\text{, choose}$$

$$(\frac{W}{L})_{N-PAIR}=4.$$

For current sources I_{b1}, I_{b2}, I_{b3}, I_{b4}, I_{b6}, and I_{b7} are all with the same value I_{TAIL}=25μA. I_{ref} is I_{TAIL}/4=6.25μA.

2) Current switch M_{111}

M111 works in saturation region when it is on and cut off region when it is off as the common mode voltage swings from rail-to-rail.

The V_{GS} of switch transistor controls the current transition region width with the common mode voltage. There are some disadvantages if the transition region is too narrow. We choose $V_{dsat,M111}$=0.5V when all of the current I_{b7} flows through M_{111}.

Rail-to-Rail Op Amp Design (cont'd)

$$(\frac{W}{L})_{M111} = \frac{2I_D}{K_{PN}V_{dsat,M111}{}^2} = \frac{2\times 25mA}{7.3584\times 10^{-5}A/V^2\times(0.5V)^2} = 2.718\,,$$

Let $(\frac{W}{L})_{M111} = 3$.

3) Square root circuit, M_{121}-M_{126}

We should select a proper working point for this part of circuit to obtain a good square root characteristic. If the overdrive voltage $V_{ov}=V_{dsat}$ = (V_{GS}-V_T) is too low, the MOSFET may work near the transition region, which is between strong inversion and weak inversion region.
If V_{ov} is too large, because of velocity saturation effect, the I_{DS} vs. V_{DS} characteristic may become somewhat near linear rather than quadratic, which will also introduce some error.

Let us select V_{ov}=0.3V,

$$(\frac{W}{L})_{M121\sim M125} = \frac{2I_D}{K_{PP}V_{dsat}{}^2} = \frac{2\times 25mA}{1.9346\times 10^{-5}A/V^2\times(0.3V)^2} = 28.72\,,$$

Rail-to-Rail Op Amp Design (cont'd)

Choose $(\frac{W}{L})_{M121\sim M125} = 28$.

M_{126} is just a level shift transistor, its size is not critical, we just let $(\frac{W}{L})_{M126} = 28$.

4) Summing circuit, M_{21}~M_{24}, M_{211}, and M_{212}

M_3, M_{21} and bias current I_{b2} form folded cascode structure, as well as M_4, M_{22} and bias current I_{b3}. Although the quiescent current through M_{21} (M_{22}) is $I_{TAIL}/2$, its maximum current is I_{TAIL}.

Let V_{dsat} of M_{21} (M_{22}) to be 0.25V when it is conducting I_{TAIL}, we can get

$$(\frac{W}{L})_{M21,M22} = \frac{2I_D}{K_{PP}V_{dsat}^{\ 2}} = \frac{2\times 25mA}{1.9346\times 10^{-5}A/V^2\times(0.25V)^2} = 41.3522,$$

Choose $(\frac{W}{L})_{M21,M22} = 40$.

Similarly for M_{23} (M_{24}), we get $(\frac{W}{L})_{M23,M24} = 12$,

Rail-to-Rail Op Amp Design (cont'd)

The maximum drain current for M_{211} and M_{212} is $2I_{TAIL}$. We can get

$$(\frac{W}{L})_{M211,M212} = 24 .$$

5) The output stage M_{220} and M_{221}

To have an output swing from rail-to-rail, the minimum biasing current should be

$$I_{D,BIAS,\min} = I_{RL,\max} = \frac{Vdd}{R_L} = \frac{1.65V}{20K\Omega} = 82.5mA$$

To leave some margin, we choose the bias current as 100μA.

To have a rail-to-rail swing from V_{dd}-0.2V to $-V_{ss}$+0.2V as required by the design specification, we should have a small V_{dsat} for the M_{220}, we choose $V_{dsat,M220}$=0.2V, the geometry ratio of M_{220} is given by

$$(\frac{W}{L})_{M220} = \frac{2I_D}{K_{PN}V_{dsat}^{\ 2}} = \frac{2\times 100mA}{7.3584\times 10^{-5}A/V^2\times(0.2V)^2} = 67.95,$$

We choose $(\frac{W}{L})_{M220} = 68 .$

Rail-to-Rail Op Amp Design (cont'd)

Let us check whether gm2 can satisfy the phase margin requirement or not. There should be $p_2 = \frac{g_{m2}}{C_L} \geq 2.5GBW$.

Let us calculate g_{m2} first,

$$g_{m2} = \sqrt{2I_D K_{PN} (\frac{W}{L})_{M220}} = \sqrt{2 \times 100mA \times 7.3584 \times 10^{-5} A/V^2 \times 68} = 1000.3mA/V$$

So

$p_2 = \frac{g_{m2}}{C_L} = \frac{1000.3mA/V}{20pF} = 50.02 \times 10^6 rad/s = 7.96MHz \geq 2.5GBW = 2.5MHz$, the phase margin specification can be satisfied.

Actually, if we ignore other higher non-dominant poles except p_2, we can calculate the phase margin as

$$PM = 180° - \tan^{-1}\frac{GBW}{p_1} - \tan^{-1}\frac{GBW}{p_2}$$

$$\approx 90° - \tan^{-1}\frac{g_{m1}/C_m}{g_{m2}/C_L} = 90° - \tan^{-1}\frac{80mA/V/10pF}{50.02 \times 10^6 rad/s} = 80.9°$$

Rail-to-Rail Op Amp Design (cont'd)

For M_{221}, which works in diode region and with bulk connected to -Vss, we can get its V_T as,

$$V_{T,M221} = V_{TO} + g(\sqrt{2|f_F| - V_{BS,M221}} - \sqrt{2|f_F|})$$

$$\overset{V_{BS,M221} = -V_{GS,M220}}{=\!=\!=\!=\!=\!=\!=\!=\!=} V_{TO} + g(\sqrt{2|f_F| + V_{GS,M220}} - \sqrt{2|f_F|})$$

$$= 0.6443V + 0.7003V^{1/2}(\sqrt{0.7V + (0.2 + 0.6443)V} - \sqrt{0.7V}) = 0.9286V$$

$$(\frac{W}{L})_{M221} = \frac{g_{m2}}{K_{PN}(V_{sup} - V_{T,M221} - V_{GS,M220})} = 8.903,$$

Choose $(\frac{W}{L})_{M221} = 9$.

6) Bias voltages Vb1, Vb3 and Vb4

a) Vb1

Assume voltage drop for Ib1 is 0.4V,

$$|V_{GS,M122}| = \sqrt{\frac{2I_D}{K_{PP}(W/L)_{M122}}} + |V_{T,M122}| = 1.209V$$

Rail-to-Rail Op Amp Design (cont'd)

Thus

$V_{b1}=V_{drop,Ib1}+|V_{GS,M122}|=1.61V$, let V_{b1}=1.6V

a) Vb2, Vb3 and Vb4

Similarly, we can calculate Vb2 as

$V_{b2}=V_{drop,Ib7}+V_{GS,M111}=1.67V$, let V_{b2}=1.7V.

For Vb3 and Vb4,

$V_{b3}=V_{drop,M211}+V_{GS,M23}=1.44V$, let V_{b3}=1.5V.

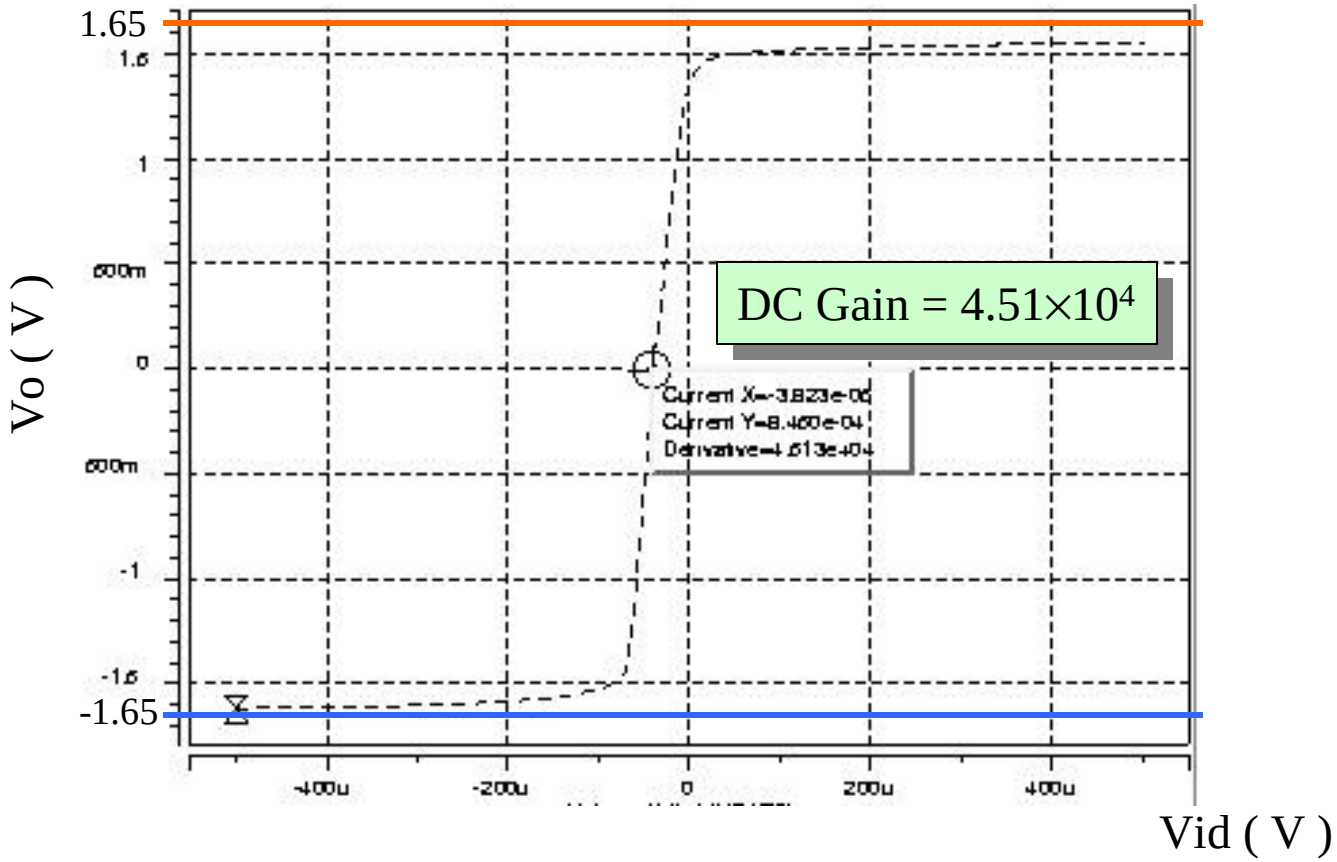
$V_{b4}=V_{drop,Ib2}+|V_{GS,M21}|=1.55V$, let V_{b4}=1.6V.

7) Modifications according to HSPICE simulation

HSPICE simulation shows that all specifications are met without any changes to the parameters calculated above, but the output voltage swing, only from –1.6V to 1.4V. Change the bias current of the output stage from 100μA to 125μA. The total power consumption increase by about 80μW to 0.938mW, but still meets the specification.

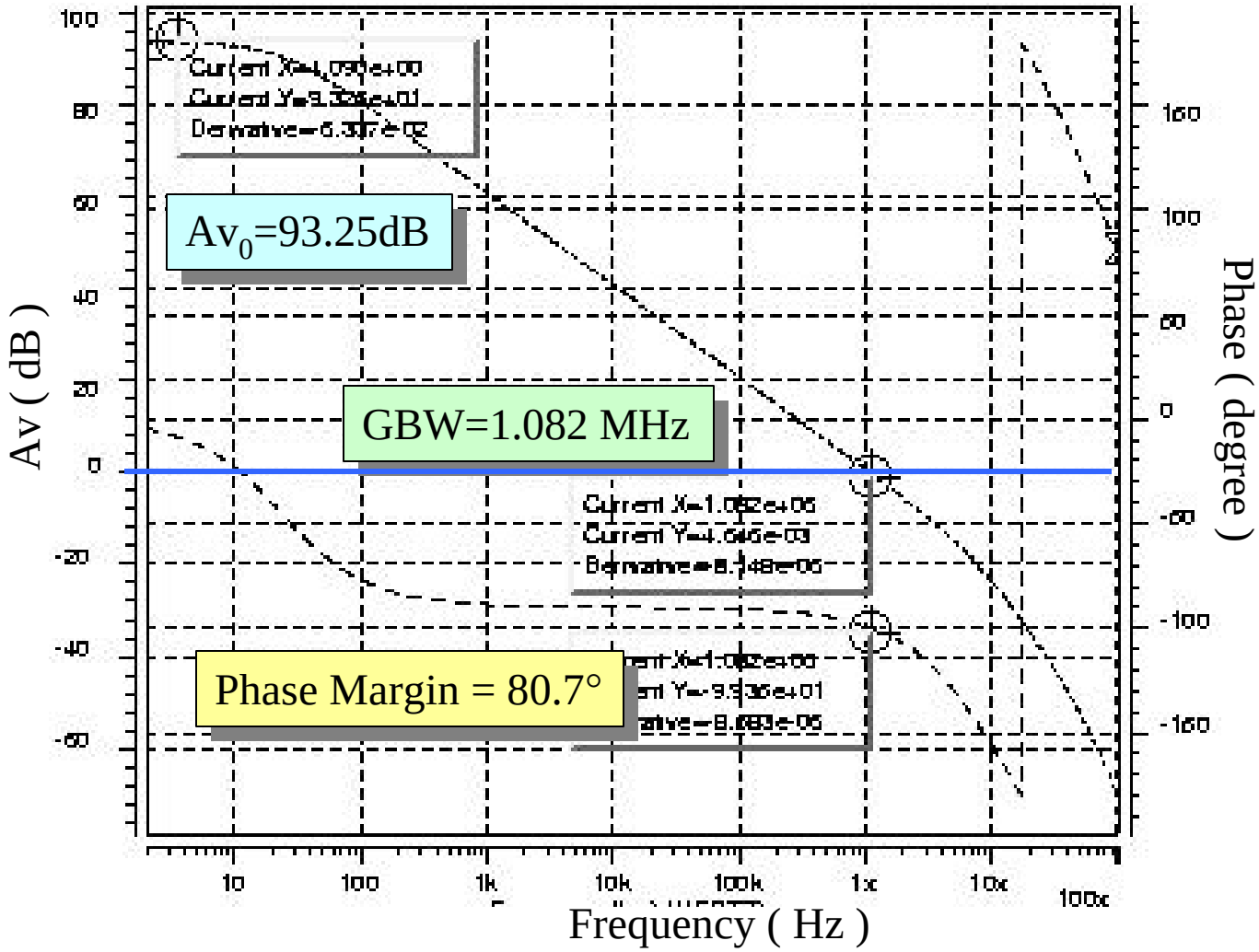
Rail-to-Rail Op Amp Simulation Results

- Simulation results
  - DC input/output characteristics



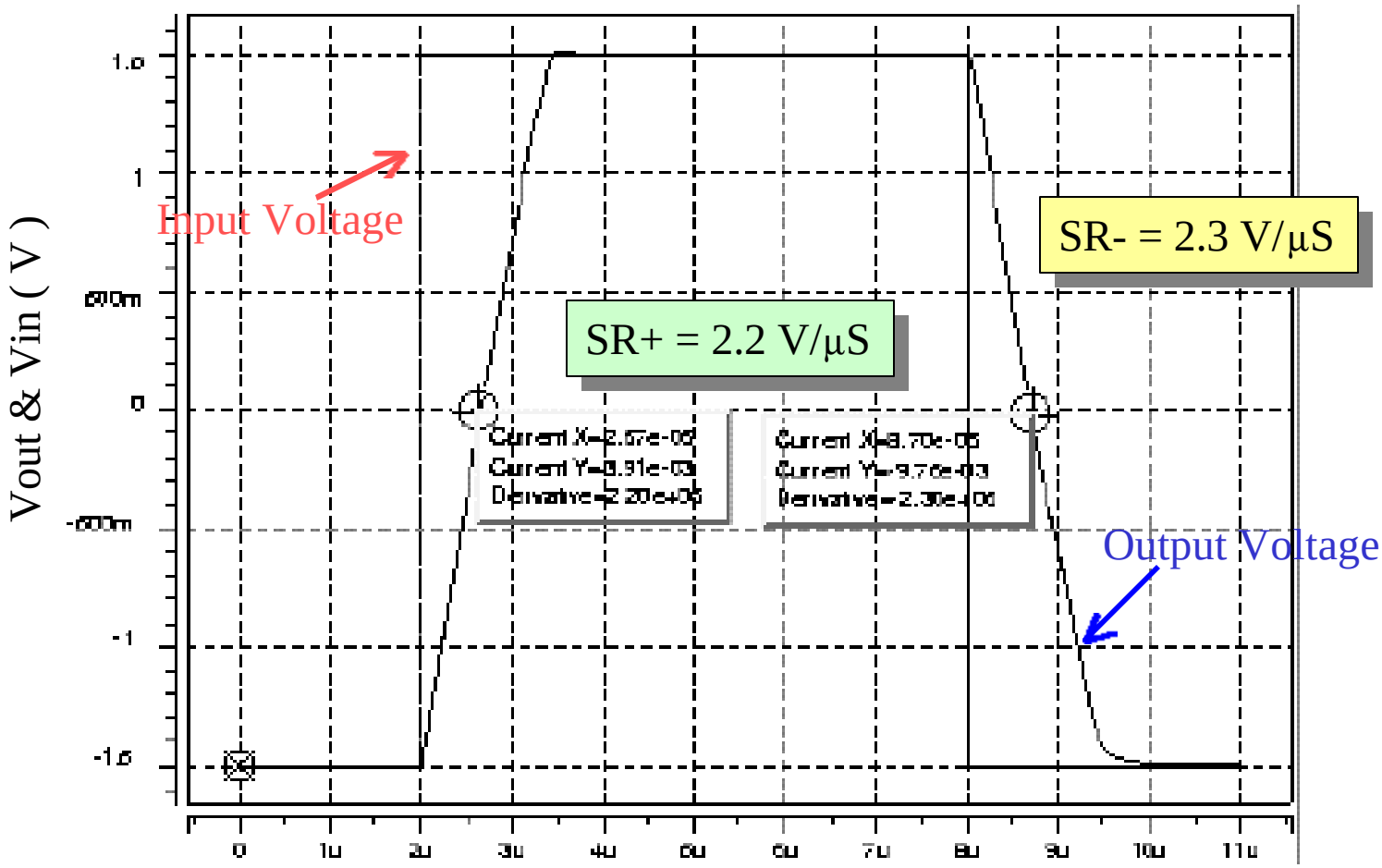
Rail-to-Rail Op Amp Simulation Results (cont'd)

– Frequency response



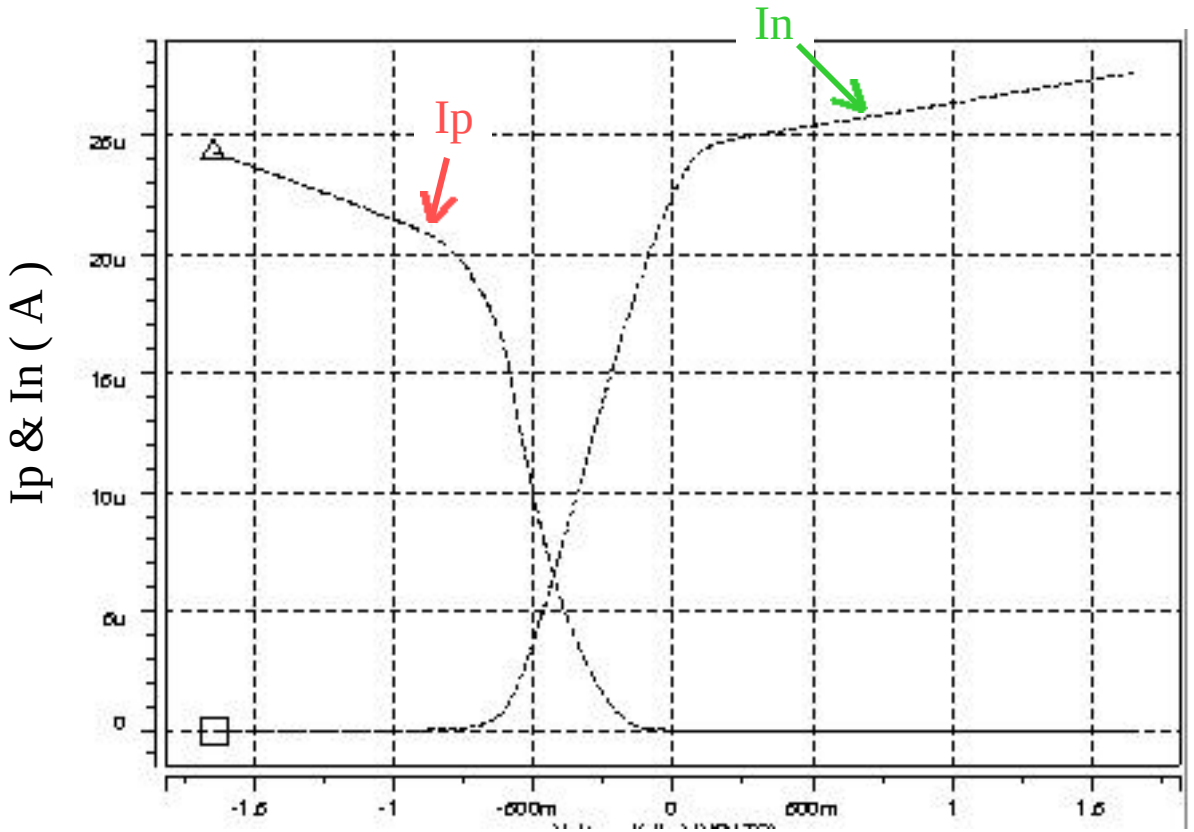
Rail-to-Rail Op Amp Simulation Results (cont'd)

– Transient response (as a unity gain buffer, output voltage swing -1.5V ~ 1.5V)



Rail-to-Rail Op Amp Simulation Results (cont'd)

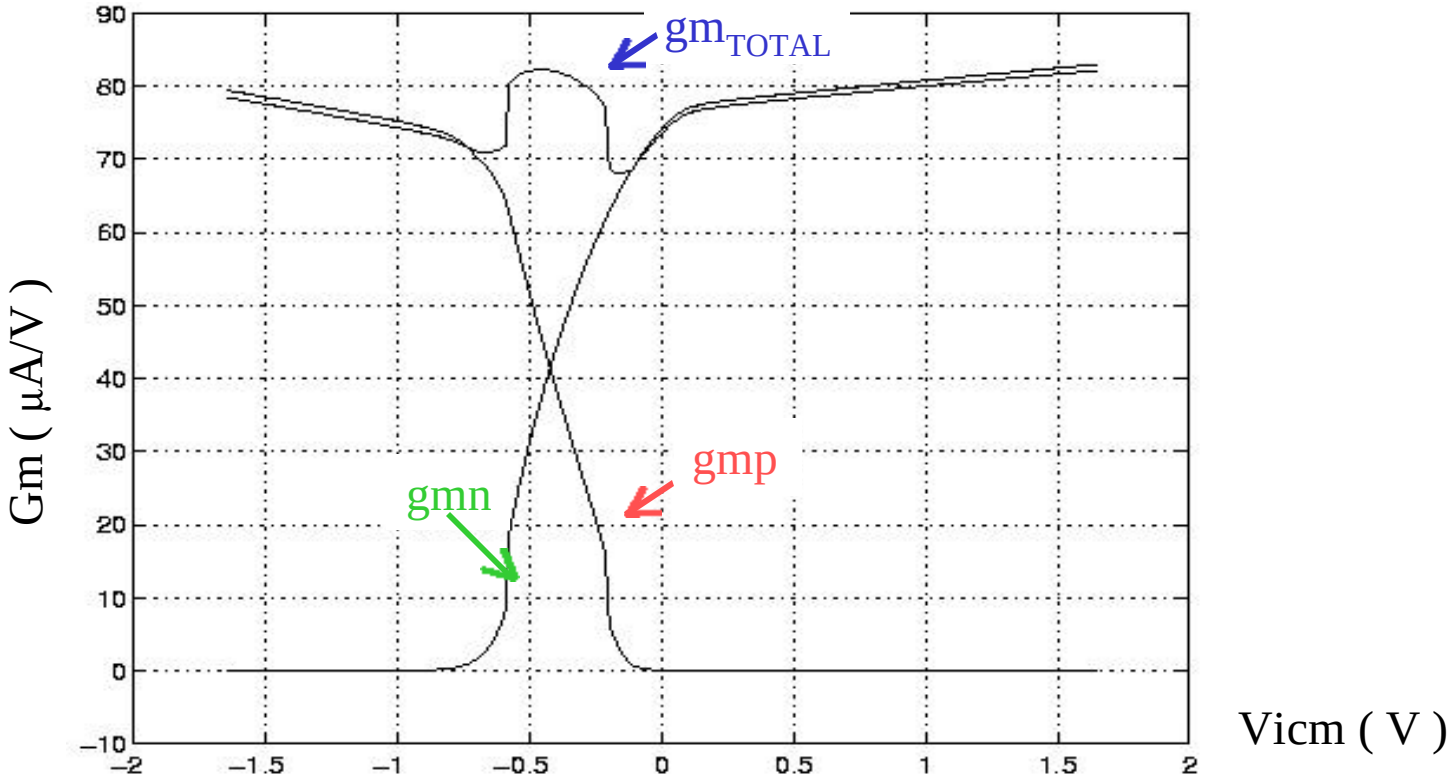
– Tail currents vs. common mode voltage



Note: The switching point can be set by Vb2 in the diagram on slide #25. The transition slope can be controlled by the (W/L) of M111.

Rail-to-Rail Op Amp Simulation Results (cont'd)

– First stage transconductance vs. common mode voltage



	Average	Minimum	Maximum
Gm_{TOTAL} (uA/V)	77.5	68.1	82.3
Deviation		-12.3%	6.2%

Rail-to-Rail Op Amp Simulation File

- HSPICE file

```
2-Stage Op Amp with Rail-to-Rail Input Structure 2

.options list node post
.include ami_n8cu_level3
.op

* Parameter definitions

.param lam = 0.6u ln = 2.4u lp=2.4u ln3=4.8u lp1=4.8u
+ wp1=76.8u wn3=19.2u wn111=7.2u wp121=67.2u wp21=96u
+ wn23=28.8u wn211=57.6u
+ wpb1=153.6u wnb7=48u wnb8=12u
+ wn220=163.2u wn221=21.6u

* Netlist

m1 10 ninm 2 2 cmosp W=wp1 L=lp1 AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'
m2 11 ninp 2 2 cmosp W=wp1 L=lp1 AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'

m3 8 ninm 1 nvss cmosn W=wn3 L=ln3 AD='5*lam*wn3' AS='5*lam*wn3'
+ PS='2*wn3+10*lam' PD='2*wn3+10*lam'
m4 9 ninp 1 nvss cmosn W=wn3 L=ln3 AD='5*lam*wn3' AS='5*lam*wn3'
+ PS='2*wn3+10*lam' PD='2*wn3+10*lam'

m111 5 nvb2 1 nvss cmosn W=wn111 L=ln AD='5*lam*wn111' AS='5*lam*wn111'
+ PS='2*wn111+10*lam' PD='2*wn111+10*lam'
```

Rail-to-Rail Op Amp Simulation File (cont'd)

```
m121 7 7 nvdd nvdd cmosp W=wp121 L=lp AD='5*lam*wp121' AS='5*lam*wp121'
+ PS='2*wp121+10*lam' PD='2*wp121+10*lam'
m122 4 nvb4 5 nvdd cmosp W=wp121 L=lp AD='5*lam*wp121' AS='5*lam*wp121'
+ PS='2*wp121+10*lam' PD='2*wp121+10*lam'
m123 3 4 nvdd nvdd cmosp W=wp121 L=lp AD='5*lam*wp121' AS='5*lam*wp121'
+ PS='2*wp121+10*lam' PD='2*wp121+10*lam'
m124 6 6 7 7 cmosp W=wp121 L=lp AD='5*lam*wp121' AS='5*lam*wp121'
+ PS='2*wp121+10*lam' PD='2*wp121+10*lam'
m125 nvss 6 4 4 cmosp W=wp121 L=lp AD='5*lam*wp121' AS='5*lam*wp121'
+ PS='2*wp121+10*lam' PD='2*wp121+10*lam'
m126 3 3 2 2 cmosp W=wp121 L=lp AD='5*lam*wp121' AS='5*lam*wp121'
+ PS='2*wp121+10*lam' PD='2*wp121+10*lam'

m21 12 nvb1 8 nvdd cmosp W=wp21 L=lp AD='5*lam*wp21' AS='5*lam*wp21'
+ PS='2*wp21+10*lam' PD='2*wp21+10*lam'
m22 20 nvb1 9 nvdd cmosp W=wp21 L=lp AD='5*lam*wp21' AS='5*lam*wp21'
+ PS='2*wp21+10*lam' PD='2*wp21+10*lam'

m23 12 nvb3 10 nvss cmosn W=wn23 L=ln AD='5*lam*wn23' AS='5*lam*wn23'
+ PS='2*wn23+10*lam' PD='2*wn23+10*lam'
m24 20 nvb3 11 nvss cmosn W=wn23 L=ln AD='5*lam*wn23' AS='5*lam*wn23'
+ PS='2*wn23+10*lam' PD='2*wn23+10*lam'

m211 10 12 nvss nvss cmosn W=wn211 L=ln AD='5*lam*wn211' AS='5*lam*wn211'
+ PS='2*wn211+10*lam' PD='2*wn211+10*lam'
m212 11 12 nvss nvss cmosn W=wn211 L=ln AD='5*lam*wn211' AS='5*lam*wn211'
+ PS='2*wn211+10*lam' PD='2*wn211+10*lam'

m220 nout 20 nvss nvss cmosn W=wn220 L=ln AD='5*lam*wn220' AS='5*lam*wn220'
+ PS='2*wn220+10*lam' PD='2*wn220+10*lam'
```

Rail-to-Rail Op Amp Simulation File (cont'd)

```
m221 20 nvdd 21 nvss cmosn W=wn221 L=ln AD='5*lam*wn221' AS='5*lam*wn221'
+ PS='2*wn221+10*lam' PD='2*wn221+10*lam'

mb1 30 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam'
mb2 5 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam'
mb3 2 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam'
mb4 8 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam'
mb5 9 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam'
mb6 nout 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam' M=5

mb7 40 40 nvss nvss cmosn W=wnb7 L=ln AD='5*lam*wnb7' AS='5*lam*wnb7'
+ PS='2*wnb7+10*lam' PD='2*wnb7+10*lam'
mb8 6 40 nvss nvss cmosn W=wnb8 L=ln AD='5*lam*wnb8' AS='5*lam*wnb8'
+ PS='2*wnb8+10*lam' PD='2*wnb8+10*lam'
mb9 3 40 nvss nvss cmosn W=wnb7 L=ln AD='5*lam*wnb7' AS='5*lam*wnb7'
+ PS='2*wnb7+10*lam' PD='2*wnb7+10*lam'
mb10 1 40 nvss nvss cmosn W=wnb7 L=ln AD='5*lam*wnb7' AS='5*lam*wnb7'
+ PS='2*wnb7+10*lam' PD='2*wnb7+10*lam'

cm nout 21 10p
```

Rail-to-Rail Op Amp Simulation File (cont'd)

```
* Load
cl nout 0 20p
rl nout 0 20k

* Current & voltage sources

irefp 30 nvss 25u
irefn nvdd 40 25u

vb1 nvdd nvb1 1.6
vb4 nvdd nvb4 1.6
vb2 nvb2 nvss 1.7
vb3 nvb3 nvss 1.5

einp ninp ncm input 0 0.5
einm ninm ncm input 0 -0.5

vcm ncm 0 0
vin input 0 -3.824e-5 ac = 1

vdd nvdd 0 1.65
vss nvss 0 -1.65

* Test cards

.dc vin -0.5m 0.5m 10u
.ac dec 100 2 100x
.probe ac vdb(nout)

.end
```

Rail-to-Rail Input Stage, Structure 3 [3][4][6]

- Using current switches to change the tail current of input differential pairs

- Basic idea
  - We know that, by first order approximation, for a MOS transistor working in strong inversion and saturation region, square law applies, that is

    $I_D = K(V_{GS} - V_T)^2$, and $gm = 2\sqrt{KI_D}$,

    where $K = \frac{1}{2} KP(\frac{W}{L})$
  - Suppose for the N and P input pairs, $KP_N(\frac{W}{L})_N = KP_P(\frac{W}{L})_P = 2K$

    and the tail currents of N and P pairs are equal, with the value of I_{tail}.

Rail-to-Rail Input Stage, Structure 3 (cont'd)

– When the input common mode voltage is in the mid-range, both of N and P pairs are conducting, so the total transconductance is

$$gm_T = gm_N + gm_P = 2\sqrt{2KI_{TAIL}}$$

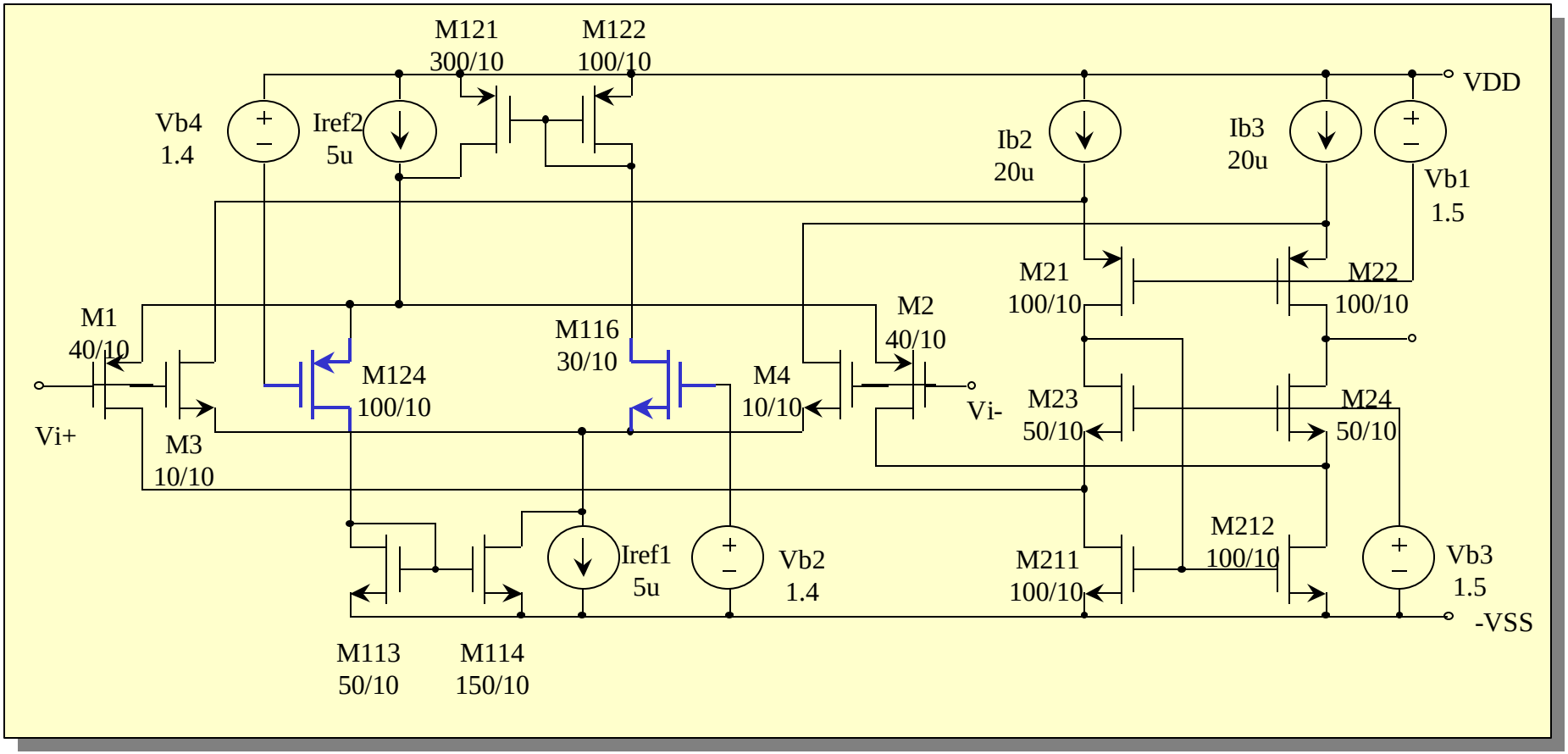
– When the input common mode voltage is close to Vdd, the N pair operates. And when it is close to the -Vss, the P pair operates. In both cases, the total transconductance is only **half** of that when both of N and P pairs operate.

$$gm_T = gm_N = gm_P = \sqrt{2KI_{TAIL}}$$

We can increase the tail current to **4** times of its original value to have the same transconductance as that when both of N and P pairs operate.

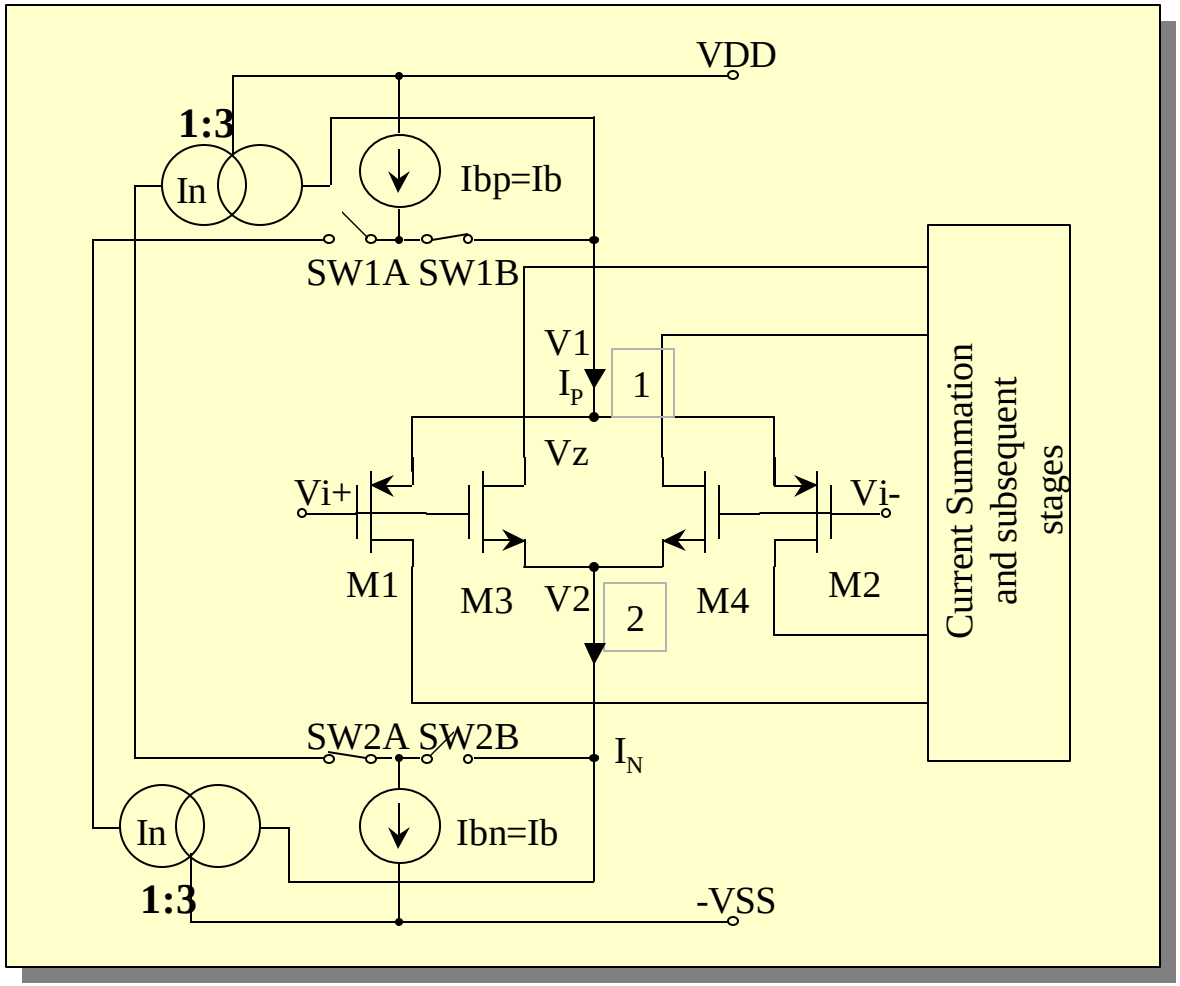
Rail-to-Rail Input Stage, Structure 3 (cont'd)

- The circuit



Rail-to-Rail Input Stage, Structure 3 (cont'd)

- Conceptual circuit



- When common mode input voltage, Vicm, is close to $-V_{ss}$, SW1B and SW2A are on, and SW1A and SW2B off.
- When Vicm is close to Vdd, SW1A and SW2B are on, and SW1B and SW2A off.
- In between, SW1B and SW2B are on, SW1A and SW2A off.
- In practice, SW1B and SW2B are never required, just short circuits. Say, if SW1A is on, Ibp will be diverted to the 1:3 current mirror; if SW1A is off, Ibp will provide tail current for M1 and M2.

Rail-to-Rail Input Stage, Structure 3 (cont'd)

- Working principle
  - If both of the input pairs operate, the total gm of the complementary input stage is 2 times of the gm with one single pair. In order to obtain the same gm when only one of the pairs operates, the tail current has to be 4 times larger.
  - The current switches M116 and M124 compare the common mode input voltage with with Vb2=1.4V and Vb4=1.4V, respectively. In the common mode input range from Vss to Vss+1.3V only the P channel input pair operates. In this range, the current switch M116 conducts while M124 is off. The current Iref1=5uA now flows through M116 to a 1:3 current multiplier M121-M122. Since Iref1 is equal to Iref2, I_p equals 4Iref1=20uA.
  - In the common mode input range from Vss+1.5V to Vdd-1.5V both of the input pairs operate. In this range, M116 and M124 are off, and the tail currents of N and P pairs are 5uA.

Rail-to-Rail Input Stage, Structure 3 (cont'd)

- In the common mode input range from Vdd-1.3V to Vdd, only the N channel pair operates. The current swith M124 conducts while M116 is off. The current Iref2=5uA now flows through M124 to a 1:3 current multiplier M113-M114. I_N equals 4Iref2=20uA.
- It can be calculated that for each input range, the total gm is

$$gm = 2\sqrt{2KIref} \quad \text{where} \quad K = \frac{1}{2}KP_N(\frac{W}{L})_N = \frac{1}{2}KP_P(\frac{W}{L})_P$$

- In the takeover regions of the current switches, Vss+1.3V to Vss+1.5V and Vdd-1.5V to Vdd-1.3V, the total gm of the input stage increases with about 15% above its nominal value.

  Which can be proved by the following analysis.

  If the common mode input voltage is between Vss+1.3V and Vss+1.5V, the M116 is partly conducting, and the rest of tail current flows through M3 and M4, which is assumed to be Ix here. So the tail current of the P pair is Iref+3(Iref-Ix).

Rail-to-Rail Input Stage, Structure 3 (cont'd)

The total gm of the input stage is given by

$$gm_T = \sqrt{2K}\left(\sqrt{Ix} + \sqrt{Iref + 3(Iref - Ix)}\right)$$

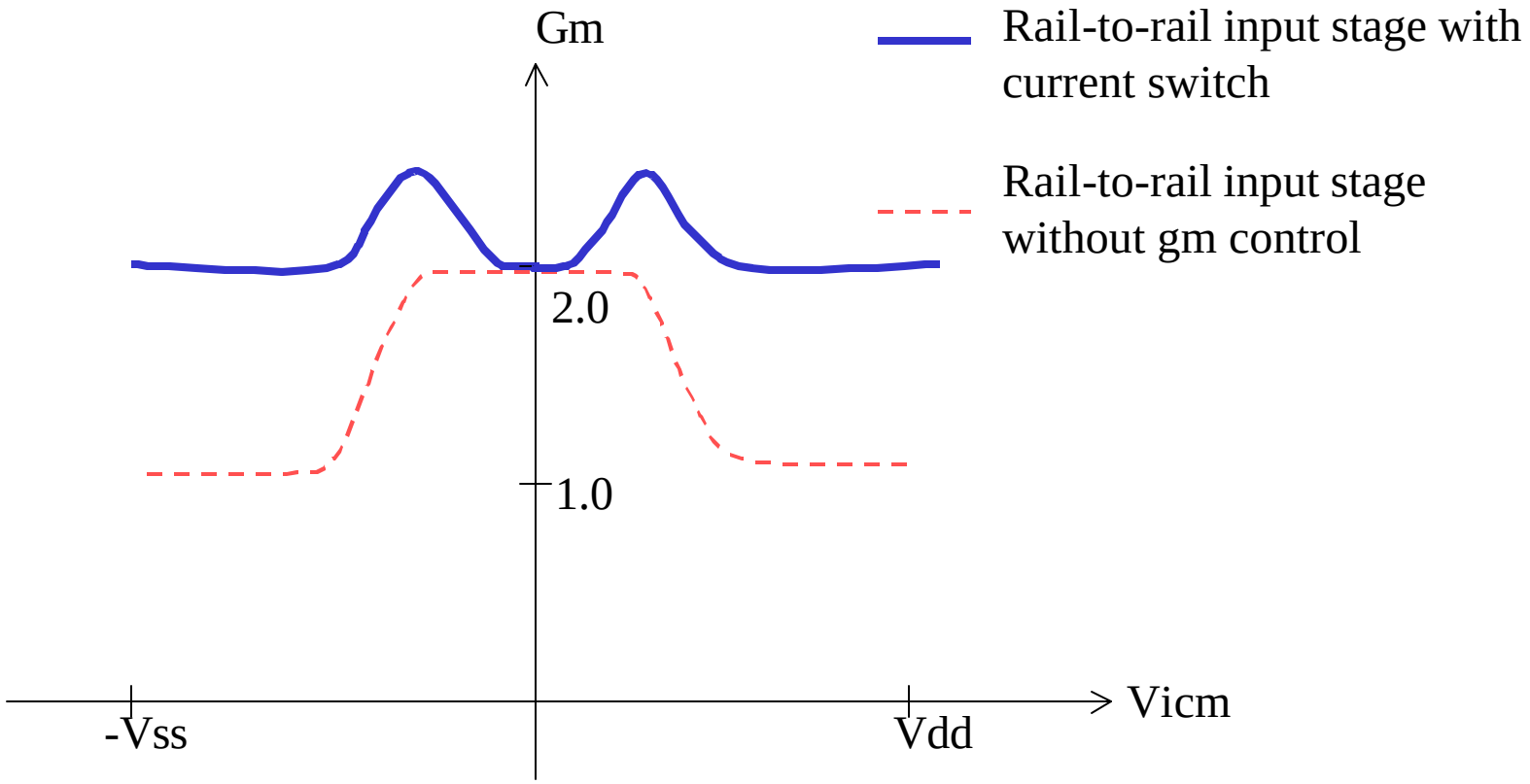
Calculate the maximum value of this equation, we can obtain that when Ix=1/3Iref, gm_T has its maximum value. Which yields

$$gm_T = \sqrt{2KIref}\left(\sqrt{\frac{1}{3}} + \sqrt{3}\right) = 2.31\sqrt{2KIref} = 2\sqrt{2KIref}\,(1 + 15.5\%)$$

Which is about 15% larger than its nominal value $2\sqrt{2KIref}$.

Rail-to-Rail Input Stage, Structure 3 (cont'd)

- Transconductance vs. input common mode voltage

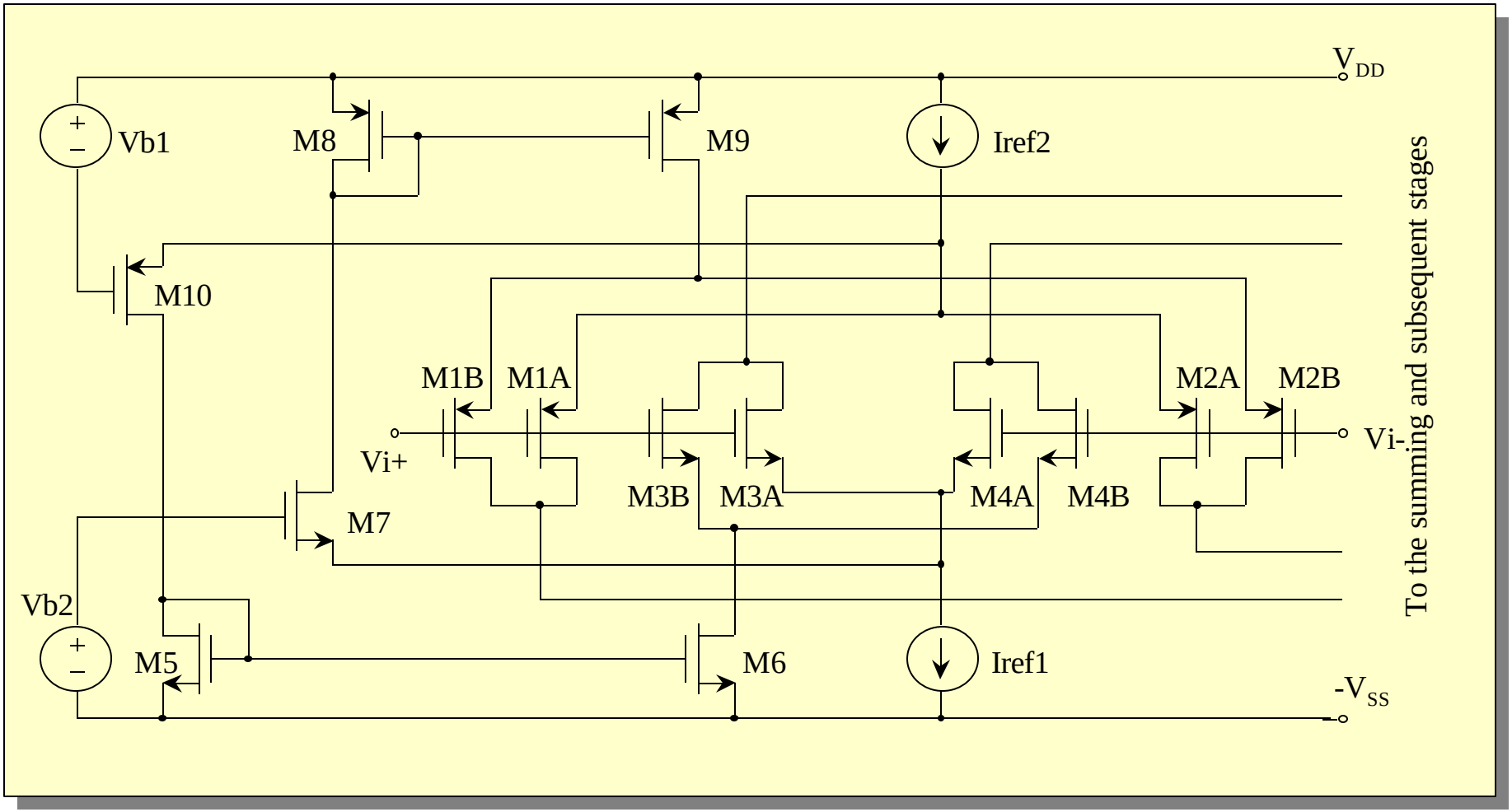


Rail-to-Rail Input Stage, Structure 4 [5]

- Another constant-gm input stage with current-switch. When only N (or P) input pair works, activate another N (or P) pair (we call it backup pair) to compensate the transconductance loss.
- Basic idea
  - In the previous constant-gm rail-to-rail input stage, when the common mode input voltage is in the middle range, both of the P and N pairs are operating, the total bias current is $I_N+I_P=2I_S$ ($I_N=I_P=I_S$). But when the common mode voltage is close V_{DD} or $-V_{SS}$, only one of the differential pairs operates, the bias current is $4I_S$. So the slew rate of the amplifier is the function of the common mode voltage, and has the variation of 2 times.
  - How can we keep the gm constant, and at the same time the slew rate not to vary so much? …
  - We can have 2 N-type pairs and 2 P-type pairs. One N pair (or P pair) are biased normally, we call it main pair. But another N pair (or P pair), the backup pair, is biased by the current steered from the main P pair (or N pair) if the main P pair can not work properly -- the current may also be controlled by current switch.

Rail-to-Rail Input Stage, Structure 4 (cont'd)

- The circuit [4]



Rail-to-Rail Input Stage, Structure 4 (cont'd)

- Working principle
  - When the common mode input voltage is in the middle range, P type pair (M1A, M2A) and N type pair (M3A, M4A) operate. Both of M7 and M10, which work as current switches, are off, thus there is no tail current flowing through the backup pairs (M1B, M2B) and (M3B, M4B). The total transconductance $gm_T=gm_P+gm_N=2gm$ (assume Iref1=Iref2=Iref, and $KP_N(W/L)_N=KP_P(W/L)_P$). The sum of the tail currents is Iref1+Iref2=2Iref.
  - When the common mode input voltage is close to V_{DD}, the current switch M10 is on, and Iref2 is steered through M10, mirrored by current mirror M5 and M6, and provides the tail current with the value of Iref for the N type differential pair (M3B and M4B). The total transconductance $gm_T=2gm$, the sum of the tail currents is 2Iref.

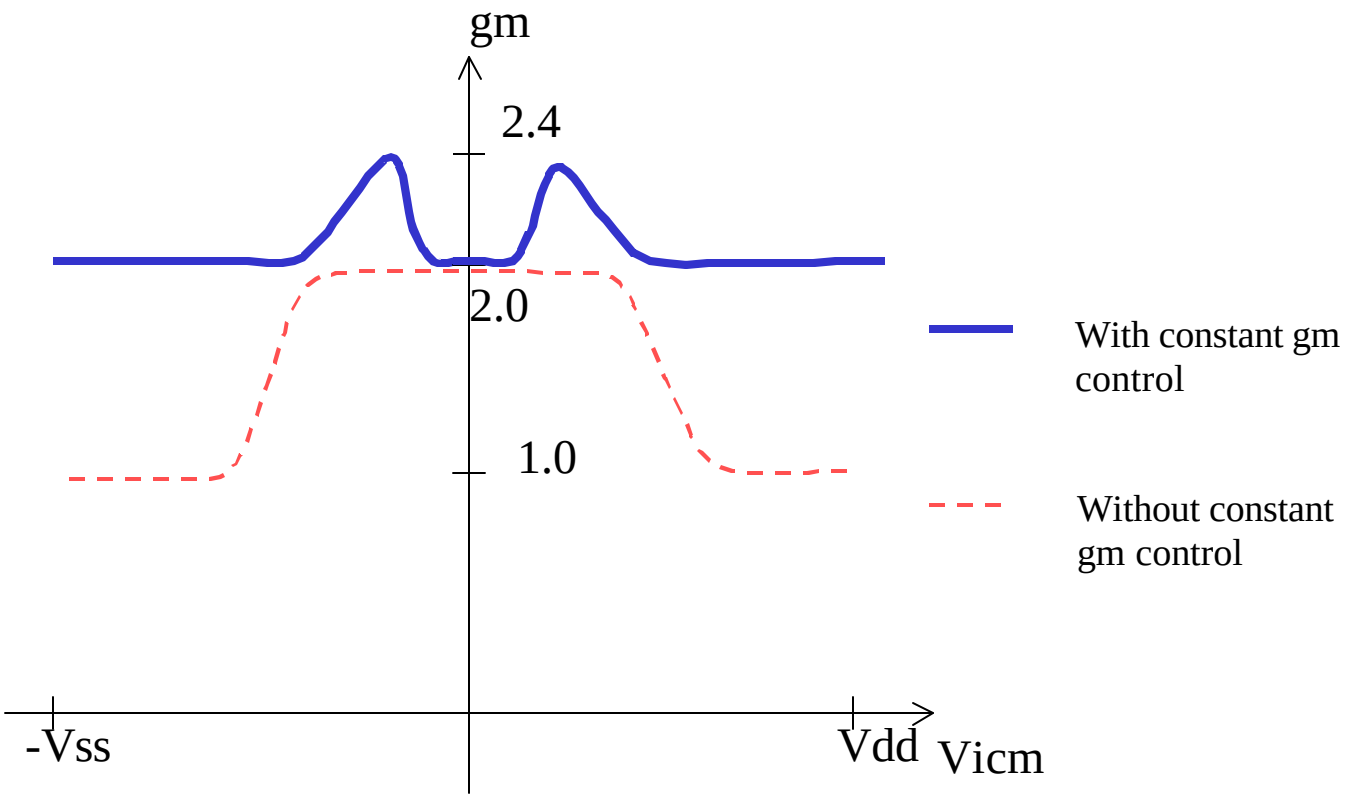
Rail-to-Rail Input Stage, Structure 4 (cont'd)

- When the common mode input voltage is close to V_{DD}, the current switch M7 is on, and Iref1 flows through M7, mirrored by current mirror formed with M8 and M9, and provides the tail current with the value of Iref for the P type differential pair (M1B, M2B). The total transconductance gm_T=2gm, the sum of the tail currents is 2Iref.

- Actually, the N backup pair (M3B,M4B) takes the role of primary P pair (M1A, M2A) when Vicm is close to V_{DD} and the current switch M10 is on. The P backup pair (M1B,M2B) takes the role of primary P pair (M3A, M4A) when Vicm is close to $-V_{SS}$ and the current switch M7 is on.

Rail-to-Rail Input Stage, Structure 4 (cont'd)

- Transconductance vs. input common mode voltage



Rail-to-Rail Input Stage, Structure 4 (cont'd)

- We may notice that there are 2 bumps on the gm curve, where the transconductance is 20% greater than its nominal value. The bumps are at take-over regions.
- By simple analysis we can know why it is so. If Vicm is at its upper take-over region (close to V_{DD}), assume that the tail current of the primary P pair I_{PA} is Ix, then the tail current of the primary N pair I_{NA} is Iref, and tail current of the backup N pair I_{NB} is Iref-Ix. The total transconductance is

$$gm_T = \sqrt{2K}\,(\sqrt{Iref} + \sqrt{Ix} + \sqrt{Iref - Ix})$$

Calculate the maximum value of this expression, we can get, when $I_x = I_{ref}/2$, Gm has its maximum value, which is

$$gm_T = \sqrt{2KIref}\,(\sqrt{2} + 1) = 2.4\sqrt{2KIref}$$

which is about 20% larger than its nominal value $2\sqrt{2KIref}$.

Rail-to-Rail Op Amp Design

Let us design a rail-to-rail input Op Amp with the same specifications on slide #31 utilizing rail-to-rail input stage Structure 4.

- **Design procedure**

1) Tail current and input transistors

By the same procedure we have discussed in slide #35, we can get the geometry ratios for N and P input pairs as $(W/L)_{P-PAIR} = 16$ and $(W/L)_{N-PAIR} = 4$.

For this structure, both of the N pair and P pair are actually divided into 2 branches each. Let us say the N half, one is the main differential pair (M_{3A} and M_{4A}), which operates if the common mode voltage is at its working region, the other is backup pair (M_{3B} and M_{4B}), which operates only if the P channel main pair (M_{1A} and M_{2A}) can not operate and the input common mode voltage turns on the current switch M_{10}. The current switch M_{10} and the current mirror (M_5 and M_6) accomplish the takeover.

Rail-to-Rail Op Amp Design (cont'd)

The geometry ratios of the input pairs should be divided by 2, so

$$(W/L)_{P-PAIR}' = \frac{(W/L)_{P-PAIR}}{2} = 8 \text{ and } (W/L)_{N-PAIR}' = \frac{W/L)_{N-PAIR}}{2} = 2.$$

The tail current I_{TAIL} (which is 25μA as calculated in the previous design) is also divided into 2 branches, so $I_{TAIL}' = 12.5\mu A = I_{ref2} = I_{ref1}$.

2) Current switches, M7 and M10

The V_{GS} of switch transistors M7 and M10 controls the current transition region width with the common mode voltage. We should avoid overlapping N and P transition regions, because in the transition region, the total gm deviates from its nominal value. If the 2 transition regions get together, the deviations will also add together. -- Let us say the extreme case that the transition regions overlap exactly, and at one point of the common mode voltage, each of the 4 pairs conducts tail current with the same magnitude, $I_{TAIL}'/2$. The total *gm* will be $\sqrt{2}$ times of its nominal value at this point, the same with structure 1 working in strong inversion region!

Rail-to-Rail Op Amp Design (cont'd)

So we choose $V_{dsat,M7}=V_{dsat,M10}=0.25V$, a relatively small value to avoid overlapping,

$$(\frac{W}{L})_{M7} = \frac{2I_D}{K_{PN}V_{dsat,M7}^{\ 2}} = \frac{2\times 12.5mA}{7.3584\times 10^{-5}A/V^2\times(0.25V)^2} = 5.436\ ,$$

Choose $(\frac{W}{L})_{M7} = 5$.

$$(\frac{W}{L})_{M10} = \frac{2I_D}{K_{PP}V_{dsat,M10}^{\ 2}} = \frac{2\times 12.5mA}{1.9346\times 10^{-5}A/V^2\times(0.25V)^2} = 20.67\ ,$$

Choose $(\frac{W}{L})_{M10} = 20$.

To avoid overlapping the 2 transition regions, in addition to have a small V_{GS} for M_7 and M_{10}, we should also carefully select the takeover voltages V_{b1} and V_{b2}. That is, V_{b1} and V_{b2} should be small enough to separate the two transitions regions apart, so the takeover voltage for M_7 is close to -Vss, and that of M_{10} close to Vdd.

Rail-to-Rail Op Amp Design (cont'd)

Let us assume when M_7 is fully on, the minimum voltage at source of M_7 is –Vss+0.25V, the 0.25V is for the V_{DS} of the current source I_{ref1}. Then

$$V_{T,M7} = V_{TO} + g\,(\sqrt{2|f_F| - V_{BS,M7}} - \sqrt{2|f_F|})$$

$$= 0.6443V + 0.7003V^{1/2}(\sqrt{0.7V + 0.25V} - \sqrt{0.7V}) = 0.7410V,$$

$$V_{b2} = V_{dsat,Iref1} + V_{T,M7} + V_{dsat,M7} = 0.25V + 0.7410V + \sqrt{\frac{2I_{TAIL}'}{(W/L)_{M7}\,nKP}} = 1.251V,$$

to leave some margin, let V_{b2}=1.3V,

Similarly, we can get the bias voltage source V_{b1} as 1.33V, let V_{b1}=1.35V.

3) Summing circuit, M_{21}~M_{24}, M_{211}, and M_{212}, and output stage M_{220} and M_{221}

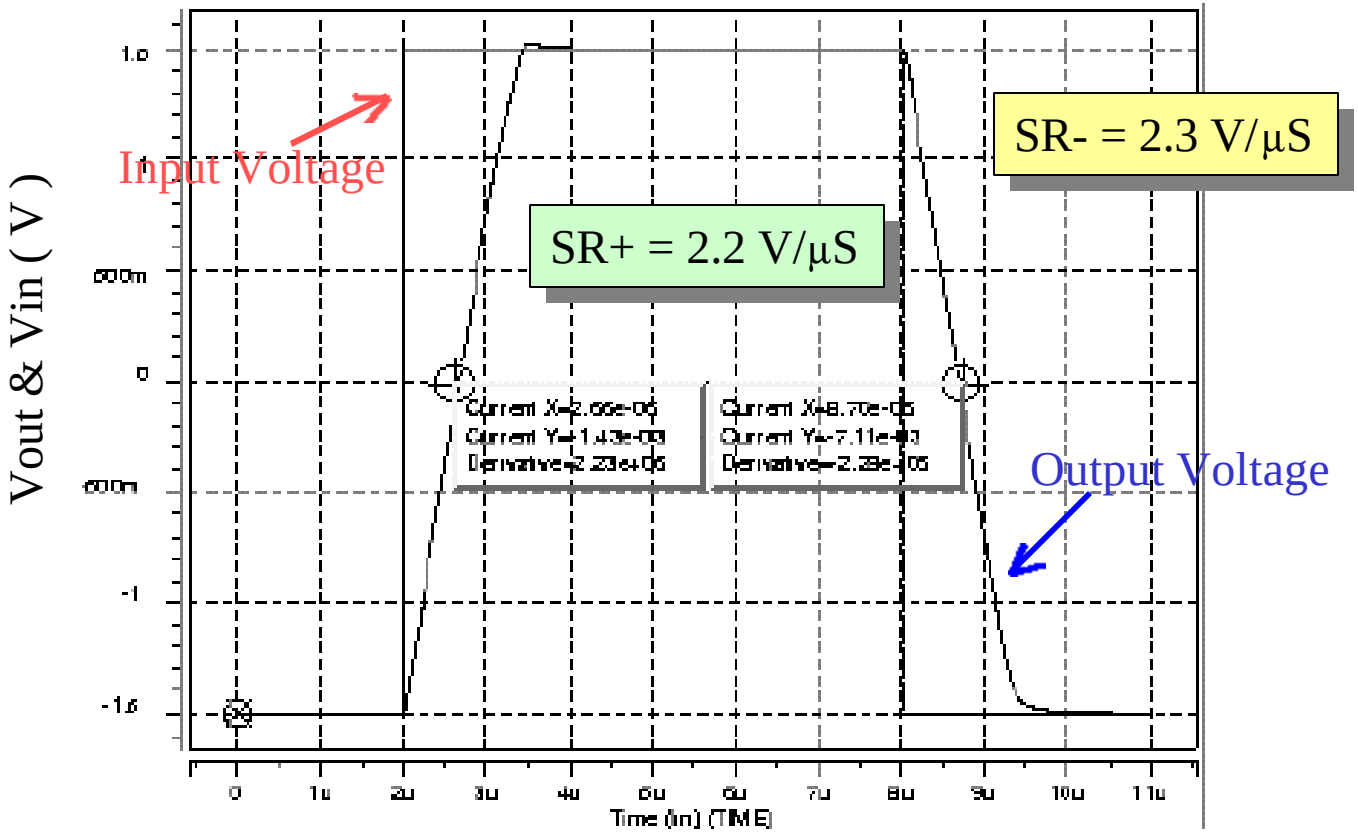
These 2 parts are the same with the design procedure on slide #38 and #39.

4) Modifications according to HSPICE simulation

No modifications for the input stage. For the output stage we just increased the bias current to 125μA to increase the output voltage swing.

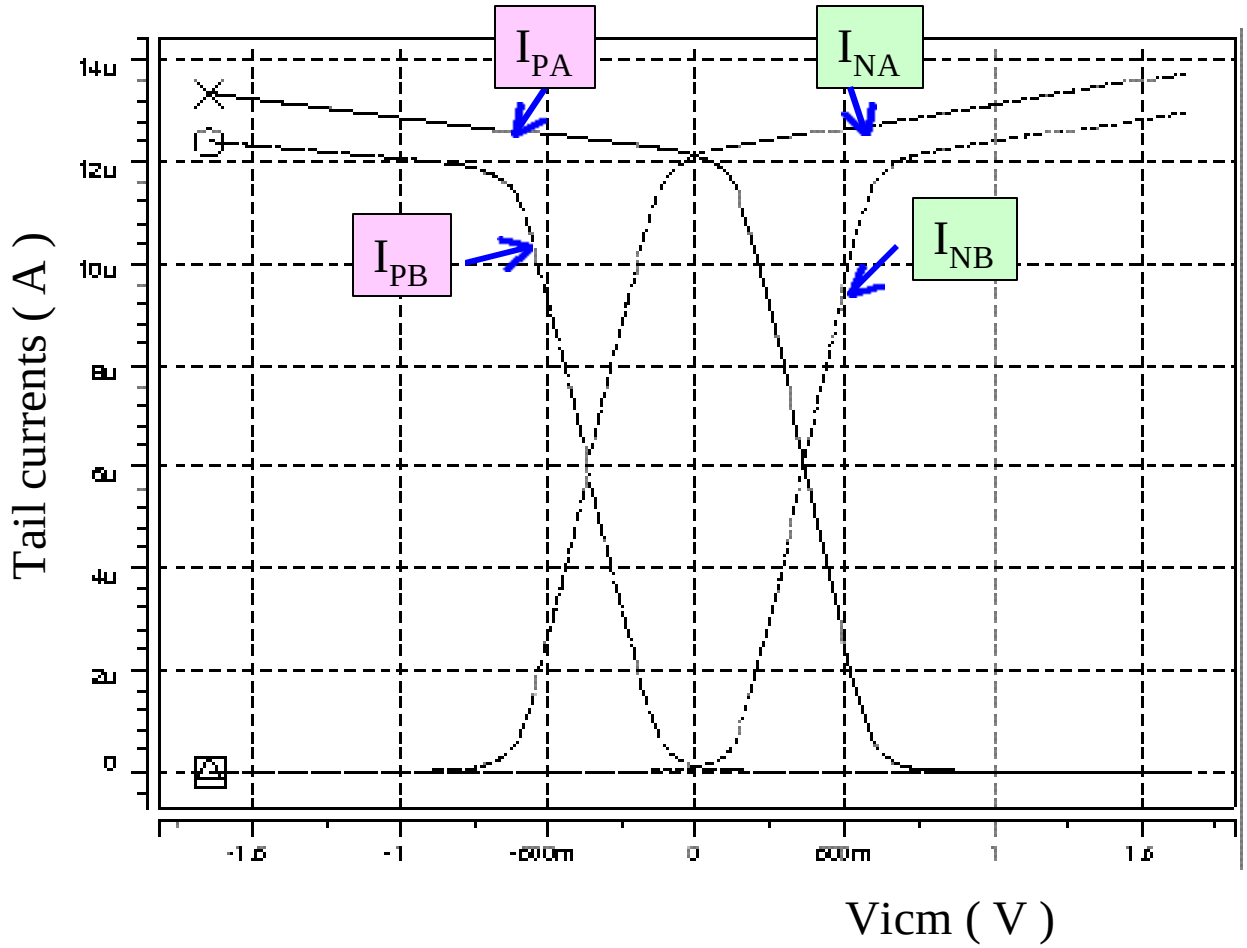
Rail-to-Rail Op Amp Simulation Results

- Simulation results (as DC input output characteristics, and frequency response are very similar with those of previous design, we do not plot here).
  - Transient response



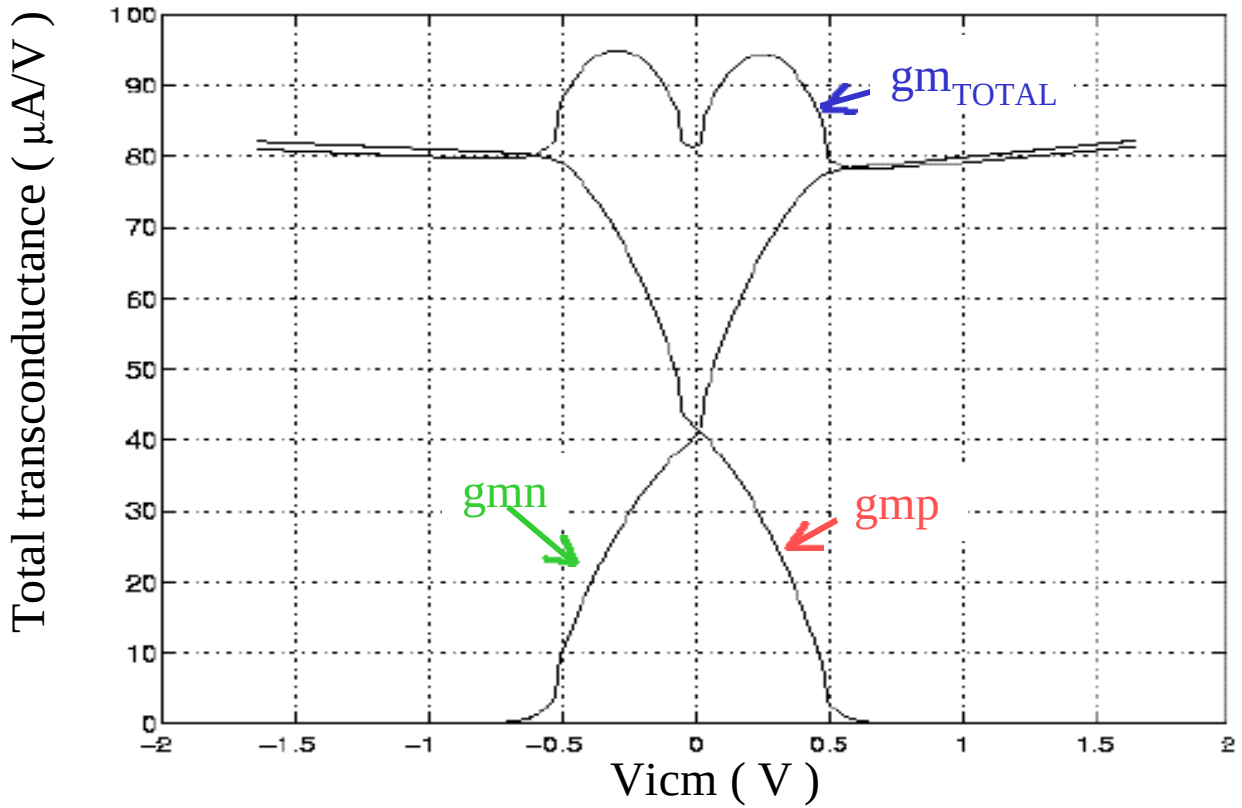
Rail-to-Rail Op Amp Simulation Results (cont'd)

– Tail currents v.s. common mode voltage



Rail-to-Rail Op Amp Simulation Results (cont'd)

– Transconductance v.s. common mode voltage



	Average	Minimum	Maximum
Gm_{TOTAL} (uA/V)	83.2	78.1	95
Deviation		-6.2%	14.2%

Rail-to-Rail Op Amp Simulation File

- HSPICE file

```
2-Stage Op Amp with Rail-to-Rail Input Structure 4

.options list node post
.include ami_n8cu_level3
.op

* Parameter definitions

.param lam = 0.6u ln = 2.4u lp=2.4u ln3=3.6u lp1=3.6u
+ wp1=28.8u wn3=7.2u wn5=21.6u wp8=28.8u wn7=12u wp10=48u
+ wp21=96u wn23=28.8u wn26=57.6u wpb1=76.8u wnb10=24u
+ wn220=163.2u wn221=21.6u

* Netlist

m1a 10 ninm 2 2 cmosp W=wp1 L=lp1 AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'
m2a 11 ninp 2 2 cmosp W=wp1 L=lp1 AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'

m1b 10 ninm 4 4 cmosp W=wp1 L=lp1 AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'
m2b 11 ninp 4 4 cmosp W=wp1 L=lp1 AD='5*lam*wp1' AS='5*lam*wp1'
+ PS='2*wp1+10*lam' PD='2*wp1+10*lam'
```

Rail-to-Rail Op Amp Simulation File (cont'd)

```
m3a 8 ninm 1 nvss cmosn W=wn3 L=ln3 AD='5*lam*wn3' AS='5*lam*wn3'
+ PS='2*wn3+10*lam' PD='2*wn3+10*lam'
m4a 9 ninp 1 nvss cmosn W=wn3 L=ln3 AD='5*lam*wn3' AS='5*lam*wn3'
+ PS='2*wn3+10*lam' PD='2*wn3+10*lam'

m3b 8 ninm 3 nvss cmosn W=wn3 L=ln3 AD='5*lam*wn3' AS='5*lam*wn3'
+ PS='2*wn3+10*lam' PD='2*wn3+10*lam'
m4b 9 ninp 3 nvss cmosn W=wn3 L=ln3 AD='5*lam*wn3' AS='5*lam*wn3'
+ PS='2*wn3+10*lam' PD='2*wn3+10*lam'


m7 6 nvb2 1 nvss cmosn W=wn7 L=ln AD='5*lam*wn7' AS='5*lam*wn7'
+ PS='2*wn7+10*lam' PD='2*wn7+10*lam'

m5 5 5 nvss nvss cmosn W=wn5 L=ln AD='5*lam*wn5' AS='5*lam*wn5'
+ PS='2*wn5+10*lam' PD='2*wn5+10*lam'
m6 3 5 nvss nvss cmosn W=wn5 L=ln AD='5*lam*wn5' AS='5*lam*wn5'
+ PS='2*wn5+10*lam' PD='2*wn5+10*lam'

m10 5 nvb1 2 2 cmosp W=wp10 L=lp AD='5*lam*wp10' AS='5*lam*wp10'
+ PS='2*wp10+10*lam' PD='2*wp10+10*lam'

m8 6 6 nvdd nvdd cmosp W=wp8 L=lp AD='5*lam*wp8' AS='5*lam*wp8'
+ PS='2*wp8+10*lam' PD='2*wp8+10*lam'
m9 4 6 nvdd nvdd cmosp W=wp8 L=lp AD='5*lam*wp8' AS='5*lam*wp8'
+ PS='2*wp8+10*lam' PD='2*wp8+10*lam'


m21 12 nvb1 8 nvdd cmosp W=wp21 L=lp AD='5*lam*wp21' AS='5*lam*wp21'
+ PS='2*wp21+10*lam' PD='2*wp21+10*lam'
m22 20 nvb1 9 nvdd cmosp W=wp21 L=lp AD='5*lam*wp21' AS='5*lam*wp21'
+ PS='2*wp21+10*lam' PD='2*wp21+10*lam'
```

Rail-to-Rail Op Amp Simulation File (cont'd)

```
m23 12 nvb3 10 nvss cmosn W=wn23 L=ln AD='5*lam*wn23' AS='5*lam*wn23'
+ PS='2*wn23+10*lam' PD='2*wn23+10*lam'
m24 20 nvb3 11 nvss cmosn W=wn23 L=ln AD='5*lam*wn23' AS='5*lam*wn23'
+ PS='2*wn23+10*lam' PD='2*wn23+10*lam'

m26 10 12 nvss nvss cmosn W=wn26 L=ln AD='5*lam*wn26' AS='5*lam*wn26'
+ PS='2*wn26+10*lam' PD='2*wn26+10*lam'
m27 11 12 nvss nvss cmosn W=wn26 L=ln AD='5*lam*wn26' AS='5*lam*wn26'
+ PS='2*wn26+10*lam' PD='2*wn26+10*lam'

mb1 30 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam'
mb2 2 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam'
mb3 8 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam' M=2
mb4 9 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam' M=2
mb5 nout 30 nvdd nvdd cmosp W=wpb1 L=lp AD='5*lam*wpb1' AS='5*lam*wpb1'
+ PS='2*wpb1+10*lam' PD='2*wpb1+10*lam' M=10

mb10 40 40 nvss nvss cmosn W=wnb10 L=ln AD='5*lam*wnb10' AS='5*lam*wnb10'
+ PS='2*wnb10+10*lam' PD='2*wnb10+10*lam'
mb11 1 40 nvss nvss cmosn W=wnb10 L=ln AD='5*lam*wnb10' AS='5*lam*wnb10'
+ PS='2*wnb10+10*lam' PD='2*wnb10+10*lam'

m220 nout 20 nvss nvss cmosn W=wn220 L=ln AD='5*lam*wn220' AS='5*lam*wn220'
+ PS='2*wn220+10*lam' PD='2*wn220+10*lam'

m221 20 nvdd 21 nvss cmosn W=wn221 L=ln AD='5*lam*wn221' AS='5*lam*wn221'
+ PS='2*wn221+10*lam' PD='2*wn221+10*lam'
```

Rail-to-Rail Op Amp Simulation File (cont'd)

```
cm nout 21 10p

* Load
cl nout 0 20p
rl nout 0 20k

* Current & voltage sources

ibiasp 30 nvss 12.5u
ibiasn nvdd 40 12.5u

vb1 nvdd nvb1 1.35
vb2 nvb2 nvss 1.3
vb3 nvb3 nvss 1.55

einp ninp ncm input 0 0.5
einm ninm ncm input 0 -0.5

vcm ncm 0 0
vin input 0 -19.585u ac = 1

vdd nvdd 0 1.65
vss nvss 0 -1.65

* Test cards

.dc vin -1m 1m 2u
.ac dec 100 2 100x
.probe ac vdb( nout )

.end
```

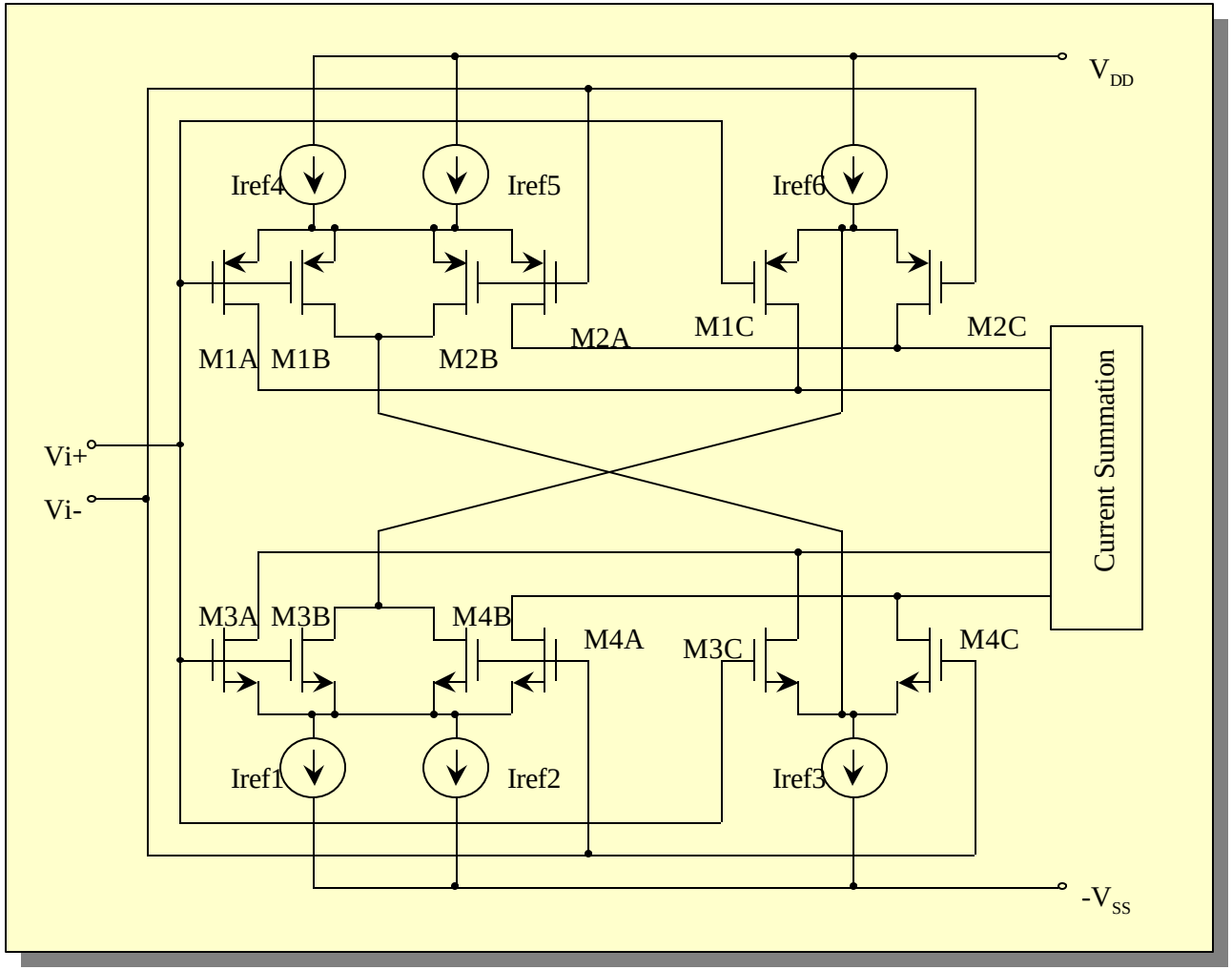
Rail-to-Rail Input Stage, Structure 5 [7]

- Using Hex-Pair Structure to control the tail currents backup pairs

- Basic idea
  - The underlying idea of this structure is similar to structure 4. We utilize main and backup pairs to have a constant gm, and at the same time, a constant total biasing current which will not change with the common mode input voltage. But here we apply an new bias current sensing scheme, which is also utilized in [18].

Rail-to-Rail Input Stage, Structure 5 (cont'd)

- The circuit [7]

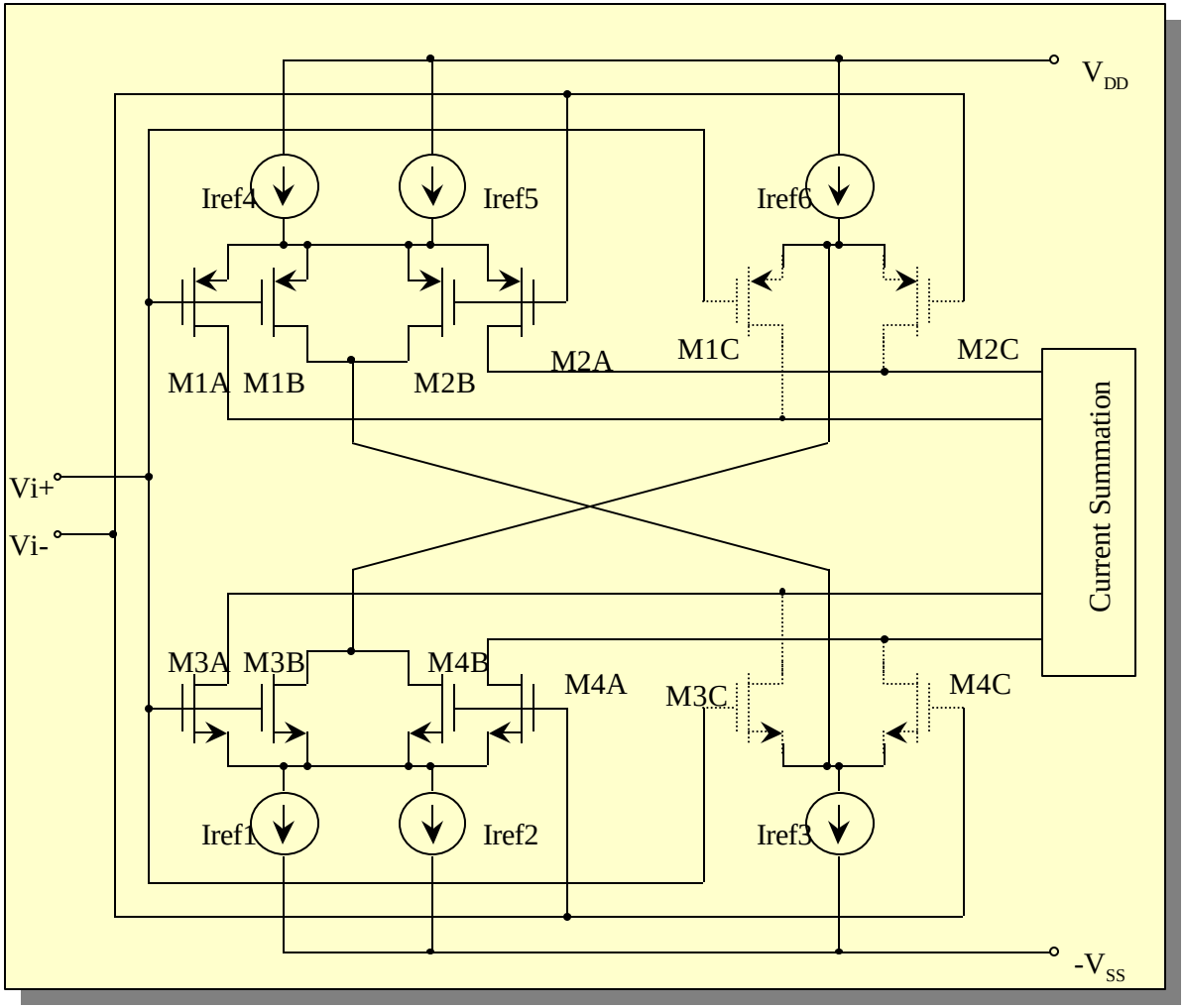


Note:
1) Iref1 to Iref6 are with the same value, Iref.
2) All of the P transistors have the same geometry, $(W/L)_P$, for all of the N transistors, $(W/L)_N$.
and

$$K = \frac{1}{2} KP_N \left(\frac{W}{L}\right)_N = \frac{1}{2} KP_P \left(\frac{W}{L}\right)_P$$

Rail-to-Rail Input Stage, Structure 5 (cont'd)

- Working principle



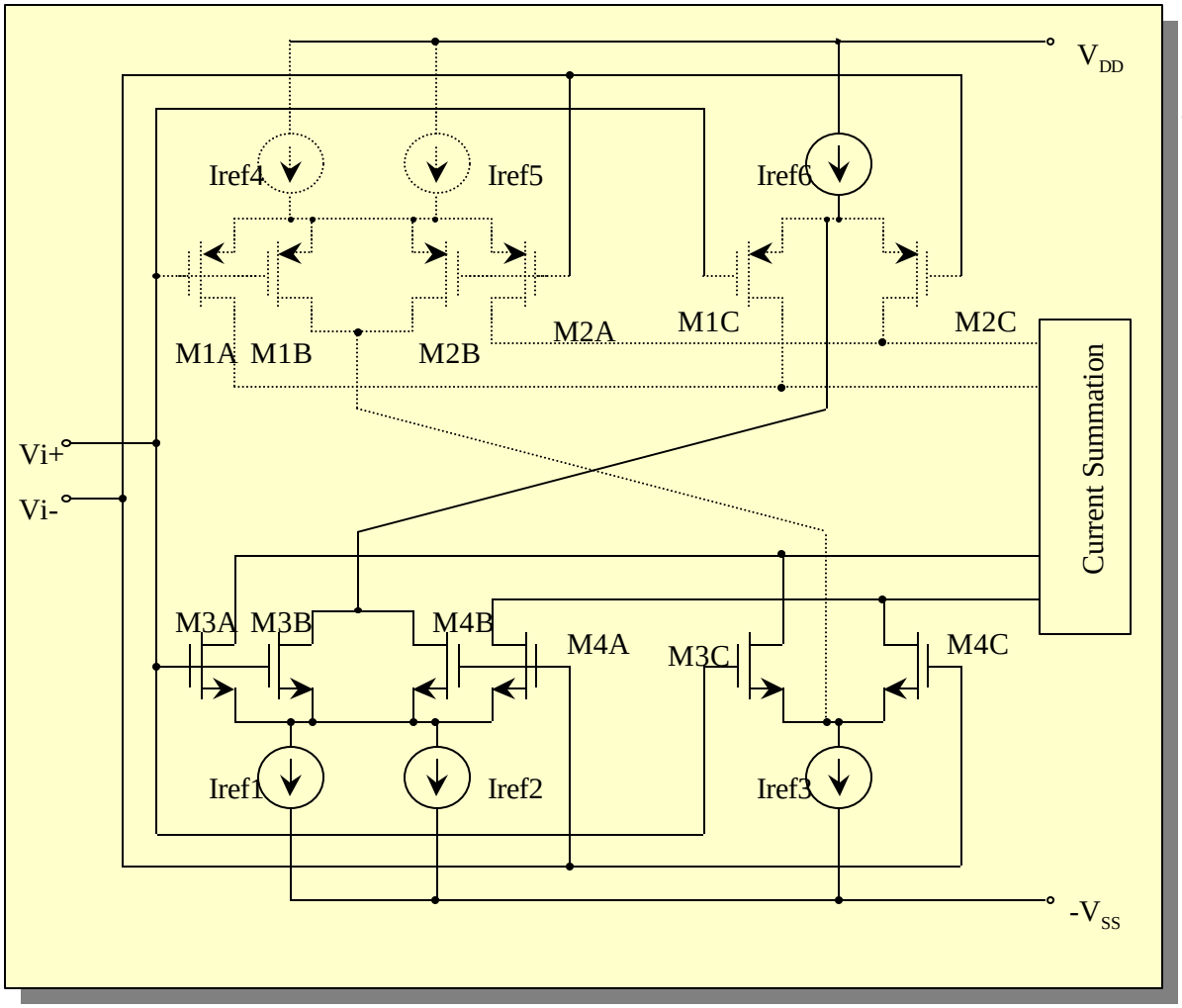
- When the common mode input voltage is in its middle range.

Both of the N and P channel devices have sufficient gate bias to operate. In the N-channel circuitry, both M3A and M4A contribute signal current, with a transconductance set by half of the total current available, i.e., Iref. The other half of the tail current, also Iref, is diverted to M3B and M4B, since all of the N transistors are of the equal size, and have the same mean gate source voltage. This diverted current in turn draws the tail current Iref6 away from the P channel pair M1C and M2C, switching them off.

On the P side, M1A and M2A contribute signal current. And the current of M1B, M2B draws away the tail current of M3C and M4C.

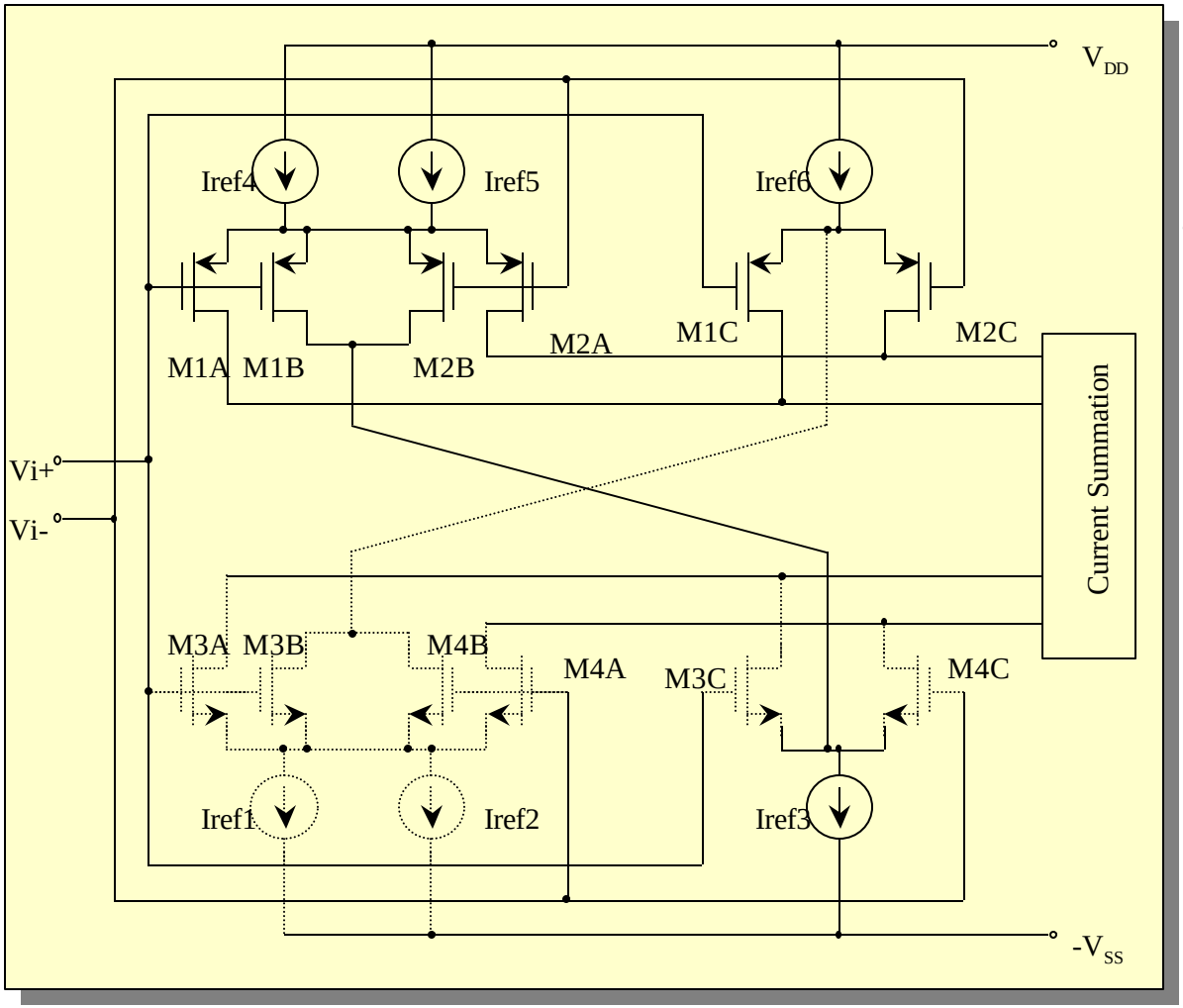
Hence, the total signal output is supplied by 4 transistors, M1A, M2A, M3A and M4A. The transconductance is 2gm, and the total tail current available is 2Iref.

Rail-to-Rail Input Stage, Structure 5 (cont'd)



- When the common mode input voltage is close to V_{DD}.
  None of the P channel transistors have sufficient gate source voltage to remain active. The current sources supplying M1A, M1B, M2A, and M2B collapse and turn off. M3C and M4C become active and contribute signal current to the output. Hence, the total signal output is again supplied by 4 transistors, M3A, M4A, M3C and M4C . The total transconductance is 2gm, and the total tail current available is still 2Iref.

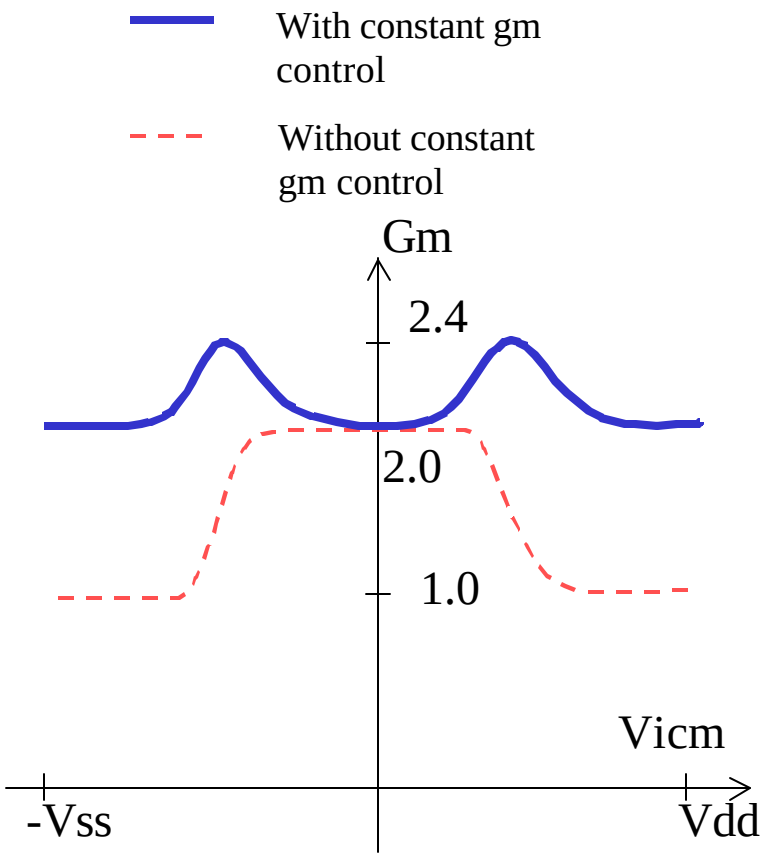
Rail-to-Rail Input Stage, Structure 5 (cont'd)



- When the common mode input voltage is close to $-V_{SS}$.
  None of the N channel transistors have sufficient gate source voltage to remain active. The current sources supplying M3A, M3B, M4A, and M4B collapse and turn off. M1C and M2C become active and contribute signal current to the output. Hence, the total signal output is again supplied by 4 transistors, M1A, M2A, M1C and M2C . The total transconductance is 2gm, and the total tail current available is still 2Iref.

Rail-to-Rail Input Stage, Structure 5 (cont'd)

- Transconductance vs. input common mode voltage



– Similar to constant-gm input stage structure 4, there are also 2 bumps on the gm curve, where the transconductance is 20% greater than its nominal value. The bumps are at take-over regions.

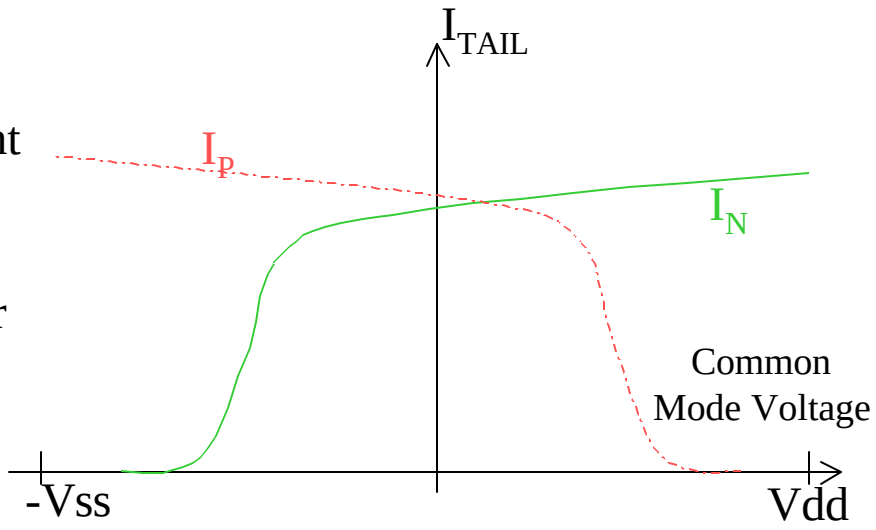
– By similar analysis we can determine the maximum value of the total transconductance is

$$gm_T = \sqrt{2KIref}(\sqrt{2}+1) = 2.414\sqrt{2KIref}$$

which is about 20% larger than its nominal value $2\sqrt{2KIref}$.

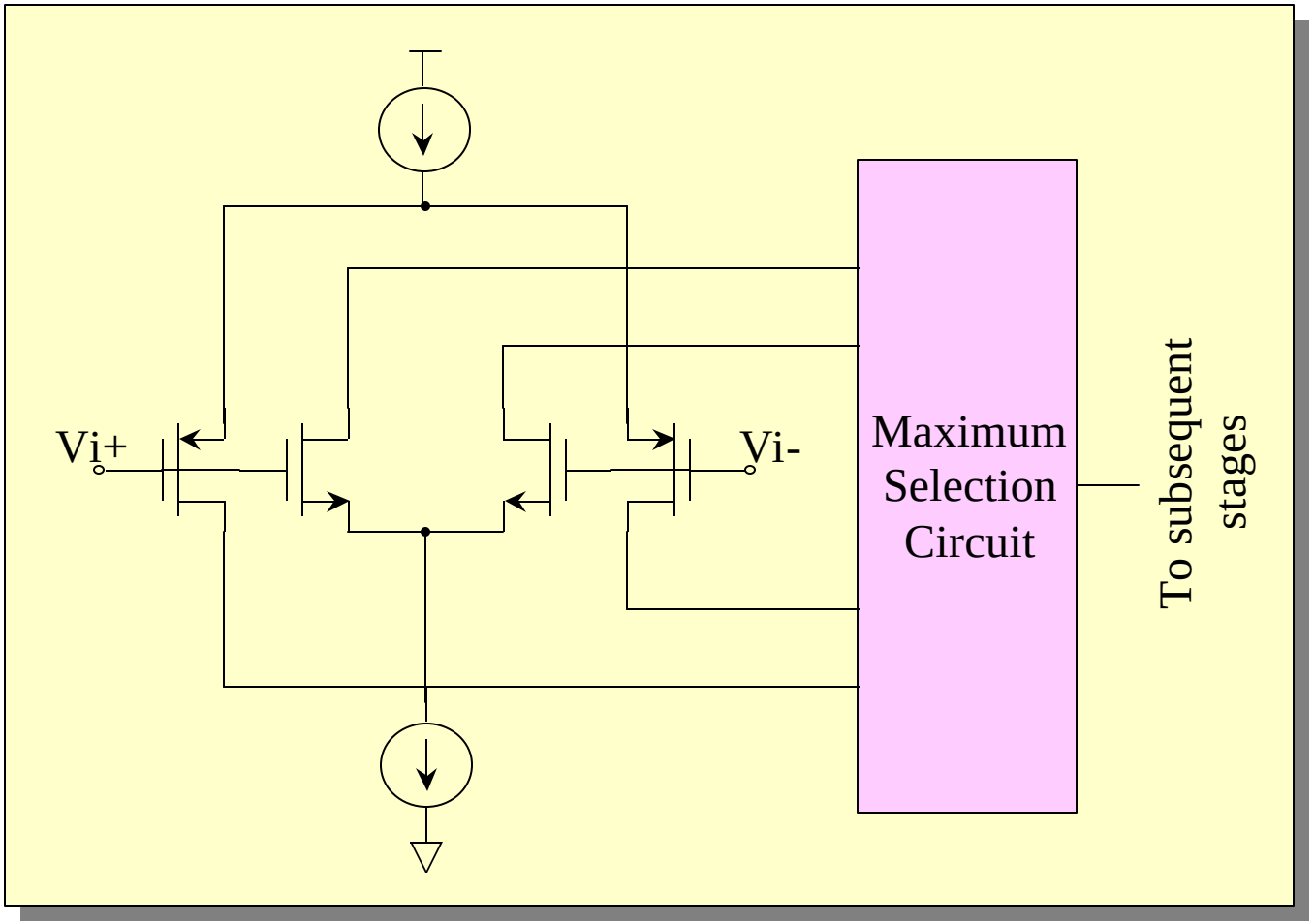
Rail-to-Rail Input Stage, Structure 6 [8][9]

- Using Maximum/Minimum selection circuit
- The basic idea
  - From previous analysis, we know that, when the common mode voltage drives the tail current transistor out of saturation region, the tail current of a differential pair decreases dramatically with the common mode voltage. As shown in the following figure.
  - The differential pair, whichever it is N pair or P pair, with the larger current should be working properly. We just try to choose the pair with larger working current, and discard the output of another pair.



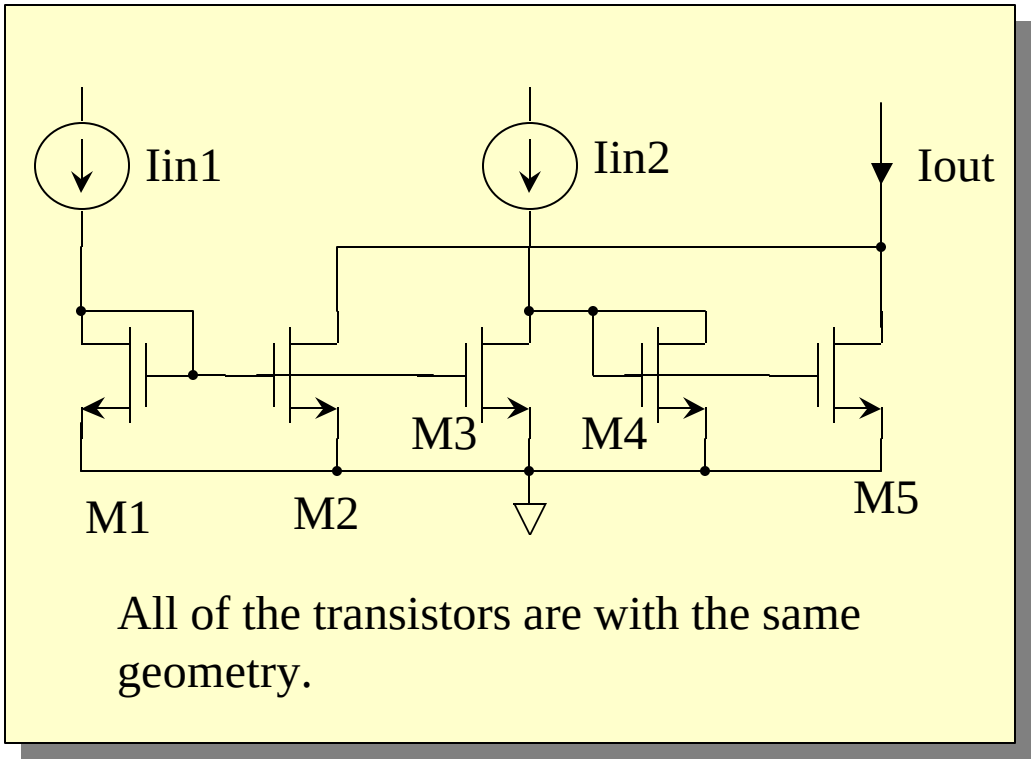
Rail-to-Rail Input Stage, Structure 6 (cont'd)

- The block diagram



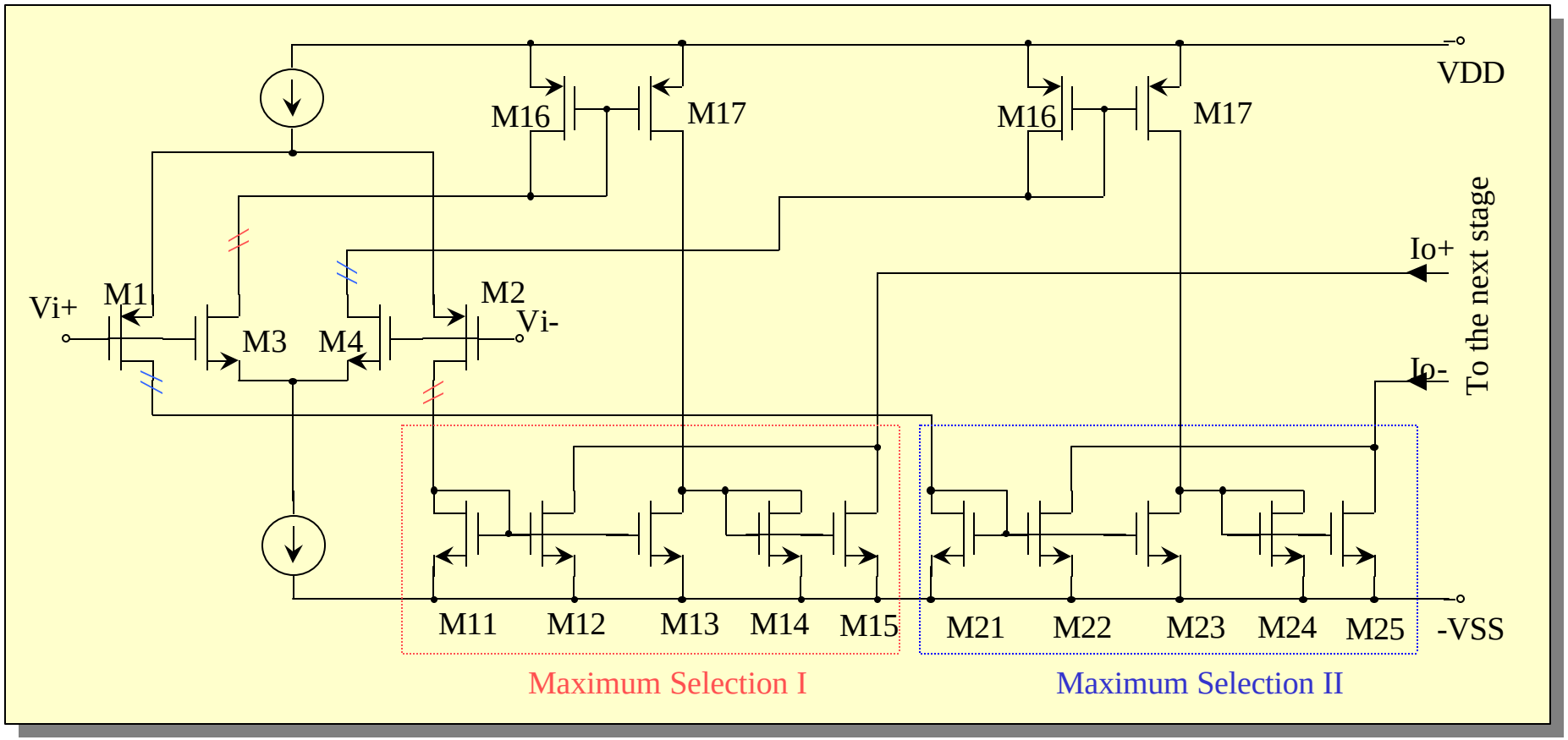
Rail-to-Rail Input Stage, Structure 6a (cont'd)

- Maximum Current Selection Circuit
  - When Iin1>Iin2, M2 and M3 try to mirror Iin1, but as Iin2<Iin1, there is no enough current for M3 to sink, M3 will work in Ohmic region and its V_{DS} is very small. M4 and M5 are off. So Iout = Iin1
  - When Iin2>Iin1, $I_{D,M2}=I_{D,M3}=Iin1$, $I_{D,M4}=I_{D,M5}=Iin2-Iin1$.Iout = $I_{D,M5}+ I_{D,M3}=Iin1+(Iin2-Iin1)=Iin2$



Rail-to-Rail Input Stage, Structure 6a (cont'd)

- The whole input stage



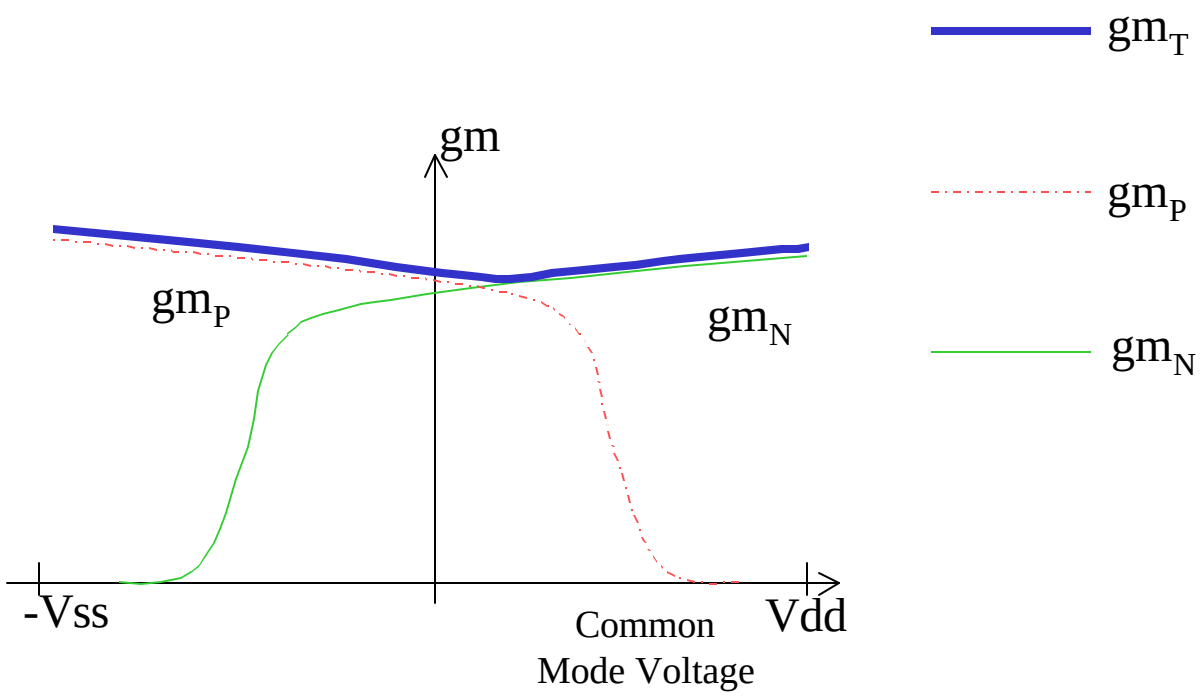
Please notice that wires with // are connected to Maximum Current Selection I, and the wires with // are connected to Maximum Current Selection II.

Rail-to-Rail Input Stage, Structure 6a (cont'd)

- Working Principle
  - Please notice that if we apply a positive differential voltage to the inputs Vi+ and Vi-, the currents of M1 (P type) and M4 (N type) will decrease, and the currents of M2 (P type) and M3 (N type) will increase. We apply the current of M2 and mirrored current of M3 to Maximum Selection Circuit I, and current of M1 and the mirrored current of M4 to Maximum Selection Circuit II.
  - When the common mode input voltage is close to Vdd, the tail current of the P input pair decreases, the maximum selection circuits conduct the drain currents of N pair to the outputs.
  - When the common mode input voltage is close to -Vss, the tail current of the N input pair decreases, the maximum selection circuits conduct the drain currents of P pair to the outputs.
  - At the outputs, we get the larger currents of the 2 input pairs, and hence the larger gm.

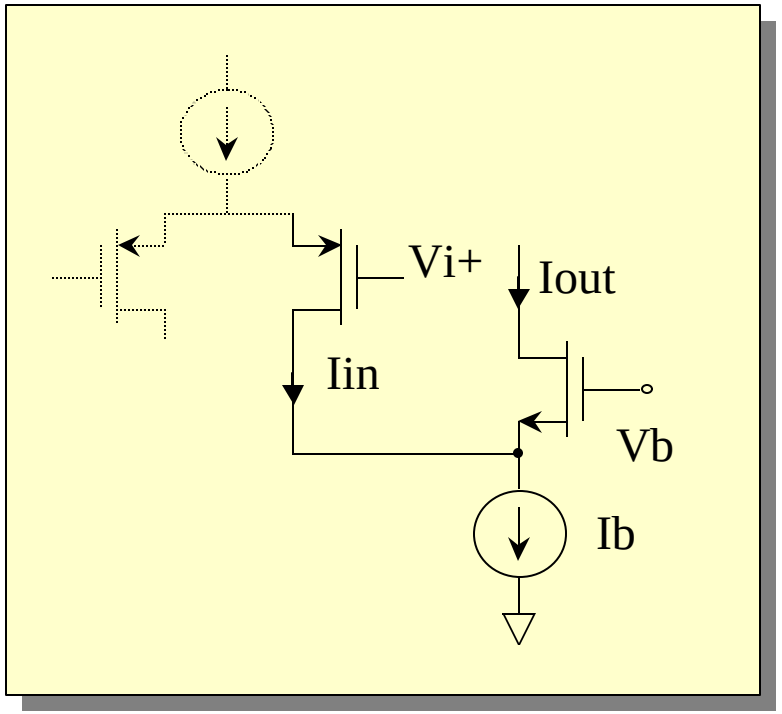
Rail-to-Rail Input Stage, Structure 6a (cont'd)

- Transconductance vs. input common mode voltage



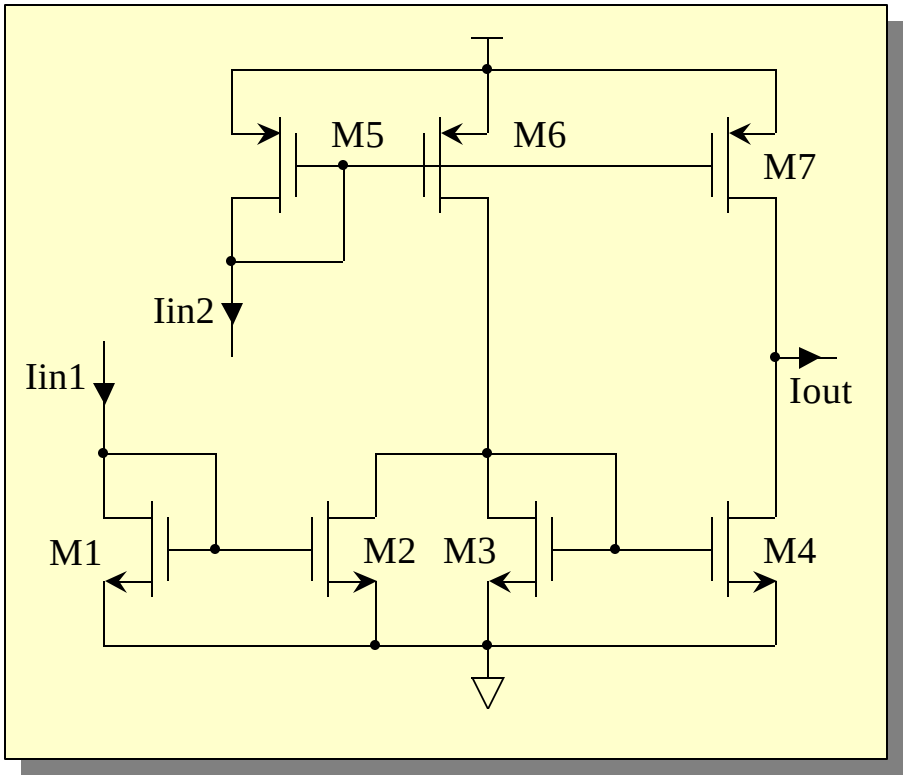
Rail-to-Rail Input Stage, Structure 6b (cont'd)

- There is another configuration which utilizes folded cacode circuit and minimum selection circuit to get the maximum gm
  - As in the folded cascoded shown in the circuit below, if Iin is at it maximum value, we will get a minimum Iout. So with this folded cascode circuit, we can not use maximum selection circuit, instead, we should use minimum selection circuit.
  - Why folded cascode circuit?
  - The key advantage of this configuration over the previous one is that it has a wider commom mode range! If it is properly biased, we can get a common mode range which may exceed the power supply rails!



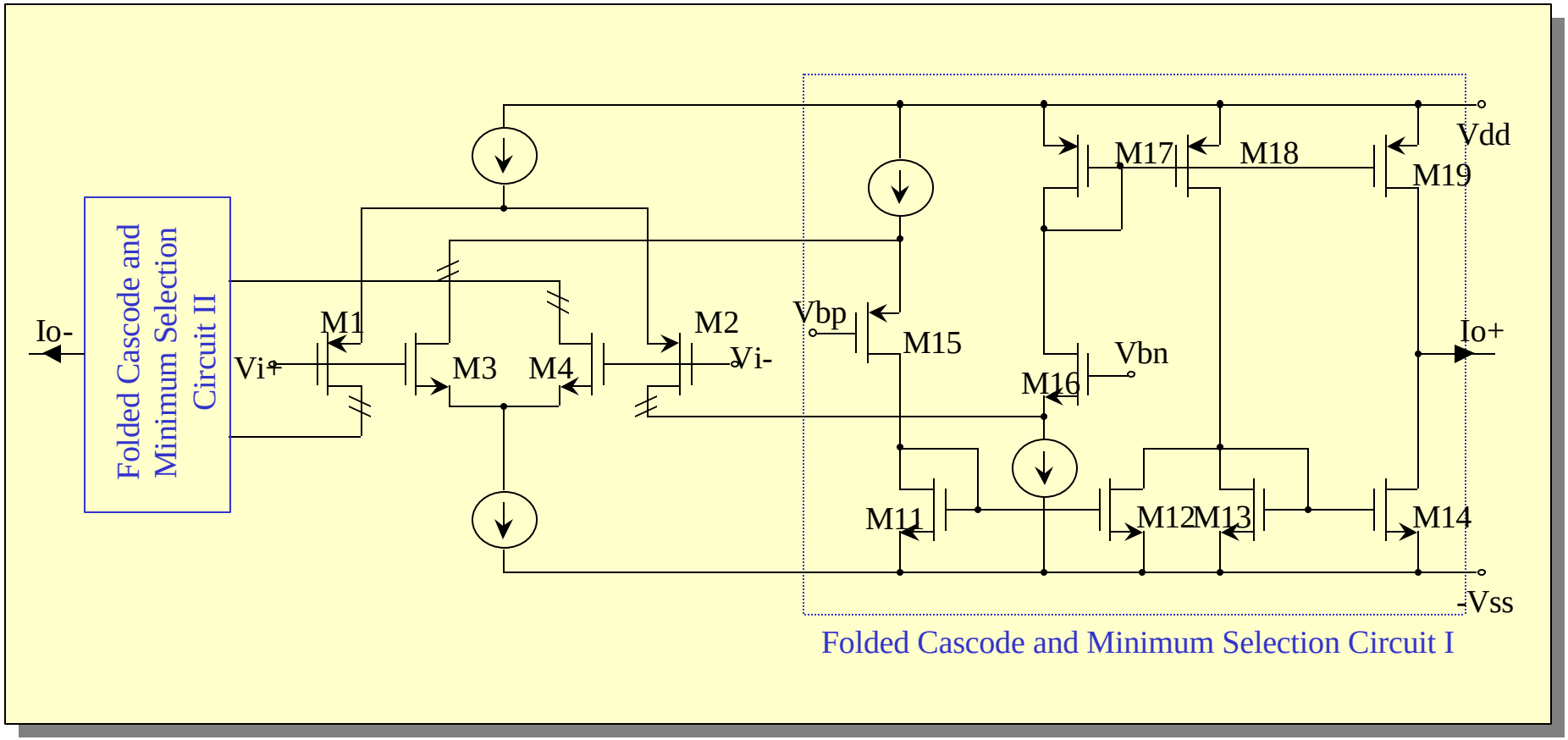
Rail-to-Rail Input Stage, Structure 6b (cont'd)

- The minimum selection circuit
  - As shown in the right circuit, all N transistors are with the same geometry, and P transistors are with the same geometry.
  - If Iin2<Iin1, $I_{D,M5}=I_{D,M6}=I_{D,M7}$=Iin2, M2 works in ohmic region, and M3 and M4 are off. Iout= $I_{D,M7}$=Iin2.
  - If Iin1<Iin2, $I_{D,M5}=I_{D,M6}=I_{D,M7}$=Iin2, $I_{D,M1}=I_{D,M2}$=Iin1,
    $I_{D,M3}=I_{D,M4}$=Iin2-Iin1,
    Iout= $I_{D,M7}-I_{D,M4}$=Iin2-(Iin2-Iin1)=Iin1



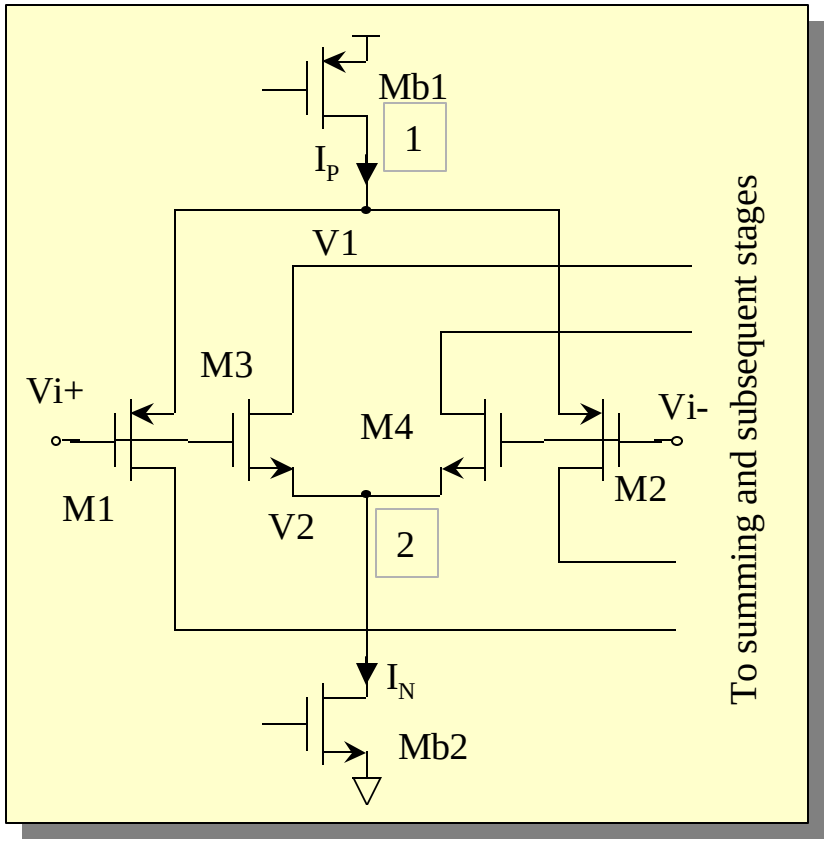
Rail-to-Rail Input Stage, Structure 6b (cont'd)

- The input stage with folded cascode and minimum selection circuit



Rail-to-Rail Input Stage, Structure 7 [10]

- Using electronic zener diode to keep $V_{GSn} + |V_{GSp}|$ constant
- Basic idea
  - We have know that to have a constant gm, we can use square-root circuit to keep $(\sqrt{I_P} + \sqrt{I_N})$ constant, -- is there any other way to do that?



- Please observe the complementary input stage

$$V_{12} = V_1 - V_2 = V_{GSN} + |V_{GSP}|$$

$$V_{GSN} = \sqrt{\frac{I_N}{2K}} + V_{TN} \quad \text{and} \quad |V_{GSP}| = \sqrt{\frac{I_P}{2K}} + |V_{TP}|$$

where $$K = \frac{1}{2} KP_N \left(\frac{W}{L}\right)_N = \frac{1}{2} KP_P \left(\frac{W}{L}\right)_P$$

so

$$(\sqrt{I_P} + \sqrt{I_N}) = \sqrt{2K}\,(V_{GSN} + |V_{GSP}| - V_{TN} - |V_{TP}|)$$

$$= \sqrt{2K}\,(V_{12} - V_{TN} - |V_{TP}|)$$

Rail-to-Rail Input Stage, Structure 7 (cont'd)

- To keep $(\sqrt{I_P} + \sqrt{I_N})$ constant is equivalent to keep $V_{GSN} + |V_{GSP}|$ constant if the transistors work in strong inversion region!
- We can get this conclusion by another way

  $gm_T = gm_N + gm_P$

  $gm_N = 2K(V_{GSN} - V_{TN})$ and $gm_P = 2K(|V_{GSP}| - |V_{TP}|)$

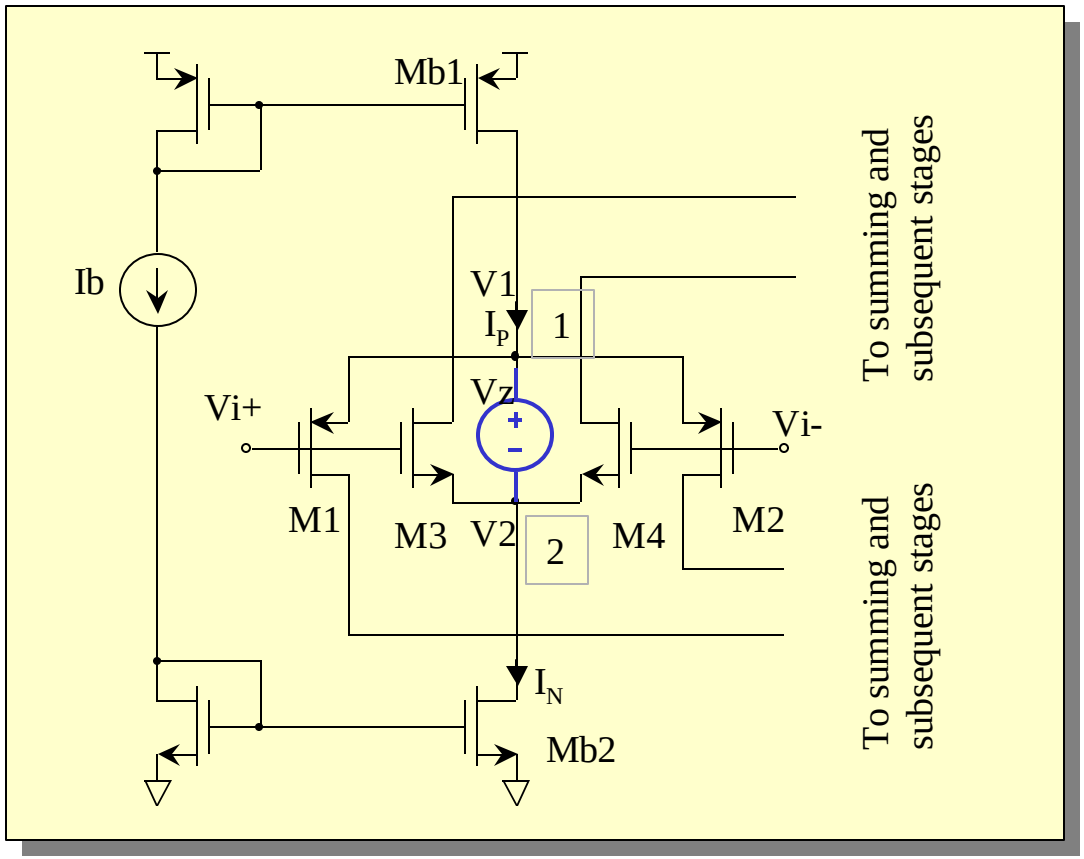
  so

  $gm_T = gm_N + gm_P = 2K(V_{GSN} + |V_{GSP}| - V_{TN} - |V_{TP}|)$

  To get a constant Gm, we should keep $V_{GSN} + |V_{GSP}|$ constant.
- Instead of controlling the tail current of the differential pair to have a constant gm_T, we can keep $V_{GSN} + |V_{GSP}|$ constant!
- This idea is shown in the block circuit diagram in the following.

Rail-to-Rail Input Stage, Structure 7 (cont'd)

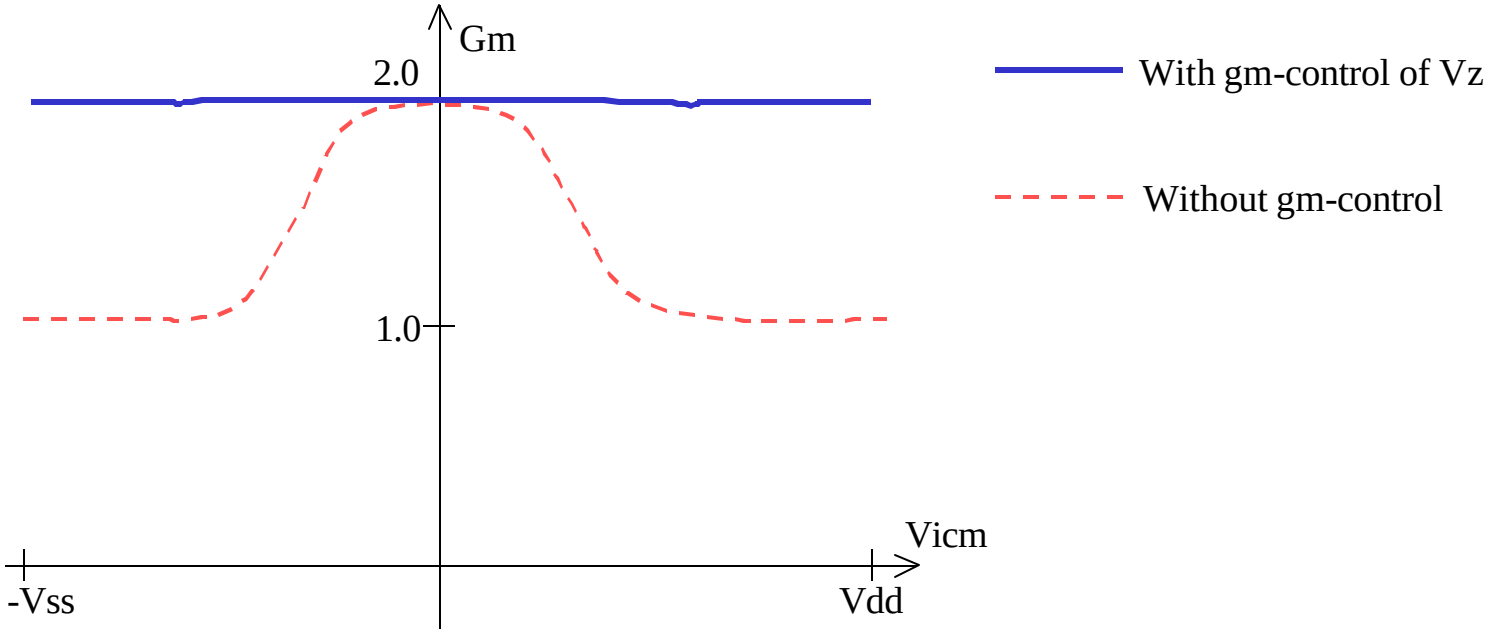
- The circuit showing the principle



Please notice that the floating voltage source Vz keeps VGSN+|VGSP| constant, the value of Vz is defined by $Vz = \frac{gm_T}{2K} + V_{TN} + |V_{TP}|$

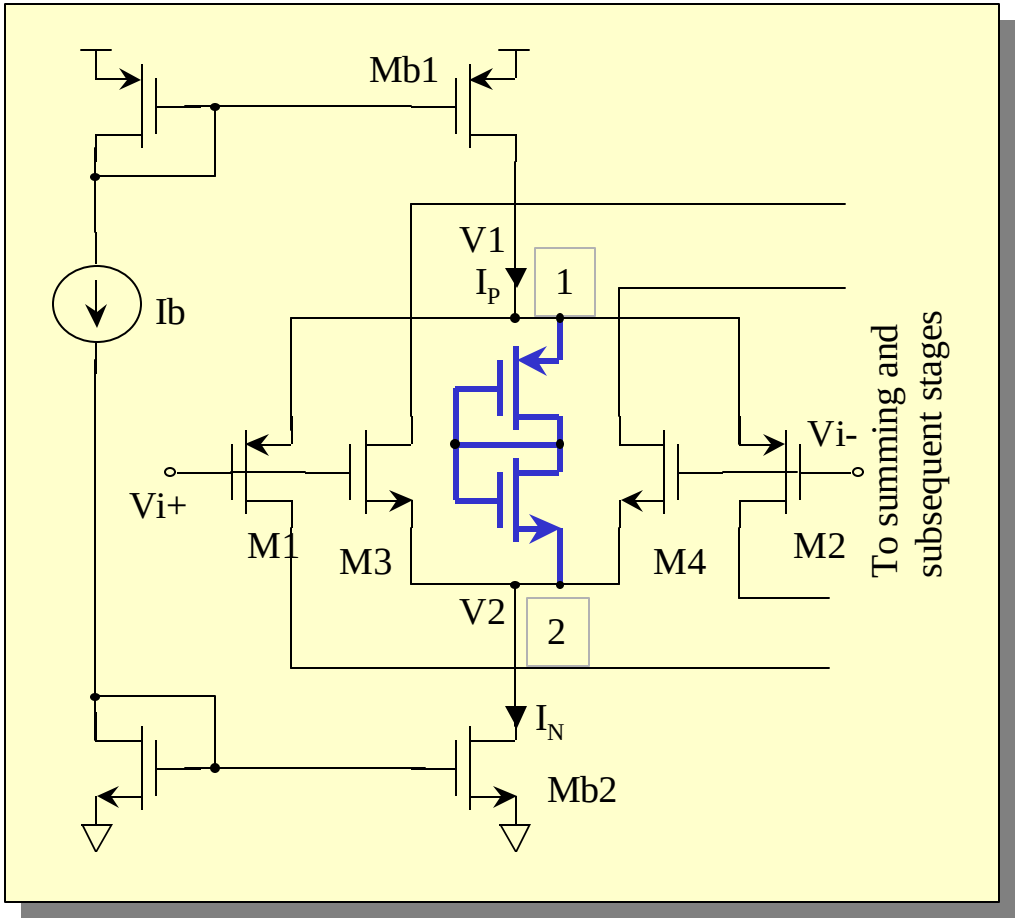
Rail-to-Rail Input Stage, Structure 7 (cont'd)

- Transconductance vs. input common mode voltage of the circuit in previous slide (with ideal voltage source Vz)



Rail-to-Rail Input Stage, Structure 7 (cont'd)

- One implementation with a simple electronic zener of 2 dioded connected CMOS FETs [10]

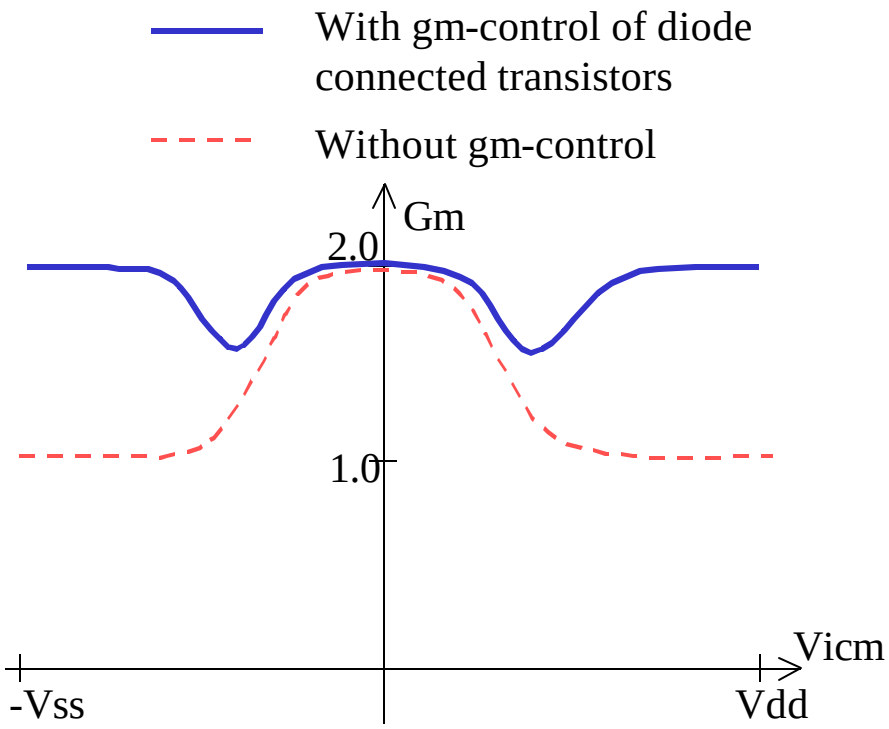


In this circuit, the voltage source Vz is replaced by 2 diode connected MOS transistors.

The small and large signal behavior of this electronic zener deviates from that of an ideal voltage source, which may introduce gm control error shown in next slide.

Rail-to-Rail Input Stage, Structure 7 (cont'd)

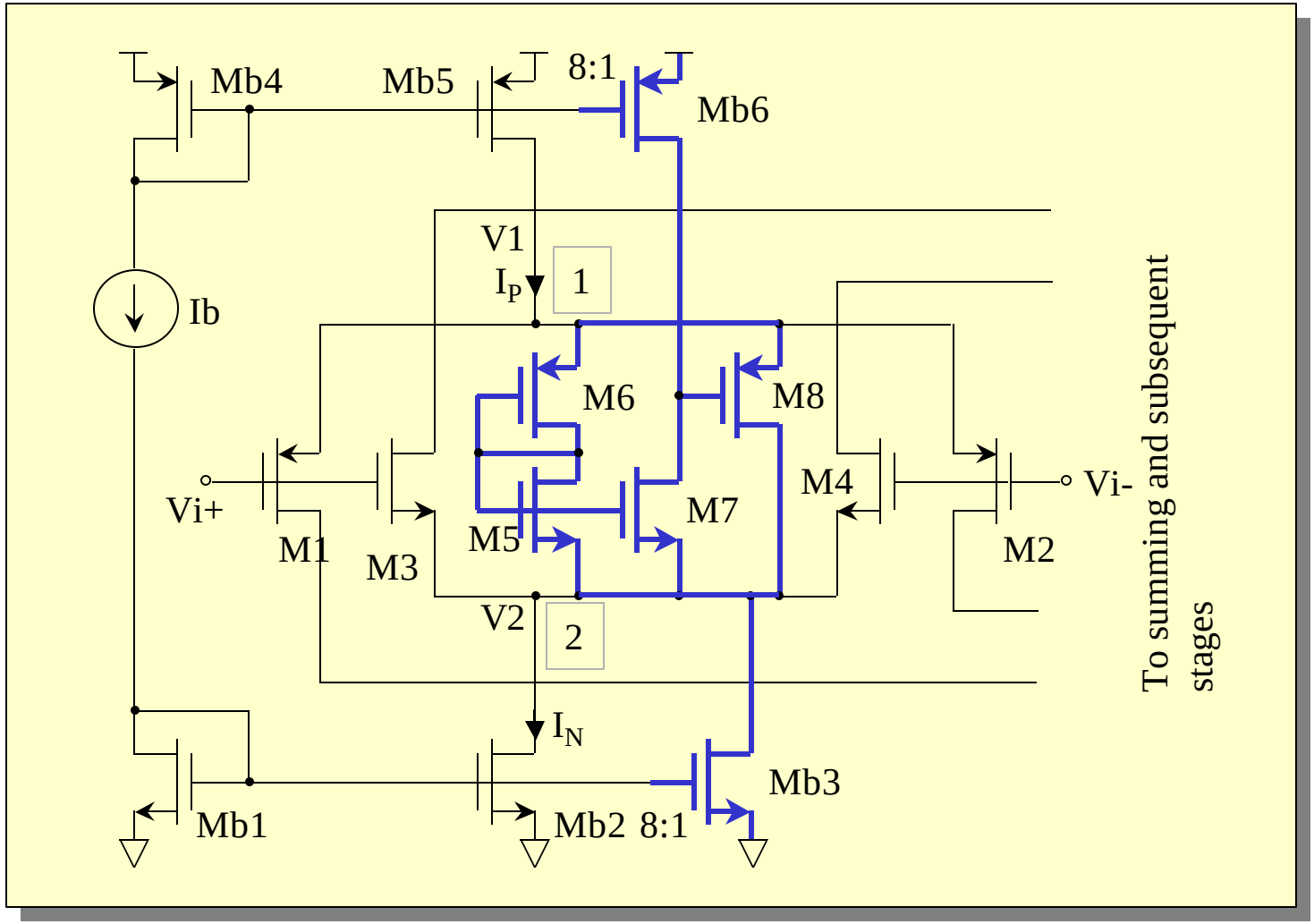
- Transconductance vs. input common mode voltage



Because of the non-ideality of the diode-connected transistors from ideal voltage sources, there are 2 dips in the transisconductance curve.

Rail-to-Rail Input Stage, Structure 7 (cont'd)

- A more precise electronic zener implementation [10]



Rail-to-Rail Input Stage, Structure 7 (cont'd)

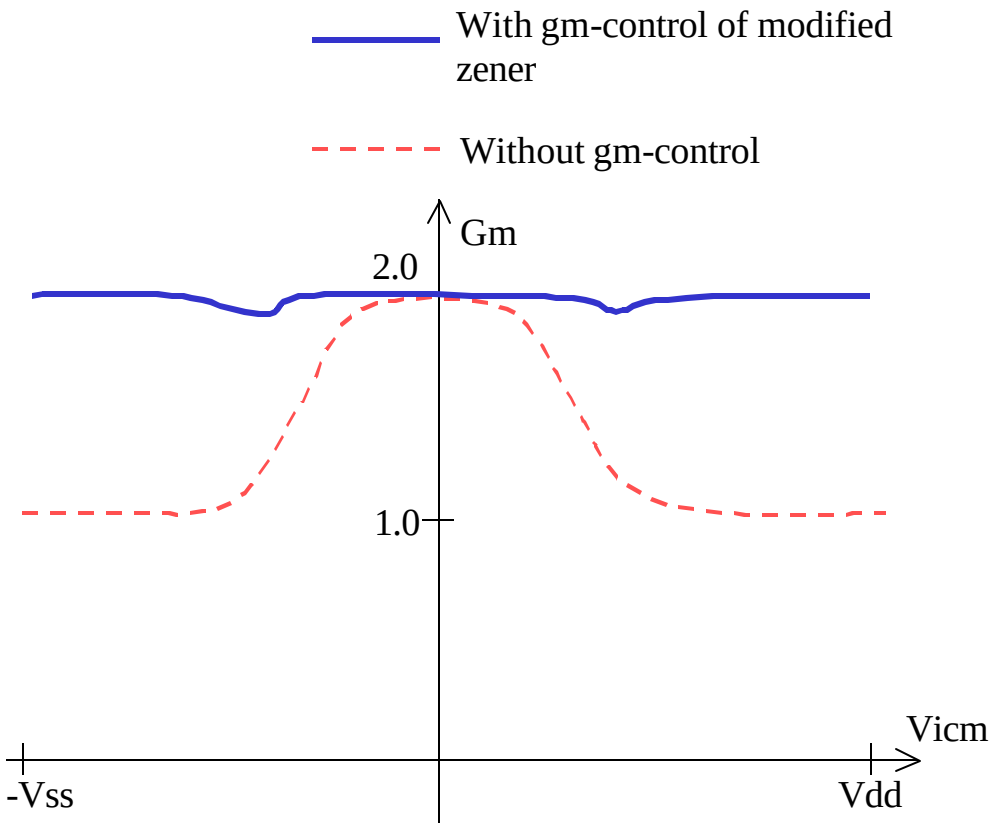
- Working Principle
  - In this circuit, the electronic zener is implemented by transistors M5-M8, Mb3, and Mb6. Mb3 and Mb6 are current sources.
  - As the load of M7 is a current source, and M5, M6, M7 and M8 form a feedback loop which defines the current through M7. Please note that M5 and M7 are current mirrors, $I_{D,M5} = I_{D,M7}$. So the current through M5 and M6 is constant. M5-M8 loop is equivalent to a zener with very low resistance. By small signal analysis, we can obtain the conductance for the electronic zener is

$$g_{equ} = \frac{g_{m5} g_{m6}}{g_{m5} + g_{m6}} \left(\frac{g_{m7}}{g_{m5}} \frac{g_{m8}}{g_{o7} + g_{o,Mb6}} + 1 \right)$$

which is $\left(\frac{g_{m7}}{g_{m5}} \frac{g_{m8}}{g_{o7} + g_{o,Mb6}} + 1 \right)$ times larger than that the simple zener implementation.

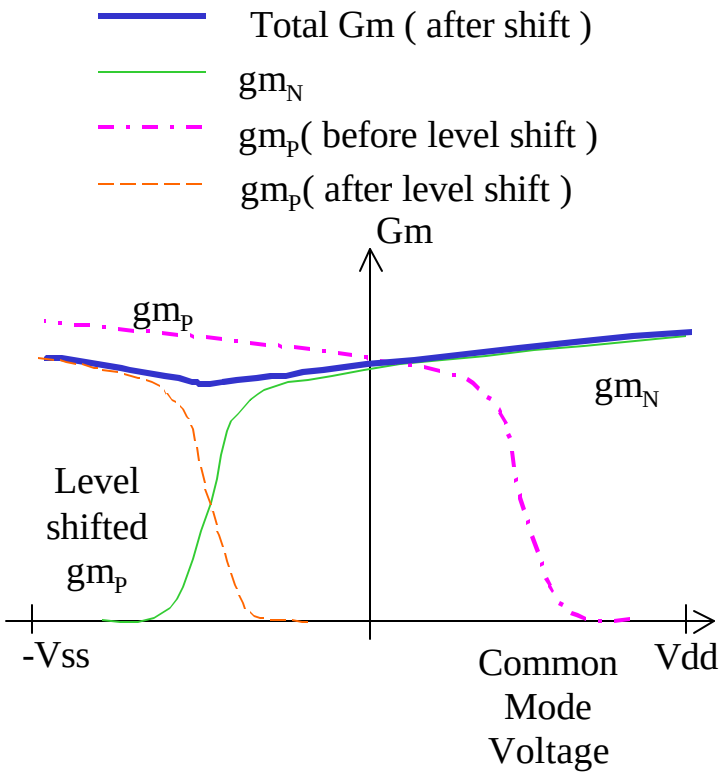
Rail-to-Rail Input Stage, Structure 7 (cont'd)

- Transconductance vs. input common mode voltage

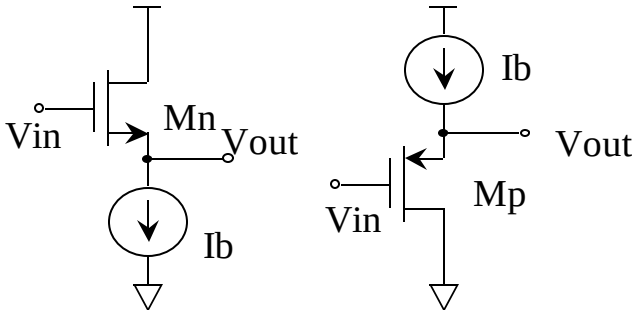


Rail-to-Rail Input Stage, Structure 8 [11]

- Using DC shifting circuit to change the input DC level
- Basic idea

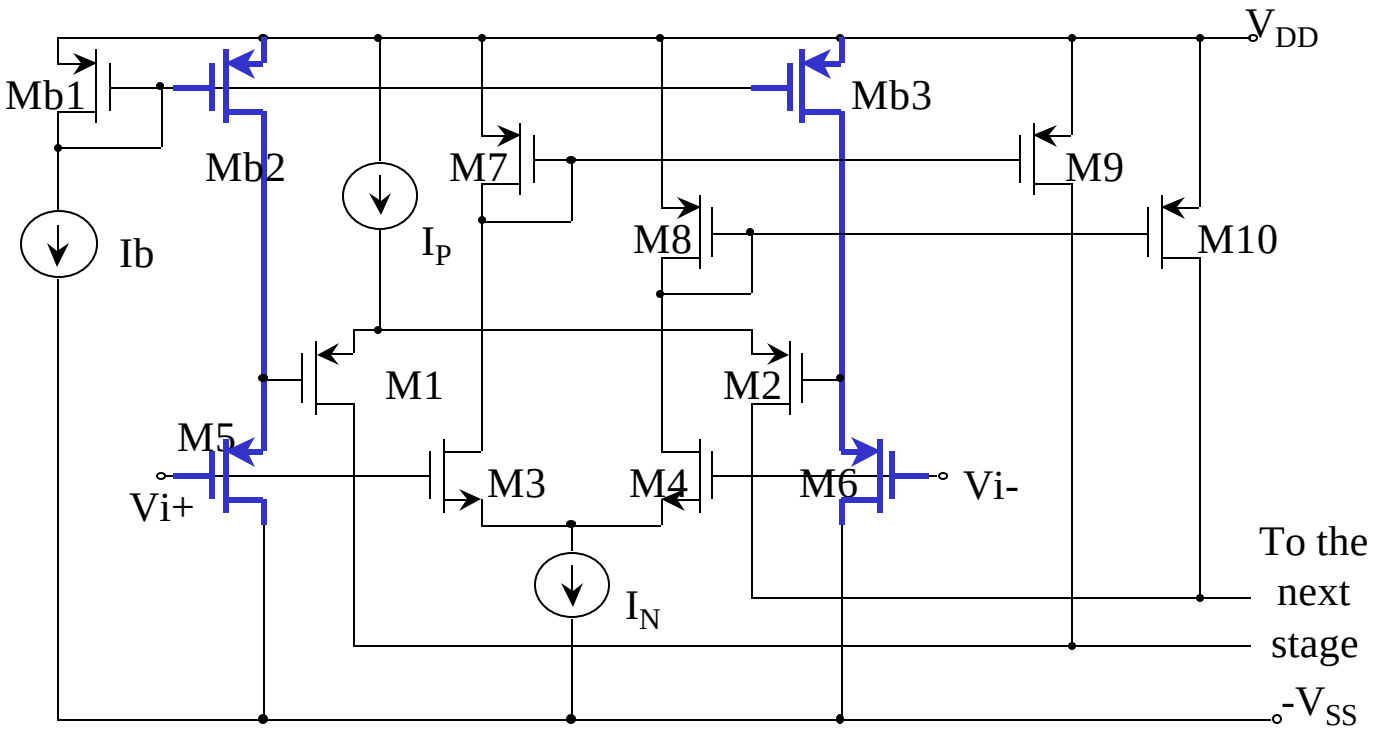


- We may notice that there is an overlap between gm_N and gm_P, so in the middle of the common mode voltage, the transconductance is doubled.
- How about shift one of the gm_N and gm_P curve? And let the transition regions of gm_N and gm_P come together, so that the total transisconductance will be nearly constant among the common mode input range.
- Level shift can be implemented by common source voltage follower. We can change the shift level by altering the bias current Ib.



Rail-to-Rail Input Stage, Structure 8 (cont'd)

- The circuit [11]

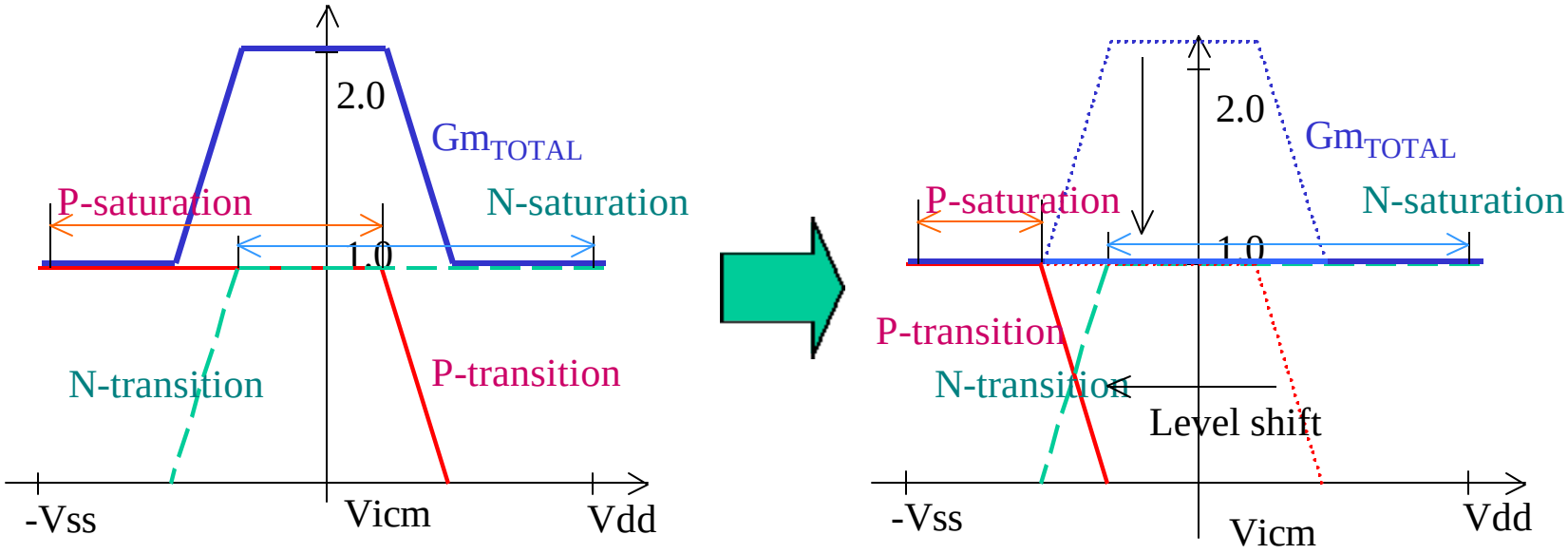


Note: 1) M5 and M6 are level-shifting transistors

2) The voltage shifted by M5 and M6 can be altered by changing Ib

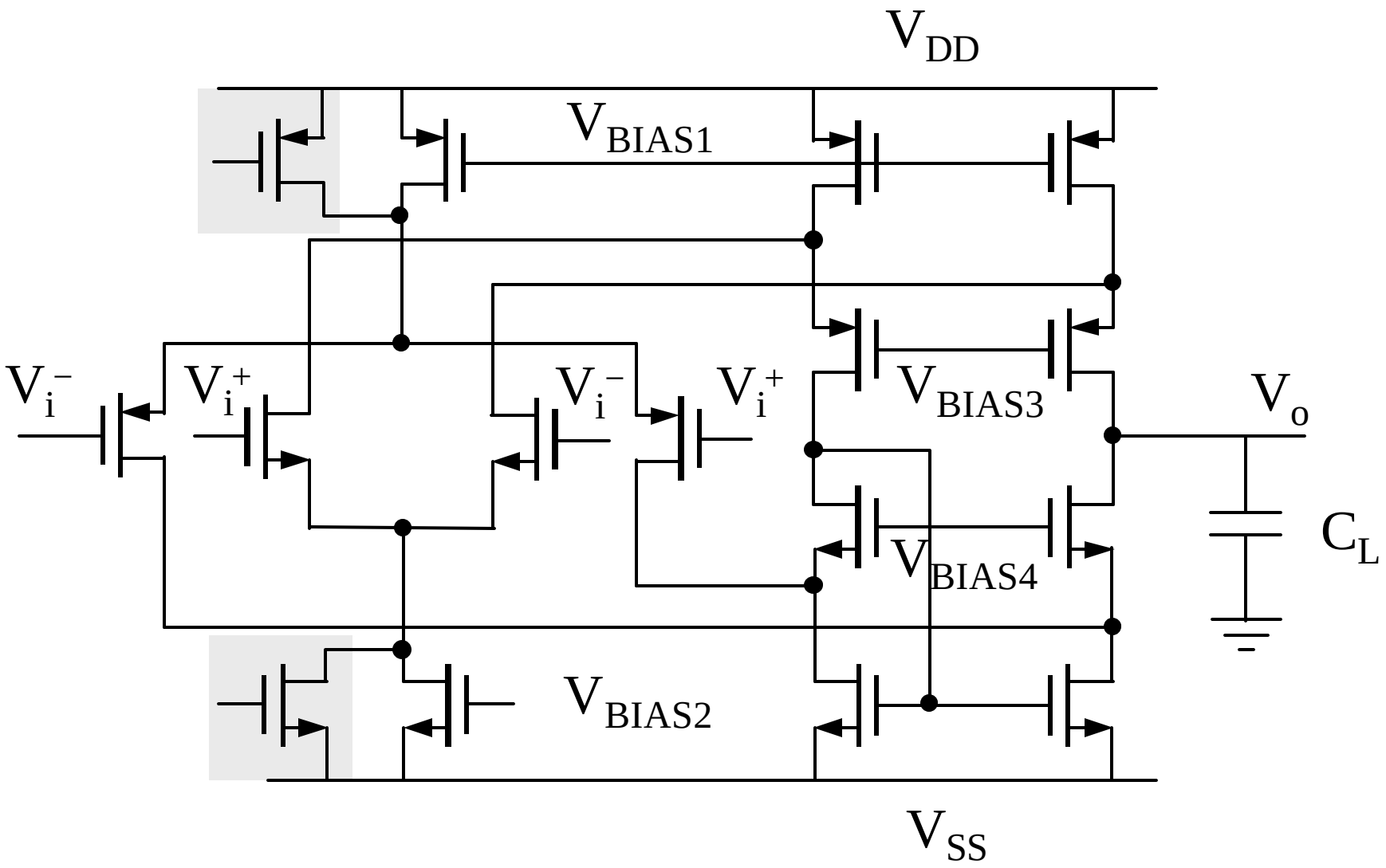
Rail-to-Rail Input Stage, Structure 8 (cont'd)

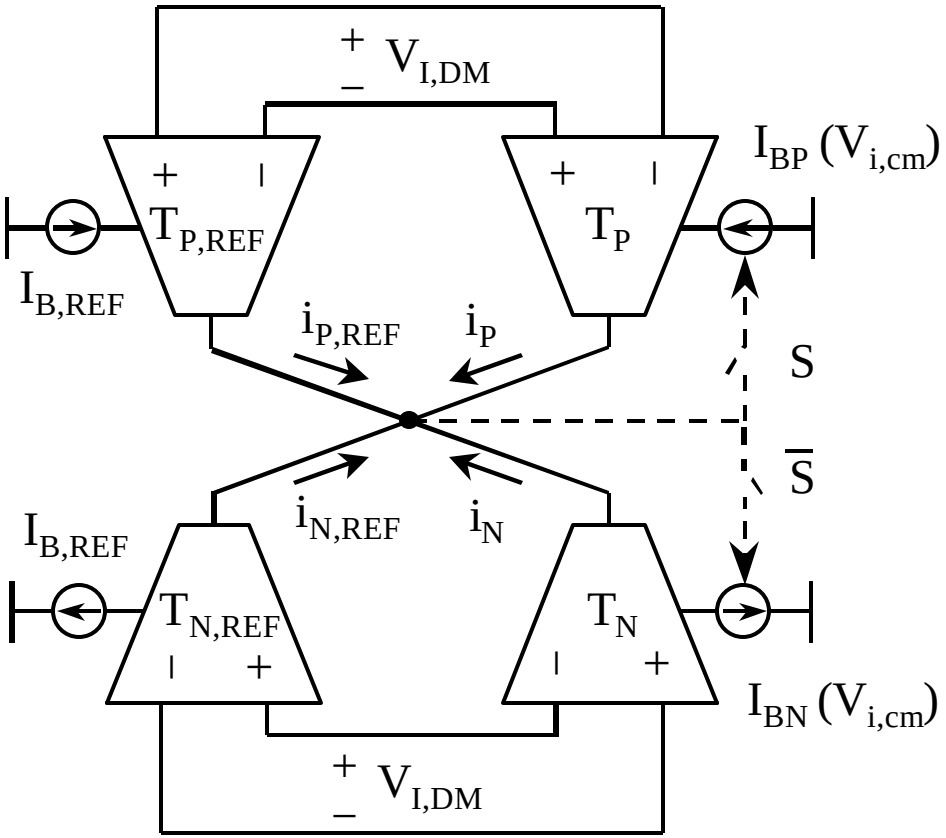
- Working principle
  - The input voltages are shifted by M5, M6 by $|V_{GS,M5,M6}|$ towards the positive power supply rail, so the transition region for gm_P is shifted by the same value towards the negative power supply rail.
  - The transistions region of gm_N and gm_P overlap and we can get an constant gm over the common mode range.

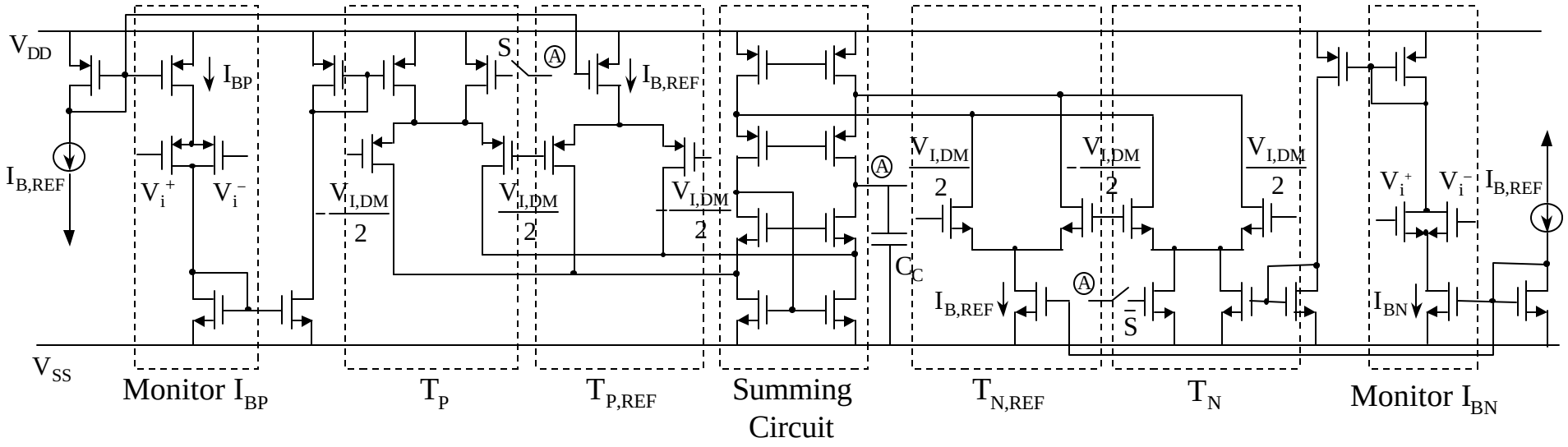


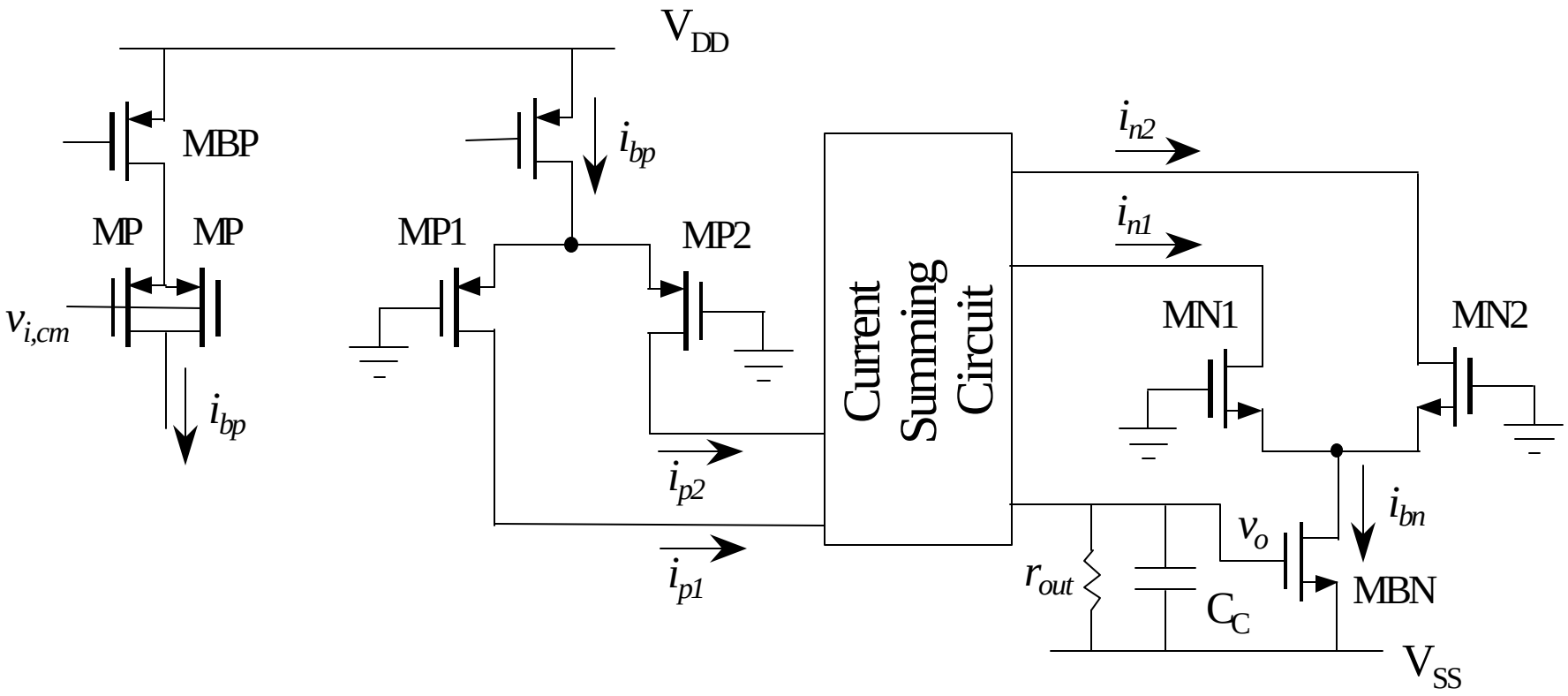
Rail-to-Rail Input Stage, Structure 8 (cont'd)

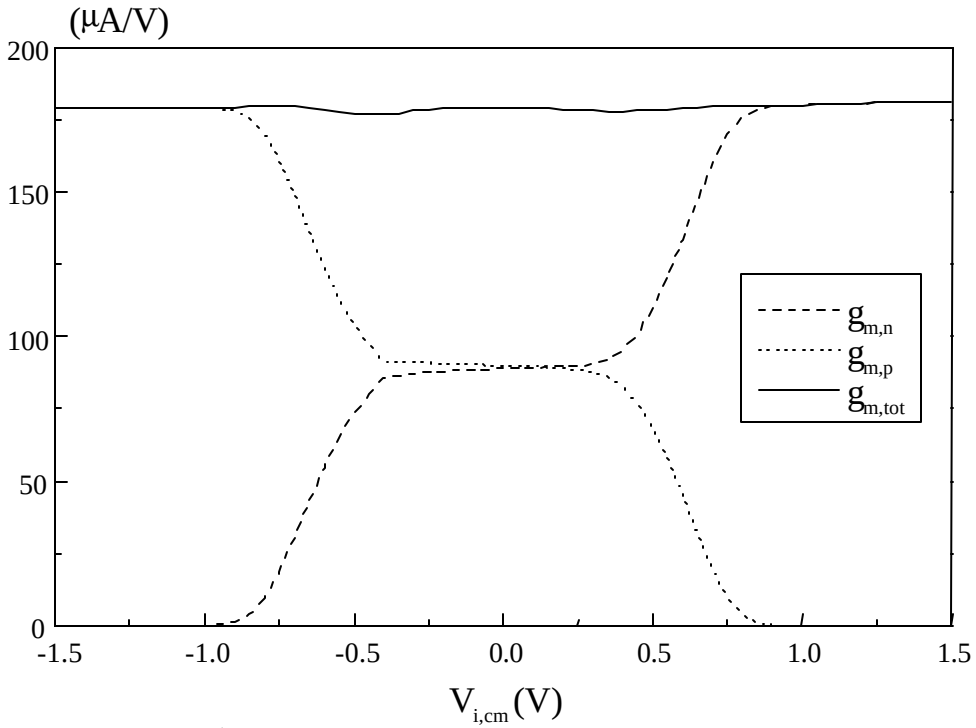
- Characteristics
  - We can obtain very small gm variation (±5%) if the DC shift level is tuned well [11].
  - This circuit structure is sensitive to the power supply changes and V_T variations, but we can add some auto-bias circuit to overcome this problem.

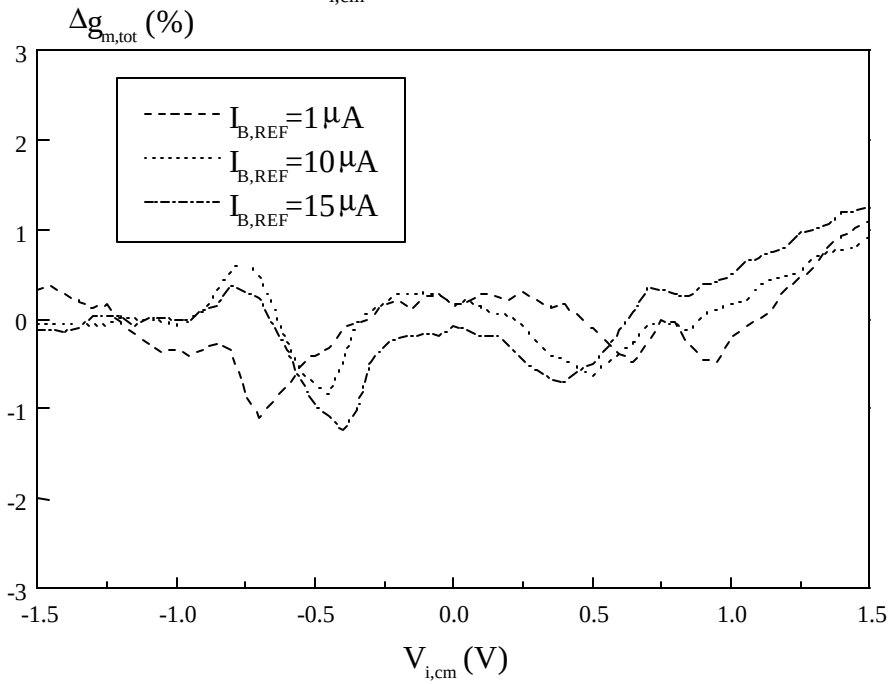

V_{DD}
V_{BIAS1}
V_i^-
V_i^+
V_i^-
V_i^+
V_{BIAS3}
V_o
C_L
V_{BIAS4}
V_{BIAS2}
V_{SS}

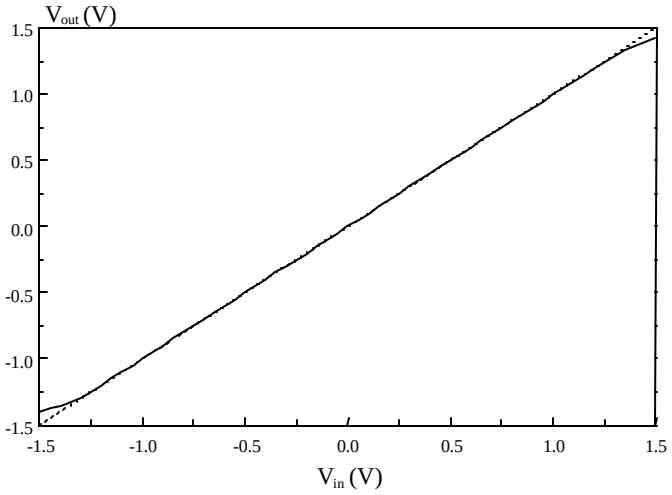

+
V I,DM
–
I BP (V i,cm)
T P,REF
T P
I B,REF
i P,REF
i P
S
S
i N,REF
i N
I B,REF
T N,REF
T N
I BN (V i,cm)
+
V I,DM
–


V_DD
I_BP
I_B,REF
V_i^+
V_i^−
S
A
I_B,REF
V_I,DM / 2
V_I,DM / 2
V_I,DM / 2
C_C
V_I,DM / 2
V_I,DM / 2
V_I,DM / 2
I_B,REF
A
S̄
V_i^+
V_i^−
I_B,REF
I_BN
V_SS
Monitor I_BP
T_P
T_P,REF
Summing Circuit
T_N,REF
T_N
Monitor I_BN


V_{DD}
MBP
i_{bp}
MP
MP
MP1
MP2
$v_{i,cm}$
i_{bp}
i_{p2}
i_{p1}
Current Summing Circuit
i_{n2}
i_{n1}
MN1
MN2
i_{bn}
v_o
r_{out}
C_C
MBN
V_{SS}


(μA/V)
200
150
100
50
0
-1.5
-1.0
-0.5
0.0
0.5
1.0
1.5
$V_{i,cm}$ (V)
$g_{m,n}$
$g_{m,p}$
$g_{m,tot}$


$\Delta g_{m,tot}$ (%)
3
2
1
0
-1
-2
-3
-1.5
-1.0
-0.5
0.0
0.5
1.0
1.5
$V_{i,cm}$ (V)
$I_{B,REF}$=1μA
$I_{B,REF}$=10μA
$I_{B,REF}$=15μA



Experimental amplifier behavior in unity-gain feedback configuration: (a) dc transfer characteristic, (b) transient response.

Summary and Comparison

Case	Principle	Δgm	Slew Rate	CMRR	Advantage	Limitations
1	$I_N + I_P = const$ [1][2][6]	N/A for weak inversion 40% if in strong inversion	Constant	56dB@10Hz, 52dB@100KHz, measured in [2]	Small gm variation (6%) in weak inversion operation	Only work well in weak inversion, can not used in high speed application
2	$\sqrt{I_N} + \sqrt{I_P} = const$ [3] [16]	-12% +6% (simulated in this presentation)	$\sqrt{2}$times variation	80 dB / 53 dB (measured in [3])		Depends on quadratic characteristics of MOSFETs, which is not exactly followed for short channel transistors in sub-micron processes
3	4 times I_N or I_P when only one pair operates [3][4][6]	+15% systematic gm variation	2 times variation	70dB / 43 dB (measured in [4])	Somewhat simple	1) Same with case 2, but we can change 4 to other numbers to have smaller gm variation for short channel transistors 2) Systematic gm deviation of 15% even for ideal MOSFETs with quadratic characteristics
4	Current switch, backup pairs [5]	+20% systematic gm variation	Constant	N/A	Constant slew rate	Systematic gm deviation of 20% even for ideal MOSFETs with quadratic characteristics
5	6-pair structure, back pairs [7]	+20% systematic gm variation (analytical), ±10% (measured in [7])	Constant	N/A	Constant slew rate	Same with Case 4
6	Max/min selection [8][9]	7% (simulated [9]) 5% (strong inversion, measured [8]) 20% (weak inversion, measured [8])	Constant	N/A		Somewhat complex
7	Electronic zener [10]	8% (measured)		80 dB / 43 dB (measured in [10])		Same with Case 2
8	Level shift [11]	±4% after tuning 13% before tuning (measured)		≥80 dB (DC) (measured in [11])	Simple	Gm variation sensitive to V_T variation and power supply voltage change

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[2] W.-C. S. Wu, W. J. Helms, J. A. Kuhn, and B. E. Byrkett, "Digital-compatible high-performance operational amplifier with rail-to-rail input and output ranges," *IEEE Journal of Solid-State Circuits*, vol. 29 , no. 1, pp. 63-66, January 1994

[3] R. Hogervorst, R. J. Wiegerink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-gm rail-to-rail input stage," *IEEE Proc. ISCAS* 1992, pp. 2876-2879

[4] R. Hogervost, J. P. Tero, R. G. H. Eschauzier and J. H. Huijsing, "A compact power-efficient 3-V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1505-1513, December 1994

[5] R. Hogervorst, S. M. Safai, and J. H. Huijsing, "A programmable 3-V CMOS rail-to-rail opamp with gain boosting for driving heavy loads," *IEEE Proc. ISCAS 1995*, pp. 1544-1547

[6] J. H. Huijsing, R. Hogervorst, and K.-J. de Langen, "Low-power low-voltage VLSI operational amplifier cells," *IEEE Trans. Circuits and Systems-I*, vol. 42. no. 11, pp. 841-852, November 1995

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[7] W. Redman-White, "A high bandwidth constant *gm*, and slew-rate rail-to-rail CMOS input circuit and its application to analog cell for low voltage VLSI systems," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 701-712, May 1997

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