REPORT

PROJECT #1

Design of a

CMOS Operational Amplifier

Course No. EE610

Course Name: Analog Electronic Design

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Objective:

To design a two stage operational amplifier to meet the following specifications:

1) Open Loop gain > 2000
2) GBW > 1 MHz
3) Power Supply = +/- 5V
4) Load Capacitance = 10 pF
5) Slew Rate >= 2V/µS
6) Output Range > +/- 3.5V
7) Input CMR > +/- 3V
8) Channel Length = 10 µm

Design Method

The Op-amp consists of two stages:

1) The differential amplifier stage.
2) Common source amplifier.

We assume the transistors to be symmetrical.

Basic relationships used in the designing process:

1) Slew Rate	$SR = I_5/C_c$
2) First Stage Gain	$A_{v1} = g_{m2}(r_{o2} \parallel r_{o3})$
3) Second Stage Gain	$A_{v2} = g_{m7}(r_{o6} \parallel r_{o7})$
4) Gain Bandwidth	$GBW = g_{m2}/Cc$
5) Common Mode Gain	$A_{cm} = (r_{o2} \parallel r_{o4})/r_{o5}$
6) Differential mode gain	$A_d = A_{v1} * A_{v2}$
7) Common Mode Rejection Ratio	$CMRR = A_d / A_{cm}$

The design is started using the specification given for load capacitance C_L. We assume the value of the compensating capacitance to be greater than C_L / 5 to get phase margin greater than 45°.

$\boldsymbol{C_c \geq C_L/5}$ = 10 pF/5 = 2 pF.
We take the value of C_c to be 2.5 pF.

Now using the relationship for slew rate(1) we calculate the current I_5.

$\boldsymbol{SR = I_5/C_c}$

$I_5 = SR * C_c = 2 * 10^6 * 2.5 * 10^{-12} = 5\ \mu A$

Let us assume $I_5 = 6\ \mu A$.

Hence we get $I_1 = I_2 = I_3 = I_4 = I_5 /2 = 3\ \mu A$.

Now using the formula for GBW(4) we calculate g_{m2}.

$\boldsymbol{GBW = g_{m2}/C_c}$
$g_{m2} = GBW * C_c$
$= 1 * 10^6 * 2 * \Pi * 2.5 * 10^{-12}$

= 1.57 * 10-5 V/A

Using the values for g_{m2} and I_2 we calculate the widths of transistors M1 and M2 using the general formula for g_m

$$g_m = \sqrt{\left(2 * k' * \frac{W}{L} * I_d\right)}$$

Using the value of g_{m2} and I_2 we obtain W = 5.8 µm.
But maintaining thte aspect ratio W/L >= 1 the minimum value of W2 is 10 µm.

W1 = W2 = 10 µm

** Further calculations will be done using the obtained value only **

Now the widths of transistors M3, M4, M5 are obtained using the input CMR value in such a way that the none of the transistor goes into saturation for the given conditions. The condition that the transistor does not go into saturation is that $V_{DS} \geq V_{GS} - V_T$.

For negative CMR the width of M5 is adjusted such that

-ve CMR = $(V_{GS} - V_T)_5 + V_{GS2} - 5$

The V_{GS} of the transistor is obtained using the relation:

$$I_d = ½ k' W/L (V_{GS} - V_T)^2$$

Using this relation V_{GS2} = 0.891 V.

The given –ve CMR is –3V , but to give some margin for simulation we assume it to be -4V for design purpose.

-4 = $(V_{GS} - V_T)_5$ + 0.891 – 5

$(V_{GS} - V_T)_5$ = 0.109 V .

Using this value of $(V_{GS} - V_T)_5$ and the value of I_5 in the current equation we calculate the width of transistor M5. This width is also

W5 = 10 µm

Similarly for +ve CMR = 4 V width of M3 and M4 is obtained in such a way that none of the two go into saturation.
+ve CMR = 5 – $(V_{GS} - V_T)_4$

$(V_{GS} - V_T)_4$ = 1 V.

Using this value of $(V_{GS} - V_T)_4$ and the current I_4 in the current equation we obtain the width of M4. This width is obtained as 2.5 µm. Normally the W/L of any transistor is greater than 1. So we take the width of M4 as 10µm. As M3 and M4 are matched W3 = W4.

W3 = W4 = 10 µm

Thus we have obtained the widths of all the transistors of the first stage.

For second stage we assume the current I_7 is assumed to be $5*I_5$ since we assumed Cc to be 1/5th of CL to maintain the slew rate.

$I_7 = 30\mu A$

The output swing of the amplifier is used to determine the widths of the transistors M6 and M7. Also the width of the transistor M6 is to be adjusted so as to adjust the W/L ratios with transistor M8 so as to give the required current.

For negative output swing the width of M7 is adjusted so that it does not go out of saturation.

-ve Vo = $(V_{GS} - V_T)_7 - 5$

The given output swing is –3.5 V but assuming it to be –4 V, about 0.5 V more than the specification we calculate $(V_{GS} - V_T)_7$.

$(V_{GS} - V_T)_7 = 1$ V.

Using this value and the current I7 in the current equation we calculate the width of transistor M7.

This width has to be adjusted according to the W/L and the current ratios of the transistor M8, which is the current source.

Let the current at M8 = 6 µA. (For minimum power consumption)

Now from the expression:

$$I_{d5} = I_8 \frac{(W/L)_5}{(W/L)_8}$$

Using this we get the width of M8 as:

W8 = 10 µm

In order to make the W/L ratio to be 1, we assume the width to be 10 µm.

Using this W8 we calculate the width of M7 is calculated again and found out to be

W7 = 50 µm

For this width again the $(V_{GS} – V_T)_7$ is calculated to obtain the output swing and verify whether it is as per the specifications.

$(V_{GS} – V_T)_7 = 0.442$ V

Vo = 0.442 – 5
= -4.558 V.

For +ve output swing the width of M6 is adjusted so that it does not go out of saturation.

Assuming the output swing to be 4V we get $(V_{GS} – V_T)_6 = 1$ V. Using this value and the value of current I_6 in the current equation we calculate the width of M6.

W6 =75 µm

Thus we have obtained the widths of all the transistors. All these values are summarized in the table below:

Sr. No.	Transistor	Length (L) (µm)	Width (W) (µm)	Current (Id) (µA)
1	M1	10	10	3
2	M2	10	10	3
3	M3	10	10	3
4	M4	10	10	3
5	M5	10	10	6
6	M6	10	75	30
7	M7	10	50	30
8	M8	10	10	6

SIMULATION AND RESULTS

Cadence was used to simulate the op-amp designed and to obtain various parameters. The widths of all the transistors were entered as per what was calculated and the lengths of all the transistors was taken as 10 µm. Simulation was performed using the model file ourCMOS.m which included all the specifications of the transistor AMI 1.5µ.

DC Bias Analysis

DC bias analysis was done to measure the currents and voltages. The values obtained were almost equal to what was calculated theoretically.

Before any AC analysis was done DC Offset Voltage was calculated.

Connecting and op-amp in a unity gain configuration (connecting a feedback to the inverting terminal) and grounding the non inverting input terminal the DC offset voltage was obtained.

DC offset voltage = -4.494 µV.

This voltage was connected as the dc input to the amplifier for all further transient and AC analysis.

Transient Analysis

Transient analysis was done using an input sine wave of 10 µV and a frequency of 100Hz (lesser than the first pole of the amplifier) at one input of the amplifier and the other input was grounded. Open loop gain was calculated by observing the output waveform's amplitude (peak to peak).

Differential Mode Gain: -

Differential mode gain was found out to be 12506.06 which is very less than the hand calculated value. This might be due to the fact that the transistors used were of 10 µm length whereas the specifications used in the model were of 1.5 µm.

Thus **Ad = 12506.06**

Common Mode Gain: -

The common mode gain was measured by giving an input of 3 V and a frequency 10Hz (first pole of CM gain is very less). The obtained gain value was very less as compared to the hand calculated value and the common mode gain was found out to be 0.0019. Since all the transistors and the currents through each are perfectly balanced we get such a low value of the common mode gain.

Thus **Acm = 0.0019**

Common Mode Rejection Ratio: -

Using the open loop gain and the common mode gain we calculate the CMRR.
CMRR = 20 log (Ad/Acm)

CMRR = 116 dB.

Output swing: -

Next the output swing of the amplifier output is measured. For this the input to the amplifier is given such that the output just swings upto the given specifications. This input was found out to be 200 μV for which the output swings up to 4.5 V in both directions.

Output swing = ± 4.5 V.

Slew Rate: -

Now the slew rate is obtained. For this the circuit is connected in a unity gain configuration and a sinusoidal input of magnitude equal to the CMR and frequency less than the GBW of the amplifier or a rapidly changing pulse can be used as input. We need to give a rapidly changing input. In our simlation a pulse input of magnitude –5 V to 5 V with a rise time of 0.1 μsec and period of 10ms was used as an input. The output is observed till it loses its sinusoidal shape and turns to become linear. The slope of this linear output gives the slew rate of the amplifier.

Slew Rate = 2.7 V/μsec.

Common Mode Range: -

For checking the common mode range we connected a common mode DC signal equal to the CMR given in the specifications and found out the DC operating points of each transistor that is we obtained the Vds and Vgs of each transistor and checked whether each transistor was in saturation or not.
We found out that for common mode input of 3 V we got all transistors to be in saturation and similarly for common mode input of –3 V also we found out that all the transistors were in saturation . Thus the CMR > ± 3 V.

Common Mode Range CMR > ± 3 V.

Phase Margin and Bandwidth: -

The phase margin of the op-amp was measured by simulating the plot of the gain in dB over frequency in logarithmic scale. The frequency at which the gain went to 0 dB

(Gain = 1) was measured. The phase margin of the amplifier is obtained from the plot of phase versus frequency at this particular frequency. Also the –3 db frequency was obtained from the plot of gain (dB) versus frequency which gives the 3 dB bandwidth.

The value of the compensating capacitor was reduced to 2.2 pF to have a phase margin in a suitable limit.

From the plot of gain versus frequency the unity gain frequency was obtained to be 710.6 KHz and the phase margin was obtained to be 60.66 °. The GBW was obtained to be 1.71 MHz.

Thus

Phase Margin = 60.66 °
-3 dB Frequency (Bandwidth) GBW = 1.71 MHz.

Also the width of M6 was increased to 85 μm to meet the current requirements and increase the transconductance of the transistor. This change did not affect the saturation conditions and also helped in obtaining a good value of the bandwidth and phase margin. This changes did not affect the other parameters of the amplifier and they all where within the specifications.

All the circuit configurations and the plots for each simulation are attached in this report.

<u>Hand Calculated Values and the Simulated Values:</u>

Sr No.	Parameter	Hand Calculated Values	Simulated Values (as per graph)
1	Open Loop Gain		12506
2	Common mode gain		0.00195
3	CMRR		116 dB
4	GBW		1.71 MHz
5	Phase Margin		60.66 °
6	Slew Rate		2.7 V /μsec
7	Input CMR		± 3 V
8	Output Range		± 4.6 V
9	Power Supply		± 5 V

Final Simulation results:-

Open Loop Gain = 12506
Common Mode Gain = 0.00195
CMRR = 116 dB
Output Range = $\pm$ 4.6 V
Slew Rate = 2.7 V/ μsec
Common Mode Range = $\pm$ 3 V
Phase Margin = 61 °
Gain BandWidth = 1.71 MHz