1.457304, 0.505334, 0.495759, 0.037408 and 0.001736 for the $\boldsymbol{Q}$ matrix.

Next, we chose $\boldsymbol{P} = \boldsymbol{I}_2$ and adjusted the scalar α so that

$$\left\| \left[\frac{1}{\sqrt{\alpha}} \boldsymbol{A}_1, \frac{1}{\sqrt{1-\alpha}} \boldsymbol{A}_2 \right] \right\| < 1.$$

Consequently, we found $\alpha = 0.54$ and $\beta = 0.46$. Then the $\boldsymbol{Q}$ matrix was derived from (35) as

$$\boldsymbol{Q} = \begin{bmatrix} 0.272964 & 0.036040 & -0.216456 & 0.103763 \\ 0.036040 & 0.320809 & -0.074999 & -0.213642 \\ -0.216456 & -0.074999 & 0.233872 & -0.012962 \\ 0.103763 & -0.213642 & -0.012962 & 0.233725 \end{bmatrix}$$

with the eigenvalues equal to 0.507094, 0.497351, 0.054326, and 0.002600. Since $\|\boldsymbol{A}\| = 0.500001$, from (33) and (41) it follows that $|\Delta \boldsymbol{A}\| \leq 0.001836$ and $L \geq 9.089145$, respectively.

VI. Conclusion

Based on the Fornasini-Marchesini second LSS model, the stability of 2-D discrete systems has been treated using the 2-D Lyapunov equation with constant coefficients. After showing sufficient conditions for a 2-D discrete system to be asymptotically stable, a sufficiency condition that ensures the absence of overflow oscillations has been presented under the assumption that a 2-D discrete system is used by saturation arithmetic. In addition, the relationship between the stability margin of a 2-D discrete system and the 2-D Lyapunov equation has been examined. It has been shown that an upper bound stated in this paper is less conservative than the previous ones.

References

[1] E. Fornasini and G. Marchesini, "Doubly-indexed dynamical systems: State-space models and structural properties," *Math. Syst. Theory*, vol. 12, pp. 59–72, 1978.

[2] ——, "On the internal stability of two-dimensional filters," *IEEE Trans. Automat. Contr.*, vol. AC-24, pp. 129–130, Feb. 1979.

[3] ——, "Stability analysis of 2-D systems," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 1210–1217, Dec. 1980.

[4] T. Hinamoto, "The Fornasini-Marchesini model with no overflow oscillations and its application to 2-D digital filter design," in *Proc. 1989 IEEE Int. Symp. Circuits Syst.* Portland, OR, May 1989, pp. 1680–1683.

[5] T. Hinamoto, "2-D Lyapunov equation and filter design based on the Fornasini-Marchesini second model," *IEEE Trans. Circuits Syst. I*, vol. 40, pp. 102–110, Feb. 1993.

[6] W.-S. Lu, "Some new results on stability and stability robustness of Fornasini-Marchesini state-space 2-D digital filters," in *Proc. IEEE Southeastcon'94*, Miami, FL, Apr. 1994, pp. 21–25.

[7] ——, "On a Lyapunov approach to stability analysis of 2-D digital filters," *IEEE Trans. Circuits Syst. I*, vol. 41, pp. 665–669, Oct. 1994.

[8] ——, "On robust stability of 2-D discrete systems," *IEEE Trans. Automat. Contr.*, vol. 40, pp. 502–506, Mar. 1995.

[9] S. G. Tzafestas, A. Kanellakis, and N. J. Theodorou, "Two-dimensional digital filters without overflow oscillations and instability due to finite word length," *IEEE Trans. Signal Processing*, vol. 40, pp. 2311–2317, Sept. 1992.

[10] R. P. Roesser, "A discrete state-space model for linear image processing," *IEEE Trans. Automat. Contr.*, vol. AC-20, pp. 1–10, Feb. 1975.

A Compensation Strategy for Two-Stage CMOS Opamps Based on Current Buffer

G. Palmisano and G. Palumbo

***Abstract*—The compensation with current buffer overcomes the typical drawbacks of the compensations based on nulling resistor or voltage buffer, but it is not as straightforward as the other two approaches. Indeed, a constraint on the current-buffer input resistance has to be met in order to achieve frequency compensation, since complex conjugate poles arise in the loop transfer function. In the brief design equations for an optimized compensation strategy with current buffer are determined. They allow a high gain-bandwidth product to be achieved avoiding the drawbacks which arises with voltage buffer and nulling resistor approaches.**

I. Introduction

Two-stage CMOS opamps adopt Miller compensation to achieve stability in closed-loop conditions [1]–[7]. Unfortunately, this compensation is responsible for a right half-plane zero in the open-loop gain, which is due to the forward path through the compensation capacitor to the output. An uncompensated right half-plane zero drastically reduces the maximum achievable gain-bandwidth product, since it makes a negative phase contribution to the open-loop gain at a relatively high frequency. As a consequence, in the design of two-stage opamps, compensation of the right half-plane zero is mandatory [8], [9]. After the compensation of the right half-plane zero, the maximum achievable gain-bandwidth product is limited by the second pole. Indeed, in order to guarantee an adequate phase margin, ϕ, (the phase margin to achieve the minimum settling time at 0.1% is 70° [2]) we must properly set the ratio of the second pole, ω_{p2}, to the gain-bandwidth product, ω_{GBW},[1] which is equal to the tangent K of the phase margin [3]

$$K = \tan\phi = \frac{\omega_{p2}}{\omega_{\mathrm{GBW}}}. \tag{1}$$

For example, a phase margin between 60° and 76° gives values of K from 1.73 to 4. On the other hand, the ω_{GBW} depends both on the transconductance of the first stage, g_{m1}, and on the compensation capacitance, C_C, and is given by

$$\omega_{\mathrm{GBW}} \cong \frac{g_{m1}}{C_C}. \tag{2}$$

Various techniques for compensation of the right half-plane zero in two-stage CMOS opamps have been proposed. The original of these was applied to NMOS opamps [10] and then to CMOS opamps [11]. It breaks the forward path through the compensation capacitor by introducing a voltage buffer in the compensation branch. Then, a compensation technique was proposed which uses a nulling resistor in series with the compensation capacitor [12]. Another solution works like the former but uses a current buffer to break the forward path [13]. Finally, both current and voltage buffers can be adopted for compensation of the right half-plane zero [14].

Manuscript received October 16, 1995; revised February 23, 1996. This paper was recommended by Associate Editor D. A. Johns.

The authors are with the Dipartimento Elettrico Elettronico e Sistemistico, Universitá di Catania, I-95125 Catania, Italy.

Publisher Item Identifier S 1057-7122(97)02070-9.

[1] In a pole dominant amplifier ω_{GBW} is about equal to the transition frequency ω_T.

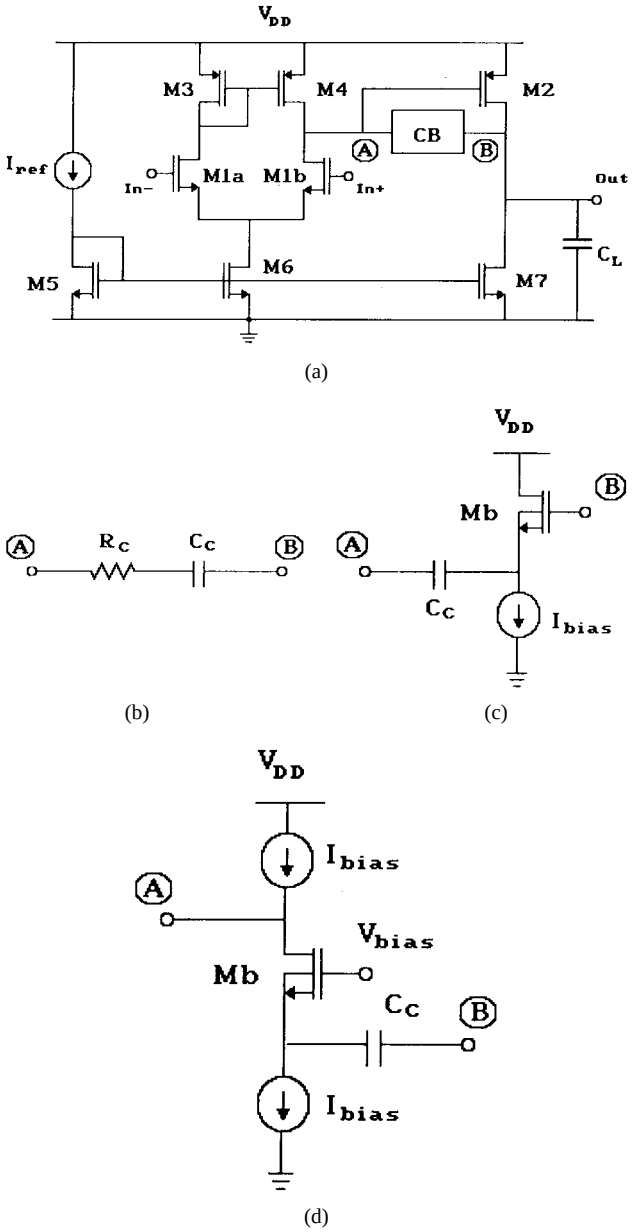

Fig. 1. (a) Two-stage opamp. (b) Nulling-resistor compensation block. (c) Voltage-buffer compensation block. (d) Current-buffer compensation block.

The most popular compensation technique is that based on the nulling resistor, since it can be implemented using only an MOS transistor biased in the triode region. From Fig. 1(a) with block CB replaced by the circuit in Fig. 1(b), the second pole frequency is

$$\omega_{p2} = \frac{g_{m2}}{C_{o1} + C_L + \frac{C_{o1}C_L}{C_C}} \cong \frac{g_{m2}}{C_L\left(1 + \frac{C_{o1}}{C_C}\right)} \tag{3}$$

where g_{m2} is the transconductance of the second stage, C_L is the load capacitor, and C_{o1} is the equivalent capacitance on the output of the first stage. Substituting (2) and (3) in (1) and solving for C_C we get

$$C_C = \frac{g_{m1}}{2g_{m2}}K\left(1 + \sqrt{1 + \frac{4g_{m2}}{Kg_{m1}}\frac{C_{o1}}{C_L}}\right)C_L \cong \frac{g_{m1}}{g_{m2}}KC_L. \tag{4}$$

Thus, the compensation capacitor is linearly dependent on the load capacitance.

The adoption of an ideal voltage buffer (i.e., with zero output resistance) to compensate the right half-plane zero gives the same second pole as (3) and, hence, the same ω_{GBW}. On the other hand, the finite output resistance of a real voltage buffer leads to a left half-plane zero, that can be efficiently exploited to perform a pole-zero compensation and to increase the amplifier gain-bandwidth [16]. Following this last compensation strategy, with block CB in Fig. 1(a) replaced by the circuit in Fig. 1(c), the second pole is [16]

$$\omega_{p2} = \frac{g_{m2}}{C_L}\frac{C_C - C_b}{C_{o1} + C_b} \tag{5}$$

where C_b is the feedforward capacitance of the voltage buffer. Again, substituting (2) and (5) in (1) and solving for C_C we get

$$\begin{aligned} C_C &= \frac{C_b}{2}\left(1 + \sqrt{1 + 4\frac{g_{m1}}{g_{m2}}K\frac{(C_{o1} + C_b)C_L}{C_b^2}}\right) \\ &\cong \frac{C_b}{2} + \sqrt{\frac{g_{m1}}{g_{m2}}K(C_{o1} + C_b)C_L}. \end{aligned} \tag{6}$$

The compensation capacitor given by (6) has a lower value than that given by (4), and, apart from the small contribution of C_b, is dependent on the geometric media of $C_{o1} + C_b$ and C_L [16]. In terms of gain-bandwidth product, the compensation based on voltage buffer is also better than the optimized compensation which is based on nulling resistor [15].

On the other hand, the compensation based on current buffer [i.e., block CB in Fig. 1(a) replaced by the circuit in Fig. 1(d)] seems to be very efficient both for the gain-bandwidth [17], [18] and the PSRR performance [13], [19]–[21]. Moreover, it does not have the drawback of the voltage buffer which reduces the amplifier output swing.

Considering an ideal current buffer in the compensation branch, the second pole is given by [17]

$$\omega_{p2} = \frac{g_{m2}}{C_{o1}\left(1 + \frac{C_L}{C_C}\right)} \tag{7}$$

which leads to a compensation capacitor

$$\begin{aligned} C_C &= \frac{g_{m1}}{2g_{m2}}K\left(1 + \sqrt{1 + \frac{4g_{m2}}{Kg_{m1}}\frac{C_L}{C_{o1}}}\right)C_{o1} \\ &\cong \frac{g_{m1}}{2g_{m2}}KC_{o1} + \sqrt{\frac{g_{m1}}{g_{m2}}KC_{o1}C_L}. \end{aligned} \tag{8}$$

Since usually $C_b \leq C_{o1} < C_L$ and $g_{m1} < g_{m2}$, the first term of (8) is negligible and (8) is just lower than (6). Hence the performance obtainable with an ideal current buffer is slightly better than that using an optimized design based on a voltage buffer. A quite ideal current buffer can be achieved with a BiCMOS technology using a common-base rather than a common-gate transistor. However, compensation with a real current buffer (i.e., with finite input resistance) is not as straightforward as other compensation approaches. Indeed, as will be shown in the next section, some proper conditions must be satisfied in order to guarantee that it works correctly.

In this brief a compensation strategy for two-stage opamps is discussed which is based on a real current buffer. Proper design conditions are determined as well as the equations for an optimized design.

II. Proposed Compensation Strategy

Consider the circuit in Fig. 2 which is the small-signal equivalent circuit of the amplifier in Fig. 1(a) with block CB replaced by

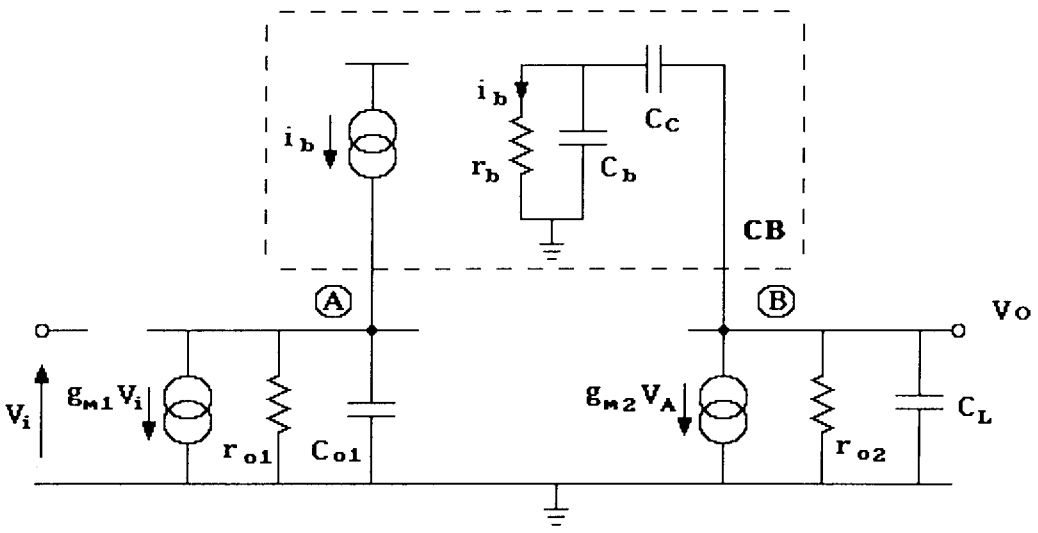

Fig. 2. Small-signal model of the two-stage opamp with current buffer compensation.

Fig. 1(d), and assume, for the sake of simplicity, a current buffer with an ideal frequency response (i.e., without the input capacitance, C_b). From (A1.3) of Appendix I, we get

$$A_\nu(s) \cong \frac{g_{m1}r_{o1}g_{m2}r_{o2}\left(1+\frac{C_C}{g_{mb}}s\right)}{(1+C_Cr_{o1}g_{m2}r_{o2}s)\left[1+\left(\frac{C_{o1}}{g_{m2}}+\frac{C_{o1}C_L}{C_Cg_{m2}}\right)s+\frac{C_{o1}C_L}{g_{m2}g_{mb}}s^2\right]} \tag{9}$$

where $g_{mb} = 1/r_b$ is the input conductance of the current buffer. Equation (9) has a left half-plane zero, and, unless g_{mb} is higher than $4g_{m1}$, has two complex and conjugate poles.[2] The complex poles have a pole frequency ω_o and damping factor ξ given by

$$\omega_o = \sqrt{\frac{g_{m2}g_{mb}}{C_{o1}C_L}} \tag{10a}$$

$$\xi = \frac{1}{2}\sqrt{\frac{g_{mb}}{g_{m2}}\frac{C_{o1}}{C_L}}\left(1+\frac{C_L}{C_C}\right). \tag{10b}$$

For the optimized case in term of bandwidth, g_{mb} is equal to $2g_{m1}$, as will be shown below, ξ is lower than 0.5, and the complex poles give rise to an underdamped behavior. In order to guarantee dominant pole behavior, the real part of the poles (i.e., the term $\xi\omega_o$) must be set greater than $\omega_{\rm GBW}$. Hence, it follows that

$$g_{mb} > \frac{2}{1+\frac{C_C}{C_L}}g_{m1}. \tag{11}$$

Setting the ratio of g_{mb} to g_{m1} equal to β, parameter K is given by

$$K = \tan\left(90^\circ - \tan^{-1}\frac{2\xi\frac{\omega_T}{\omega_o}}{1-\left(\frac{\omega_T}{\omega_o}\right)^2} + \tan^{-1}\frac{\omega_T}{\omega_z}\right) = \tan\left(-\tan^{-1}\left(\frac{C_{o1}(C_L+C_C)g_{m1}}{C_C^2g_{m2}-\frac{1}{\beta}C_{o1}C_Lg_{m1}}\right)+\tan^{-1}\beta\right). \tag{12}$$

[2]The condition to have only real poles is $g_{mb} \geq 4\frac{C_LC_C^2}{C_{o1}(C_L+C_C)^2}g_{m2}$. It gives $g_{mb} > 4g_{m1}$ substituting the lower value of C_C determined in the following [(14)].

Equation (12) can be written as

$$\frac{\beta+K}{K\beta-1}C_C^2 - \frac{g_{m1}}{g_{m2}}C_{o1}C_C - \frac{g_{m1}}{g_{m2}}\frac{1}{\beta}\left(\beta+\frac{\beta+K}{K\beta-1}\right)C_{o1}C_L = 0 \tag{13}$$

and solving for C_C, we get

$$C_C = \frac{g_{m1}}{g_{m2}}\frac{K\beta-1}{\beta+K} \times \left(1+\sqrt{1+4\frac{g_{m2}}{g_{m1}}\frac{\beta+K}{K\beta-1}\left(1+\frac{1}{\beta}\frac{\beta+K}{K\beta-1}\right)\frac{C_L}{C_{o1}}}\right)\frac{C_{o1}}{2} \cong \frac{g_{m1}}{2g_{m2}}\frac{K\beta-1}{\beta+K}C_{o1} + \sqrt{\frac{g_{m1}}{g_{m2}}\left(\frac{K\beta-1}{\beta+K}+\frac{1}{\beta}\right)C_LC_{o1}} \tag{14}$$

Term $(K\beta-1)/(\beta+K)$ is an increasing function of β and K, and tends to the value of K, which is always lower than 4, for $\beta \to \infty$. Since $C_{o1} < C_L$ and $g_{m1} < g_{m2}$ the first term in (14) is negligible, and the optimum value of β is that which minimizes the term in the bracket and meets the constraint imposed by (11). For a phase margin greater than 60°, a rough estimation gives $\beta = 2$.[1]

Setting $\beta = 2$ in (14), the compensation capacitor is lower than that for the case of ideal current buffer (i.e., $\beta = \infty$). Indeed, comparing the two terms of (14), the first term (i.e., the smaller one) is reduced at least by 60%, and the second term, which is reduced by increasing the phase margin, is reduced by 18% and 27% for phase margins of 60° and 70°, respectively. This means at least an 18% increase in $\omega_{\rm GBW}$.

Taking into account the input capacitance of the current buffer, the above considerations are still valid, as shown in Appendix II.

III. Simulation Results

In order to validate the proposed compensation strategy, the two-stage opamp in Fig. 1(a) was designed using the model parameter of a 2 μm CMOS process. The design parameters in Table I were used, giving the electrical parameters shown in Table II. A comparison between the frequency response using the nulling resistor compensation strategy [block CB in Fig. 1(b)], the optimized one with voltage

[1]The minimum of the term in the bracket is given by $\beta = \frac{1+\sqrt{1+K^2}}{K}$, which results in $1.28 \leq \beta \leq 1.73$ for $1.73 \leq K \leq 4$, but the C_C values found do not verify (11).

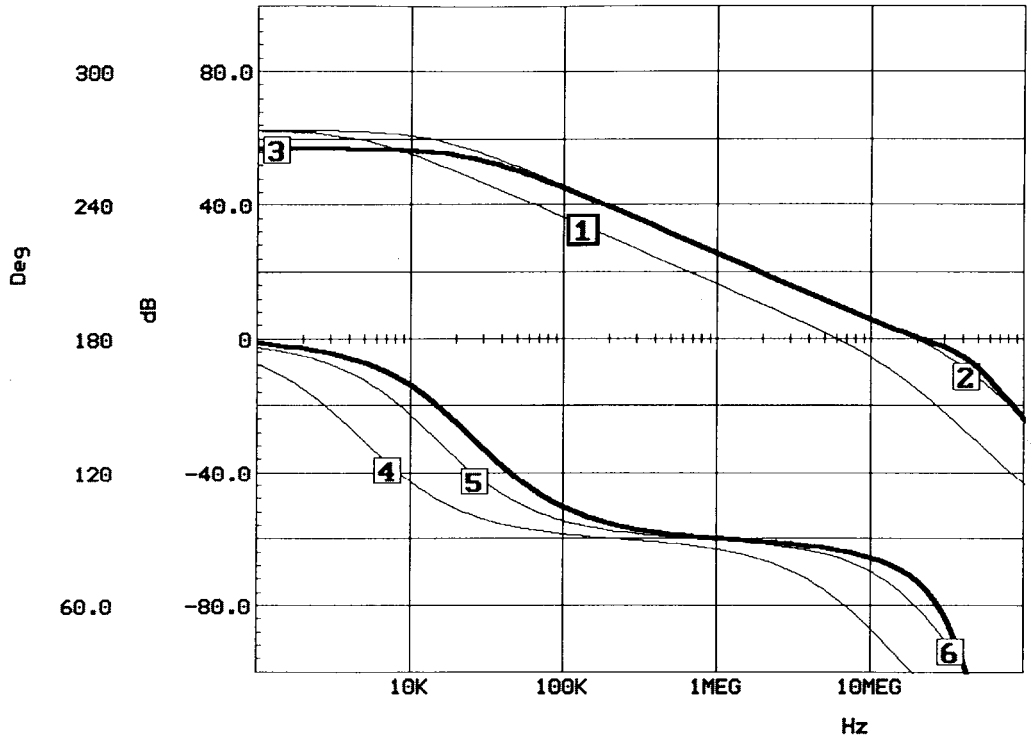

Fig. 3. Frequency response of the two-stage opamp: (1) and (4) with nulling resistor; (2) and (5) with the optimized voltage buffer; (3) and (6) with the optimized current buffer.

TABLE I
GEOMETRICAL DIMENSIONS AND BIAS

M1a,M1b	16/2
M3,M4	32/4
M2	64/2
M5	4/2
M6	8/2
M7	32/2
I_{ref}	10 μA
V_{DD}	5 V

TABLE II
ELECTRICAL PARAMETERS

g_{m1}	110 μA/V
g_{m2}	425 μA/V
C_{o1}	0.115 pF
C_L	5 pF
K	2

buffer [block CB in Fig. 1(c)], and the proposed compensation with current buffer [block CB in Fig. 1(d)] is shown in Fig. 3.

According to the traditional nulling resistor approach, the values of C_C and f_T are 2.5 pF and 5 MHz, respectively. In the optimized compensation with voltage buffer the values of C_C and f_T are 0.8 pF and 20 MHz, respectively, while for that with current buffer the values of C_C and f_T are 0.75 pF and 28 MHz, respectively. The power dissipation for the nulling resistor, the voltage buffer and the current buffer are 590, 630, and 790 μW, respectively. Moreover, due to the lower resistance on node A, the compensation with current buffer has a gain reduced of about 6 dB. It is apparent the compensation with current buffer has the best gain-bandwidth product. The gain-bandwidth product resulting from simulation differs by only 33% from that calculated by (2) with (14).

The implementation of the compensation with current buffer in Fig. 1(d) was that first proposed by Ahuja [13]. However, a better and commonly used implementation is achieved by embodying the current buffer in the differential stage, in series with the source-coupled pair. This reduces the complexity of the circuit, improves the low-frequency PSRR and the amplifier gain, and does not need more power dissipation than the approach with nulling resistor.

IV. FINAL REMARKS AND CONCLUSION

The simulation in Fig. 3 compares different compensation strategies applied to the amplifier in Fig. 1(a) with fixed values for g_{m1} and g_{m2}. However, a better way to compare different types of optimized compensations in terms of gain-bandwidth product is that of assuming the overall transconductance to be equal, which also accounts also for g_{mb}. Under this condition, the compensation with voltage buffer provides an ω_{GBW} higher than that with nulling resistor, as previously described [16]. For voltage buffer (VB) and current buffer (CB) compensations, assuming the overall transconductance to be equal means

$$g_{m1(\mathrm{VB})} + g_{m2(\mathrm{VB})} + g_{mb(\mathrm{VB})} = g_{m1(\mathrm{CB})} + g_{m2(\mathrm{CB})} + g_{mb(\mathrm{CB})}. \tag{15}$$

Considering the same g_{m1} for both voltage and current buffer compensations and remembering that the current buffer transconductance (i.e., input conductance g_{mb}) for an optimized design is equal to $2g_{m1}$, and that $g_{mb(\mathrm{VB})}$ is usually much lower than $g_{m2(\mathrm{VB})}$ [16], (15) becomes

$$g_{m2(\mathrm{VB})} = g_{m2(\mathrm{CB})} + 2g_{m1}. \tag{16}$$

Now, according to (16) and assuming phase margins of 60° and 70°, the optimized compensation with voltage buffer provides an ω_{GBW} which is 40% and 25% higher than that obtained with current buffer.

On the other hand, the compensation based on current buffer avoids the drawback of reducing the amplifier output swing due to the voltage buffer. Moreover, the optimized compensations with voltage buffer and that with nulling resistor are both affected by a pole-zero doublet which arises from process tolerances, and are responsible for a low high-frequency PSRR.

Appendix I

The transfer function of the circuit in Fig. 2 is given by

$$A_\nu(s) \cong \frac{g_{m1}r_{o1}g_{m2}r_{o2}(1+r_b(C_C+C_b)s)}{1+a_1s+a_2s^2+a_3s^3} \quad \text{(A1.1a)}$$

where

$$a_1 = (C_C+C_b)r_b + C_{o1}r_{o1} + (C_L+C_C)r_{a2} + C_Cr_{o1}g_{m2}r_{o2} \quad \text{(A1.1b)}$$

$$a_2 = C_{o1}C_Cr_{o1}r_b + [C_CC_b + C_b(C_L+C_C)]r_{a2}r_b + [C_{o1}(C_L+C_C) + C_bC_Cg_{m2}r_b]r_{o1}r_{o2} \quad \text{(A1.1c)}$$

$$a_3 = C_{o1}(C_LC_C + C_bC_L + C_bC_C)r_{o1}r_{02}r_b \quad \text{(A1.1d)}$$

since r_b is much lower than r_{01} and r_{02}, coefficient a_1 and a_2 can be rewritten

$$a_1 \cong C_Cr_{o1}g_{m2}r_{o2} \quad \text{(A1.2a)}$$

$$a_2 \cong [C_{o1}(C_L+C_C) + C_bC_Cg_{m2}r_b]r_{01}r_{o2} \quad \text{(A1.2b)}$$

Assuming a pole dominant behavior, with the dominant pole given by $1/(C_Cr_{o1}g_{m2}r_{o2})$ (i.e., the inverse of the coefficient of term s in the denominator of (A1.1) [23]), and representing with g_{mb} the input conductance of the current buffer, (A1.1) can be approximated as (A1.3) shown at the bottom of the page.

Appendix II

Introducing the input capacitance C_b, and assuming (as is the case) that its contribution to the zero is negligible, from (A1.2) in Appendix I, we get

$$K = \tan\left(90^\circ - \tan^{-1}\left[\frac{\left(\frac{C_{o1}}{g_{m2}} + \frac{C_b}{g_{mb}} + \frac{C_{o1}C_L}{g_{m2}C_C}\right)\frac{g_{m1}}{C_C}}{1-\left(\frac{C_{o1}(C_L+C_b)}{g_{m2}g_{mb}} + \frac{C_{o1}C_LC_b}{g_{m2}g_{mb}C_C}\right)\left(\frac{g_{m1}}{C_C}\right)^2}\right] + \tan^{-1}\frac{g_{m1}}{g_{mb}}\right)$$

$$\cong \tan\left(90^\circ - \tan^{-1}\left[\frac{C_CC_{o1}g_{mb} + C_CC_bg_{m2} + C_LC_{o1}g_{mb}}{C_C^2\beta g_{m2} - C_{o1}(C_L+C_b)g_{m1}}\right] + \tan^{-1}\frac{1}{\beta}\right) \quad \text{(A2.1)}$$

Equation (A2.1) gives

$$\frac{\beta+K}{K\beta-1}C_C^2 - \left(\frac{g_{m1}}{g_{m2}}C_{o1} + \frac{C_b}{\beta}\right)C_C - \frac{g_{m1}}{g_{m2}}\frac{1}{\beta}\left[\left(\beta + \frac{\beta+K}{K\beta-1}\right)C_L + \frac{\beta+K}{K\beta-1}C_b\right]C_{o1} = 0 \quad \text{(A2.2)}$$

and condition (11) now becomes

$$g_{mb} > 2\left(\frac{C_L}{C_L+C_C}\right)g_{m1} + \left(2 - \frac{C_C^2}{C_{o1}(C_L+C_C)}\frac{g_{m2}}{g_{m1}}\right)\frac{C_b}{C_C}g_{m1} \quad \text{(A2.3)}$$

For typical values, the last term of disequation (A2.3) is much lower than 1, and hence $\beta = 2$ will satisfy it. Solving (A2.2) for C_C we get

$$C_C = \frac{1}{2}\frac{K\beta-1}{\beta+K} \times \left(1 + \sqrt{1 + 4\frac{g_{m2}}{g_{m1}}\frac{\beta+K}{K\beta-1}\frac{1+\frac{1}{\beta}\frac{\beta+K}{K\beta-1} + \frac{C_b}{C_L}}{\left(1+\frac{g_{m2}}{g_{m1}}\frac{1}{\beta}\frac{C_b}{C_{o1}}\right)^2}\frac{C_L}{C_{o1}}}\right) \times \left(\frac{g_{m1}}{g_{m2}}C_{o1} + \frac{1}{\beta}C_b\right)$$

$$\cong \frac{1}{2}\frac{K\beta-1}{\beta+K}\left(\frac{g_{m1}}{g_{m2}}C_{o1} + \frac{1}{\beta}C_b\right) + \sqrt{\frac{g_{m1}}{g_{m2}}\left(\frac{K\beta-1}{\beta+K}\left(1+\frac{C_b}{C_L}\right) + \frac{1}{\beta}\right)C_LC_{o1}} \quad \text{(A2.4)}$$

Then, apart from an appreciable increase in the first term, which is the small one, the input capacitance of the current buffer does not greatly affect the value of C_C given by (14).

References

[1] J. Solomon, "The monolithic op amp: A tutorial study," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 314–332, Dec. 1974.

[2] H. Yang and D. Allstot, "Considerations for fast settling operational amplifiers," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 326–334, Mar. 1990.

[3] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. New York: Wiley, 1993.

[4] K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, 1994.

[5] Y. Tsividis, "Design consideration in single-channel MOS analog integrated circuits—A tutorial," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 383–391, June 1978.

[6] P. Gray and R. Meyer, "MOS operational amplifier design a tutorial overview," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 969–982, Dec. 1982.

[7] D. Allstot and W. Black, "Technological design consideration for monolithic MOS switched-capacitor filtering systems," in *Proc. IEEE*, Aug. 1983, vol. 17, pp. 967–986.

[8] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signals Processing*. New York: Wiley, 1986.

[9] P. Allen and D. Holberg, *CMOS Analog Circuit Design*. New York: Holt Rinehart and Winston, 1987.

$$A_\nu(s) \cong \frac{g_{m1}r_{o1}g_{m2}r_{o2}\left(1+\frac{C_C+C_b}{g_{mb}}s\right)}{(1+C_Cr_{o1}g_{m2}r_{o2}s)\left[1+\left(\frac{C_{o1}}{g_{m2}} + \frac{C_b}{g_{mb}} + \frac{C_{o1}C_L}{C_Cg_{m2}}\right)s + \frac{C_{o1}(C_CC_L+C_bC_L+C_bC_C)}{C_Cg_{m2}g_{mb}}s^2\right]}. \quad \text{(A1.3)}$$

[10] Y. Tsividis and P. Gray, "An integrated NMOS operational amplifier with internal compensation," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 748–754, Dec. 1976.
[11] G. Smaradoiu, D. Hodges, P. Gray, and G. Landsburg, "CMOS pulse-code-modulation voice codec," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 504–510, Aug. 1978.
[12] D. Senderowicz, P. Gray, and D. Hodges, "High-performance NMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 760–766, Dec. 1978.
[13] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 629–633, Dec. 1983.
[14] C. Makris and C. Toumazou, "Current-mode active compensation techniques," *Electron. Lett.*, vol. 26, no. 21, pp. 1792–1794, Oct. 11, 1990.
[15] W. Black Jr., D. Allstot, and R. Reed, "A high performance low power CMOS channel filter," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 929–938, Dec. 1980.
[16] G. Palmisano and G. Palumbo, "An optimized compensation strategy for two-stage CMOS OP AMPS," *IEEE Trans. Circuits Syst. I*, vol. 42, pp. 178–182, Mar. 1995.
[17] R. Castello, "CMOS buffer amplifier," in *Analog Circuit Design*, J. Huijsing, R. van der Plassche, and W. Sansen, Eds. Boston, MA: Kluwer Academic, 1993, pp. 113–138.
[18] R. Reay and G. Kovacs, "An unconditionally stable two-stage CMOS amplifier," *IEEE J. Solid-State Circuits*, vol. 30, pp. 591–594, May 1995.
[19] D. Ribner and M. Copeland, "Design techniques for cascoded CMOS Op Amps with improved PSRR and common-mode input range," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 919–925, Dec. 1984.
[20] M. Steyaert and W. Sansen, "Power supply rejection ratio in operational transconductance amplifier," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1077–1084, Sept. 1990.
[21] E. Sackinger, J. Goette, and W. Guggenbuhl, "A general relationship between amplifier parameters, and its application to PSRR improvement," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1173–1181, Oct. 1981.
[22] Y. Kamath, R. Meyer, and P. Gray, "Relationship between frequency response and settling time of operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 347–352, Dec. 1974.
[23] J. Millman and A. Grabel, *Microelectronics*, 2nd ed. New York: McGraw-Hill, 1987.

Design of Demodulator for the Chaotic Modulation Communication System

Henry Leung and Jennifer Lam

***Abstract*—Chaotic modulation has recently been proposed for spread spectrum (SS) and code division multiple access (CDMA) communication. It embeds the signal of transmission in the bifurcating parameter of a chaotic dynamical system, and uses the wide-band output of the chaotic system as the transmitted signal. In this brief, we consider the demodulation of this communication scheme using an adaptive filter. Not only can an adaptive filter reduce the effect of channel noise, but it also estimates the bifurcating parameter (i.e., the signal of transmission) sequentially which is required in a communication system. Three kinds of adaptive filters: the least mean square (LMS) algorithm, the recursive least square (RLS) technique and the Kalman filter, are considered here. It is found that the demodulators based on these adaptive filters outperform the standard inversion approach used in the literature.**

***Index Terms*—Adaptive filters, chaotic modulation, extended Kalman filter, least mean square algorithm, recursive least square algorithm.**

I. Introduction

Spread spectrum (SS) and code division multiple access (CDMA) is a means of transmission in which the signal occupies a bandwidth in excess of the minimum necessary to send the information. Recently there is considerable interest in the use of chaos in an SS/CDMA system [1]–[3]. One interesting approach is chaotic modulation which employs a chaotic dynamical system to modulate the signal of transmission to achieve the goal of SS/CDMA communication [4]–[7]. More precisely, the signal of transmission is stored in a bifurcating parameter of the chaotic dynamical system. By keeping this bifurcating parameter in the chaotic regime, the output wide-band signal of the dynamical system may be used as the transmitted signal. This chaotic modulation communication scheme is not only theoretically interesting, but it also offers many advantages to the conventional SS/CDMA system. For example, the chaotic modulation technique does not require any code synchronization which is essential in a conventional SS/CDMA system. However, the chaotic modulation system needs a receiver/demodulator which can estimate the parameter of the chaotic system accurately to decode the signal of transmission. The process of estimating the bifurcating parameter of a chaotic system in noise is therefore a key factor for success of this communication scheme.

The demodulator proposed in [4]–[7] uses a simple inversion for the logistic map transmitter. This demodulation technique works well when the environment is completely noise-free. When channel noise exists, the effectiveness of this inversion approach is questionable. Although some techniques have recently been developed to estimate the parameters of a chaotic signal in noise [8], [9], these techniques are developed for off-line processing (i.e., batch method) and usually require a very long data sequence for a reliable noise reduction. In addition, these methods are designed for a constant parameter chaotic system and do not possess the ability to track a time-varying

Manuscript received January 11, 1996; revised June 27, 1996. This paper was recommended by Associate Editor T. Endo.

H. Leung is with the Surface Radar Section, Defence Research Establishment Ottawa, Ottawa, Ont., Canada K1A 0Z4.

J. Lam is with the Department of Physics, University of Ottawa, Ottawa, Ont., Canada K1N 6N5.

Publisher Item Identifier S 1057-7122(97)02065-5.