

Two Stage Op-Amp: DC Solution (Part 1)

Objectives in this segment of the course are to:

1. Review necessary CMOS technology and device characteristics
2. Understand the internal configuration of a two-stage CMOS op-amp.
3. Perform analysis and determine the DC solution for the two-stage CMOS op-amp

Figure 1 shows a basic two-stage CMOS op-amp configuration. The resistance R provides biasing for the entire operational amplifier. $M1$ and $M2$ form a differential pair and thus the input of the first gain stage of the op amp. The current mirror formed by $M8$ and $M5$ supplies the differential pair with bias current I_{B1} . The input differential pair is actively loaded with the current mirror formed by $M3$ and $M4$. Node 1 forms the output of the first stage of the op amp. The second stage consists of $M6$ which is a common-source amplifier actively loaded with the transistor $M7$. It should be noted that $M7$ does not provide biasing for $M6$, and that $M6$ is biased from the gate side.

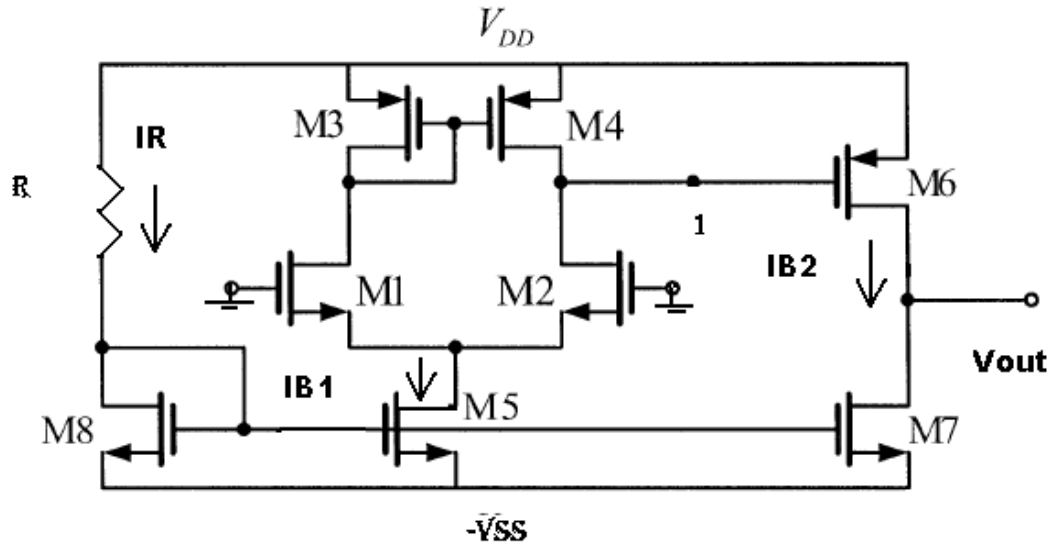


Figure 1: Two-stage CMOS op-amp. The inputs are set to zero to determine the nominal DC bias operating point.

Numerical Example:

Given:

Process parameters:

$$\mu_n C_{ox} = 60 \mu\text{A}/\text{V}^2 \text{ and } \mu_p C_{ox} = 20 \mu\text{A}/\text{V}^2,$$

$$V_{tn} \text{ (The threshold voltage of NMOS devices)} = +1\text{V and}$$

$$V_{tp} \text{ (The threshold voltage of PMOS devices)} = -1\text{V.}$$

$$\text{Supply voltages: } V_{DD} = +5\text{V and } -V_{SS} = -5\text{V}$$

$$\text{Device aspect ratios: } (W/L)_8 = 1, (W/L)_1 = (W/L)_2 = 100, (W/L)_3 = (W/L)_4 = 20.$$

$$\text{Dc bias specifications: } I_R = 1\mu\text{A}, I_{B1} = 10\mu\text{A}, I_{B2} = 100\mu\text{A}$$

DC Solution

The first step in finding the DC solution is to determine the value of the resistance R so that the bias current I_R equals the specified value ($1\mu\text{A}$ in the numerical example):

$$V_{DD} = R \cdot I_R + V_{GS8} - V_{SS}, \quad (1)$$

which yields

$$R = (V_{DD} + V_{SS} - V_{GS8})/I_R \quad (2)$$

While the values of V_{DD} , V_{SS} , and I_R are known, the voltage V_{GS8} is not. In order to solve for V_{GS8} , we observe that the device M8 operates in the active/saturation region since the gate of M8 is shorted to the drain of M8, and therefore the following conditions are met:

1. $V_{GS8} \geq V_{TN}$
2. $V_{TN} \geq V_{GD8}$

Since M8 is in the active/saturation region, we have

$$I_{D8} = I_R = (\mu_n C_{ox}/2)(W/L)_8 (V_{GS8} - V_{TN})^2 \quad (3)$$

which can be solved for V_{GS8} ,

$$V_{GS8} = \sqrt{I_R / K_8} + V_{tn}, \text{ where } K_8 = 1/2 * \mu_n C_{ox} * (W/L)_8. \quad (4)$$

For the values in the numerical example, $V_{GS8} = 1.2 \text{ V}$ The value of V_{GS8} is then substituted into (2) and the value of R is determined to be $8.8 \text{ M}\Omega$.

The value of the gate voltage V_{G8} can be found as:

$$V_{G8} = -V_{SS} + V_{GS8} = -5 + 1.2 = -3.8V \quad (5)$$

Assuming that M5 and M7 are in the active/saturation region, the specifications for the DC currents I_{B1} and I_{B2} , together with the property of the current mirror can be used to find the aspect ratios of M5 and M8:

$$\frac{(W/L)_5}{(W/L)_8} = \frac{I_{B1}}{I_R} = 10 \quad \text{and} \quad \frac{(W/L)_7}{(W/L)_8} = \frac{I_{B2}}{I_R} = 100. \quad (6)$$

The gates of M1 and M2 are grounded to obtain the nominal DC solution, thus $V_{GS1} = V_{GS2}$. Also, $I_{D1} + I_{D2} = I_{B1}$. Since M1 and M2 are identical NMOS devices having the same V_{GS} voltages, assuming that M1 and M2 are in the active/saturation region, the bias current I_{B1} divides equally between M1 and M2,

$$I_{D1} = I_{D2} = 5\mu A. \quad (7)$$

At this point we can check whether the device M5 is in the active/saturation region. The drain voltage of M5 is the source voltage of M1 and M2, i.e., the negative of the gate to source voltages of M1 and M2.

$$V_{D5} = -V_{GS1} = -V_{GS2} = -(V_{t,n} + \sqrt{I_{D1}/K_1}), \quad \text{where } K_1 = 1/2 * \mu_n C_{ox} * (W/L)_1 \quad (8)$$

The drain voltage of M5 is calculated to be $-1.04V$, which is much larger than its gate voltage $-3.8V$. Thus, M5 is indeed in the active/saturation region.

Now continuing with the PMOS devices M3 and M4, M3 is in saturation as its gate and drain terminals are connected together. Thus, the source to gate voltage of M3 can be calculated as

$$V_{SG3} = |V_{tp}| + \sqrt{I_{D3}/K_3} \quad \text{where } K_3 = 1/2 * \mu_p C_{ox} * (W/L)_3 = 200\mu A/V^2 \quad (9)$$

For the numerical example, we get:

$$V_{SG3} = 1.16V \quad (10)$$

The drain voltage of M1 is $V_{D1} = V_{DD} - V_{SG3} = 3.84V$ which shows that M1 is easily in active/saturation region. The calculation of the drain voltage of M4 is done in the next lecture.

Comments:

- The circuit utilizes two power supplies, which are $\pm 5\text{V}$ in the numerical example. The values of $\pm 2.5\text{V}$ or even lower supply voltages are also typical. Single supply voltages ($V_{SS} = 0$) are also in common use, with V_{DD} as low as 2.5 V in battery-powered electronic systems.
- An NMOS transistor operates in the active/saturation region if the gate-to-source voltage is greater than the threshold voltage V_{tn} and if the gate-to-drain voltage is less than the threshold voltage. The active/saturation region of operation is most commonly utilized in analog circuits.
- A PMOS transistor operates in the active/saturation region if the source-to-gate voltage is greater than the absolute value of the threshold voltage $|V_{tp}|$, and if the drain-to-gate voltage is less than the absolute value of the threshold voltage.
- In the active/saturation region, the effects of the drain to source voltage on the current of the device is neglected in the analysis so far. In other words, the effect of channel length modulation is not considered.