29.2 A 5mA 0.6μm CMOS Miller-Compensated LDO Regulator with -27dB Worst-Case Power-Supply Rejection Using 60pF of On-Chip Capacitance

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As dense digital circuitry is packed close to sensitive analog blocks for higher integration, SoC solutions are swamped in switching noise generated by digital circuits, RF blocks, and DC-DC converters. In this harsh environment, linear regulators have to protect noise-sensitive analog blocks like VCOs and ADCs from coupled supply noise that has amplitudes on the order of hundreds of millivolts and frequency components in the range of tens of kilohertz to hundreds of megahertz [1-2]. Along with high power-supply rejection (PSR) performance over a wide frequency range, these regulators need to exhibit low dropout to allow them to operate at the low supply voltages characteristic of state-of-the-art CMOS processes. Moreover, these LDOs need to be stable and reject noise without the aid of bulky external capacitors, using only on-chip capacitors that are constantly constrained in size by valuable silicon real estate [3-5]. Finally, these SoC LDOs are increasingly deployed at the point-of-load and hence need to supply currents in the range of 2 to 20mA [3-5].

Numerous techniques have been used to improve the PSR of linear regulators. The simplest solution is to place an RC filter in line with the power supply to filter out fluctuations before they reach the regulator [6]. However, for an integrated SoC solution, the high power losses and reduction in voltage headroom caused by this resistor would severely limit its size, thereby constraining the filter's effectiveness.

Figure 29.2.1(a) presents a methodology that utilizes an NMOS device to cascode the NMOS pass device of the linear regulator, thereby isolating it from the noisy power supply [3]. To maintain a low dropout voltage the gate of the cascoding NMOS and the supply of the error amplifier have been boosted using a charge pump. The error amplifier cannot be cascoded as conveniently as the pass device since the gate of its cascode would require a boosted voltage of two gate-source drops above the output, leading to higher complexity in the charge pump design. Hence, it uses an RC filter to suppress fluctuations in the power supply and the systematic fluctuations of the charge pump. Establishing a low RC filter pole for an SoC solution leads to critical tradeoffs: the capacitance can be increased with a significant increase in silicon real estate consumption or the resistance can be increased thereby limiting the bandwidth of the error amplifier, which would then need to operate at very low current levels to minimize the resistive drop and power dissipation in the filter.

In [4], a PSR of -40dB over a wide frequency range is achieved using an NMOS device to cascode the PMOS pass device of a Miller-compensated linear regulator, as shown in Fig. 29.2.1(b). Due to relatively high voltage-headroom (3.3V) the gate of the NMOS cascode is biased through the supply using a simple RC filter. The high voltage-headroom also allows the error amplifier, which is powered directly from the supply (versus through a cascode), to use internal cascodes and gain boosting to improve its PSR performance, leading to higher dropout and power consumption. Moreover, the circuit uses 1.2nF of on-chip decoupling capacitance that occupies an area that is prohibitively large for many VLSI SoC systems.

The regulator presented here achieves a high PSR while exhibiting a lower dropout voltage and utilizing much lower on-chip capacitance, which is valuable for modern low-voltage environments with dense packing. Figure 29.2.2 presents the simplified schematic of the proposed system to achieve high PSR performance over wideband frequencies [7]. The NMOS cascode, MNC, shields the entire regulator from fluctuations in the power supply. To maintain a low dropout voltage, the gate of the cascode needs to be biased at a voltage above the supply. This function is performed by the charge pump (CP), which powers a voltage reference, which, in turn, establishes a supply-independent bias for MNC. Since MNC acts like a voltage follower for noise at its gate, it is critical to shield the gate of MNC from supply fluctuations. The RC filter in series with the voltage reference achieves this by shunting supply ripple to ground. Notably, since the filter is placed in a path that does not carry any DC current, the filter pole can be reduced by designing as large a resistor as practically possible without a resulting loss in voltage headroom, efficiency, or bandwidth.

The system was implemented in a 0.6μm CMOS technology (V_{TN} = 0.7V, V_{TP} = -0.9V), measured, and evaluated. The charge pump is a simple voltage doubler [8] – its output is shown in Fig. 29.2.3. The voltage reference, which draws a total current of 30μA, establishes a stable bias of 2.7V for the cascode by forcing a temperature-independent current of 10μA into a diode-connected NMOS transistor and a resistor. The RC filter, which uses a 500KΩ resistor and 15pF capacitor, establishes a filter pole of roughly 20KHz to effectively attenuate supply noise. The core Miller-compensated SoC LDO uses a 3pF compensation capacitor along with a 10pF output capacitor (Fig. 29.2.2) and is capable of sourcing 5mA of load current. The error amplifier of the LDO consumes 40μA of quiescent current for meeting the transient specifications (and if the same RC filter were inserted in series with it for ripple rejection, the resistive drop across the filter would be 20V). The entire system utilizes 60pF of on-chip capacitance making it extremely compact.

The measured worst case PSRs of the Miller-compensated LDO, as shown in Fig. 29.2.4, are 3dB and -27dB without and with the cascode strategy, respectively. It is seen that the PSR of the voltage reference is roughly -20dB and starts rolling off after 10MHz; the RC filter in series, however, ensures that the roll off takes place at a much lower frequency of 20KHz. When the supply for MNC and CP is decoupled and noise is introduced only in the latter (path 'a' in Fig. 29.2.2), the system rejects noise through the combined PSR of the voltage reference and core regulator. When noise is introduced only at the drain of MNC (path 'b' in Fig. 29.2.2), which is in saturation, its high drain-resistance shields the Miller-compensated core regulator, ultimately leading to a 30dB improvement in the worst case. The cascode strategy impacts the transient response of the regulator and degrades the accuracy by approximately 171mV for a 5mA load step as shown in Fig. 29.2.5. The minimum voltage headroom required by the system is given by

$$V_{DD-\min} = \max\left\{V_{TP} + 4V_{DS-sat}, V_{OUT} + 2V_{DS-sat}\right\}, \tag{1}$$

which, given a V_{TP} of 0.9V for this process, is approximately 1.8V. The die micrograph is shown in Fig. 29.2.6.

A 5mA SoC LDO regulator utilizing 60pF of on-chip capacitance and having a worst-case PSR performance of -27dB over 50MHz has been designed. It utilizes a simple NMOS cascode, a charge pump, a voltage reference, and an RC filter to shield the entire regulator from power supply fluctuations. In conclusion, an integrated LDO with high PSR over a large bandwidth for state-of-the-art SoC environments has been presented.

References:

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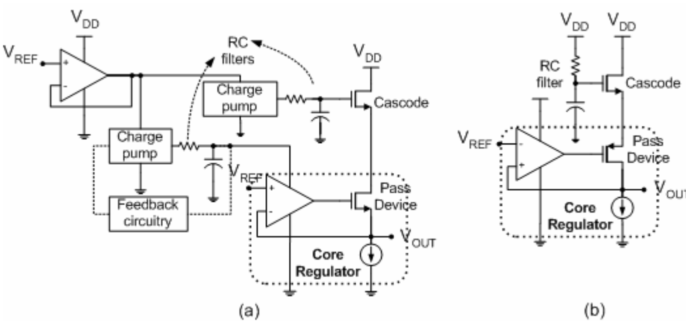

Figure 29.2.1: Previously implemented techniques to achieve high PSR.

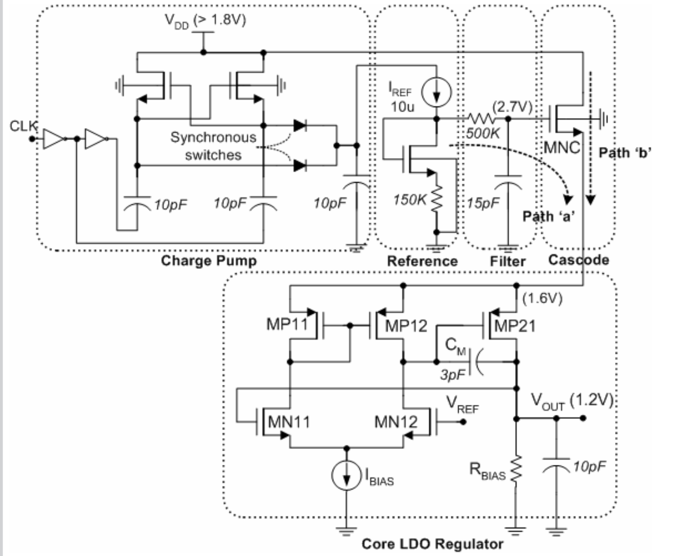

Figure 29.2.2: Schematic of technique to enhance PSR over a wide range of frequency.

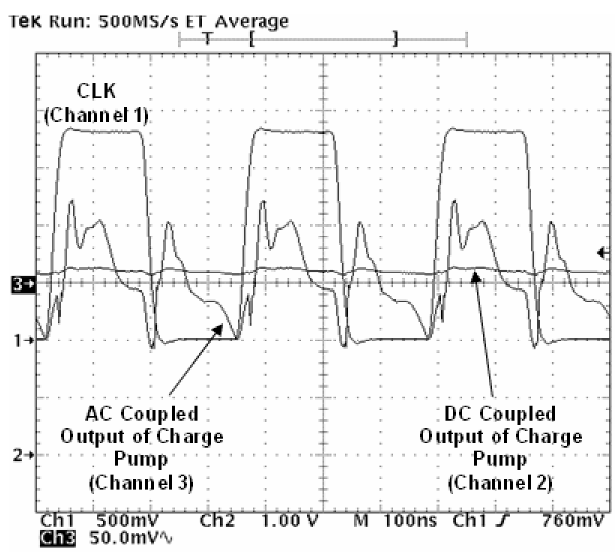

Figure 29.2.3: DC-and AC-coupled output of charge pump.

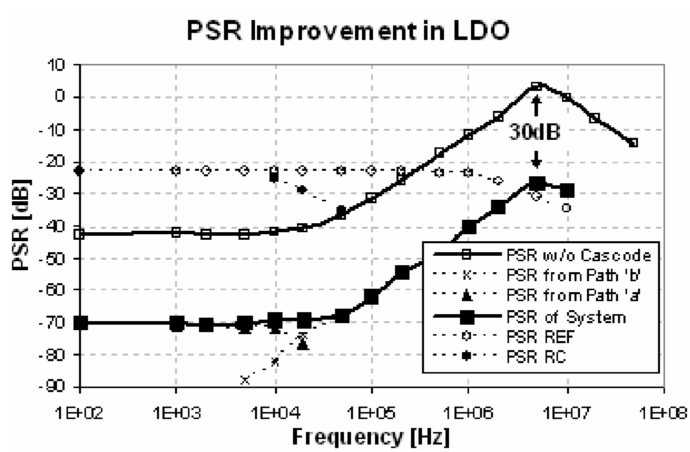

Figure 29.2.4: Improvement in PSR of Miller-compensated LDO.

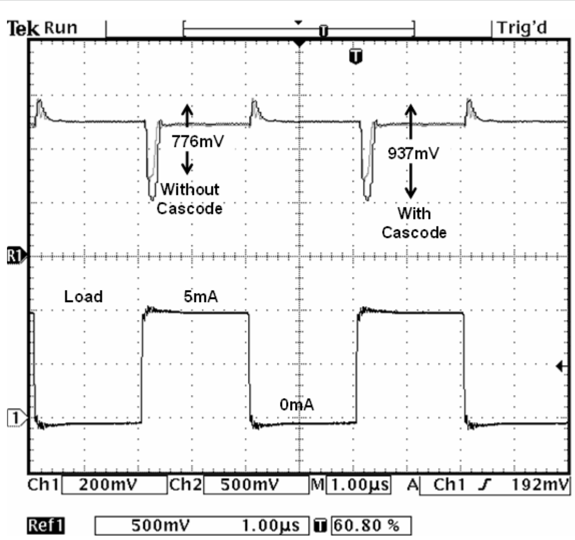

Figure 29.2.5: Impact of cascode strategy on transient response.

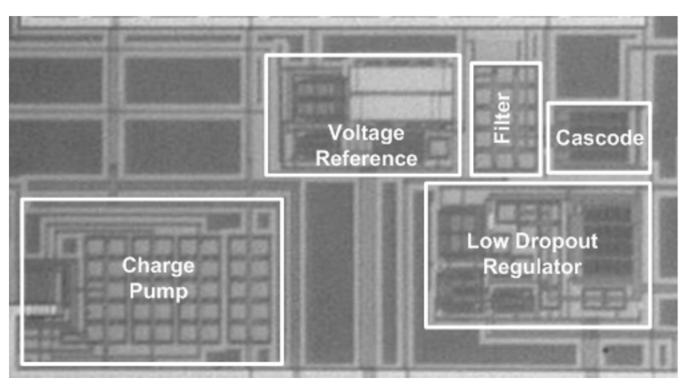

Figure 29.2.6: Die micrograph.

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