

A FOLDED-CASCODE DIFFERENTIAL AMPLIFIER

6.1 Objectives

In this lab, you will examine the voltage transfer characteristics, the output-voltage swing, and the dynamical properties of another simple MOS differential amplifier comprising an n MOS differential pair, a simple current mirror, and two pairs of p MOS transistors in a circuit arrangement called a *folded cascode*. The amplifier that you will construct and characterize is conceptually very similar to those that you investigated in Lab 4 and in Lab 5. This type of amplifier is called a *folded-cascode* differential amplifier.

6.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Unless otherwise stated, you should assume that like transistors are matched and that the Early effect is negligible. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit that you will be testing and what you will be doing in the lab.

1. Consider the differential amplifier shown in Fig. 6.1a comprising an n MOS differential pair, four p MOS transistors, and a simple n MOS current mirror. Such a circuit is called a *folded-cascode* differential amplifier. Transistors M_5 and M_6 act as cascode transistors, pinning the drains of transistors M_1 and M_2 . Transistors M_3 and M_4 act as current sources, providing a pivot point for *folding* over the differential-pair output currents, whence the name of the circuit. Which input voltage is the noninverting input? Which is the inverting input? Explain your reasoning briefly.
2. If the output voltage were fixed by a voltage source somewhere in the middle of the rails, what would be the output current in terms of I_1 and I_2 if the Early effect were negligible?
3. Do we have to make the bias current supplied by transistors M_3 and M_4 equal to I_b ? If so, explain why. If not, what constraints exist on this current with respect to I_b ?
4. Suppose that we would like to arrange for $I_3 = I_4 = I_b$. Consider the bias circuit, shown in Fig. 6.1b, which generates the required n MOS and p MOS bias voltages from

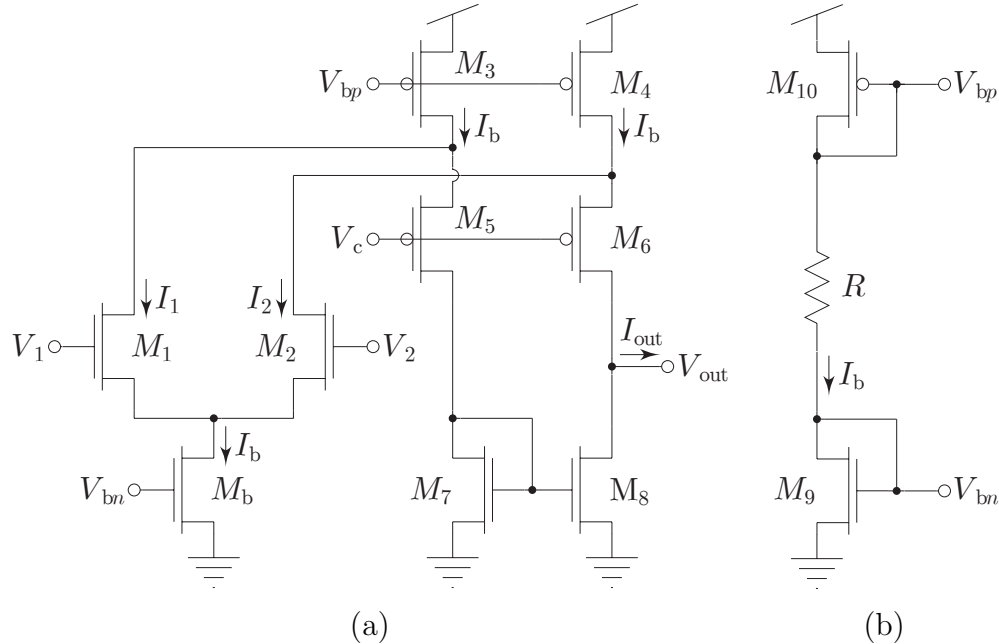


Figure 6.1: (a) A simple MOS folded-cascode differential amplifier. (b) A simple bias circuit for generating V_{bn} and V_{bp} .

the same current, I_b , whose value is determined primarily by V_{DD} and the value of R . If we want to make I_b on the order of tens of microamps (i.e., somewhat larger than the threshold currents of the n MOS and p MOS transistors), what value of R do we need to use if $V_{DD} = 5\text{ V}$?

6.3 Experiments

You will be doing three experiments in this lab. In the first experiment, you will examine the VTCs of the folded-cascode differential amplifier and its output-voltage range. In the second experiment, you will measure the incremental output resistance of the amplifier and its incremental transconductance gain. You will also compute find the differential-mode voltage gain of the circuit by node fixing. In the third experiment, you will investigate the time response of your amplifier configured as a unity-gain follower to both small- and large-amplitude steps.

6.3.1 Experiment 1: Voltage Transfer Characteristics

In Capture CIS, construct a folded-cascode differential amplifier, as shown in Fig. 6.1a, with an n MOS differential pair, a simple n MOS current mirror, and two p MOS folded cascodes. Set the bias voltages, V_{bn} and V_{bp} , with the bias circuit shown in Fig. 6.1b. You should pick a value for R so that your bias current, I_b , is on the order of microamps, which is on the

high end of moderate inversion or slightly into strong inversion. Set both the cascode bias voltage, V_c , and the inverting input of the amplifier somewhere in the middle of the rails.

For at least three different values of V_c , which range from ground to at most slightly below the value of V_{bp} , sweep the noninverting input around the inverting one in fine increments while measuring V_{out} . In your report, include a single plot showing all of these VTCs. You will probably notice a kink in the high-gain region of each VTC. How does the position of this kink change with the value of V_c ?

Set the value of V_c so that the kink disappears from the high-gain region. As you did in Lab 4 and in Lab 5, sweep the noninverting input from one rail to the other, measuring V_{out} for five different values of the voltage on the inverting input. In your report, include a single plot showing all of these VTCs. How does the behavior of this amplifier compare to those of the amplifiers that you investigated in Lab 4 and in Lab 5?

6.3.2 Experiment 2: Transconductance, Output Resistance, and Gain

Set the inverting input to the voltage that you used initially in Experiment 1, and set the differential-mode input voltage to zero. For each of the values of V_c that you used in Experiment 1, measure the current flowing into the output of the amplifier as you sweep V_{out} from one rail to the other. In your report, turn in a single plot showing all of these output current-voltage characteristics. You will probably also notice a kink in these output current-voltage characteristics. How does the location of these kinks correlate to those that you observed in the VTCs? Fit a straight line to the shallowest part of the output current-voltage characteristic and extract a value of the incremental output resistance of the circuit. Show the best-fit line on the plot with all of the output current-voltage characteristics.

Next, set the value of V_c so that the kink disappears and fix the output voltage somewhere in the middle of the rails and measure the current flowing out of the amplifier as you sweep V_{dm} around zero. You should sweep V_{dm} over a sufficiently large range that I_{out} saturates both for positive and for negative values of V_{dm} . Fit a straight line to the curve around where $V_{dm} = 0$ and extract a value of the incremental transconductance gain of the circuit with the output voltage fixed from the slope of the best-fit line. Also, record the limiting values of I_{out} in both the positive and the negative directions. In your report, include a plot showing I_{out} versus V_{dm} along with the best-fit line.

From your incremental output resistance and your incremental transconductance gain, compute the differential-mode voltage gain of your circuit. How does this value of for the differential-mode gain compare to that which you obtained for the amplifier of Lab 4 and of Lab 5?

6.3.3 Experiment 3: Unity-Gain Follower Step Response

Configure your amplifier as a unity-gain follower by connecting the output to the inverting input, as you did in Lab 5. Now, load the output of your follower-connected amplifier with a 10 pF by connecting it between the output of your amplifier and ground.

Apply a small-amplitude square wave to the input of your circuit and observe both the input and output waveforms. The peak-to-peak amplitude of your square wave should be

smaller than the range of differential-mode voltages over which the I_{out} versus V_{dm} curve that you measured in Experiment 2 was approximately linear. The DC offset should be sufficiently large that the bias transistor of the differential pair always remains in saturation. Adjust the frequency of the square wave and the transient simulation time so that you can simultaneously see V_{out} settle into its final value after both an up-going and a down-going step. Is the response symmetrical? Does the amplifier exhibit approximately linear behavior? Extract a time constant both for the up-going and for the down-going output transitions. How do these compare with that which you compute from the value of the load capacitance and the differential-mode transconductance gain that you found in Experiment 2? In your report, include a single plot showing both scope traces along with the extracted time constants.

Next, increase the amplitude of your square wave so that it is a couple of volts. Again, the DC offset should be sufficiently large that the bias transistor of the differential pair always remains in saturation. Adjust the frequency of the square wave and the transient simulation time so that you can simultaneously see V_{out} settle into its final value after both an up-going and a down-going step. Is the response symmetrical? You will probably notice that the output of the amplifier follows a linear trajectory in time over most of its response to the large input step. This behavior is called *slewing*, and the constant rate of change of the output voltage with respect to time is called the *slew rate* of the amplifier. Extract a slew rate for both for the up-going and for the down-going output transitions. How do these compare with those which you compute from the measured values of the load capacitance and the limiting values of the output current? In your report, include a single plot showing both scope traces along with the extracted slew rates.

6.4 Postlab

In Experiments 1 and 2, you probably noticed kinks in your amplifier's VTCs and in its output current-voltage characteristics. Provide a concise explanation of the origin of this behavior and how it depends on the value of the cascode bias voltage, V_c . Also, explain how we should pick the value of V_c in order to obtain a kinkless VTC.