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PAPER Special Section on Analog Circuit Techniques and Related Topics

CMOS Zero-Temperature-Coefficient Point Voltage Reference with Variable-Output-Voltage Level

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SUMMARY A CMOS voltage reference circuit based on a voltage at the zero-temperature-coefficient point of drain current is proposed. The output voltage of the proposed circuit is variable by a substrate bias. The proposed circuit is simulated with a standard 0.8-μm CMOS technology. The output voltage keeps 800 mV, and its fractional temperature coefficient is 9.94 ppm/°C over the temperature range from −100°C to 150°C at a zero-bias. The PSRR of the output voltage is −42.55 dB at 100 Hz. The minimum power-supply voltage is 2.1 V. The output voltage can be shifted down to 670 mV while maintaining its temperature-insensitivity.

key words: *voltage reference, zero-temperature-coefficient point, variable-reference-voltage level, substrate bias, CMOS*

1. Introduction

A voltage reference circuit is an important analog building block. The output voltage of the voltage reference circuit requires satisfying three conditions of "independence," that is, temperature-independence, supply-independence and process-independence.

A bandgap voltage reference is the most popular voltage reference circuit [1]–[3]. By using that the bandgap voltage of silicon shows quite little dependence on temperature, the temperature-independent reference voltage can be obtained. The conventional bandgap voltage reference circuit has been implemented with bipolar process technology. Then, many alternative versions of the bandgap voltage reference circuit have been proposed for the coming of a CMOS era.

One of the representative versions of the voltage reference uses the difference of threshold voltages between enhancement- and depletion-mode MOS transistors [4]. The other versions are based on the characteristic of a MOSFET operating in weak inversion [5]–[7]. On the other hand, another way for obtaining the bandgap voltage is to use multiple parasitic bipolar transistors that can be fabricated in a CMOS technology, such as substrate bipolar transistors or lateral bipolar transistors [8]–[10]. The bandgap voltage of silicon keeps the magnitude of 1.205 V. In recent years, the voltage reference with sub-1 V output is desired for low-voltage or low-power applications.

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This paper proposes the voltage reference circuit based on the voltage at the zero-temperature-coefficient point of drain current (ZTCP). The output voltage of the proposed voltage reference can be controlled by applying a substrate bias voltage to compensate the dependence of the output voltage on the process and a process parameter deviation. By using this controllability, the output voltage can also be shifted to various levels while maintaining the temperature-insensitivity. In fact, however, the proposed circuit uses a polysilicon resistor, and its temperature dependence causes a drift with the temperature for the output voltage. A compensation technique for the temperature dependence of the resistor using "thermal term product cancellation" is proposed. The proposed circuit can be implemented with the fully-CMOS technology. The operation of the proposed circuit is verified by SPICE simulation, and the corresponding performances are discussed.

2. Zero-Temperature-Coefficient Point

It has been experimentally known that the temperature coefficient of the drain current of the MOSFET shows almost zero at a specific gate-source voltage. The principle of the zero-temperature-coefficient point has been theoretically analyzed in [11].

When the MOSFET operates in a saturation region, according to the gradual-channel model, the drain current is expressed as

$$I_D = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2 , \tag{1}$$

where μ is the mobility, C_{ox} the gate oxide capacitance, W and L are the channel width and length respectively, and V_T is the threshold voltage. In this equation, the mobility and the threshold voltage are dependent on the temperature. Their temperature dependence is modeled as

$$\mu = KT^{-\frac{3}{2}}, \tag{2}$$

$$V_T = V_T(T_0) - \alpha_T \cdot (T - T_0), \tag{3}$$

respectively, where K is the constant of proportion, T the absolute temperature, T_0 the normal temperature, e.g., T_0 = 300 K, and α_T the temperature coefficient of the threshold voltage [12]. Substitution of Eqs.(2) and (3) for Eq.(1) finally yields the equation which express the gate-source voltage at the ZTCP (ZTCP voltage). If the ZTCP voltage is designated as V_{ZTCP}, it is expressed as

$$V_{\mathrm{ZTCP}} = V_T(T_0) + \frac{1}{3}\alpha_T T + \alpha_T T_0. \quad (4)$$

Although V_{ZTCP} is a function of the absolute temperature T, it can be regarded as almost constant because T is multiplied by the coefficient of $(1/3\alpha_T)$.

Consideration of the body effect for Eq.(4) yields

$$V_{\mathrm{ZTCP}} = V_{T0} + \gamma\left(\sqrt{2\phi_{F0} + V_{SB}} - \sqrt{2\phi_{F0}}\right) + \frac{1}{3}\alpha_T T + \alpha_T T_0, \quad (5)$$

where V_{T0} is the threshold voltage at $V_{SB} = 0$ and $T = T_0$, γ the body-effect coefficient, and ϕ_{F0} is Fermi potential at $T = T_0$. It is understood from Eq.(5) that the application of a backgate bias voltage to the MOSFET makes the ZTCP voltage controllable.

3. CMOS Zero-Temperature-Coefficient Point Voltage Reference

3.1 Basic Principle

When the MOSFET operates in the saturation region, introducing the transconductance parameter β into Eq.(1), the drain current is a function of the gate-source voltage, and is rewritten as

$$I_D = f(V_{GS}) = \frac{\beta}{2}(V_{GS} - V_T)^2. \quad (6)$$

Meanwhile, the gate-source voltage is the inverse function of f, and expressed as

$$V_{GS} = f^{-1}(I_D) = \sqrt{\frac{2I_D}{\beta}} + V_T. \quad (7)$$

If the drain current at the ZTCP (ZTCP current) is designated as I_{ZTCP}, from Eqs.(6) and (7), the ZTCP current and voltage are expressed as

$$I_{\mathrm{ZTCP}} = f(V_{\mathrm{ZTCP}}), \quad (8)$$
$$V_{\mathrm{ZTCP}} = f^{-1}(I_{\mathrm{ZTCP}}), \quad (9)$$

respectively, where I_{ZTCP} and V_{ZTCP} are regarded as constant with the temperature. From Eq.(9), if the ZTCP current flows into the MOSFET, the ZTCP voltage, which is almost independent of the temperature, can be obtained.

The use of a bootstrap bias technique allows the substitution of Eq.(8) for (9), and it yields

$$V_{\mathrm{ZTCP}} = f^{-1}(f(V_{\mathrm{ZTCP}})) = V_{\mathrm{ZTCP}}, \quad (10)$$

that is, the ZTCP voltage is generated by itself [13]. Therefore, a bias voltage independent of the temperature and the power-supply can be obtained. From Eq.(4), however, the ZTCP voltage is directly dependent on the threshold voltage. This means that the ZTCP voltage is dependent on the process, and susceptible to the deviation of the threshold voltage.

The substrate bias is one of the useful techniques for high-performance circuits [14]. By applying the substrate bias voltage, the dependence of the ZTCP voltage on the process and the deviation of the threshold voltage can be compensated. From Eq.(5), the ZTCP voltage is variable by applying the substrate bias voltage to the MOSFET. Therefore, even if the dependence on the process or the deviation of the threshold voltage deviates the ZTCP voltage from a desired value, the application of the proper substrate bias voltage can correct the ZTCP voltage value. Also, by using this characteristic, the ZTCP voltage can be shifted to the various levels. Consequently, the use of the ZTCP voltage realizes the voltage reference which owns the variable-output-voltage level.

3.2 Circuit Implementation

The schematic of the proposed voltage reference circuit with a startup circuit and a substrate bias voltage generator is shown in Fig. 1. The transistors Mp1, Mp2, Mn1, Mn2 and the resistor R_S constitute the voltage reference core circuit and form a self-biasing current loop. The output voltage of the voltage reference circuit is obtained at the gate terminal of Mn1. The transistors Mpa, Mna and Mnb constitute the startup circuit. The substrate bias voltage generator provides the n-channel MOSFET's with the substrate bias voltage, V_{sub}.

The currents I_1, I_2 and the output voltage V_{out} are independent of the power-supply [13]. If the temperature dependence of the resistor R_S is ignored and the ZTCP voltage and current of Mn1 are designated as V_{ZTCPN1} and I_{ZTCPN1} respectively, by choosing the aspect ratio of Mn1 and the resistance R_S properly so that I_1, I_2 and V_{out} would satisfy the next condition

$$\begin{cases} I_1 = I_2 = I_{\mathrm{ZTCPN1}}, \\ V_{out} = V_{\mathrm{ZTCPN1}}, \end{cases} \quad (11)$$

they become independent of both temperature and power-

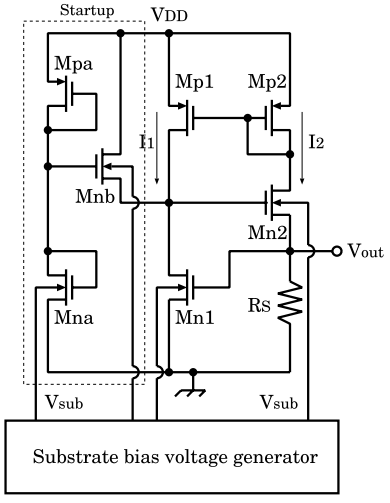

Fig. 1 Schematic of CMOS zero-temperature-coefficient point voltage reference with startup circuit and substrate bias voltage generator.

supply.

The threshold voltage is dominant in both ZTCP voltage and output voltage. This means that if the substrate bias voltage is applied to the *n*-channel MOSFET's, the variation of the output voltage almost corresponds to that of the ZTCP voltage. That is, even if the substrate bias voltage is applied, the equality of the output voltage to the ZTCP voltage of Mn1 is maintained. Consequently, the dependence of the output voltage on the process and the deviation of the threshold voltage can be compensated by the substrate bias while maintaining its temperature-insensitivity. Also, even if the resistance R_S or the mobility of an electron deviates from the desired value by ±10%, the deviation of the output voltage due to it is suppressed to only ∓1% respectively. Thus, the voltage reference circuit, which keeps the output voltage independent of the temperature, the power-supply and the process, can be implemented. By applying the substrate bias voltage, the output voltage can also be shifted to the various levels.

3.3 Compensation for Resistor Temperature Dependence —Thermal Term Product Cancellation

The proposed principle has ignored the temperature dependence of the resistor R_S, but in fact, it must be considered for the implementation of the proposed circuit. The compensation technique of the temperature dependence of the resistor R_S is proposed by using the thermal term product cancellation. In the first place, the concept of the thermal term product cancellation is developed. Suppose that $g(T)$ and $h(T)$ are functions proportional and inversely proportional to the absolute temperature respectively, they are expressed as

$$g(T) = aT, \tag{12}$$

$$h(T) = \frac{b}{T}, \tag{13}$$

where a and b are the constants of proportion respectively. The product of $g(T)$ and $h(T)$, i.e., "the product of two thermal terms" gives

$$g(T)\,h(T) = ab, \tag{14}$$

and it is obviously not dependent on the temperature. This is the concept of the thermal term product cancellation.

The output voltage of the proposed voltage reference circuit is expressed as

$$V_{out} = R_S I_2 = R_S I_1, \tag{15}$$

$$= R_S \frac{\mu_N C_{ox}}{2} \left(\frac{W}{L}\right)_{N1} (V_{GSN1} - V_{TN1})^2, \tag{16}$$

where μ_N is the mobility of the electron, and $(W/L)_{N1}$ the aspect ratio of the transistor Mn1. In this equation, the mobility μ_N, the threshold voltage V_{TN1} and the resistance R_S are dependent on the temperature. The temperature dependence of the mobility μ_N and the threshold voltage V_{TN1} are modeled by Eqs.(2) and (3) respectively, and the temperature dependence of the resistance R_S is modeled as

$$R_S = R_S(T_0) \cdot \{1 + \alpha_{RS} \cdot (T - T_0)\}, \tag{17}$$

where α_{RS} is the temperature coefficient of the resistance R_S. If $\{(C_{ox}/2)(W/L)_{N1}\}$ is represented by κ, the partial differentiation of the output voltage expressed by Eq.(16) by the absolute temperature T yields

$$\begin{aligned}\frac{\partial V_{out}}{\partial T} &= \left(\alpha_{RS}\kappa R_S \mu_N - \frac{3}{2}\kappa R_S \mu_N T^{-1}\right) V_{GSN1}^2 \\ &\quad + (3\kappa R_S \mu_N T^{-1} V_{TN1} - 2\alpha_{RS}\kappa R_S \mu_N V_{TN1} \\ &\quad + 2\alpha_{TN}\kappa R_S \mu_N) V_{GSN1} \\ &\quad + (\alpha_{RS}\kappa R_S \mu_N V_{TN1}^2 - \frac{3}{2}\kappa R_S \mu_N T^{-1} V_{TN1}^2 \\ &\quad - 2\alpha_{TN}\kappa R_S \mu_N V_{TN1}),\end{aligned} \tag{18}$$

where α_{TN} is the temperature coefficient of the threshold voltage of the *n*-channel MOSFET. If the condition $(\partial V_{out}/\partial T) = 0$ is satisfied, i.e., the temperature coefficient of the output voltage equals to zero, it is a second-order equation of V_{GSN1}. Solving it for V_{GSN1} on condition that Mn1 is not cutoff yields

$$\begin{aligned}V_{GSN1} &= V_{out} \\ &= \frac{-3V_{TN1} + 2\alpha_{RS} V_{TN1} T - 4\alpha_{TN} T}{2\alpha_{RS} T - 3}.\end{aligned} \tag{19}$$

In this equation, if the temperature dependence of the threshold voltage V_{TN1} is considered and $T = T_0$, it is rewritten as

$$V_{out} = \frac{-3V_{TN1}(T_0) + 2\alpha_{RS} T_0 V_{TN1}(T_0) - 4\alpha_{TN} T_0}{2\alpha_{RS} T_0 - 3}. \tag{20}$$

Furthermore, if the temperature dependence of the resistor is ignored and $\alpha_{RS} = 0$, the output voltage is expressed as

$$V_{out} = V_{TN1}(T_0) + \frac{4}{3}\alpha_{TN} T_0. \tag{21}$$

It corresponds to the ZTCP voltage of Mn1.

In these analyses, $R_S(T)$ and $I_1(T)$ correspond to the above-mentioned $g(T)$ and $h(T)$ respectively. That is, if the resistor R_S has a positive temperature coefficient, giving a shift to the gate-source voltage V_{GSN1}, i.e., the output voltage V_{out} from the ZTCP voltage value so that the drain current I_1 would have a negative temperature coefficient which is exactly inversely-proportional to the temperature dependence of R_S, makes it possible to compensate the temperature dependence of the resistor R_S, by the thermal term product cancellation. The necessary shift to be given to the output voltage is equal to the difference of the output voltages expressed by Eqs.(20) and (21). If the necessary shift is designated as ΔV_{out}, it is derived as

$$\Delta V_{out} = V_{out}|_{\alpha_{RS} \neq 0} - V_{out}|_{\alpha_{RS} = 0}, \tag{22}$$

$$= \frac{8\alpha_{RS}\alpha_{TN} T_0^2}{9 - 6\alpha_{RS} T_0}. \tag{23}$$

Thus, giving the shift to the output voltage from the ZTCP voltage of Mn1 by ΔV_{out} compensates the temperature dependence of the resistor R_S by the thermal term product cancellation.

4. Simulation Results

The SPICE simulation was performed with standard 0.8-μm CMOS n-well process BSIM3v3 model parameters, where the threshold voltage of the n-channel MOSFET V_{TN} = 636 mV at 300 K and its temperature coefficient α_{TN} = 0.29 mV/°C.

The characteristic of the simulated drain current versus the gate-source voltage of the n-channel MOSFET for temperature variations is shown in Fig. 2, where the aspect ratio is 2 μm/0.8 μm and the drain-source voltage is 2.25 V. The temperature is changed from 300 K to 425 K in 25 K steps. All the characteristic curves cross each other around a point. This is the ZTCP. The ZTCP voltage and current are

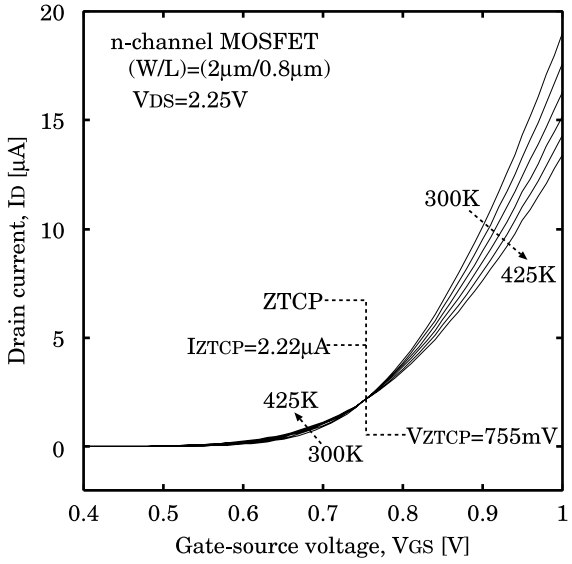

Fig. 2 Simulated drain current versus gate-source voltage for temperature variations.

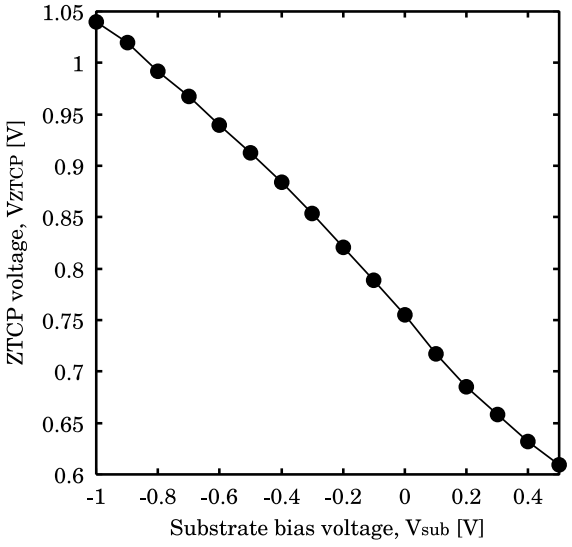

Fig. 3 Variation of ZTCP voltage by substrate bias voltage.

755 mV and 2.22 μA respectively. A similar result has also been derived from experimental measurement [11].

The variation of the ZTCP voltage by applying the substrate bias voltage is shown in Fig. 3. The substrate bias voltage is changed from −1 V to 0.5 V. If the negative substrate bias voltage is applied, the ZTCP voltage increases. On the other hand, if the positive one is applied, it decreases.

The transistor aspect ratios and the other element values of the proposed circuit are shown in Table 1. It compares the values for the case that the temperature dependence of the resistor R_S is ignored and the values for the case that it is considered and compensated, where assuming R_S as the polysilicon resistor, the temperature coefficient α_{RS} is set at 1500 ppm/°C. From Eq.(23), the necessary shift to be given to the output voltage is about 50 mV. Then, the aspect ratio of the transistor Mn1 is made smaller in order to enhance the output voltage and compensate the temperature dependence of R_S. The power-supply voltage is set at 3 V for both cases.

The comparison of the various characteristics of the proposed circuit for the cases that the temperature dependence of R_S is ignored and considered are shown in Figs. 4–7. The characteristic of the simulated output voltage versus the temperature without the substrate bias voltage is shown in Fig. 4. The theoretical values derived from Eqs.(20) and (21) are also shown for comparison. The simulated output

Table 1 Transistor aspect ratios in μm and element values.

Element	α_{RS} = 0 ppm/°C	α_{RS} = 1500 ppm/°C (Compensated)
Mpa	20/0.8	20/0.8
Mna, Mnb	2/0.8	2/0.8
Mp1, Mp2	60/0.8	60/0.8
Mn1	48.7/0.8	30/0.8
Mn2	20/0.8	20/0.8
R_S	10 kΩ	10 kΩ

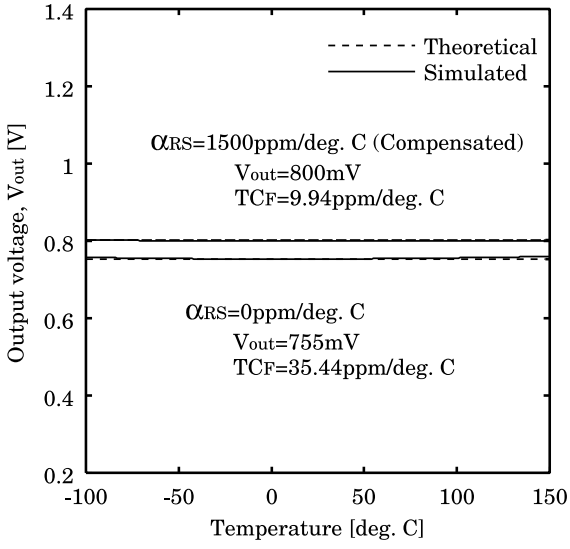

Fig. 4 Simulated output voltage versus temperature. The solid line represents the simulated values, and the dashed one represents the theoretical values.

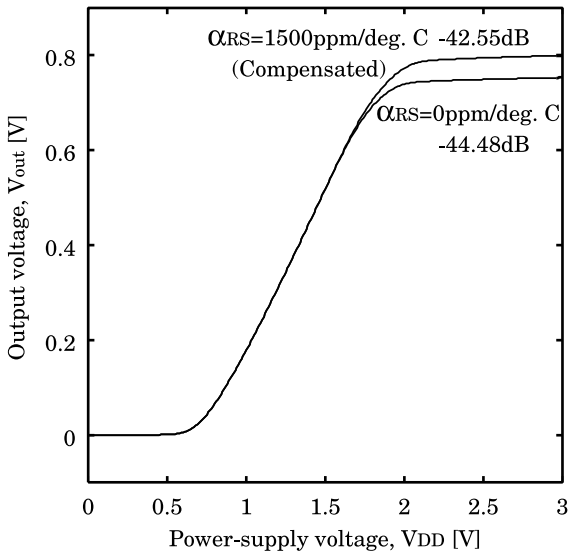

Fig. 5 Simulated output voltage versus power-supply voltage.

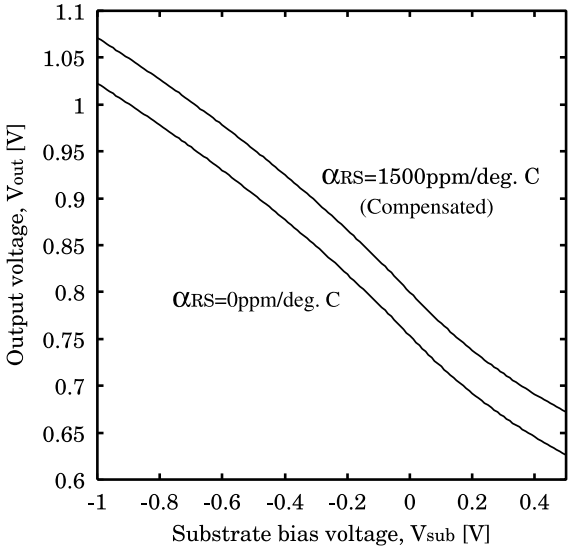

Fig. 6 Controllability of output voltage by substrate bias voltage.

voltages are almost constant with the temperature in both cases, and they are 755 mV and 800 mV respectively. The theoretical ones are 752 mV and 802 mV respectively. The errors are only −3 mV and 2 mV respectively. The given output voltage shift to compensate the temperature dependence of R_S is about 50 mV in both simulation and theory. The simulated fractional temperature coefficients (TC_F) are 35.44 ppm/°C and 9.94 ppm/°C over the temperature range from −100°C to 150°C respectively. The maximum drifts of the output voltage with the temperature are 6.7 mV and 2.0 mV respectively.

The characteristic of the simulated output voltage versus the power-supply voltage is shown in Fig. 5. The proposed circuit can operate down to 2.0 V and 2.1 V respectively, for the cases that the temperature dependence of R_S is ignored and considered. The power-supply rejection ratios (PSRR) are −44.48 dB and −42.55 dB at 100 Hz respectively.

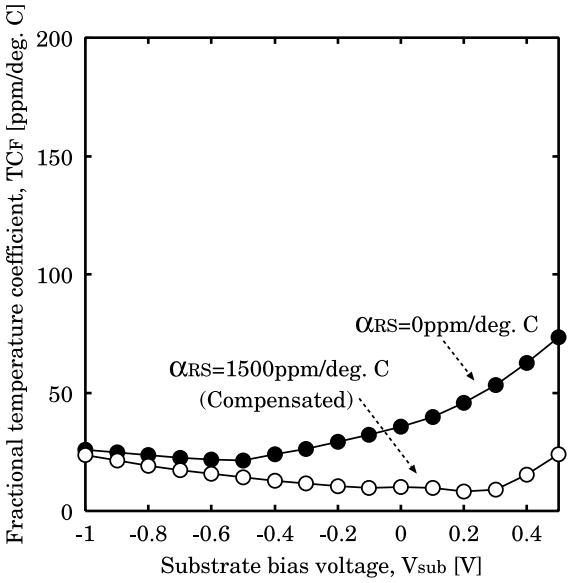

Fig. 7 Simulated fractional temperature coefficient versus substrate bias voltage. The black dots represent values for $\alpha_{RS} = 0$ ppm/°C, and the white ones represent values for $\alpha_{RS} = 1500$ ppm/°C.

The controllability of the output voltage by applying the substrate bias voltage is shown in Fig. 6, where the substrate bias voltage is changed from −1.0 V to 0.5 V. The output voltage is variable by applying the substrate bias voltage in both cases that the temperature dependence of R_S is ignored and considered. The output voltage increases for the negative substrate bias voltage, and decreases for the positive one. In the former case, the output voltage is 1.02 V at the substrate bias voltage $V_{sub} = -1.0$ V, and 0.63 V at $V_{sub} = 0.5$ V. In the latter case, the output voltage is 1.07 V at $V_{sub} = -1.0$ V, and 0.67 V at $V_{sub} = 0.5$ V. The output voltage shift of about 50 mV to compensate the temperature dependence of R_S is maintained even if the substrate bias voltage is changed. The characteristic curve for the case that the temperature dependence of R_S is ignored almost corresponds to the curve in Fig. 3. This means that the equality of the output voltage to the ZTCP voltage is almost maintained even if the substrate bias voltage is applied.

The characteristic of the simulated fractional temperature coefficient of the output voltage versus the substrate bias voltage is shown in Fig. 7. The temperature-insensitivity is maintained in both cases that the temperature dependence of R_S is ignored and considered, even if the output voltage is changed by the substrate bias voltage. In the former case, the temperature coefficient is 25.86 ppm/°C at $V_{sub} = -1.0$ V, and 73.44 ppm/°C at $V_{sub} = 0.5$ V. In the latter case, the temperature coefficient is 23.57 ppm/°C at $V_{sub} = -1.0$ V, and 23.85 ppm/°C at $V_{sub} = 0.5$ V. If the temperature dependence of R_S is ignored, the fractional temperature coefficient is maintained less than 74 ppm/°C. If considered and compensated, it is maintained less than

Table 2 Simulated performance summary of proposed voltage reference circuit. (V_{DD} = 3 V, Technology: 0.8-μm CMOS n-well)

Parameter	α_{RS} = 0 ppm/°C	α_{RS} = 1500 ppm/°C (Compensated)
Output voltage		
at zero-bias	755 mV	800 mV
at V_{sub} = −1.0 V	1.02 V	1.07 V
at V_{sub} = 0.5 V	630 mV	670 mV
TC_F (−100°C to 150°C)		
at zero-bias	35.44 ppm/°C	9.94 ppm/°C
at V_{sub} = −1.0 V	25.86 ppm/°C	23.57 ppm/°C
at V_{sub} = 0.5 V	73.44 ppm/°C	23.85 ppm/°C
Maximum output voltage drift (−100°C to 150°C)		
at zero-bias	6.7 mV	2.0 mV
at V_{sub} = −1.0 V	6.6 mV	6.3 mV
at V_{sub} = 0.5 V	11.5 mV	4.0 mV
Minimum power-supply voltage	2.0 V	2.1 V
PSRR at 100 Hz, 25°C, zero-bias	−44.48 dB	−42.55 dB
Total active area except for substrate bias voltage generator	0.17×10^{-3}mm^2	0.16×10^{-3}mm^2

24 ppm/°C. The simulated performances of the proposed voltage reference circuit are summarized in Table 2.

5. Conclusion

The CMOS voltage reference circuit based on the voltage at the zero-temperature-coefficient point of the drain current is proposed. The output voltage of the proposed circuit is variable by the substrate bias. The proposed circuit uses the polysilicon resistor, and in fact, its temperature dependence affects the temperature-insensitivity of the output voltage. The compensation technique for the temperature dependence of the resistor is proposed. The simulated output voltage keeps the sub-1 V magnitude, and furthermore, it can be shifted down to the lower level while maintaining its temperature-insensitivity. A future task is the evaluation of the reliability or the reproducibility of the proposed circuit through experimental measurement.

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