Advanced Operational Amplifiers

劉 尙 大 敎授

전 자 공 학 부

Kyungpook National University

Advanced Current Mirrors and Opamps

- ❏ Two-stage opamps in many commercial ICs
- ❏ Modern opamps gaining in popularity
- ❏ Advanced current mirrors
- ❏ Folded-cascode opamps
- ❏ Current-mirror opamps
- ❏ Fully-differential opamps: better noise rejection
- ❏ Current-feedback opamps: large gain-bandwidth product

Wide-Swing Cascode Current Mirrors

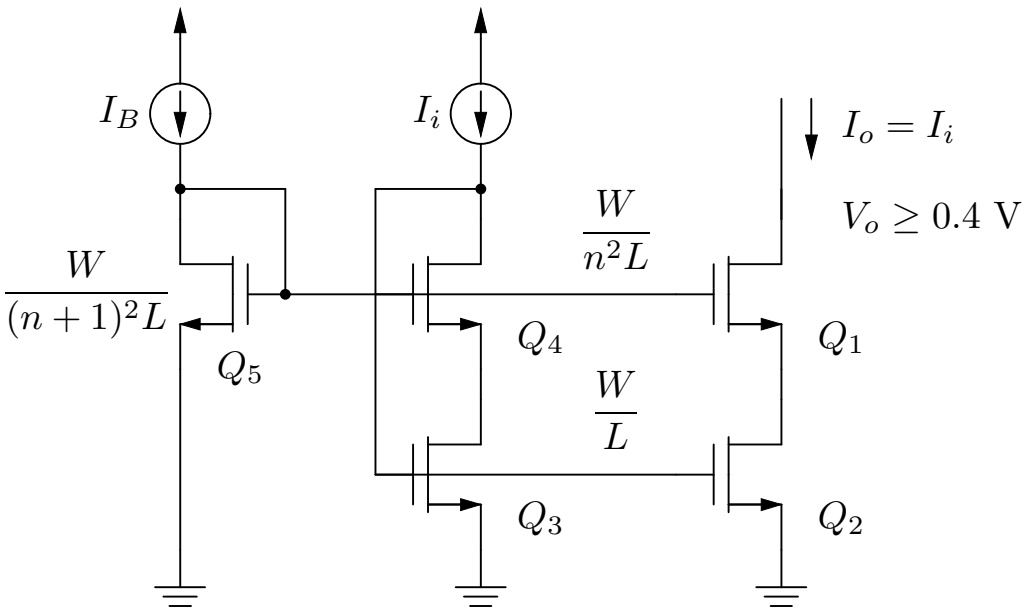
- ❏ Output-impedance degradation by short-channel effects
- ❏ R_o enhancement by cascoding: limits signal swing
- ❏ Q_4 lowers V_{DS} of Q_3 to match to V_{DS} of Q_2: $I_o = I_i$
- ❏ Q_2 and Q_3 biased at the edge of the active region.
- ❏ Effective gate-source voltages for $I_B = I_i = I_o = I_{D3}$

$$V_{\text{eff}} = V_{\text{eff2}} = V_{\text{eff3}} = \sqrt{\frac{2I_{D3}}{\mu_n C_{ox}(W/L)}}$$

$$V_{\text{eff5}} = (n+1)V_{\text{eff}}, \quad V_{\text{eff1}} = V_{\text{eff4}} = nV_{\text{eff}}$$

$$V_{G1} = V_{G4} = V_{G5} \equiv V_{\text{eff5}} + V_{tn} = (n+1)V_{\text{eff}} + V_{tn}$$

- ❏ A wide-swing cascode current mirror with two-transistor diode-connected circuit (whose input resistance $\simeq 1/g_m$)



❏ Minimum allowable output voltage for $n = 1$

$$V_{DS2} = V_{DS3} = V_{G5} - V_{GS1} = V_{G5} - (V_{\text{eff}1} + V_{tn}) = V_{\text{eff}}$$

$$\therefore V_o \geq V_{\text{eff}1} + V_{DS2} = (n+1)V_{\text{eff}} = 2V_{\text{eff}} \simeq 0.4 \sim 0.5 \text{ V}$$

❏ To ensure that all transistors are in the active region

$$V_{DS4} = V_{G3} - V_{DS3} = (V_{\text{eff}} + V_{tn}) - V_{\text{eff}} = V_{tn} > V_{\text{eff}4} = nV_{\text{eff}}$$

$$\therefore V_{tn} > nV_{\text{eff}} \simeq 0.2 \sim 0.25 \text{ V}$$

❏ Take $(W/L)_5$ smaller to bias Q_2 and Q_3 with slightly larger V_{DS} than the minimum ← no sharp boundary between linear and active regions, body effect of Q_1 and Q_4 ($V_{SB} > 0$, $V_{t1} \uparrow$, $V_{GS1} \uparrow$, $V_{DS2} \downarrow$)

$$V_{DS2} \simeq V_{\text{eff}} + (0.1 \sim 0.15) \text{ V}$$

❏ $L_2 = 2.5\lambda$ and $L_1 = 4\lambda$ (twice L_{min}) to reduce short-channel effects ($V_{DS2} < V_{DS1}$) and maximize the pole frequency ($\omega_{p2} \propto 1/L,\ 1/L^2$)

Wide-Swing Constant-g_m Bias Circuit

❏ Minimizes most of second-order imperfections caused by the finite-output impedance without greatly restricting signal swings.

❏ n-channel wide-swing cascode current mirror: $Q_1 - Q_5$

❏ p-channel wide-swing cascode current mirror: $Q_6 - Q_{10}$

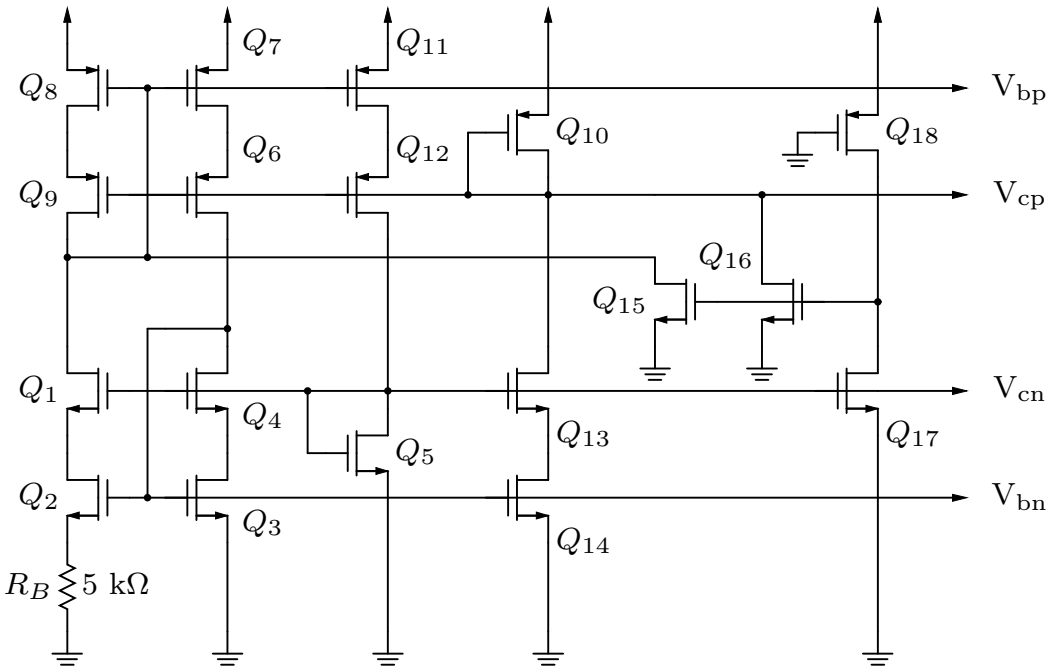
❏ Cascode bias circuit: $Q_{11} - Q_{14}$

❏ Start-up circuit: $Q_{15} - Q_{18}$

❏ This bias circuit for stabilized g_ms allows the performance of realized opamps to be accurately predicted using moderately simple equations.

❏ This constant-g_m bias circuit had been realized and verified for a 0.8-μm CMOS technology, and is very important in analog design.

❑ A wide-swing constant-g_m bias circuit: small W/L for Q_{18}



Enhanced Output-Impedance Mirrors

❑ Cascode current mirror with *regulated cascode transistor* to increase output resistance $R_o \rightarrow$ gain boosting

❑ Basic idea is to use a negative feedback amplifier to keep V_{DS} of Q_2 as stable as possible $\rightarrow I_o$ is less sensitive to the output signal.

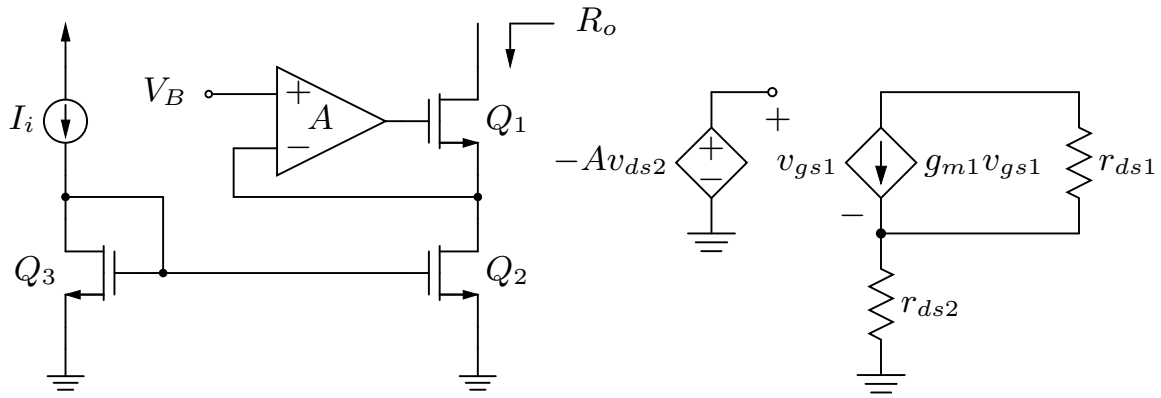
$$R_o = [g_{m1} r_{ds1}(1+A)+1]\, r_{ds2} + r_{ds1} \simeq g_{m1} r_{ds1} r_{ds2}(1+A)$$

❑ Practical limitation of R_o by a parasitic conductance between the drain of Q_1 and its substrate due to short-channel effects
$\leftarrow$ substrate current by impact ionization

❑ Reduced enhancement for bipolar transistors due to the base current

❑ Need for local compensation capacitors to prevent ringing and substantial increase of settling time for large signal transients

❏ An enhanced output-impedance current mirror



❏ Circuit equations for regulated cascode current mirror: $R_o = v_t/i_t$

$$v_{gs1} = -Av_{ds2} - v_{ds2} = -(1+A)v_{ds2} = -(1+A)r_{ds2}i_t$$

$$i_t = g_{m1}v_{gs1} + (v_t - r_{ds2}i_t)/r_{ds1}$$

$$v_t = (r_{ds1}+r_{ds2})i_t - g_{m1}r_{ds1}v_{gs1} = [r_{ds1}+r_{ds2}+(1+A)g_{m1}r_{ds1}r_{ds2}]i_t$$

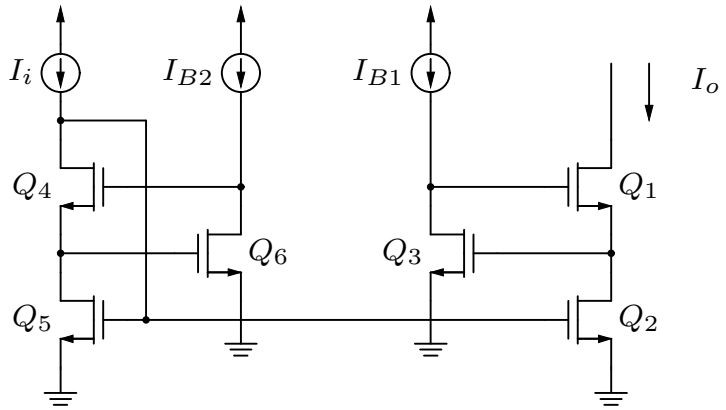
Säckinger Realization of Enhanced R_o Mirrors

❏ The feedback amplifier is realized by CS amplifiers: $A \simeq g_{m3}r_{ds3}/2$

$$R_o = (g_{m1}r_{ds1})r_{ds2}\left(\frac{g_{m3}r_{ds3}}{2}\right) = \frac{g_{m1}g_{m3}r_{ds1}r_{ds2}r_{ds3}}{2}$$

❏ The signal swing is significantly reduced due to the feedback amplifier.

$$V_{DS5} \equiv V_{DS2} = V_{GS3} = V_{\text{eff}3} + V_{tn} \gg V_{\text{eff}2}$$



Wide-Swing Current Mirror with Enhanced R_o

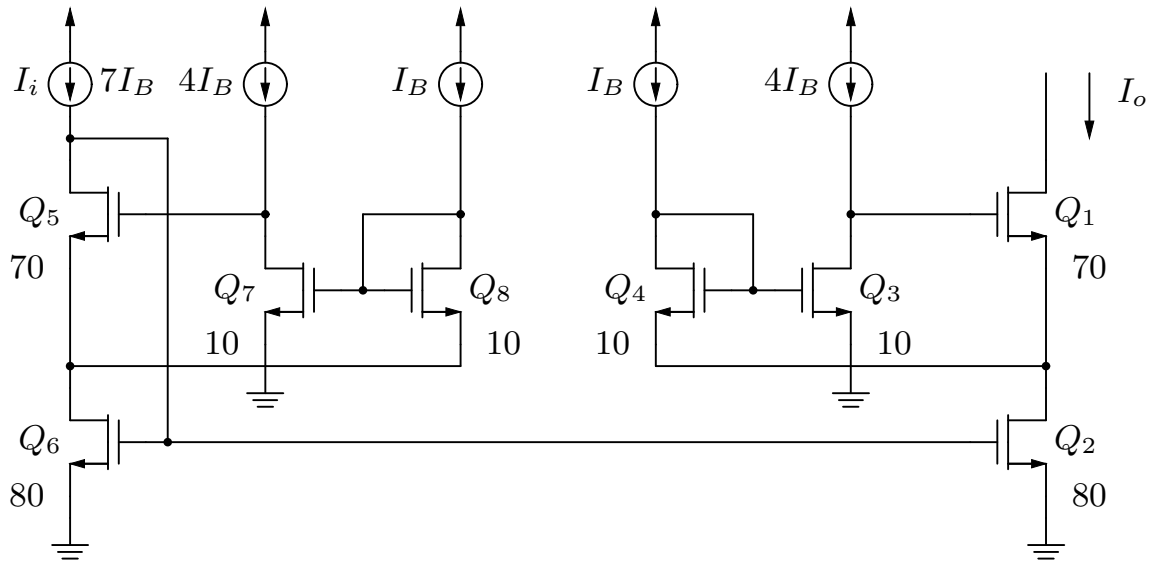
- Diode-connected transistors Q_4 and Q_8 are used as dc level shifters.
- All transistors are biased with the same current density and the same V_{eff} except for Q_3 and Q_7: $V_{\text{eff}} = \sqrt{2I_D/\mu_n C_{ox}(W/L)}$

$$I_i = 7I_B, \quad V_{\text{eff}3} = V_{\text{eff}7} = 2V_{\text{eff}}$$

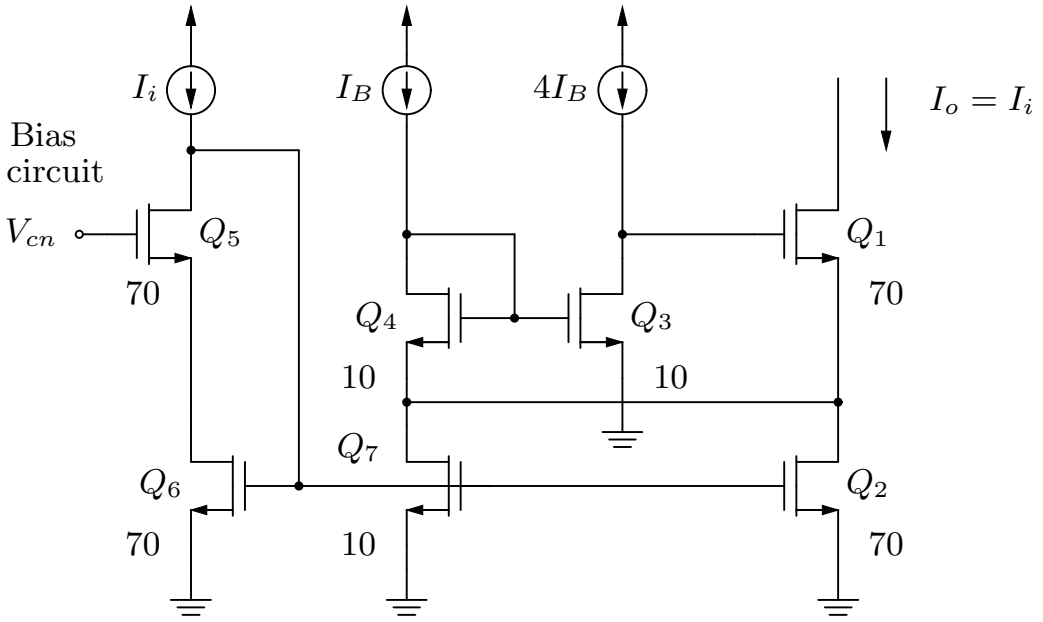
$$V_{DS2} = V_{G3} - V_{GS4} = (2V_{\text{eff}} + V_{tn}) - (V_{\text{eff}} + V_{tn}) = V_{\text{eff}}$$

- Power dissipation of this mirror with the shown W/L values would be almost doubled over that of a classical cascode mirror.
- Power dissipation can be reduced at the expense of speed by biasing the enhancement circuitry (Q_3, Q_4, Q_7, Q_8) at lower current density.

- A wide-swing current mirror with enhanced output impedance



❑ A modified version of wide-swing enhanced output-impedance mirror: slightly mismatching, but less area, instability, and power dissipation



Folded-Cascode Opamp

❑ Modern CMOS opamps are designed to drive only capacitive loads.

❑ No voltage buffer → higher speed and larger signal swing.

❑ Only a *single* high-impedance node at the output of an opamp.

❑ The admittance at all other node is on the order of g_m.

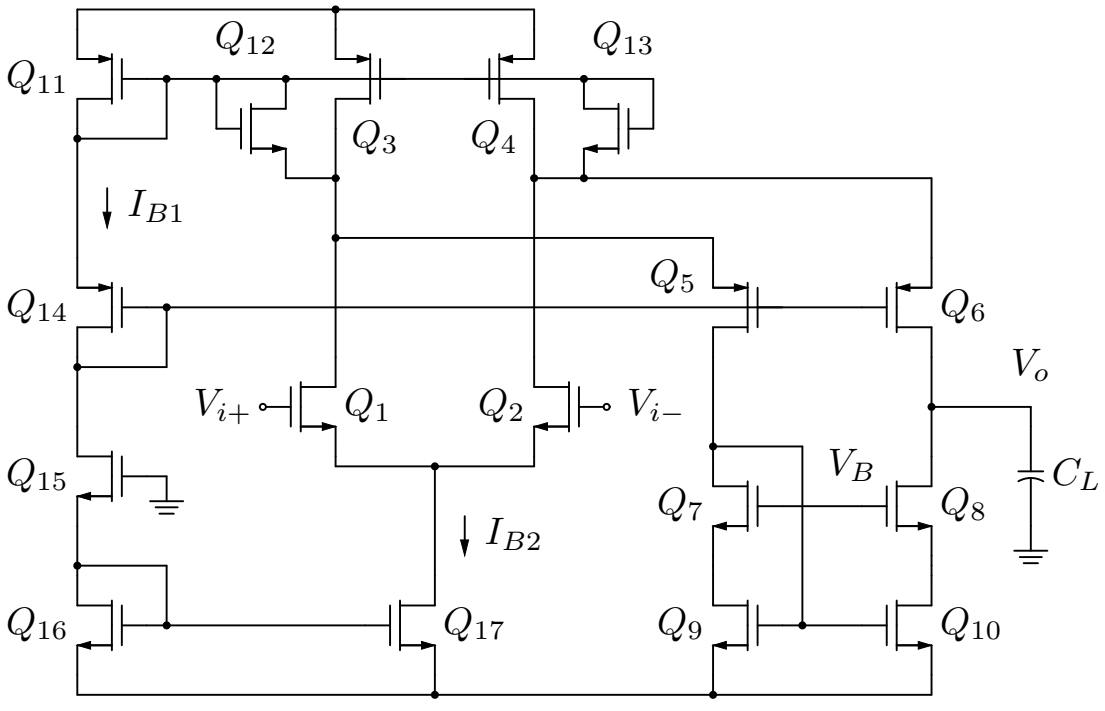
❑ The speed of the opamp is maximized by having all internal node of low impedance → reduced voltage signals and large current signals → *current-mode opamps* ($\omega_H \simeq 1/\sum \tau_i = 1/\sum R_{io}C_i$).

❑ The compensation is usually achieved by the load capacitance: larger C_L, more stable but slower.

❑ These opamps = operational transconductance amplifiers (OTAs)

- Q_1, Q_2 = differential transistors
- Q_5, Q_6 = cascode transistors + dc level shifters
- A single stage with a high gain of 3000 due to the high output resistance by cascoding
- $Q_7 \sim Q_{10}$ = Wilson, cascode, or wide-swing current mirror
- Q_{12}, Q_{13} = *clamp transistors*: to increase the slew rate and recover quickly from slewing as clamping the drain voltages of Q_1 and Q_2
- Dominant pole compensation by C_L or an additional capacitor
- Lead compensation by a resistor placed in series with C_L
- Bias current of cascode transistors is derived by a current subtraction → I_{B1}, I_{B2} from the same bias circuit using *replication principle*

- A folded-cascode operational amplifier with clamp transistors



Small Signal Analysis

- Two signal paths have slightly different transfer functions due to poles and zeros caused by the current mirror. For an nMOS mirror, a pole-zero doublet occurs at frequencies greater than ω_{ta} and can be ignored.
- Ignoring HF poles and zeros ($\omega_{p2} \gg \omega_{ta}$) and assuming that g_{m5} and g_{m6} are much larger than g_{ds3} and g_{ds4}, the transfer function is given by

$$A_V = \frac{V_o}{V_i} \simeq g_{m1} Z_L(s) = \frac{g_{m1} R_o}{1 + sR_o C_L} \quad \left(R_o = \frac{g_m r_d^2}{3} \sim \frac{g_m r_d^2}{2} \right)$$

- The unity-gain frequency of the opamp

$$\omega_{ta} \simeq \frac{g_{m1}}{C_L} = \frac{\sqrt{2 I_{D1} \mu_n C_{ox} (W/L)_1}}{C_L}$$

- Maximizing g_{m1} maximizes the unity-gain bandwidth ω_{ta} for the given load capacitance C_L (dominant pole).

- g_{m1} is maximized by using wide nMOST and larger bias current than that of cascode and mirror MOSTs of the output node → maximizes R_o and dc gain, better thermal noise performance ($v_n^2 = 4kT\frac{2}{3g_m}$)
- A practical upper limit on the ratio of I_{D1} to I_{D5} might be around 4 due to biasing by current subtraction.
- Lead compensation by a resistor R_C: chosen to place a zero at $1.2\omega_{ta}$

$$A_V = \frac{g_{m1}}{1/R_o + 1/(R_C + 1/sC_L)} \simeq \frac{g_{m1}(1 + sR_C C_L)}{sC_L}$$

- The second poles are primarily due to the time constants introduced by the resistances and parasitic capacitances at the sources of the p-channel cascode transistors: C_{s6}, $R_{s6} = \frac{1}{g_{m6}}(1 + R_L/r_{ds6})$

Slew Rate

- A large differential input voltage → Q_1 to be turned on hard, Q_2 to be turned off → I_{D4} will be directed through Q_6 into C_L.

$$\text{SR} = \frac{I_{D4}}{C_L}$$

- Since designing $I_{B2} > I_{D3}$, both Q_1 and the current source I_{B2} will go into the triode region: $I_{D3} = I_{D1} = I_{D17}$.
- The source and drain voltage of Q_1 approaches V_{SS} to decrease I_{B2}.
- When coming out of slewing, the source and drain voltage of Q_1 must slew back to a voltage close to V_{DD}.
- This additional slewing time greatly increases the transient times and the distortion for switched-capacitor applications.

- Clamp transistors Q_{12}, Q_{13} are turned off during normal operation.
- Their main purpose is to clamp the drain voltages of Q_1 or Q_2 so they don't change as much during slewing.
- A second effect dynamically increases the bias currents of Q_3 and Q_4 during slewing.
- Q_{12} conducts with the current coming from Q_{11}.
- The current increase in Q_{11} causes the currents in Q_3 and Q_4 to also increase until the sum of the currents Q_3 and Q_{12} is equal to I_{B2}.
- The increase in bias current of Q_4 results in an increase of the maximum current available for charging C_L.

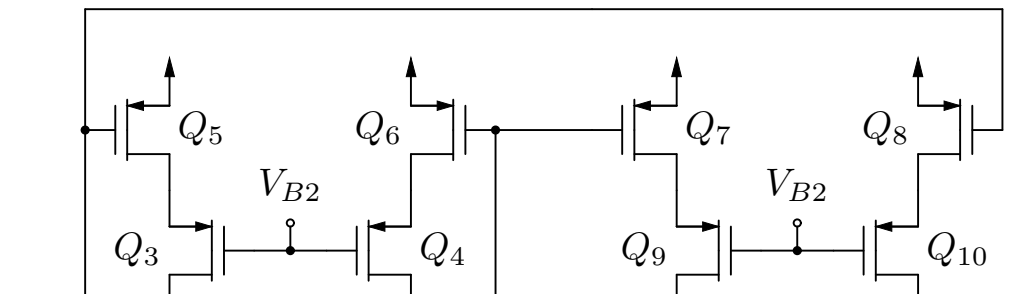
Current-Mirror Opamp

- ❏ Another popular opamp for driving on-chip capacitive loads
- ❏ All nodes are low impedance except for the output node.
- ❏ A reasonable overall gain can be achieved by using good current mirrors with high output impedance.
- ❏ Approximate transfer function for current gain K

$$A_V = \frac{V_o}{V_i} = Kg_{m1}Z_L(s) = \frac{Kg_{m1}R_o}{1+sR_oC_L}$$

- ❏ Unity-gain frequency

$$\omega_{ta} \simeq \frac{Kg_{m1}}{C_L} = \frac{K\sqrt{2I_{D1}\mu_n C_{ox}(W/L)_1}}{C_L}$$



- ❏ A current-mirror opamp with wide-swing cascode current mirrors: $I_{D12} = KI_{D11} = KI_{D1} = KI_B/2$

❏ Total current is known for a given power-supply voltages and P_D.

$$I_t = (3+K)I_{D1} = P_D/(V_{DD} - V_{SS})$$

❏ For larger values of K, the opamp transconductance $G_m \equiv Kg_{m1}$ is larger, ω_{ta} is also larger if not limited by high-frequency poles, and the dc gain A_0 is larger for fixed I_t.

$$\omega_{ta} = \frac{Kg_{m1}}{C_L} \equiv \frac{G_m}{C_L} = \frac{K}{\sqrt{3+K}} \frac{\sqrt{2I_t\mu_n C_{ox}(W/L)_1}}{C_L}$$

$$R_o \simeq \frac{g_{m10}r_{ds10}^2}{2} = \frac{\sqrt{2KI_{D1}\mu_p C_{ox}K(W/L)_1}}{2} \frac{V_A^2}{(KI_{D1})^2}$$

$$= \frac{\sqrt{2\mu_p C_{ox}(W/L)_1}}{2} \frac{V_A^2}{K(I_{D1})^{3/2}}$$

$$A_0 = Kg_{m1}R_o = \frac{(3+K)\sqrt{\mu_n\mu_p}C_{ox}(W/L)_1 V_A^2}{I_t}$$

❏ A practical upper limit on K might be around *five*.

❏ The important nodes to determine the nondominant poles are the drain of Q_1 primarily, and the drains of Q_2 and Q_9 secondly.

❏ For given I_t, increasing K ($I_{D1} \downarrow$, $W_8 \uparrow$) increases the time constant of these nodes. $\rightarrow$ The second pole moves to lower frequencies.

❏ For high speed operation, K might be taken as small as one. $K = 2$ might be a reasonable compromize for general purpose.

❏ Slew rate of the current-mirror opamp

$$\text{SR} = \frac{KI_B}{C_L}$$

❏ For $K = 4$, 4/5 of the total bias current will be available for charging or discharging C_L during slewing $\leftarrow 4I_B/(I_B + 0 + 0 + 4I_B)$.

- This result gives a current-mirror opamp superior slew rates even when compared to a folded-cascode opamp with clamp transistors.
- No large voltage transients due to low impedance nodes.
- For the larger bandwidth and slew rate, the current-mirror opamp is usually preferred over a folded-cascode opamp.
- However, CMO will suffer from larger thermal noise (smaller g_m) because input transistors are biased at a lower proportion of I_t.
- Example 6.3: analysis for transistor sizes given in Table 6.2
  (1) $K = 2$, $I_{D1} = I_t/(3+K) = (P_D/5)/5 = 80\ \mu$A
  (2) $g_{m1} = \sqrt{2I_{D1}\mu_n C_{ox}(W/L)_1} = 1.7$ mA/V
  (3) $f_{ta} = Kg_{m1}/2\pi C_L = 54$ MHz
  (4) SR $= KI_B/C_L = K2I_{D1}/C_L = 32\ \text{V}/\mu\text{s}$

Linear Settling Time

- Time constant for linear settling time: affected by both the feedback factor β and the effective load capacitance C_L, 0.1% $t_s = 7\tau$

$$\tau = \frac{1}{\omega_{3\text{dB}}} = \frac{1}{\beta\omega_{ta}}, \quad \omega_{ta} = \frac{g_{m1}}{C_C}, \ \frac{g_{m1}}{C_L}, \ \frac{Kg_{m1}}{C_L}$$

- Feedback factor by return ratio analysis: C_C = compensation capacitance, C_p = input capacitance of opamp (parasitic + switch)

$$\beta = \frac{1/s(C_1+C_p)}{1/s(C_1+C_p)+1/sC_2} = \frac{C_2}{C_1+C_2+C_p}$$

- Effective load capacitance: C_i = input capacitance of the next stage

$$C_L = C_i + C_C + \frac{C_2(C_1+C_p)}{C_1+C_2+C_p}$$

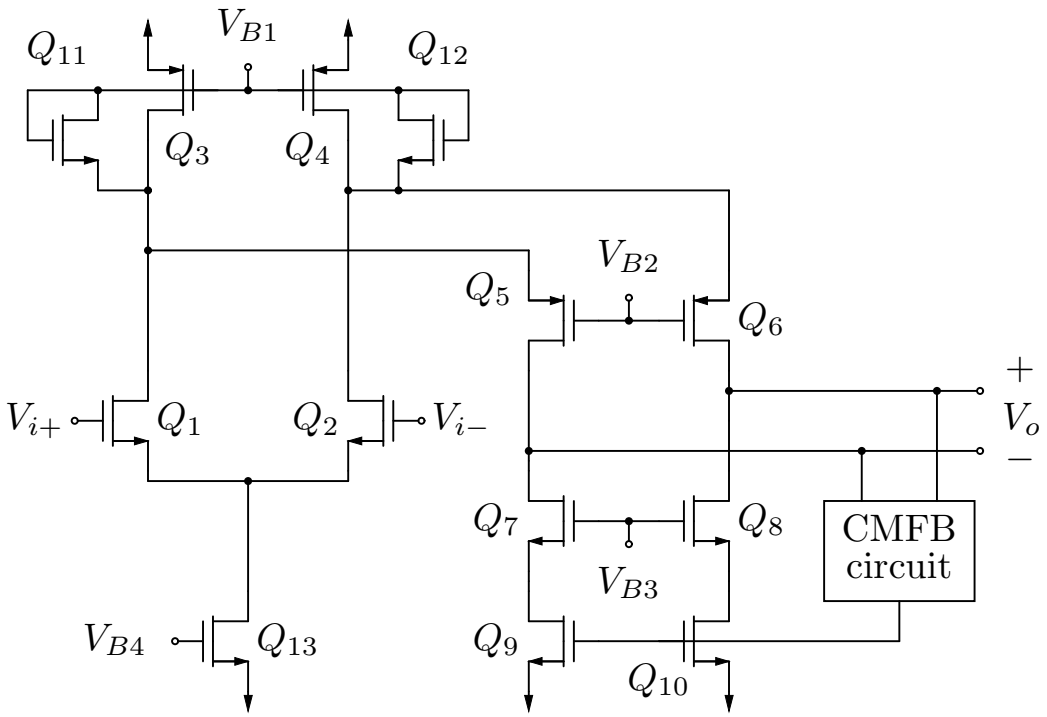
Fully Differential Opamps

- ❏ Balanced circuits: symmetric and differential inputs and outputs
- ❏ Rejection of common-mode noise from the substrate and switches
- ❏ But can not reject a differential noise by voltage-dependent nonlinearities that cause more noise to feed into one signal path than the other.
- ❏ One drawback is that a common-mode feedback circuit must be added.
- ❏ The design of a good CMFB circuit is not trivial: the speed performance comparable to the differential path, the limitation of continuous-time CMFB circuits on maximum allowable signal, the glitch injection and increase of load capacitance for switched-capacitor CMFB circuits.
- ❏ Slew-rate reduction due to fixed-bias currents in output current mirror
- ❏ Regardless of limitations, differential designs are becoming more popular.

Fully Differential Folded-Cascode Opamp

- ❏ Cascode current sources: Q_7 and Q_8, Q_9 and Q_{10}
- ❏ The CMFB circuit will detect the average of two output signals.
- ❏ The negative slew rate is limited by the bias currents of Q_9 or Q_{10}.
- ❏ Clamp transistors Q_{11}, Q_{12} to minimize transient voltage changes.
- ❏ Drain nodes of the input devices will be responsible for the second pole → each signal path consists of only this and output nodes.
- ❏ The complementary topology with nMOS as cascode transistor is often a reasonable choice for high-speed designs. But the dc gain would become smaller due to the input transistors of pMOS.

❏ A fully differential folded-cascode opamp



Fully Differential Current-Mirror Opamp

❏ Topology selection: whether the dc gain or bandwidth is more important, whether C_L or second pole is limiting the bandwidth.

❏ nMOS input transistors: larger dc gain, lower thermal noise.

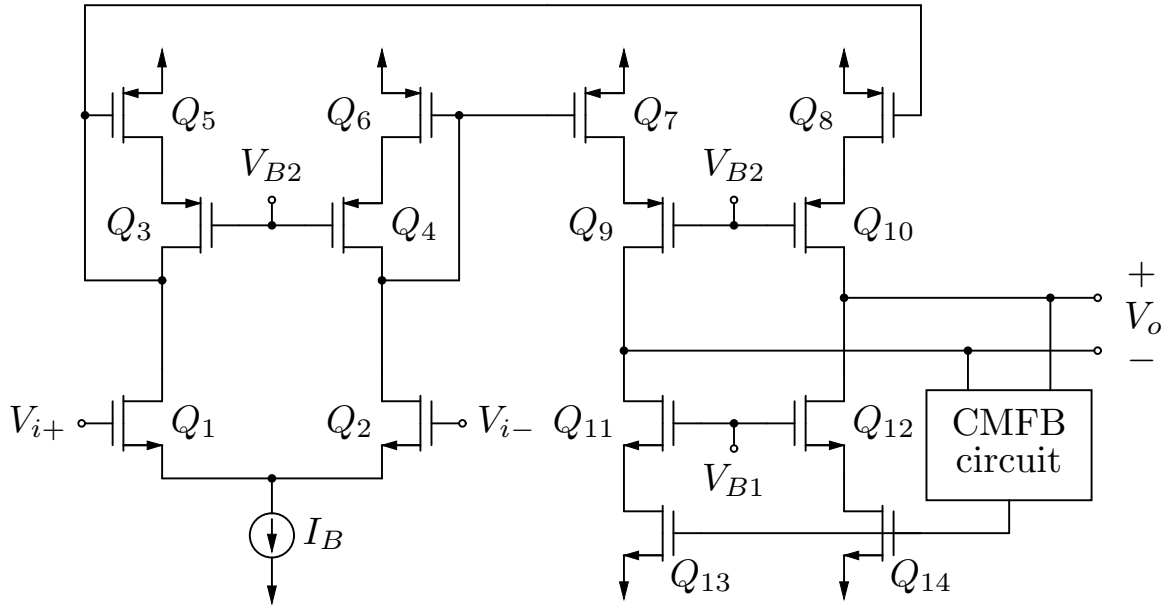
❏ pMOS input transistors: larger bandwidth, lower 1/f noise.

❏ For a general-purpose fully differential opamp: large pMOS input transistors, a current gain of $K = 2$, and wide-swing enhanced output-impedance cascode mirrors and current sources.

❏ The negative slew rate is limited by the bias currents of Q_{13} or Q_{14}.

❏ It is possible to modify the designs to improve slew rate at the expense of small-signal performances using additional circuitry.

❑ A fully differential current-mirror opamp



Alternative Fully Differential Opamps

❑ A fully differential current-mirror opamp with bidirectional output drive: four current mirrors having two outputs for sourcing and sinking.

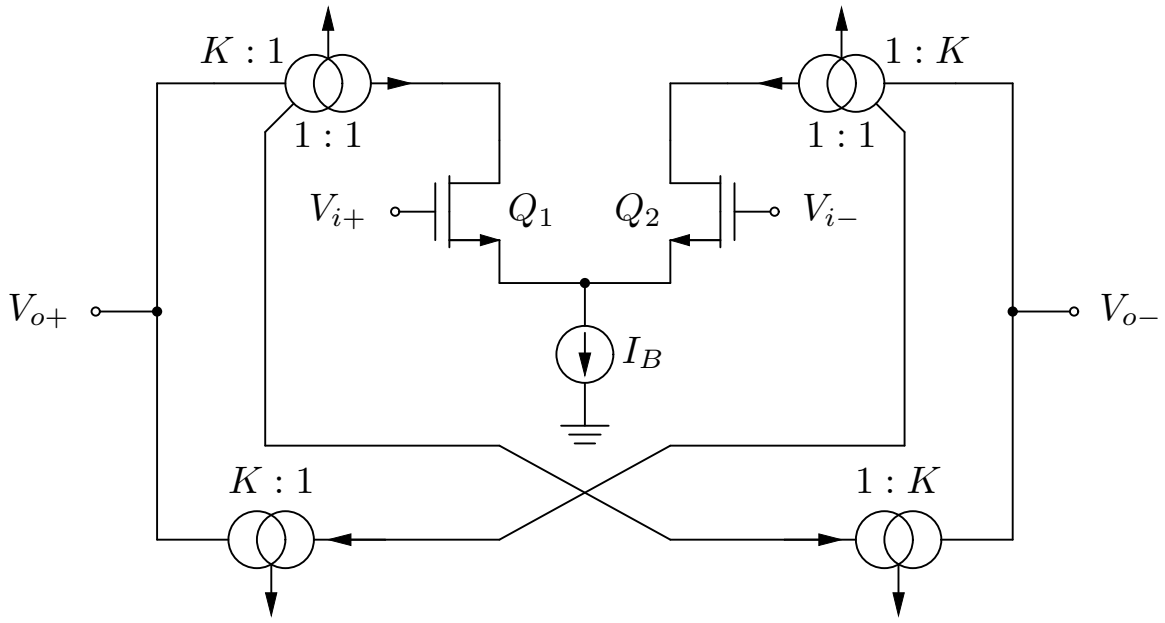
For a large differential input, the current going into V_{o+} will be KI_B, and the current being sinked from V_{o-} will also be KI_B due to other mirror.

❑ A class AB fully differential current-mirror opamp: low power, two differential pairs connected in parallel, a differential pair Q_3, Q_4, a level shifter (Q_1: source follower, Q_2: diode), small I_B (class AB).

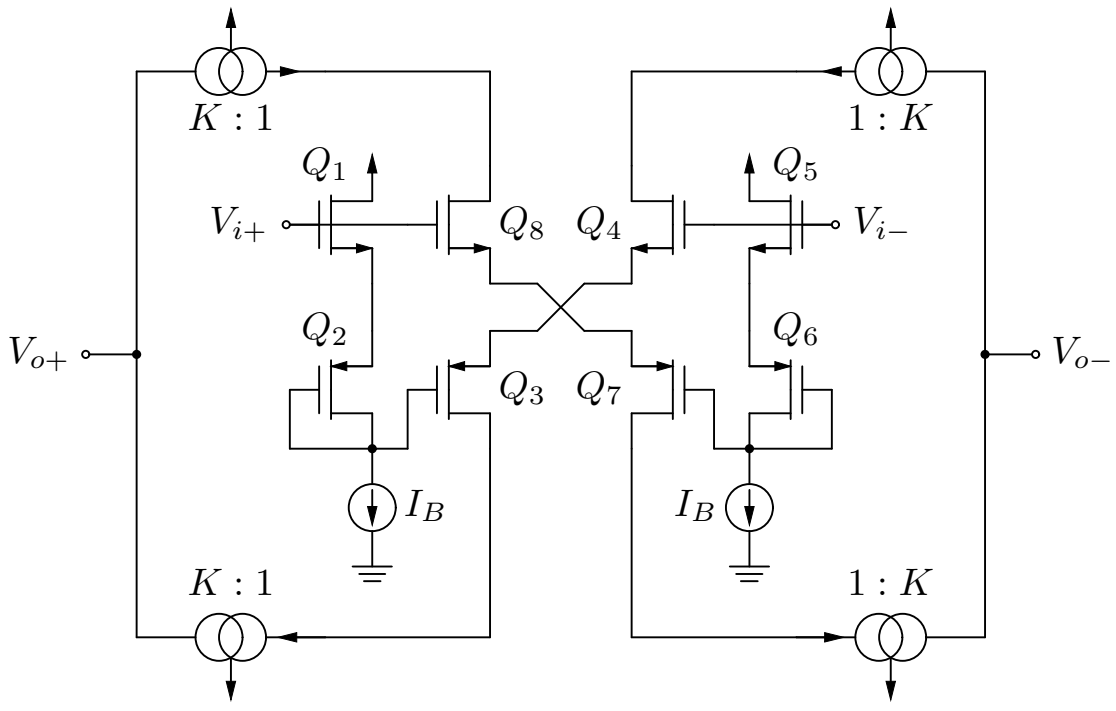
For a large differential input voltage, the pair Q_3, Q_4 turns off, while the current through the pair Q_7, Q_8 increases dynamically due to a lowered gate voltage of Q_7 → a very large slew-rate performance, but a major problem for low supply voltage due to $V_{CM} \geq 2V_{GS} + V_{\text{eff}} = 2V_t + 3V_{\text{eff}}$

❑ Level shifters → noise increase, lowering second poles by parasitics

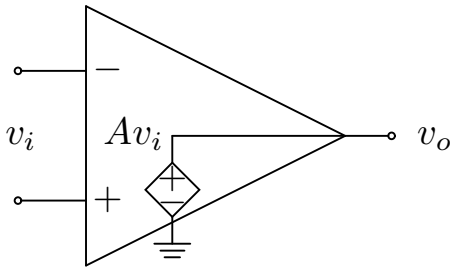
❏ A fully differential current-mirror opamp with bidirectional output drive: the CMFB circuit is not shown.



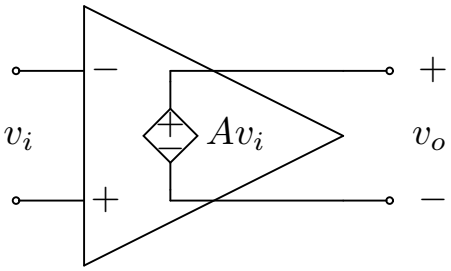
❏ A class AB fully differential opamp: the CMFB circuit is not shown.



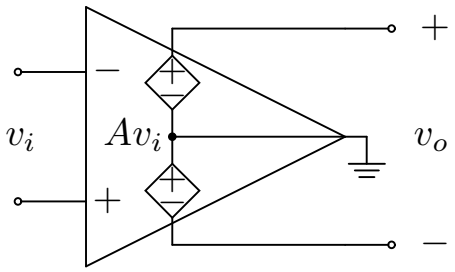
❏ A fully differential opamp composed of two single ouput opamps



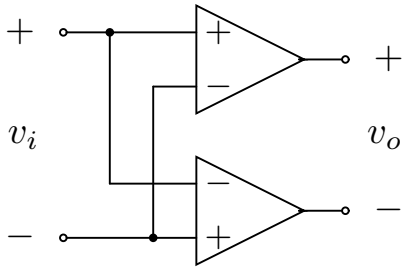
Single output



Differential output

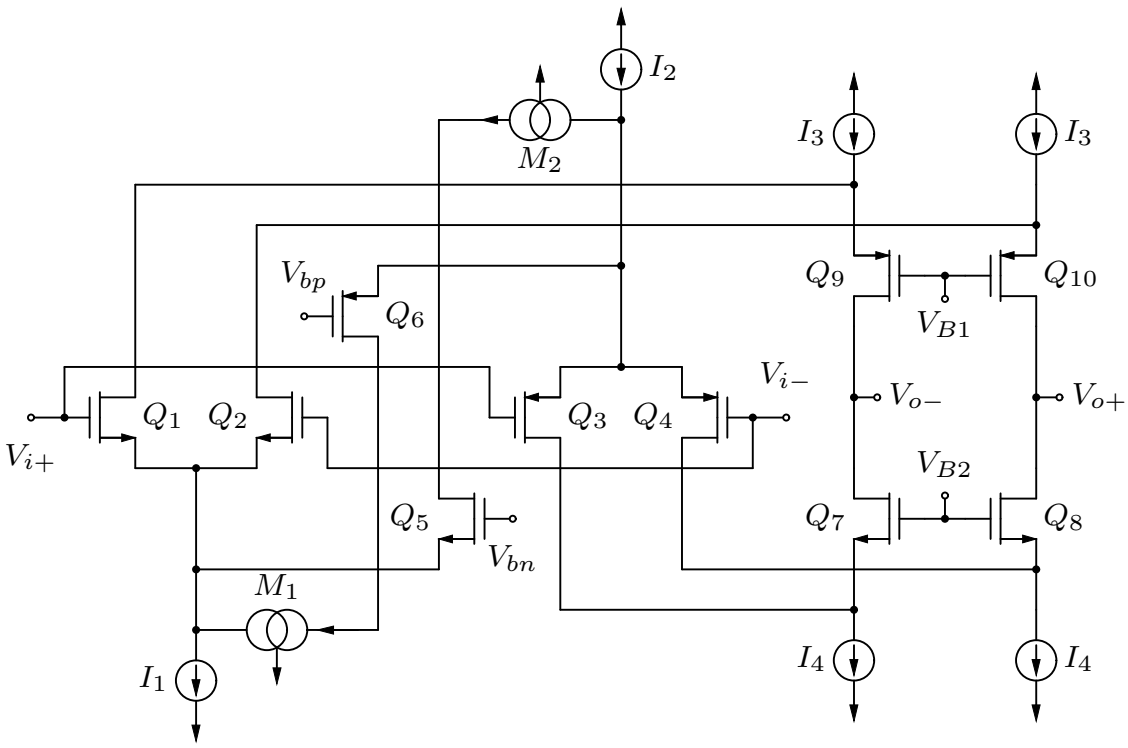


Balanced differential output



Implementation

❏ A fully differential opamp having rail-to-rail ICMR: $\Delta G_m < 15\%$



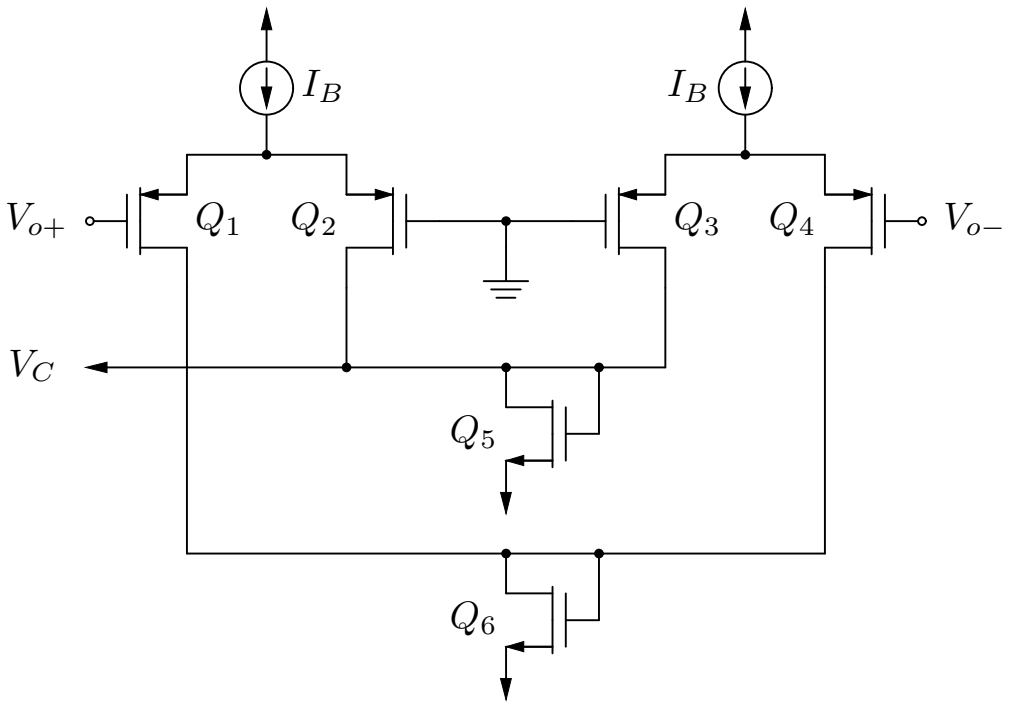
Common-Mode Feedback Circuits

- The CMFB circuitry is often the most difficult part of the opamp to design → two approaches (continuous time, switched capacitor)
- Continuous-time approach: limitation on signal swing, dependence of CM voltage V_{CM} on signal due to finite CMRR, circuit nonlinearity, and device mismatch → unstability of common-mode loop
- For input differential signal V_d, $I_{D1} = I_{D3}$ and $I_{D2} = I_{D4}$ assuming $V_{CM} \equiv (V_{o+} + V_{o-})/2 = 0$, CMRR $= \infty$ (I_D depends only on V_d)

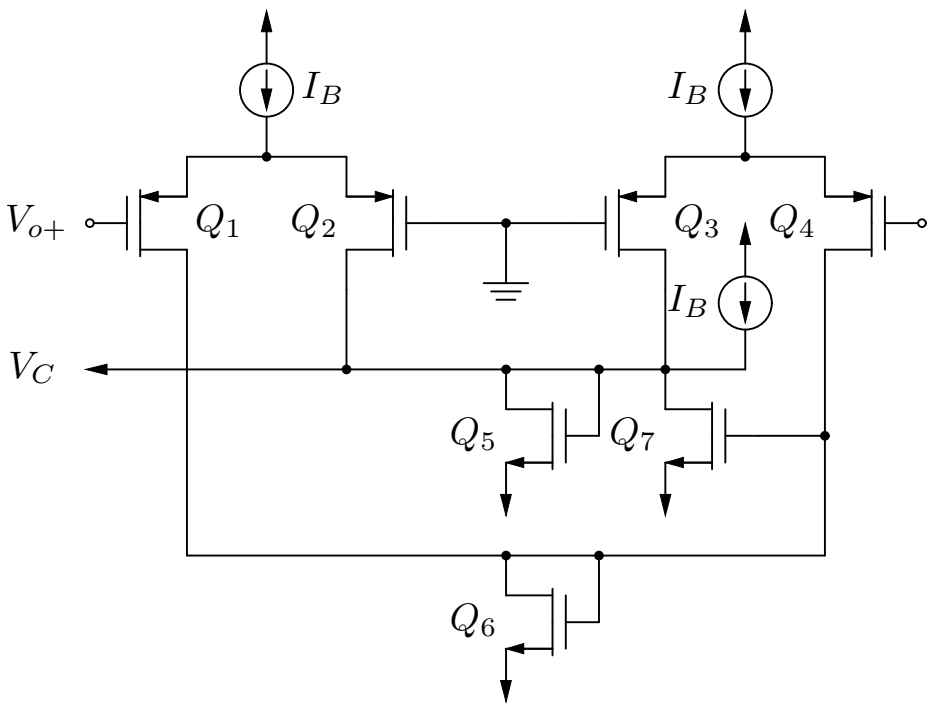
$$I_{D5} = I_{D2} + I_{D3} = (I_B/2 + \Delta I) + (I_B/2 - \Delta I) = I_B$$

Thus I_{D5} will not change even when large differential signal voltages are present. If V_C is used to control the bias voltages of the output stage, the bias currents in the output stage will be independent of whether the input differential signal is present or not.

- A continuous-time CMFB circuit: $V_{CM} = 0$, V_C = control voltage

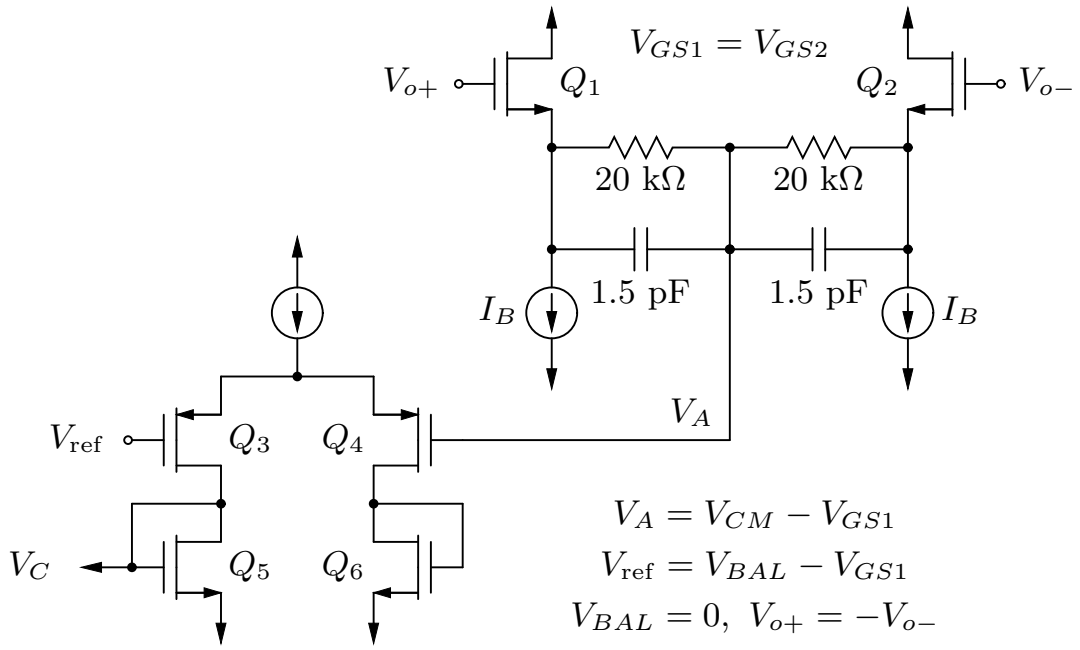


- If a positive CM voltage is present, this voltage will cause both I_{D2} and I_{D3} to increase, which causes V_C to increase. This voltage will increase the current of nMOS current sources at the output stage, which will cause the CM voltage to decrease and return to zero.
- A modified CMFB circuit having twice the common-mode gain and 0.01% linearity. If a positive common-mode voltage is present, the drain current of Q_5 will be $I_B + 4\Delta I$ instead of $I_B + 2\Delta I$.
- A alternative continuous-time CMFB circuit: less signal swing due to dc level shift, more difficult to compensate owing to additional nodes.
- The phase margin and step response of the common-mode loop should be verified by simulation for unstability by CM signals.
- Designing continuous-time CMFB circuits that are both linear and operate with low supply voltage is an area of continuing research.



- A modified CMFB circuit having twice the common-mode gain

❑ A continuous-time CMFB circuit with accurate output balancing: $V_{CM} = V_{BAL}$, linear detection of V_{CM} by two identical resistors

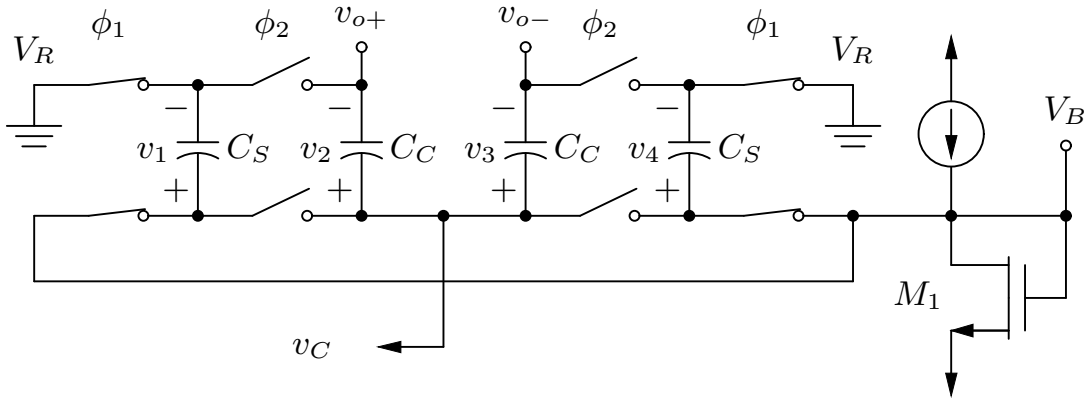


A Switched-Capacitor CMFB Circuit

❑ Use for larger output signal swing and linear detection of V_{CM}

❑ Capacitors C_C generate the average V_{CM} of the output voltages.

❑ This circuit acts like a simple RC low-pass filter having a dc input signal V_B: in steady state $v_C = V_{CM} + V_B$, $C_S = (0.1 - 0.25)C_C$



Analysis of Switched-Capacitor CMFB Circuit

- Analysis by conservation of charge: $q(\phi_1) = q(\phi_2)$
- Phase ϕ_1: $v_1' = v_4' = V_B - V_R, \quad v_C' = v_{o+}' + v_2' = v_{o-}' + v_3'$
- Phase ϕ_2: short ($v_1 = v_2$, $v_3 = v_4$), steady state ($v_2' = v_2$, $v_3' = v_3$)

$$C_S v_1' + C_C v_2' + C_C v_3' + C_S v_4' = C_S v_1 + C_C v_2 + C_C v_3 + C_S v_4$$

$$2C_S(V_B - V_R) + C_C(v_2 + v_3) = (C_C + C_S)(v_2 + v_3)$$

$$v_2 + v_3 = 2(V_B - V_R), \quad v_C = v_{o+} + v_2, \quad v_C = v_{o-} + v_3$$

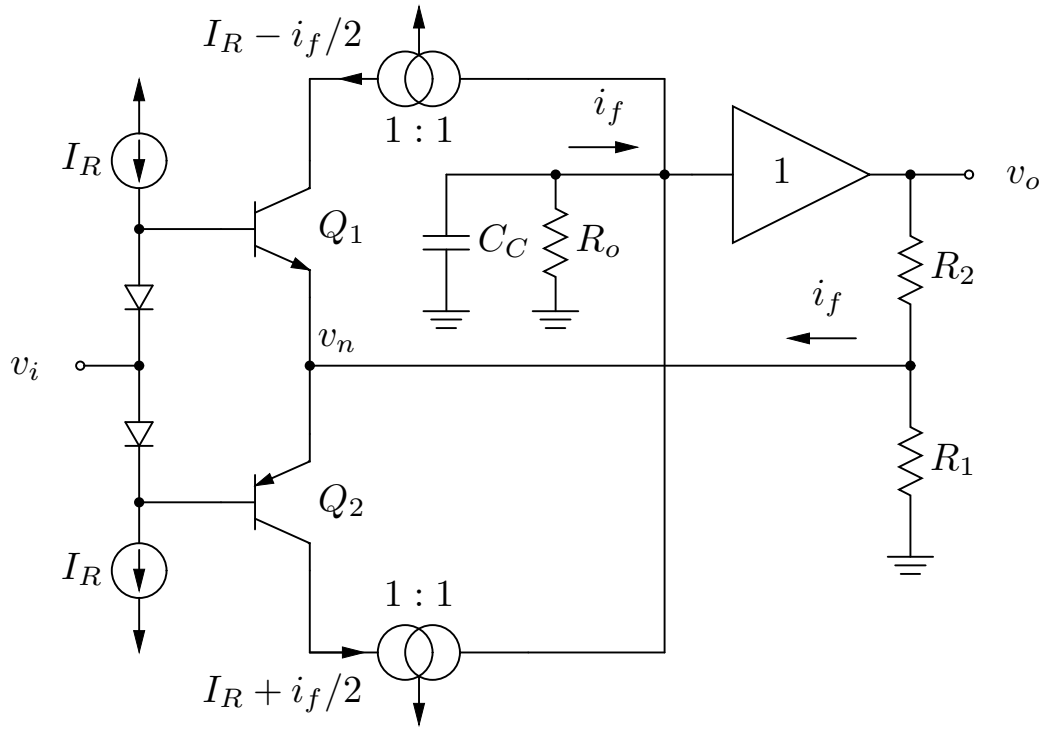
$$\therefore v_C = \frac{v_{o+} + v_{o-}}{2} + V_B - V_R \quad \rightarrow \quad V_{CM} + V_B - V_R$$

$$\therefore v_C' = \frac{v_{o+}' + v_{o-}'}{2} + V_B - V_R \quad \rightarrow \quad V_{CM} + V_B - V_R$$

Current-Feedback Opamps

- Popular recently in high gain and high speed applications using complementary bipolar technology → CMOS technology
- Feedback gain can be changed without significantly affecting loop gain → a single compensation capacitor can be used irrespective of gain.
- The input signal v_i is applied to a high-impedance input, while a feedback current i_f connects to a low-impedance node v_n.
- The voltage v_n is equal to the input signal v_i due to the class-AB unity-gain buffer of Q_1, Q_2, and two diodes for biasing.
- Because R_o is very large, a small feedback current i_f results in a large output voltage $v_o \rightarrow i_f \simeq 0$ for a finite output voltage.

❏ A current-feedback opamp: $v_i \simeq v_n$, $i_f \simeq 0$



❏ Voltage gain: $i_f \simeq 0$, $v_i \simeq v_n = v_o R_1/(R_1 + R_2)$

$$\frac{v_o}{v_i} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$$

❏ Loop gain: breaking the loop and injecting a test signal v_t at the top of R_2 ($i_f = v_t/R_2$ for $v_i = 0$) → loop gain is independent of R_1

$$A\beta \equiv -\left.\frac{v_o}{v_t}\right|_{v_i=0} = -\frac{i_f}{v_t}\frac{v_o}{i_f} = -\frac{1}{R_2}\frac{-1}{sC_C + 1/R_o} = \frac{R_o/R_2}{1 + sR_oC_C}$$

❏ Unity-gain frequency of the loop gain $A\beta$: $\omega_t \simeq 1/R_2C_C$

❏ Transfer function: $i_f = (v_o - v_i)/R_2 - v_i/R_1$, $v_o = -i_f(R_o \parallel C_C)$

$$i_f = \frac{-v_i(R_1 + R_2)}{R_1R_2 + R_1R_o/(1 + sR_oC_C)}, \quad v_o = \frac{-i_f R_o}{1 + sR_oC_C}$$

$$A_f(s) = \frac{v_o}{v_i} = \frac{i_f}{v_i}\frac{v_o}{i_f} = \frac{(R_1 + R_2)R_o}{(R_2 + R_o)R_1}\frac{1}{1 + sC_C(R_2 \parallel R_o)}$$

❏ Bandwidth: $R_o \simeq g_m r_o^2/4 \gg R_2$

$$A_f(s) \simeq \frac{R_1+R_2}{R_1}\frac{1}{1+sR_2C_C}, \quad \therefore\ \omega_{3\text{dB}} = \frac{1}{R_2C_C} = \omega_t$$

❏ The various closed-loop gains can be realized by changing R_1 without affecting the unity-gain frequency or the closed-loop stability.

❏ This independence of gain on stability does not occur for voltage-feedback amplifiers: $A_f(s) \simeq 1/\beta(1+s/\beta\omega_{ta})$, $\omega_t = \beta g_m/C_C$

❏ Limitations: $R_1 \gg 1/(g_{m1}+g_{m2})$, use of a purely resistive feedback network, but difficult to compensate if reactive components are used in the feedback network, noiser for Darlington-pair input stage.

❏ Regardless of these limitations, CFOs exhibit excellent high-frequency characteristics and are quite popular in many video and telecommunications applications.

Homework & Project

❏ Problems: 6.1, 6.2, 6.7, 6.10, 6.24.

❏ Design a fully-differential CMOS operational amplifier for the following specifications.

Performances	Specifications	Performances	Specifications
Power supply	±2.5 V	Input CMR	±1 V
C_L	0.5 pF	Output swing	±1 V
DC gain	60 dB	Settling time	15 ns

The design objective is minimizing the power dissipation. Explain why you chose your architecture over alternatives. Draw a circuit schematic with all device sizes. Include the design procedure and the calculation of design parameters. Provide simulation results for verification.