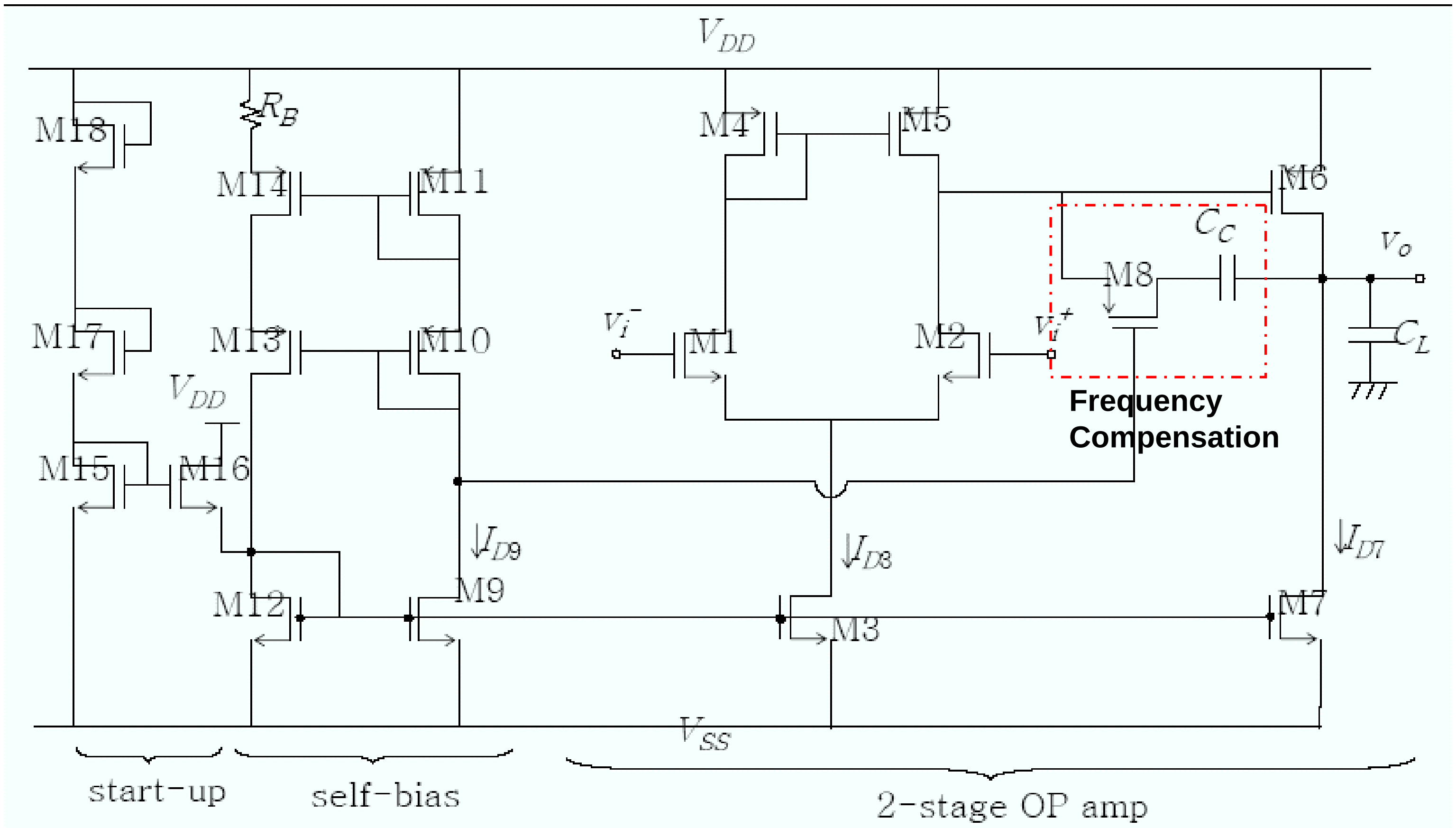
Today's agenda (11-FEB-2010)

- Thanks for participation in the design review (get some idea of process)
- Today's lecture brief – more time for addressing design-specific questions
- Specification review on Tuesday (suggest something like 1 slide each)
  - Problem specification
  - Key features/design issues
  - Block diagram
  - Table of Specifications
  - Preliminary list of specific simulations needed

Suggested Milestones

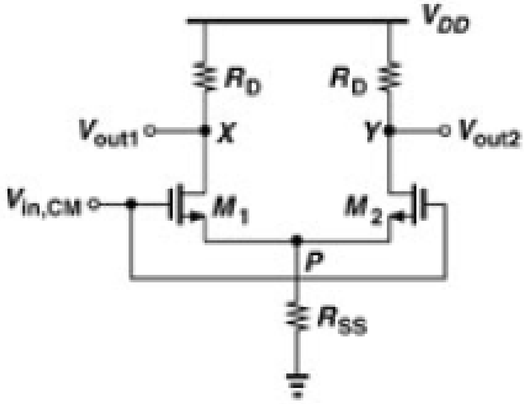
- Specification Review [Feb 16]
  - Block diagram
  - Table of key parameters
- Design Readiness Review [March 1-14]
  - Design simulations, iteration
  - Confirmation of key parameters
- Begin Layout [March 15]
  - Floorplanning
  - All April to complete layout
  - LVS checks during hierarchy build
  - Post layout simulations
- Final Design Review [early May]
  - Compile documentation, hold review
  - Final confirmation of key parameters

2 Stage OP Amp



[Reminder] Common Mode

- Common Mode Gain



$$\frac{V_{od}}{V_{ic}} = A_{cd} = \frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D$$

- Common Mode Rejection Ratio

$$CMRR = \frac{A_{dm}}{A_{cd}}$$

- Common Mode Input Voltage Range

$$V_{SS} + V_{TN1} + V_{DSAT5} + V_{DSAT1} < V_{IC} < V_{DD} - |V_{DSAT3}| - |V_{TP3}| + |V_{TN1}|$$

2 Stage OP Amp Design

- Design Process
  - Model Parameter Extraction (1/6)
    - kn : 55.84 uA/V2
    - λn : 0.025
    - Vthn : 0.776 V
    - kp : 23.51 uA/V2
    - λp : 0.055
    - Vthp : 0.858 V
  - Assign Current from Power Consumption Spec. (2/6)
    - Power Consumption : 2 mW
    - Total Current : 0.4 mA @ 5V VDD
    - Input Pair : 0.2 mA
    - Second Stage : 0.2 mA

2 Stage OP Amp Design

- Design Process
  - Determine minimum channel length (3/6)
  - Determine channel width (4/6)
    - Determine $W_{1,2}$ from voltage gain spec.

$$\begin{aligned} A_v &= g_{m1,2} \cdot (r_{o2} \| r_{o4}) \\ &= \sqrt{2\beta \frac{W}{L} I_D} \cdot (r_{o2} \| r_{o4}) \end{aligned}$$

    - Determine W_5 & Bias Voltage from power consumption & CM min.

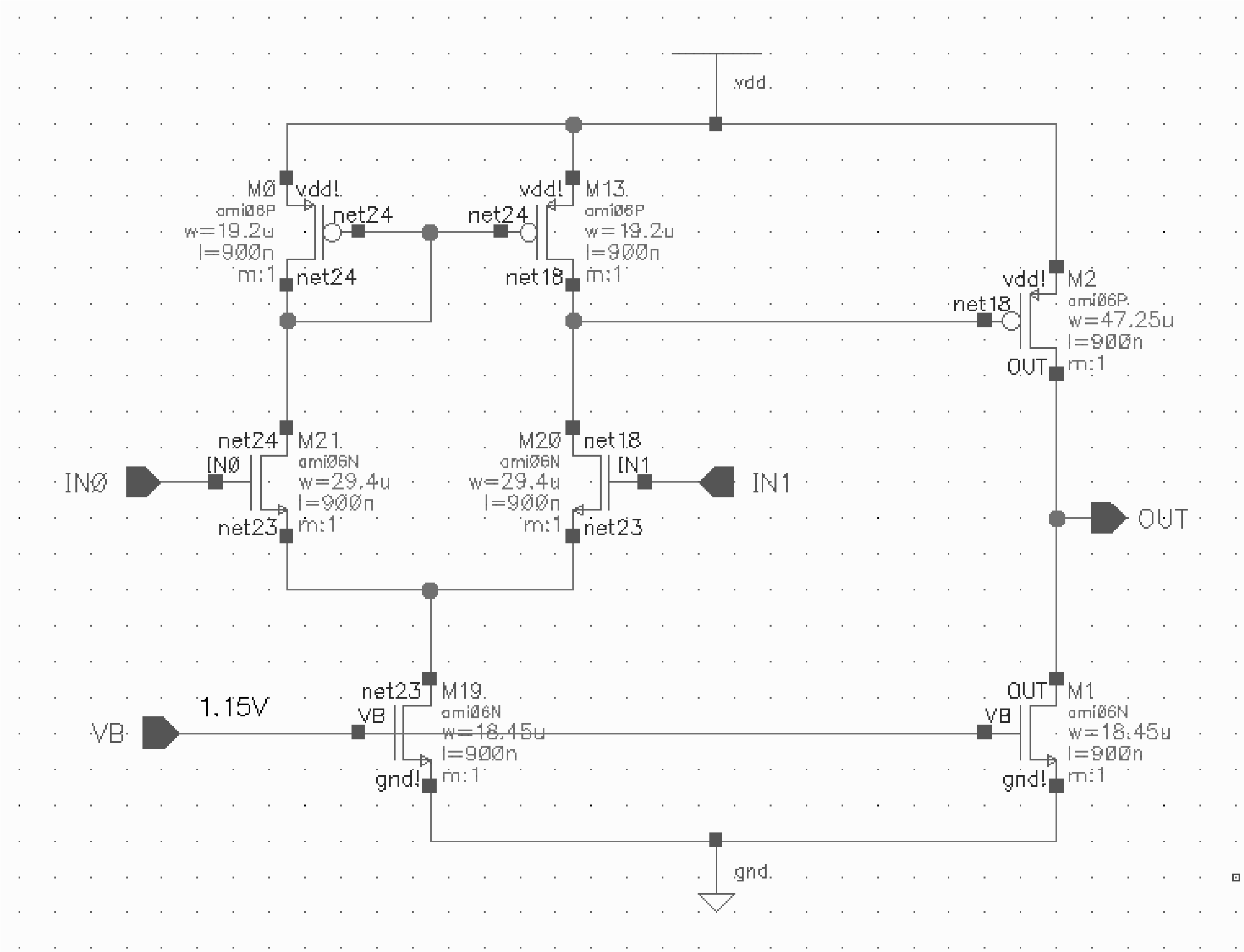
$$\mathrm{V_{SS}} + \mathrm{V_{TN1}} + \mathrm{V_{DSAT5}} + \mathrm{V_{DSAT1}} < \mathrm{V_{IC}}$$

    - Determine $W_{3,4}$ from CM max.

$$\mathrm{V_{IC}} < \mathrm{V_{DD}} - |\mathrm{V_{DSAT3}}| - |\mathrm{V_{TP3}}| + |\mathrm{V_{TN1}}|$$

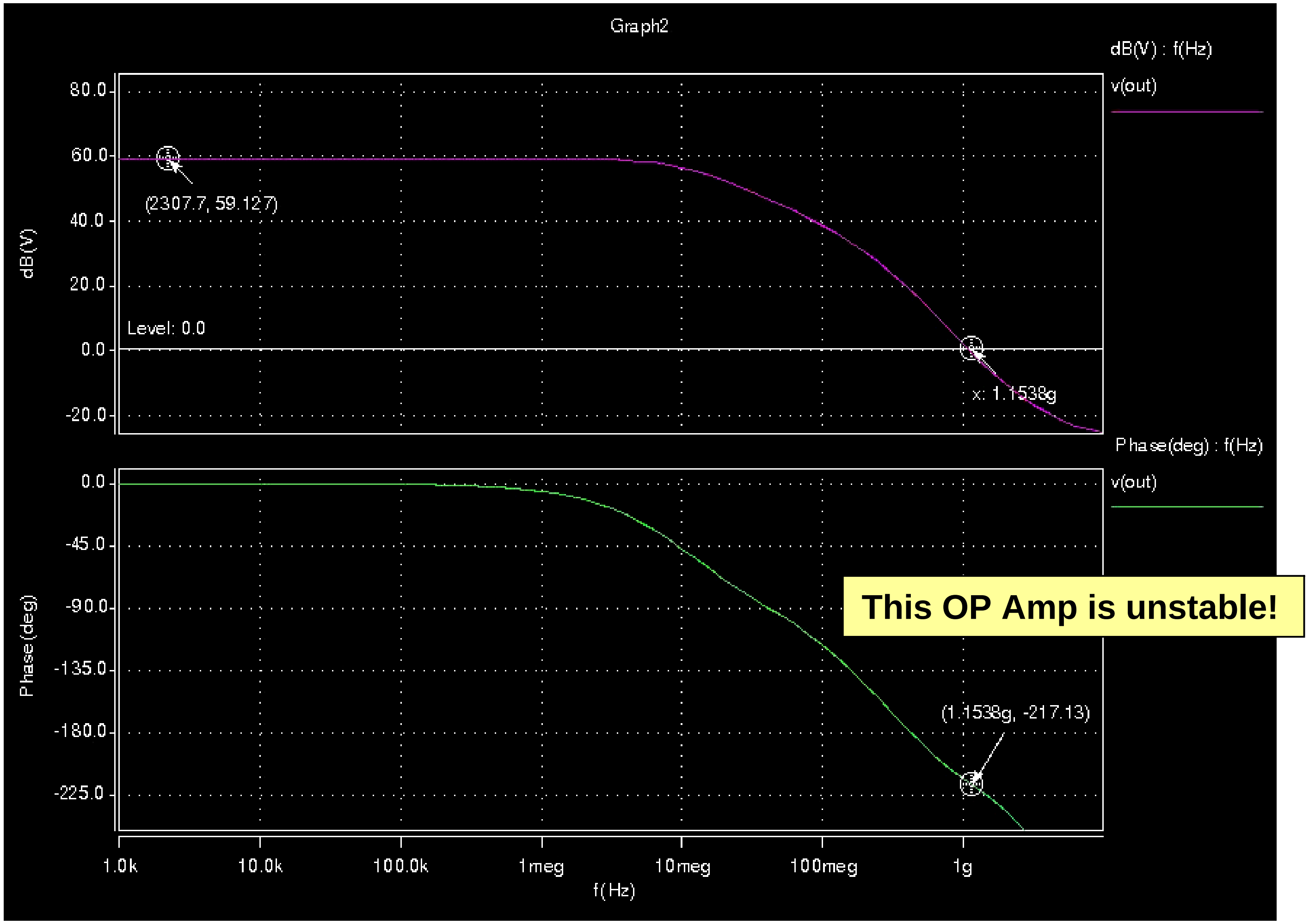
  - Determine Bias Level of Current Source Tr. (5/6)
    - Considering CM min value and the transistor size
  - Check other specifications (6/6)
    - Repeat step 4 to 6

A Calculation Example



Calculated Gain= 3000 (70dB)

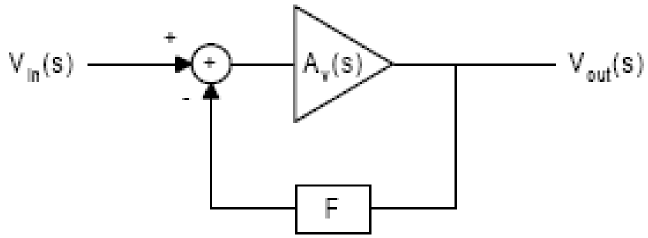
Simulation Results



Gain: 59dB

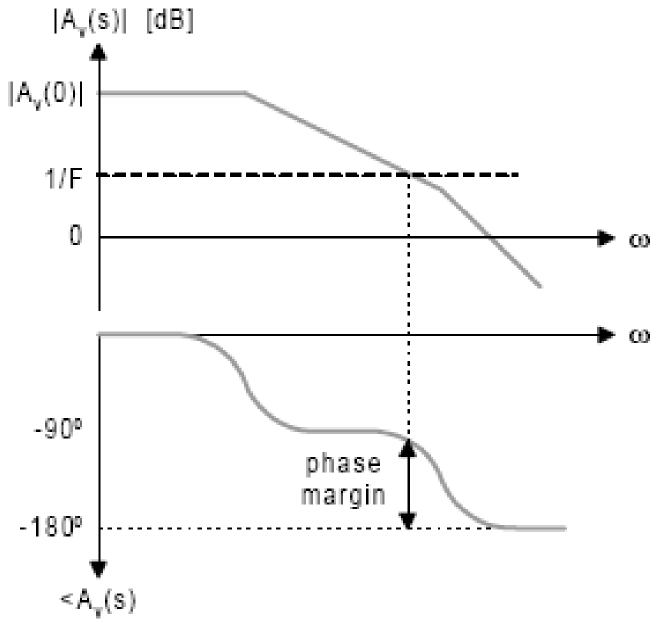
BW: 1.15 GHz

[Reminder] Feedback & Stability



$$A(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{A_v(s)}{1 + F \cdot A_v(s)}$$

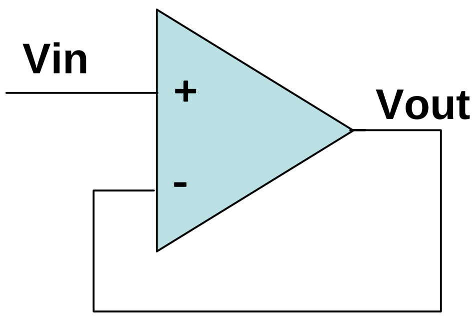
✓ Unstable Condition : $F \cdot A_v(s) = -1$

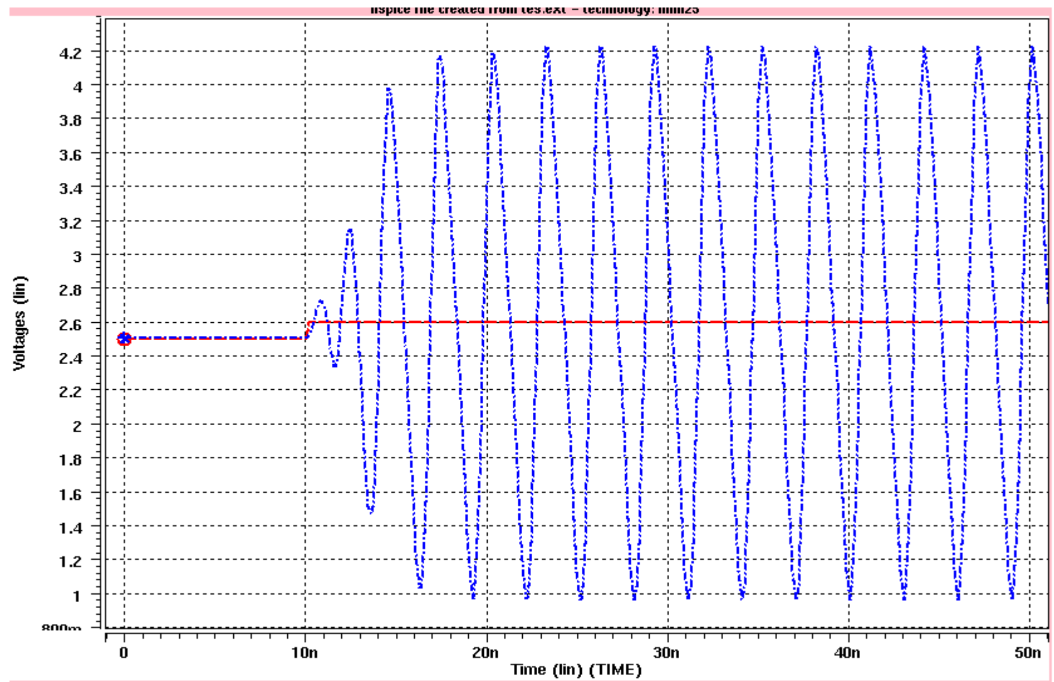


$$|A_v(s)| = \frac{1}{F} \quad \& \quad \angle A_v(s) = -180^\circ$$

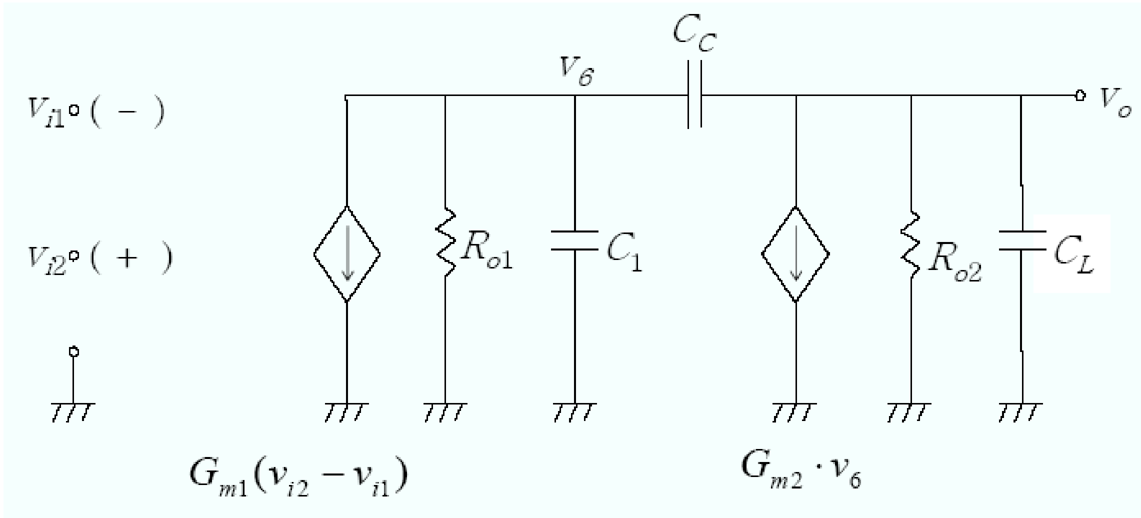
Before Frequency Compensation

- A unit gain buffer characteristic without frequency compensation





Frequency Analysis



KCL at v6 and vo nodes

$$G_{m1}\cdot(v_{i2}-v_{i1})+\left\{s(C_1+C_C)+\frac{1}{R_{o1}}\right\}\cdot v_6-sC_C\cdot v_o=0$$

$$(G_{m2}-sC_C)\cdot v_6+\left\{s(C_L+C_C)+\frac{1}{R_{o2}}\right\}\cdot v_o=0$$

(cont'd) Frequency Analysis

$$A_{dv}(s) = \frac{v_o}{v_{i2} - v_{i1}} = \frac{(G_{m1}R_{o1}) \cdot (G_{m2}R_{o2}) \cdot (1 - sC_C/G_{m2})}{\begin{bmatrix} 1 + s \cdot \{C_L R_{o2} + C_1 R_{o1} + C_C \cdot (G_{m2}R_{o2}R_{o1} + R_{o1} + R_{o2})\} \\ + s^2 \cdot \{C_1 C_L + (C_1 + C_L)\, C_C\} \cdot R_{o1}R_{o2} \end{bmatrix}}$$

$$A_{dv}(s) = \frac{A_{dv}(0) \cdot \left(1 - \frac{s}{z_1}\right)}{\left(1 - \frac{s}{p_1}\right) \cdot \left(1 - \frac{s}{p_2}\right)} \approx \frac{A_{dv}(0) \cdot \left(1 - \frac{s}{z_1}\right)}{1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2}}$$

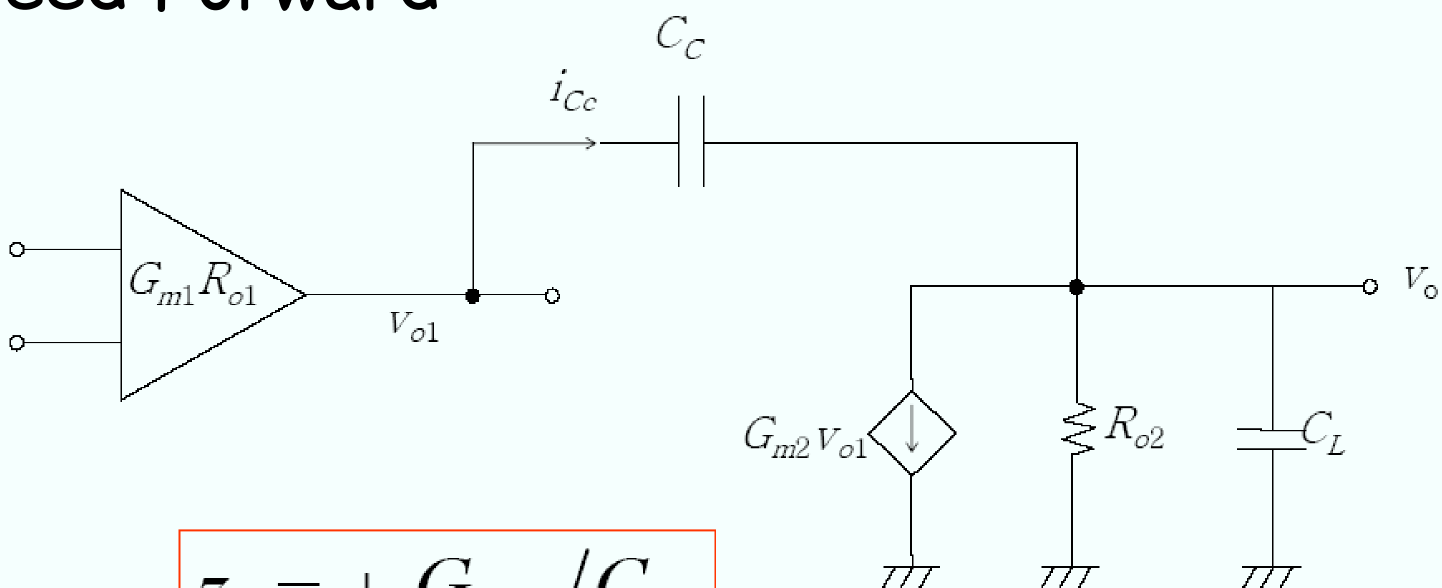
Dominant pole approximation: $|p_1| << |p_2|$

$$\boxed{p_1 = \frac{-1}{C_C \cdot (G_{m2}R_{o2}R_{o1} + R_{o1} + R_{o2}) + C_L R_{o2} + C_1 R_{o1}} \approx \frac{-1}{R_{o1} \cdot G_{m2}R_{o2} \cdot C_C}}$$

$$p_2 = \frac{+1}{p_1 \cdot \{C_C(C_1 + C_L) + C_1 C_L\} R_{o1}R_{o2}} = \frac{-G_{m2}C_C}{C_C(C_1 + C_L) + C_1 C_L}$$

Positive Zero & Pole-Zero Cancellation

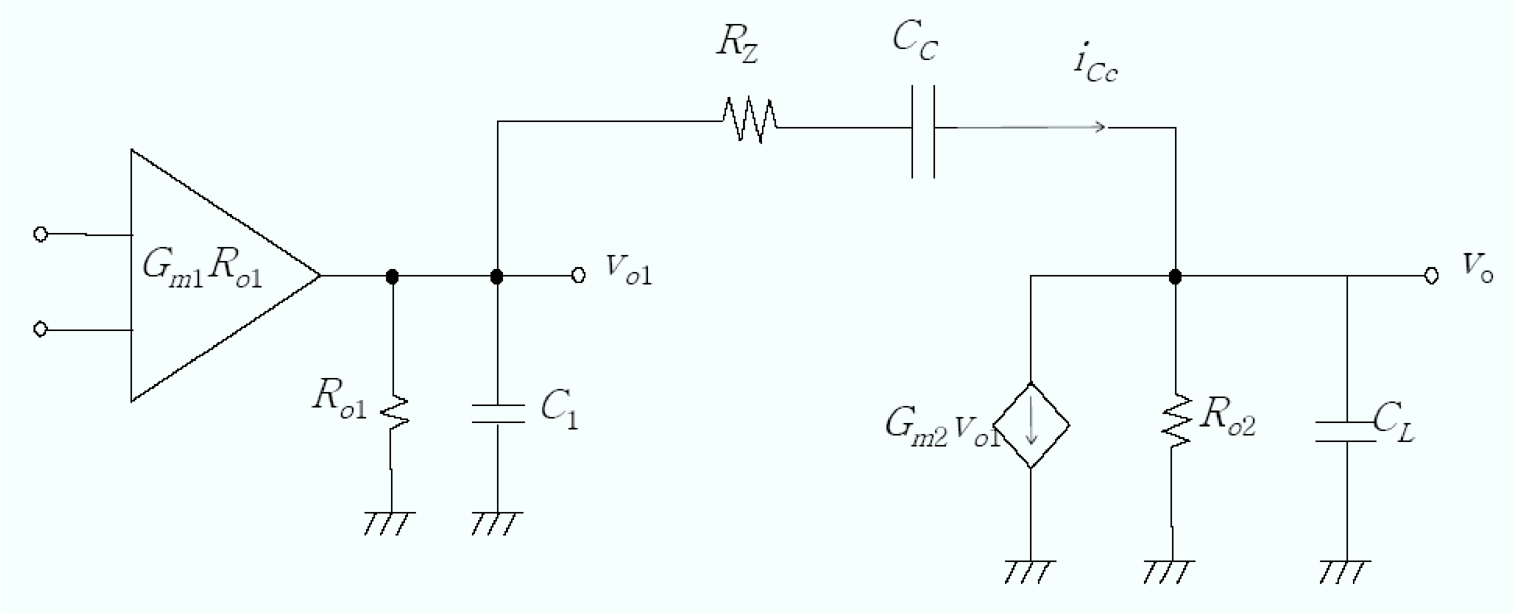
- Feed Forward



$$\boxed{z_1 = +\,G_{m2}/C_C}$$

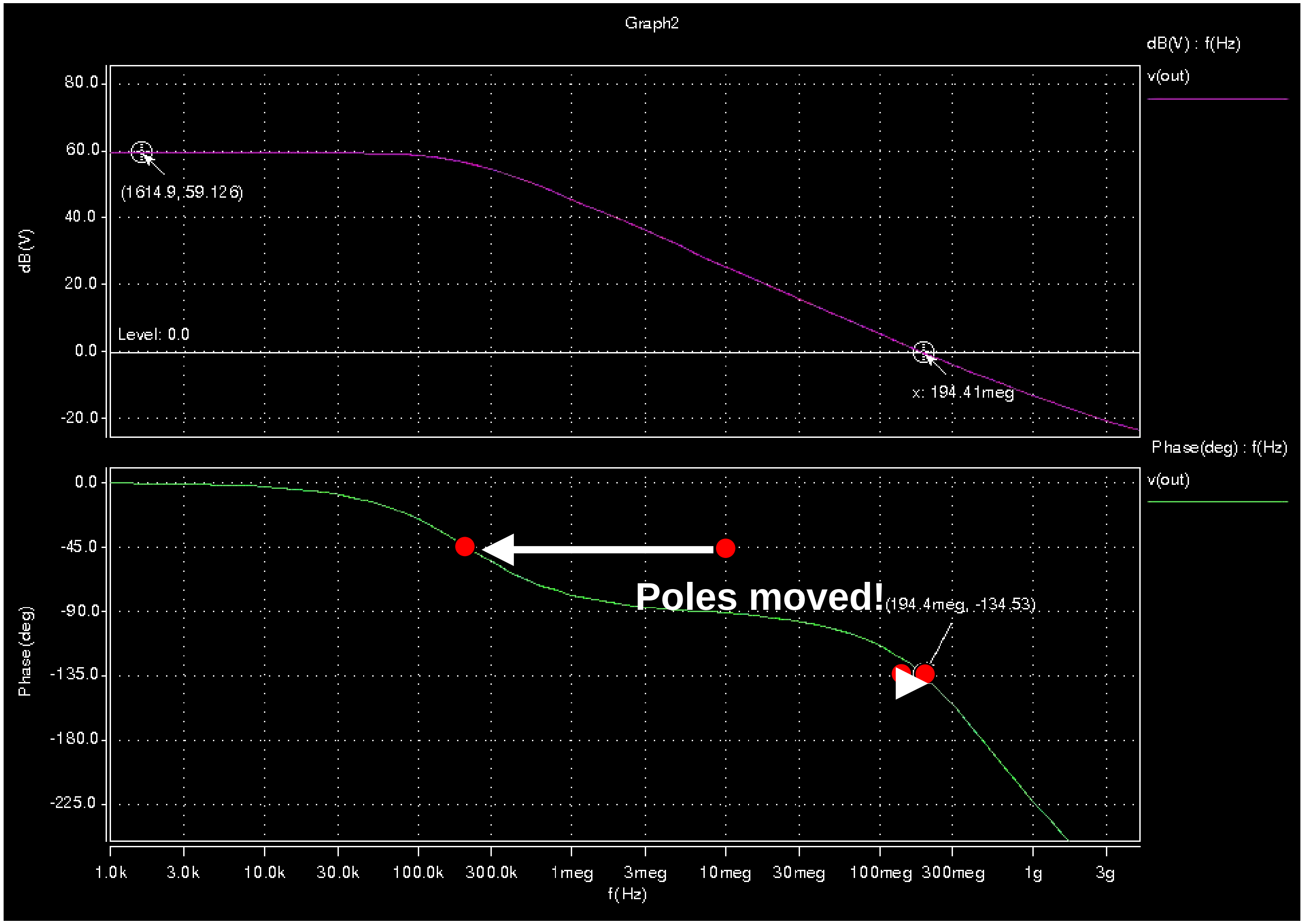
Positive Zero & Pole-Zero Cancellation

- Pole-Zero Cancellation



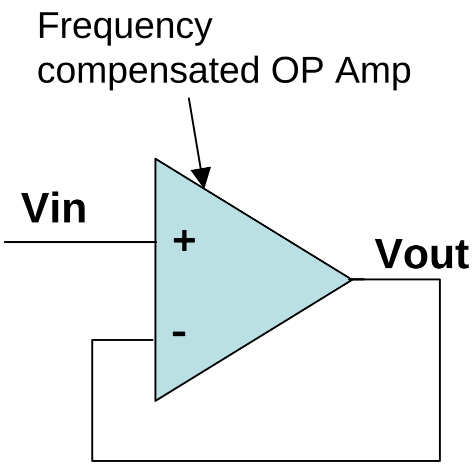
$$z_1 = \frac{G_{m2}}{C_C} \cdot \frac{1}{1 - G_{m2} \cdot R_Z}$$

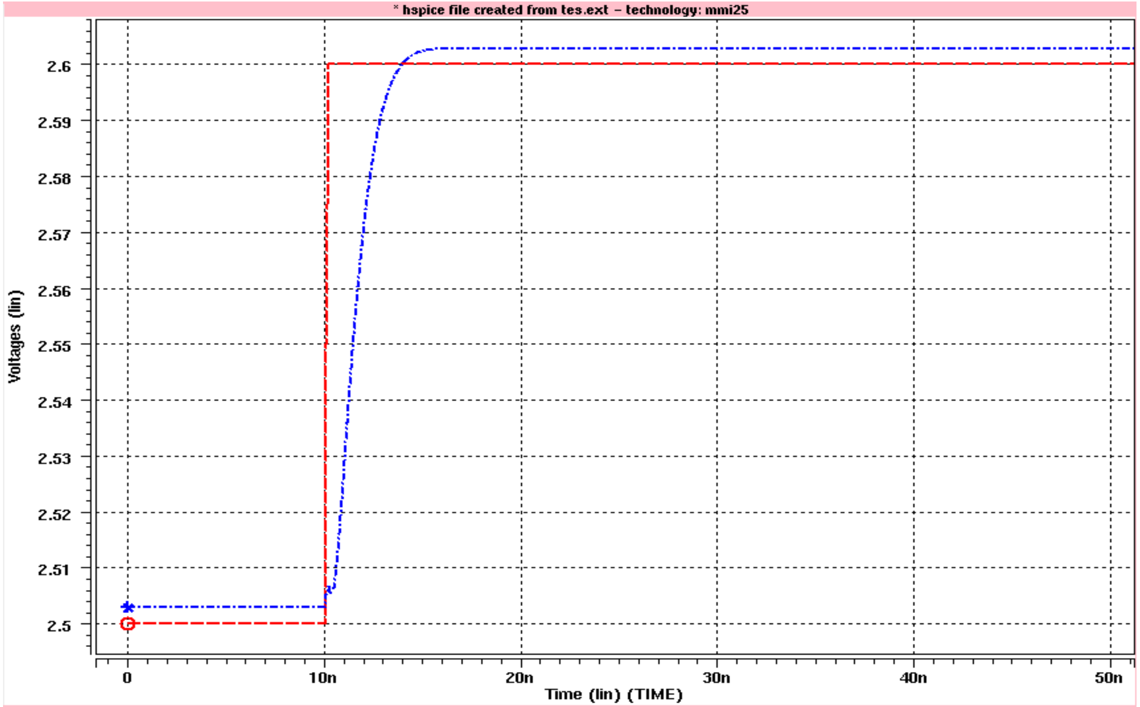
An Example of Frequency Compensation



After Frequency Compensation

- A unit gain buffer characteristic with frequency compensation





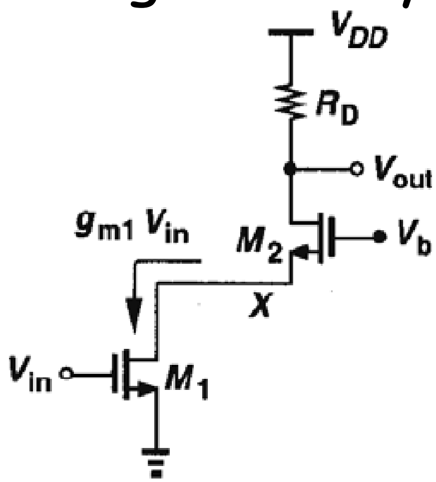
Frequency Compensation must be considered in designing OP Amps

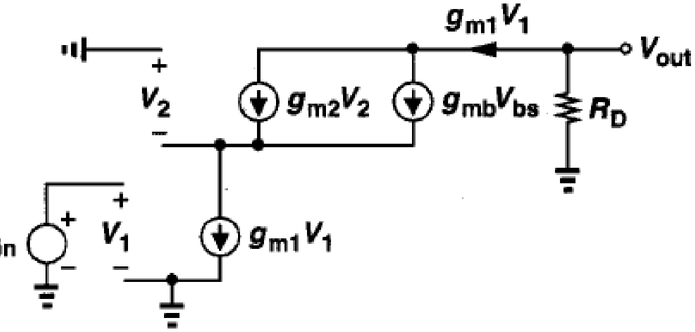
Folded Cascode Op Amp

Basic Folded Cascode
Design of Single Ended Folded Cascode

Cascode Stage

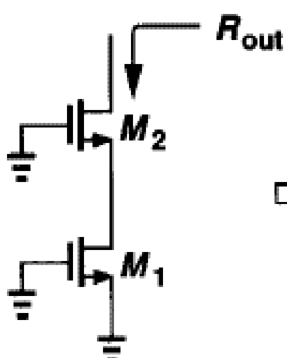
- Small Signal Analysis

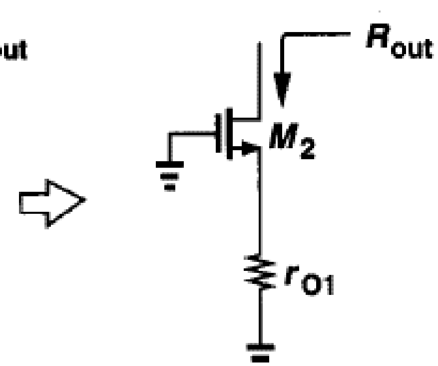




$$V_{out} = (R_{out} \parallel R_D) \cdot g_{m1} V_{in}$$
$$A_v = g_{m1} \cdot (R_{out} \parallel R_D)$$

- Rout

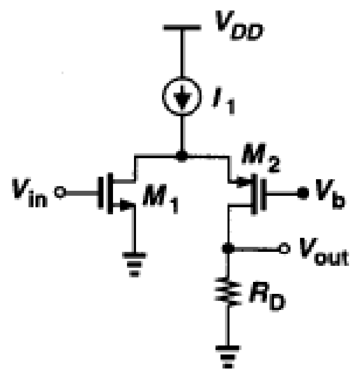




$$R_{out} = r_{o1} \cdot [(g_{m2} + g_{mb2}) r_{o2} + 1] + r_{o2}$$
$$\approx r_{o2} \cdot [r_{o1} \cdot (g_{m2} + g_{mb2}) + 1]$$

Folded Cascode Stage

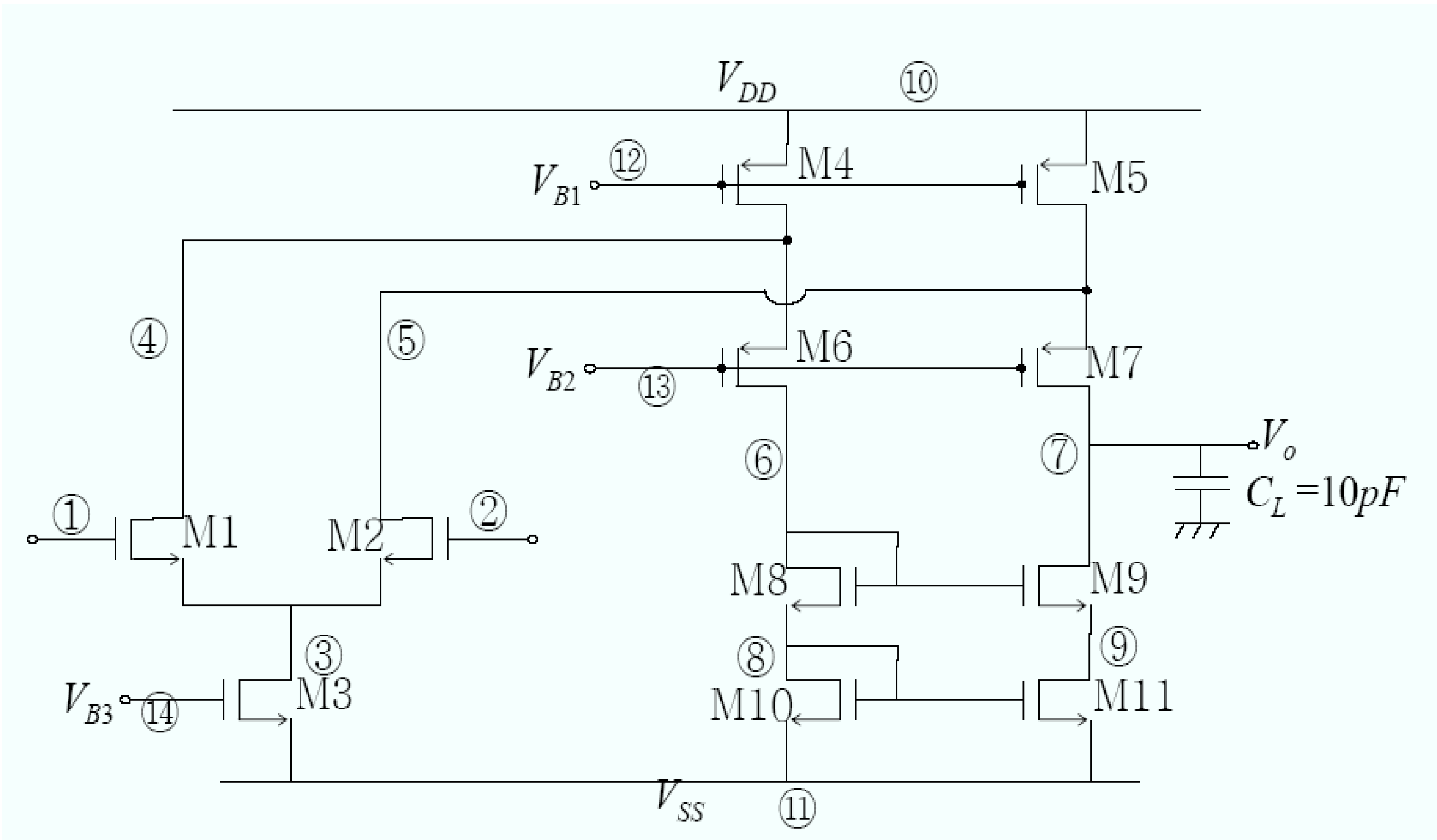
- Schematic



- Advantages
  - Wider Operating Range than telescopic cascode stage
  - Easy to set Common Mode Voltage
- Disadvantages
  - Limited Output swing
  - Large Voltage Headroom
  - Large Power Consumption

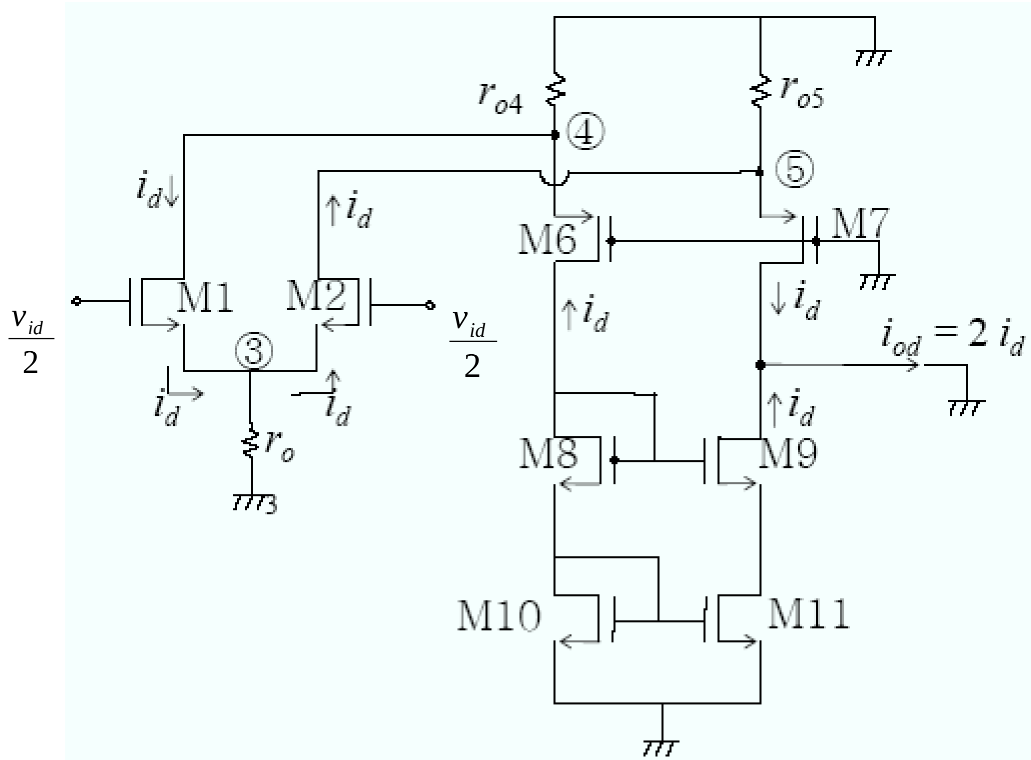
Example Folded Cascode Op Amp

- Circuit Configuration



(cont'd) Folded Cascode Op Amp

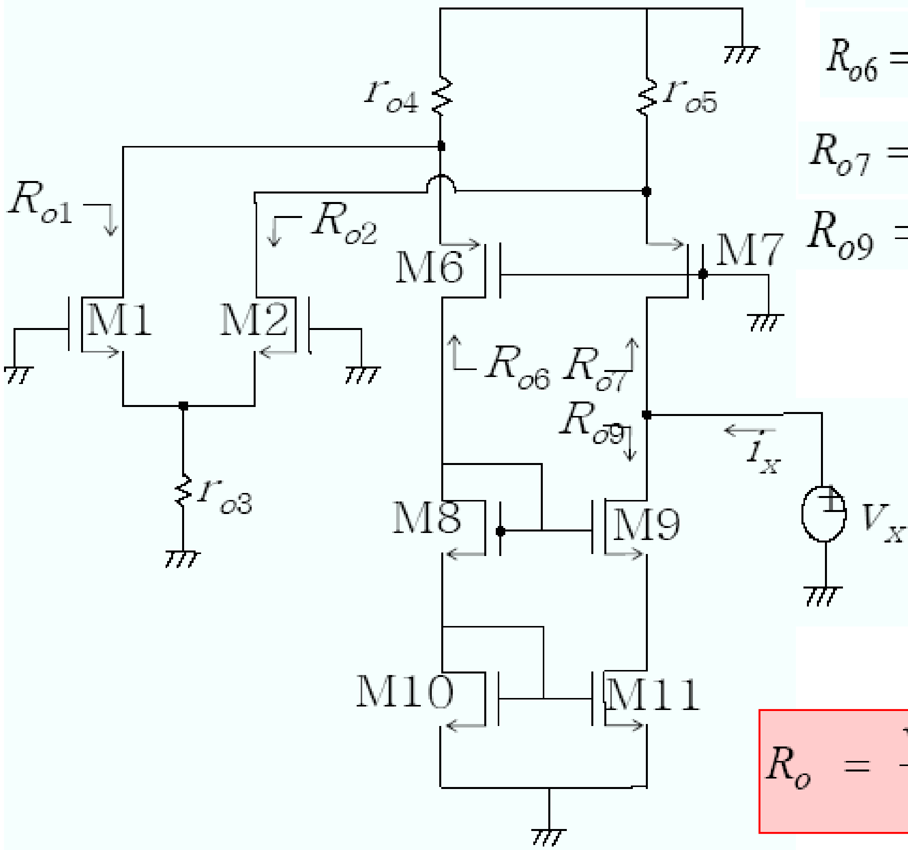
- Gm



$$i_d = \frac{v_{id}}{r_{s1} + r_{s2}} = \frac{1}{2} g_{m1} v_{id}$$

$$\boxed{G_{md} = \frac{i_{od}}{v_{id}} = \frac{2i_d}{v_{id}} = g_{m1}}$$

(cont'd) Folded Cascode Op Amp



$$R_{o1} = g_{m1}r_{o1} \cdot (r_{s2} \| r_{o3}) + r_{o1} + (r_{s2} \| r_{o3}) \approx 2r_{o1}$$

$$R_{o6} = g_{m6}r_{o6} \cdot (R_{o1} \| r_{o4}) + r_{o6} + (R_{o1} \| r_{o4}) \approx g_{m6}r_{o6} \cdot (R_{o1} \| r_{o4})$$

$$R_{o7} = g_{m7}r_{o7} \cdot ((2r_{o2}) \| r_{o5}) = R_{o6}$$

$$R_{o9} = g_{m9}r_{o9} \cdot r_{o11} + r_{o9} + r_{o11} \approx g_{m9}r_{o9} \cdot r_{o11}$$

$$i_x = i_{x7} + i_{x9}$$

$$i_{x7} = \frac{v_x}{R_{o7}} \cdot \left(1 + \frac{r_{o5}}{r_{o5} + R_{o2}}\right) \approx \frac{v_x}{(g_{m7}r_{o7}) \cdot (r_{o2} \| r_{o5})}$$

$$i_{x9} = \frac{v_x}{R_{o9}}$$

$$\boxed{R_o = \frac{v_x}{i_x} = \left\{ g_{m7}r_{o7} \cdot (r_{o2} \| r_{o5}) \right\} \| \left\{ g_{m9}r_{o9} \cdot r_{o11} \right\}}$$

(cont'd) Folded Cascode Op Amp

- Design Process (1/3)
  - Model Parameter Extraction
    - kn : 55.84 uA/V2
    - λn : 0.025
    - Vthn : 0.776 V
    - kp : 23.51 uA/V2
    - λp : 0.055
    - Vthp : 0.858 V
  - Assign Current from Power Consumption Spec.
    - Total Current : 0.375 mA
    - Input pair : 0.125 mA
    - Current mirror : 0.25 mA

(cont'd) Folded Cascode Op Amp

- Design Process (2/3)
  - Determine W3 from CM_min, CM_max Spec.
    - CM_min $\boxed{V_{SS} + V_{DSAT\,3} + V_{GS\,1} = V_{SS} + V_{DSAT\,3} + V_{DSAT\,1} + V_{THn\,1}}$
    - CM_max $\boxed{V_{DD} - \left|V_{DSAT\,4}\right| + V_{THn\,1}}$
  - Determine W4~W7 and Bias2 from Vout_max Spec.
    - Vout_max : $\boxed{V_{B2} + \left|V_{THp\,7}\right|}$ → Determine VB2
    - Assign Vdsat of M4,5 and M6,7 from Vout_max Spec
      - Eg) Vout_max=4V → Vdsat of M4,5= 0.6V, Vdsat of M6,7 = 0.4V
    - Calculate W4~7 to satisfy Vdsat & Ids of M4~7
  - Determine W8~W11 from Vout_min Spec.
    - Assign Vdsat of M8~M11 from Vout_min Spec.
      - Eg) Vout_min=0.8V → Vdsat of M8~11 = 0.4V
    - Calculate W8~11 to satisfy Vdsat and Ids of M8~11

(cont'd) Folded Cascode Op Amp

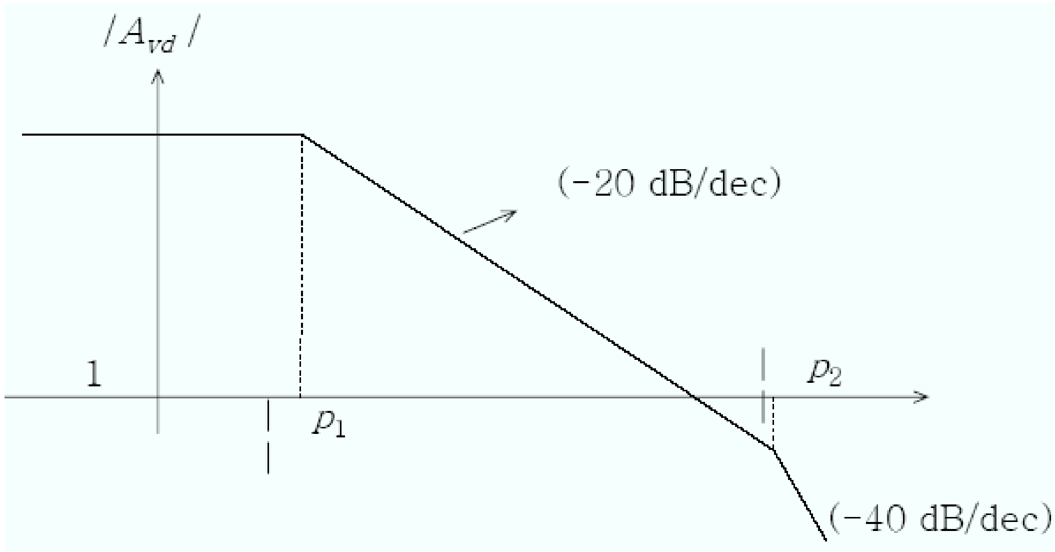
- Design Process (3/3)
  - Determine W1,2 from Gain Spec.
    - Calculate Rout_tot

$$R_o = \frac{v_x}{i_x} = \left\{ g_{m7} r_{o7} \cdot (r_{o2} \| r_{o5}) \right\} \| \left\{ g_{m9} r_{o9} \cdot r_{o11} \right\}$$

    - Calculate Required Gm value to satisfy Gain Spec.
      - Gain = Gm*Rout
    - Calculate W1,2 from Gm
  - Check other Spec. and Repeat the design process to optimize transistors size
    - Slew Rate
    - CM_min Check required
    - CMRR, PSRR
    - Check and Modify Bias Voltage to optimize transistor size.

(cont'd) Folded Cascode Op Amp

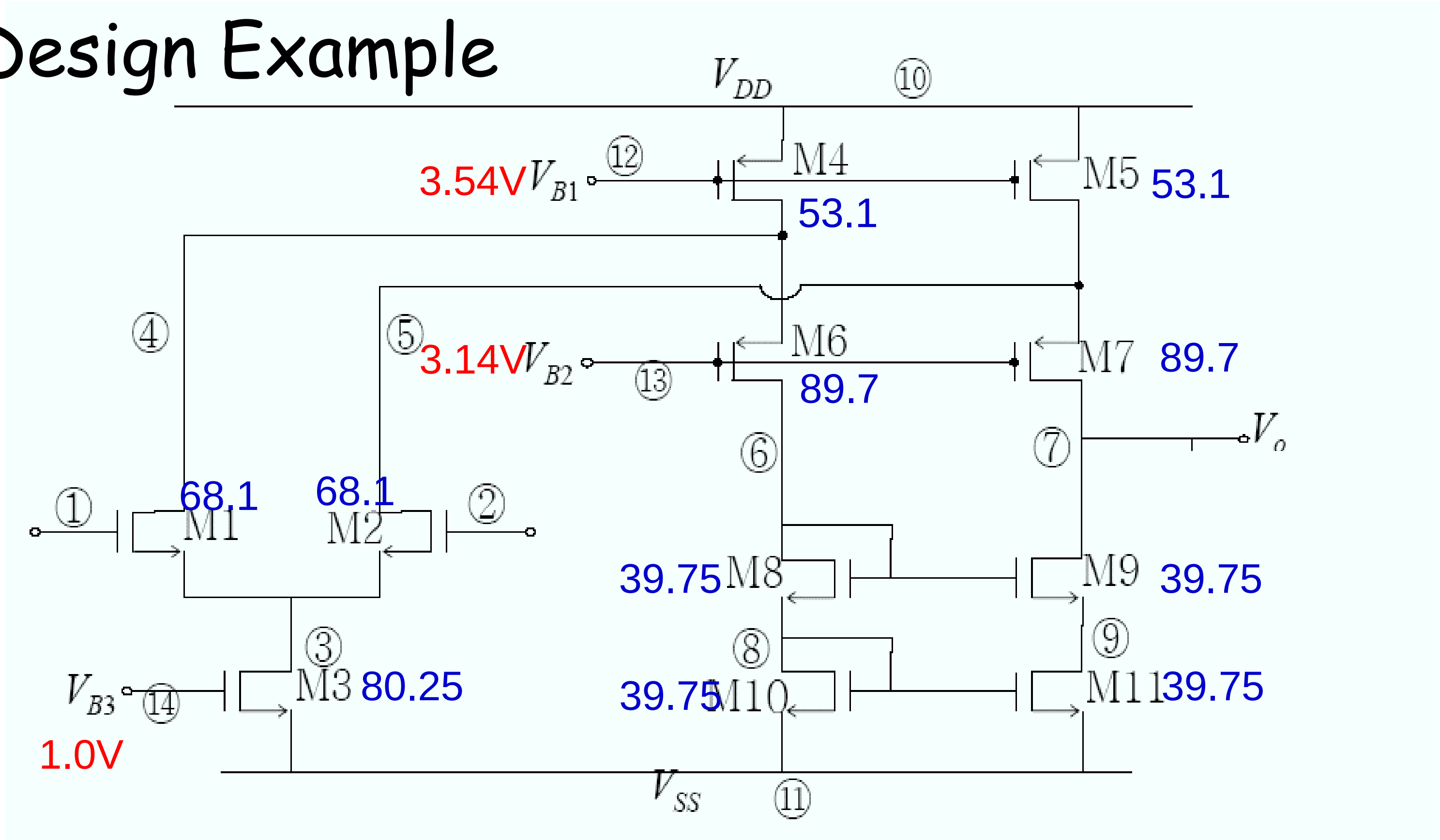
- Frequency Analysis



$$A_{vd} = g_{m1}R_o \qquad |p_1| = \frac{1}{R_o C_L} \qquad \omega_T = \frac{g_{m1}}{C_L} \qquad |p_2| = \frac{1}{r_{s6}C_6}$$

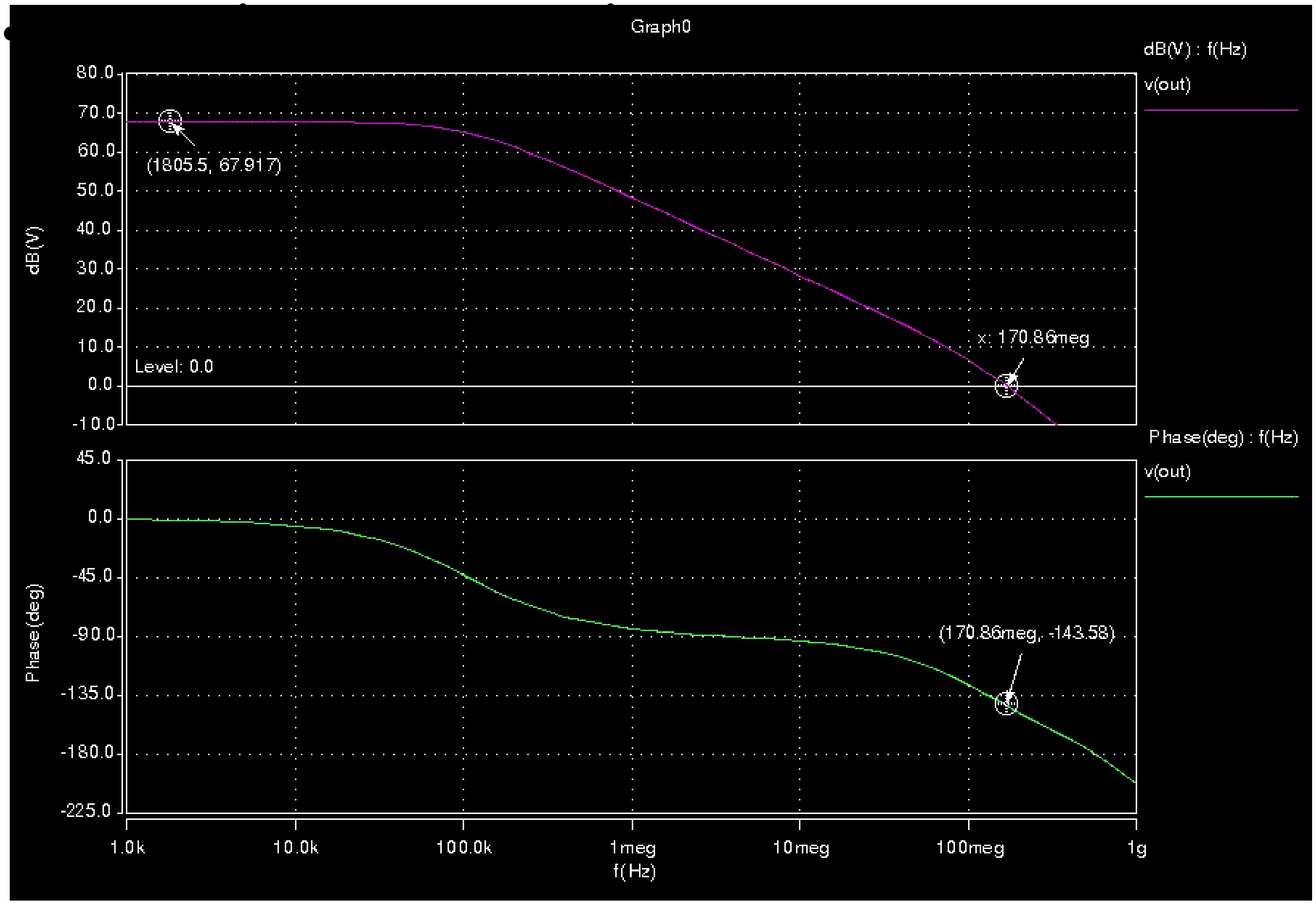
(cont'd) Folded Cascode Op Amp

- Design Example



Calculated Gain= 3000 (70dB)

(cont'd) Folded Cascode Op Amp

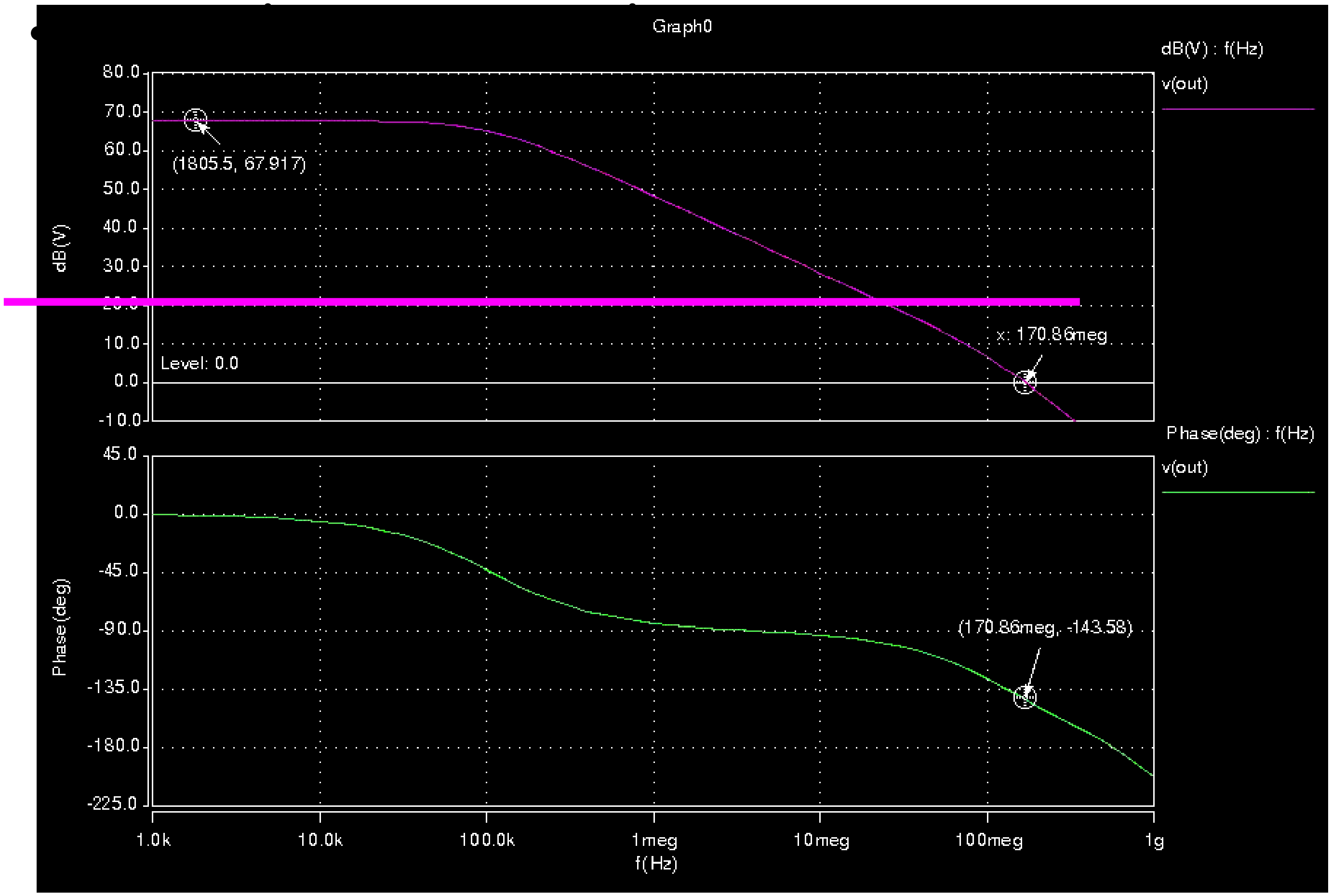


Gain: 68dB

BW: 170MHz

Loading: 2pF

In HEP applications: feedback



Gain: ~20dB

BW: 20MHz

Loading: 2pF

For next time

- Prez Day weekend prep
  - Further theoretical input to your project?
  - All items needed?
  - Schedule?

- Simulation during Lab today
  - Pick a simple circuit element and simulate

- Suggest 5 slides

- Feedback from Mike:
  - He's brought back some information from CERN
  - Future design exercises
  - Next Thursday's lecture