Bias Current Sources

- Applications
- Design objectives
  - Output resistance (& capacitance)
  - Voltage range (V_{min})
  - Accuracy
  - Noise
- Cascoding
- High-Swing Biasing

Matching

- Systematic mismatch
  - ΔV_{DS}
  - source resistance
- Random mismatch
  - Δ (W/L)
  - ΔV_{TH}
  - gradients

Random Mismatch

- Model:
  (assume square-law)

$$I_{D1} = \tfrac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH1})^2$$

$$I_{D2} = \tfrac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH2})^2$$

- Mismatch:
  ΔI_D, $\Delta(W/L)$, ΔV_{TH}

$$\Delta I_D = I_{D1} - I_{D2} \qquad I_D = 0.5(I_{D1} + I_{D2})$$

$$\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2 \qquad \left(\frac{W}{L}\right) = 0.5\left[\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2\right]$$

$$\Delta V_{TH} = V_{TH1} - V_{TH2} \qquad V_{TH} = 0.5(V_{TH1} + V_{TH2})$$

- Substitute:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)} - \frac{1}{2}\frac{\Delta V_{TH}}{(V_{GS} - V_{TH})}$$

- → choose large V_{GS}-V_{TH} (V_{ov})

Mismatch Example

$$\sigma_{\Delta\left(\frac{W}{L}\right)\Big/\left(\frac{W}{L}\right)} = 1\%$$

$$\sigma_{\Delta V_{TH}} = 3\text{mV}$$

$$V_{GS} - V_{TH} = 300\text{mV}$$

- Represent mismatch as random quantities
- Variances (squares!) add … like noise

$$\sigma^2_{\frac{\Delta I_D}{I_D}} = \sigma^2_{\Delta\left(\frac{W}{L}\right)\Big/\left(\frac{W}{L}\right)} + \frac{1}{4}\frac{\sigma^2_{\Delta V_{TH}}}{(V_{GS} - V_{TH})^2}$$

$$= (0.01)^2 + \left(\frac{3}{2\times 300}\right)^2 = (100 + 25)\times 10^{-6}$$

$$= \underline{(1.1\%)^2}$$

- Use large V_{ov} (or degeneration) for good current mirror matching

Yield

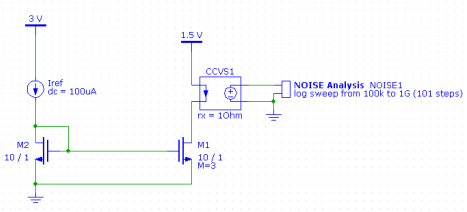
- Yield = fraction of good dies
- E.g. need ±2.2% matching
  σ = 1.1%,
  k = 2.2 / 1.1 = 2

  yield = 0.954 = 95.4%
- Typical design goal:
  ± 3σ (“6σ”), i.e. k=3

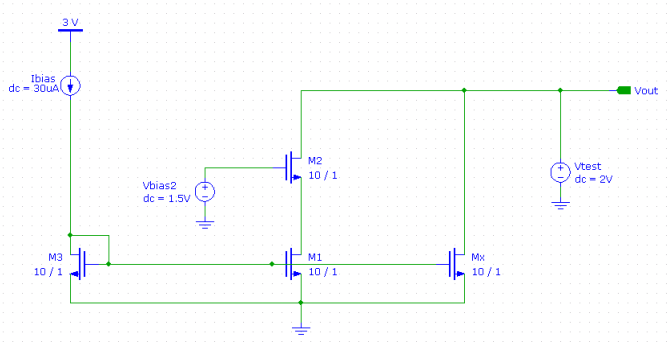
k	Yield
0.2	0.159
0.4	0.311
0.6	0.451
0.8	0.576
1.0	0.683
1.2	0.766
1.4	0.838
1.6	0.890
1.8	0.928
2.0	0.954
2.2	0.972
2.4	0.984
2.6	0.991
2.8	0.995
3.0	0.997

Noise

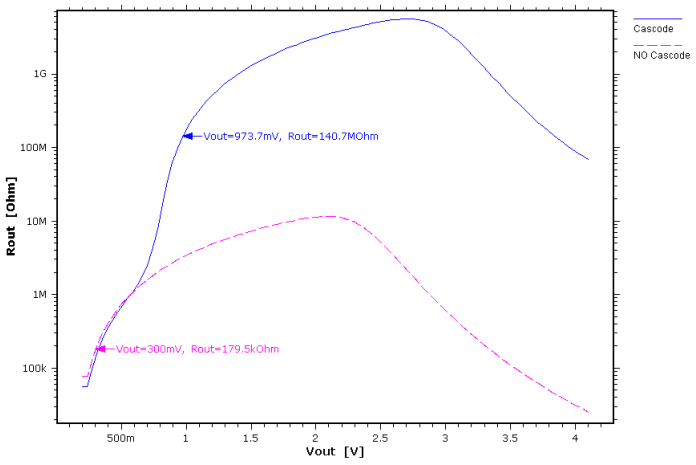
- Current source
  - Active
  - Passive
- Mirror
- Reference generator



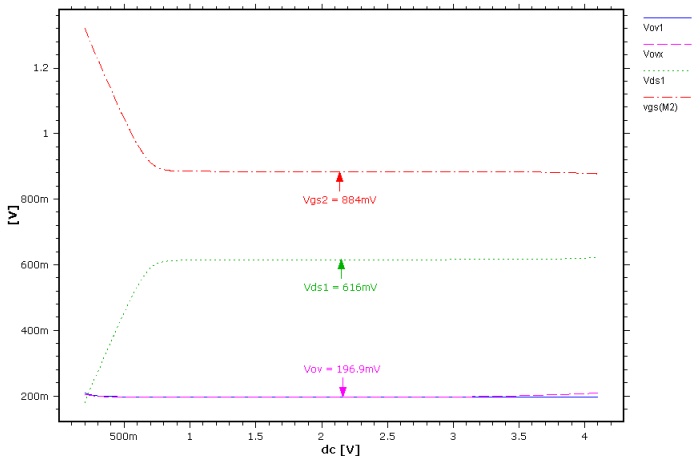
Cascoding



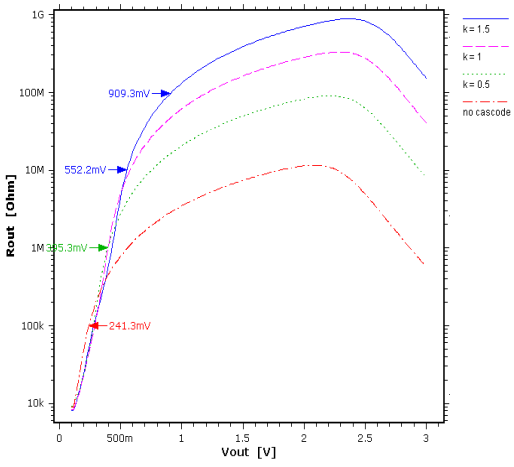
Output Resistance



Bias


Vov1
Vovx
Vds1
vgs(M2)
Vgs2 = 884mV
Vds1 = 616mV
Vov = 196.9mV
[V]
dc [V]

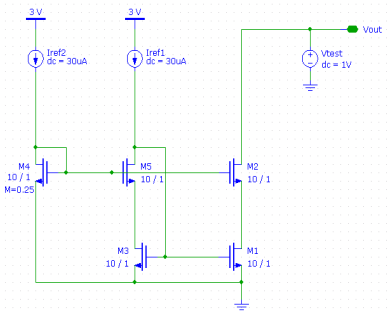
$R_{out} = f(k)$


k = 1.5
k = 1
k = 0.5
no cascode
909.3mV
552.2mV
395.3mV
241.3mV
Rout [Ohm]
Vout [V]

High-Swing Cascode Biasing

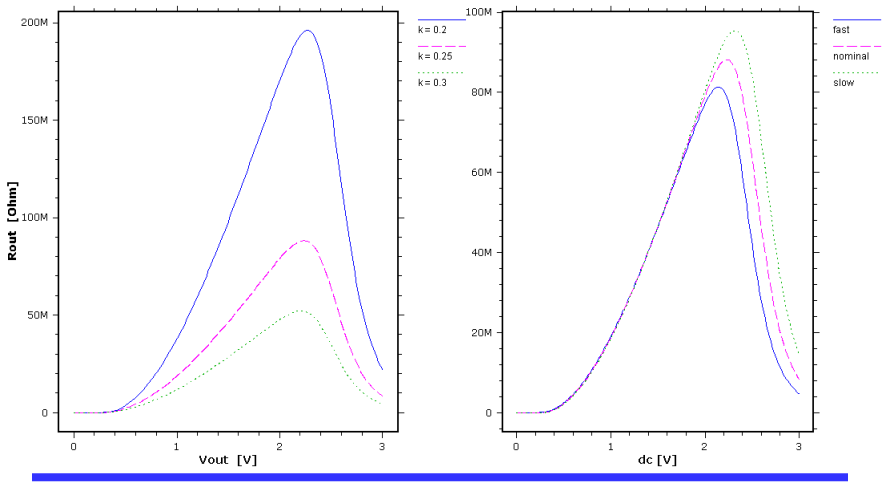
- V_{min} versus R_{out} tradeoff is very steep
  - $V_{min} > 2V_{ov}$ for cascode to be advantageous
- Goal: Set V_{bias} such that $V_{DS1} \approx kV_{ov}$
  - $k > 1$ (typical: 1.3 … 2)
  - Important for high R_{out}
  - No penalty for moderate R_{out}
- Design for insensitivity to
  - Process variations (μ, C_{ox}, V_{TH}, γ, …)
  - Reference current I_{ref}

High-Swing Bias 1

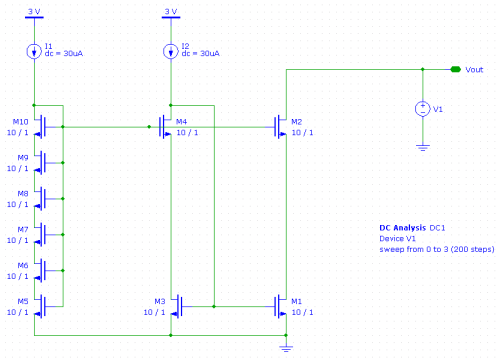


- M_4 quarter size or less (1/5 for high R_{out})
- M_5 sets $V_{DS3} = V_{DS1}$: improves matching
- Sensitive to body-effect
- $L_{current\text{-}source} = L_{cascode}$
- Simple

R_{out}

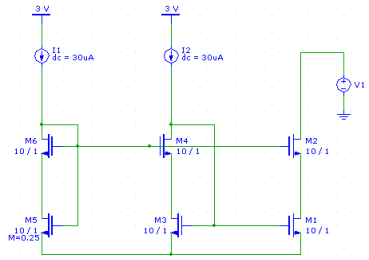


High-Swing Bias 2



- M5 … M10 replace quarter size device
- All devices same size
- Less sensitive to body-effect
- $L_{current\text{-}source} = L_{cascode}$

High-Swing Bias 3



- M_5 in triode & smaller
- All other devices same size
- Sensitive to body-effect
- $L_{current\text{-}source} = L_{cascode}$

Device Sizing

Objective:

$$V_{DS5} = K \times V_{d1}^{sat}$$

Square-law:

$$I_{D5} = \mu C_{ox} m_5 \frac{W}{L}\left(V_{GS5} - V_{TH5} - \frac{V_{DS5}}{2}\right)V_{DS5}$$

$$I_{D6} = \frac{1}{2}\mu C_{ox} \frac{W}{L}\left(V_{GS6} - V_{TH6}\right)^2$$

with

$$I_{D5} = I_{D6}$$

$$V_{GS5} = V_{GS6} + V_{DS5}$$

$$V_{GS6} = V_{TH6} + V_{d6}^{sat} \quad \text{with} \quad V_{d6}^{sat} = V_{d1}^{sat}$$

substitute

$$\left(V_{d6}^{sat}\right)^2 = m_5\left(V_{DS5} + 2V_{d6}^{sat} + 2\Delta V_{TH}\right)V_{DS5}$$

solve:

$$V_{d6}^{sat} = m_5 V_{DS5}\left(1 + \sqrt{1 + \frac{1}{m_5} + \frac{2}{m_5}\frac{\Delta V_{TH}}{V_{DS5}}}\right)$$

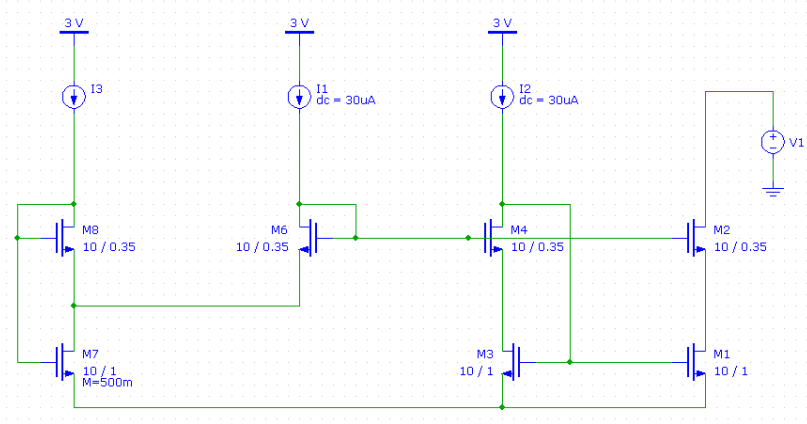
$$K = \frac{1}{m_5\left(1 + \sqrt{1 + \frac{1}{m_5} + \frac{2}{m_5}\frac{\Delta V_{TH}}{V_{DS5}}}\right)}$$

Examples:

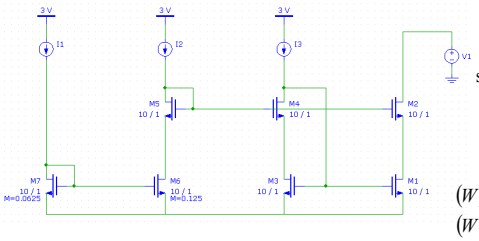
m_5 = 1/3, ΔV_{TH}=0V
K = 1

m_5 = 1/4, ΔV_{TH}=0V
K = 1.55

Different Device Length



High-Swing Bias 4



$$I_{D7} = \tfrac{1}{2}\mu C_{ox}\left(\tfrac{W}{L}\right)_7 \left(V_{d7}^{sat}\right)^2$$

$$I_{D6} = \mu C_{ox}\left(\tfrac{W}{L}\right)_6 \left(V_{d7}^{sat} - \tfrac{1}{2}V_{DS6}\right)V_{DS6}$$

solve:

$$V_{DS6} = V_{d7}^{sat}\left[1-\sqrt{1-m}\right] \quad \text{with} \quad m = \frac{(W/L)_7}{(W/L)_6}$$

e.g.:

$(W/L)_7 = 1/16$ for $V_{d7}^{sat} = 4V_{d1}^{sat}$

$(W/L)_6 = 1/8$ $m = 0.5$

then

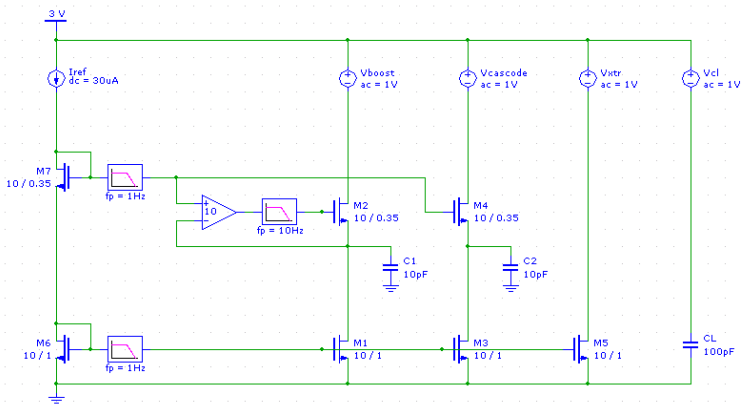
$$V_{DS6} = 0.3V_{d7}^{sat} = 1.2V_{d1}^{sat}$$

- M_6 in triode
- Insensitive to body effect
- Large device ratios
- Need 3 reference sources (increased power dissipation)

Gain Boosting

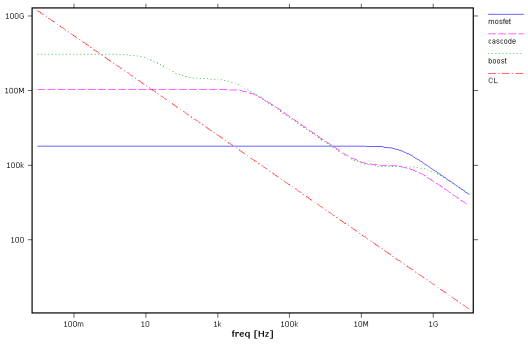
- Use feedback to further increase R_{out}
  - No increase of V_{min} (unlike double cascode)
- Local feedback → potential instability
- Beware of doublets (slow settling)
- Noise enhancement

Gain Boosting Analysis



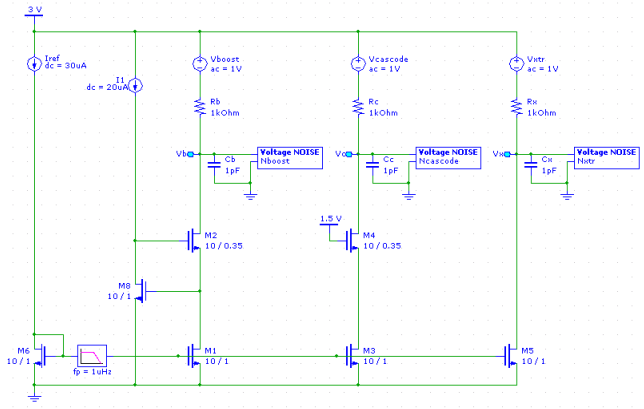
Note: C2 would not be present in an actual circuit (or smaller). It is added here to separate pole frequencies.

Z_{out}

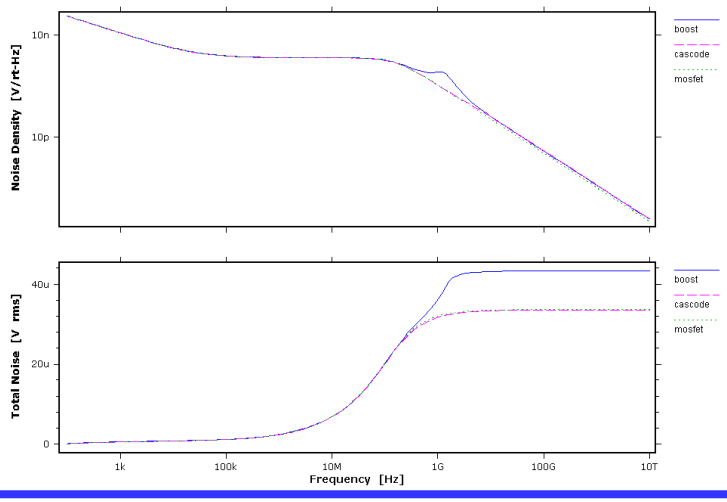


- $Z_{total} = Z_{boost} // Z_{CL}$
- Doublets → slow settling
- Booster bandwidth tradeoff:
  - push doubled above closed-loop bandwidth
  - ensure stability (nondominant pole at source of M_2)

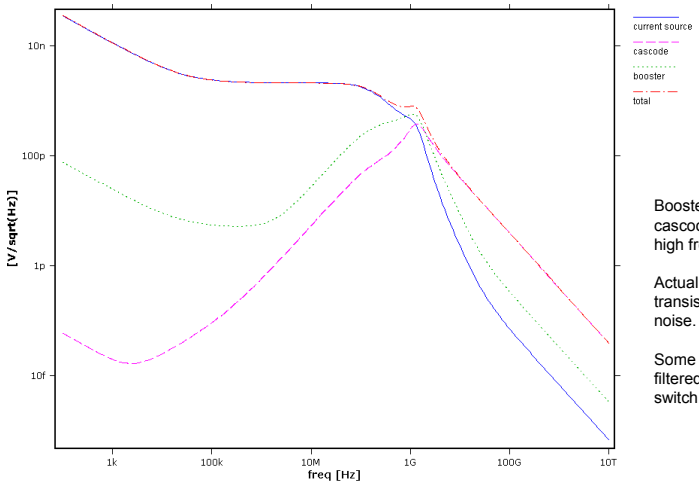
Noise Analysis



Noise Summary



Noise Detail

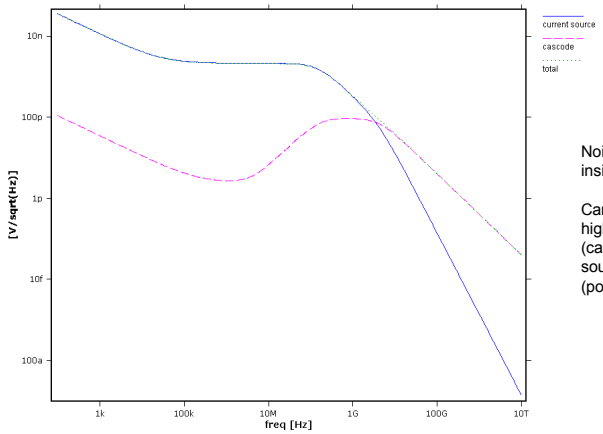


Booster amplifier and cascode contribute noise at high frequency.

Actual boosters have more transistors → additional noise.

Some noise might be filtered out by sampling switch.

Cascode Noise



Noise from cascode usually insignificant.

Can contribute substantially at high frequency with lots of (capacitive) degeneration at the source of the cascode transistor (poor layout).