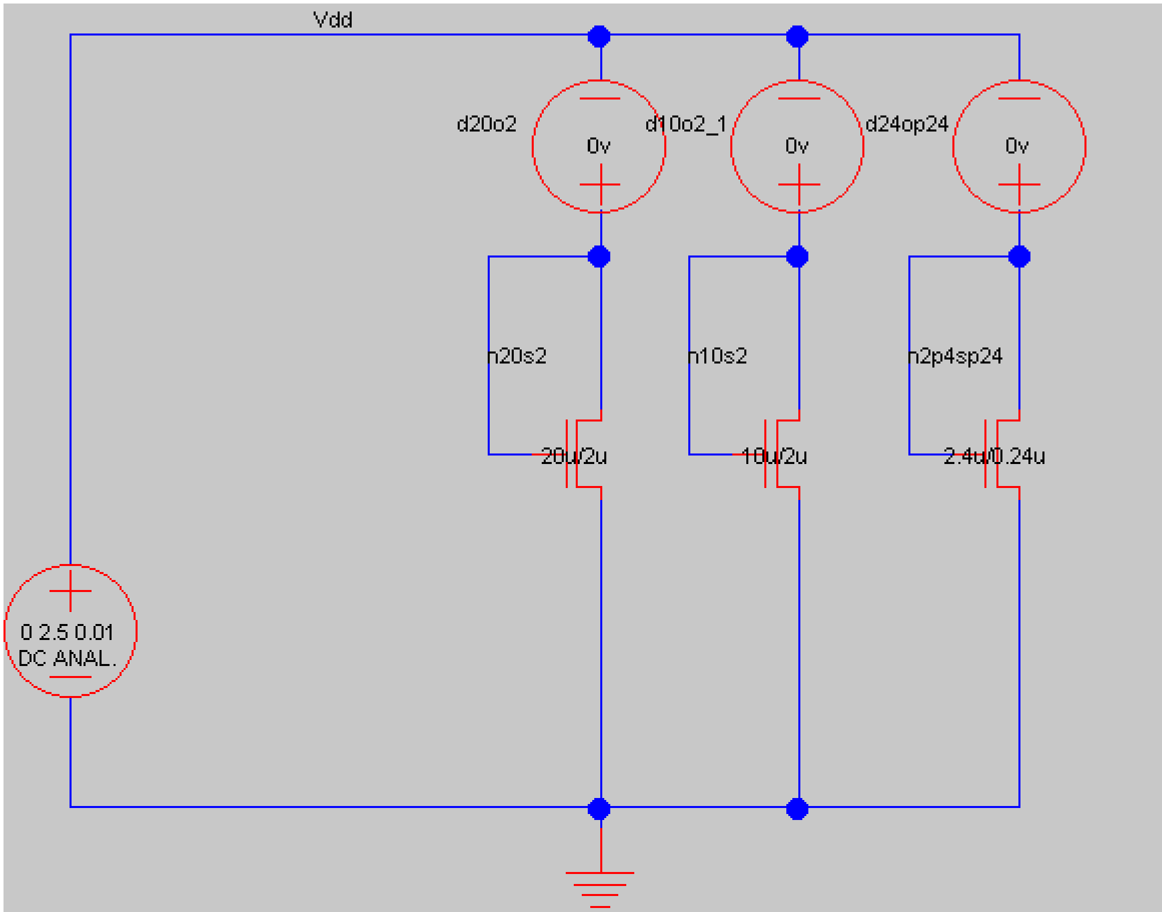
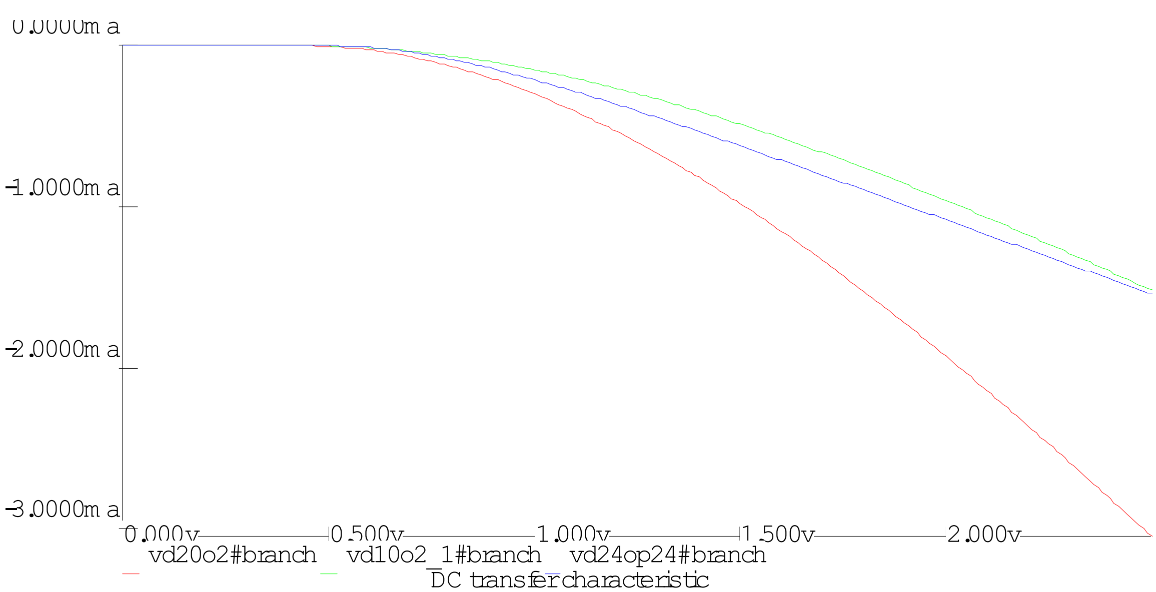
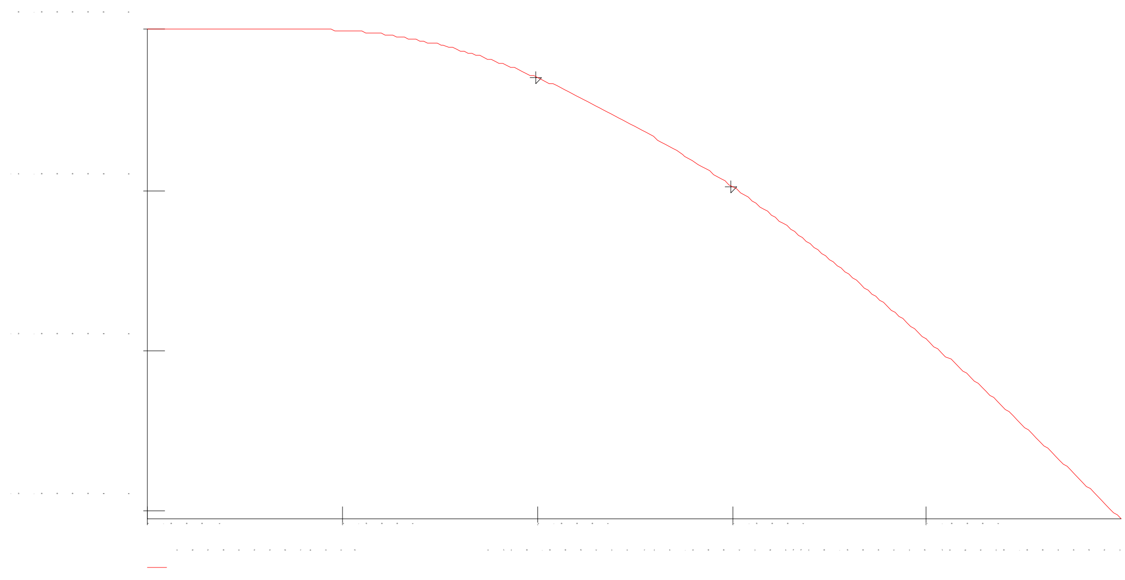
First, determine the N transistor K'n or B'n and look at the curves





Notice that the green and red lines are the same W/L. This is why fat devices L=2u are used... To get around this length modification region.



Use curve fitting to discover k' and Vt

$$IDsat(kp, W, L, Vgs, Vt, \lambda, P) := kp \cdot \frac{W}{2 \cdot L} \cdot (Vgs - Vt)^{P}$$

$kp := 171 \cdot 10^{-6}$ $\quad \lambda := 2.5 \cdot 10^{-4}$ $\quad P := 2$ $\quad Vtn := 0.50$

Given

$$IDsat(kp, 20, 2, 0.995, Vtn, \lambda, P) = .302 \cdot 10^{-3}$$
$$IDsat(kp, 20, 2, 1.2, Vtn, \lambda, P) = .593 \cdot 10^{-3}$$
$$IDsat(kp, 20, 2, 1.498, Vtn, \lambda, P) = .982 \cdot 10^{-3}$$
$$IDsat(kp, 20, 2, 2.017, Vtn, \lambda, P) = 1.979 \cdot 10^{-3}$$

$\lambda > 0$

$kpnx := Minerr(kp, Vtn)$

$kpnx = \begin{pmatrix} 1.38 \times 10^{-4} \\ 0.324 \end{pmatrix}$ $\quad kp := kpnx_{0}$ $\quad kp = 1.38 \times 10^{-4}$

$Vtn := kpnx_{1}$

$$IDsatn(W, L, Vgs) := 138 \cdot 10^{-6} \cdot \frac{W}{2 \cdot L} \cdot (Vgs - Vtn)^{2}$$

$IDsatn(20, 2, 0.995) = 3.11 \times 10^{-4}$

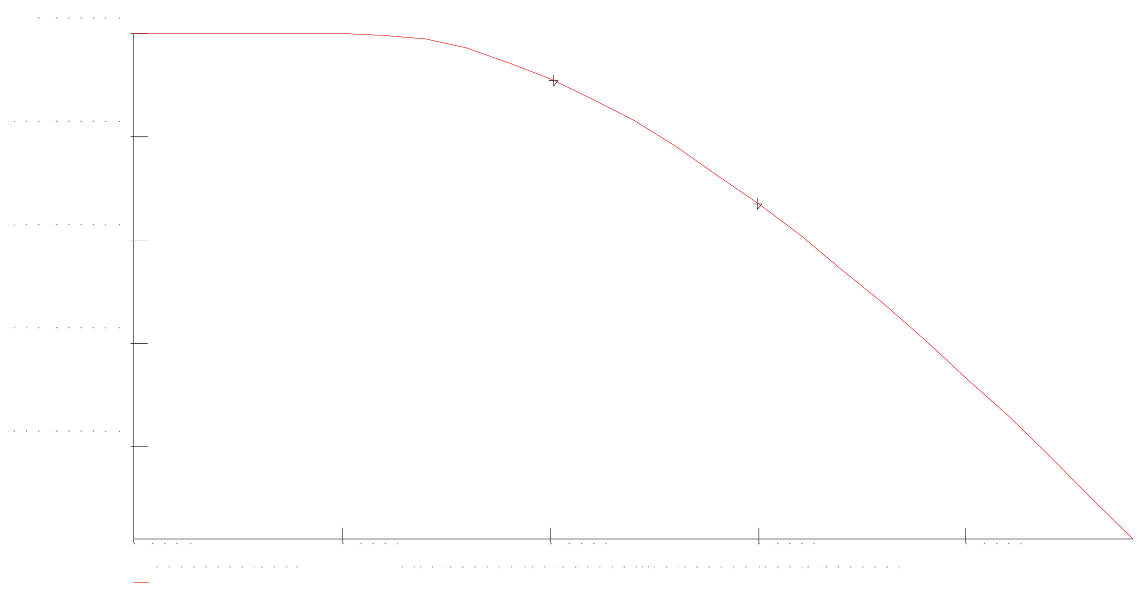
$IDsatn(20,2,1.498) = 9.516 \times 10^{-4}$

Close, but not great... May get it from graphs

$IDsatn(20,2,1.2) = 5.3 \times 10^{-4}$

$IDsatn(20,2,2.017) = 1.979 \times 10^{-3}$

Now figure out the P transistor K'p or Bpp



Apply some basic curve fitting to approximate K' and Vt

$kpp := 40 \cdot 10^{-6}$ $\qquad$ $Vtp := 0.5$

Given

$IDsat(kpp, 20, 2, 1.009, Vtp, \lambda, 2) = 57 \cdot 10^{-6}$

$IDsat(kpp, 20, 2, 1.273, Vtp, \lambda, 2) = 127 \cdot 10^{-6}$

$IDsat(kpp, 20, 2, 1.497, Vtp, \lambda, 2) = 206 \cdot 10^{-6}$

$IDsat(kpp, 20, 2, 2.004, Vtp, \lambda, 2) = 419 \cdot 10^{-6}$

$\lambda > 0$

$ptnx := Minerr(kpp, Vtp)$

$ptnx = \begin{pmatrix} 3.268 \times 10^{-5} \\ 0.403 \end{pmatrix}$ $\qquad$ $Vtp := ptnx_1$ $\qquad$ $kpp := ptnx_0$

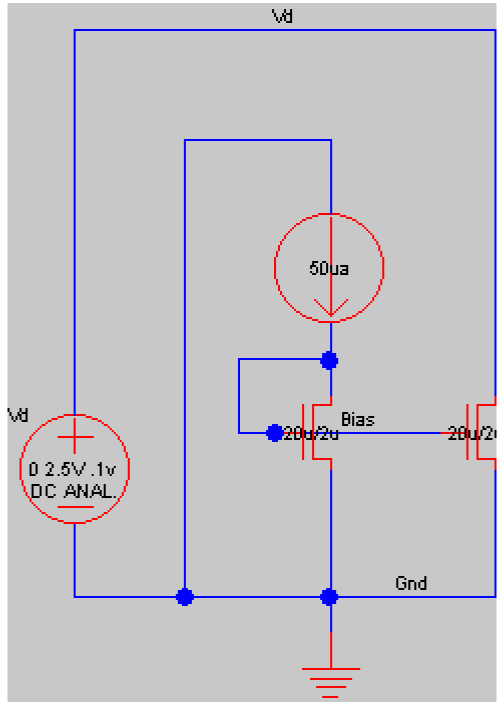
$$IDsatp(W, L, Vgs) := ptnx_0 \cdot \frac{W}{2 \cdot L} \cdot (Vgs - Vtp)^2$$

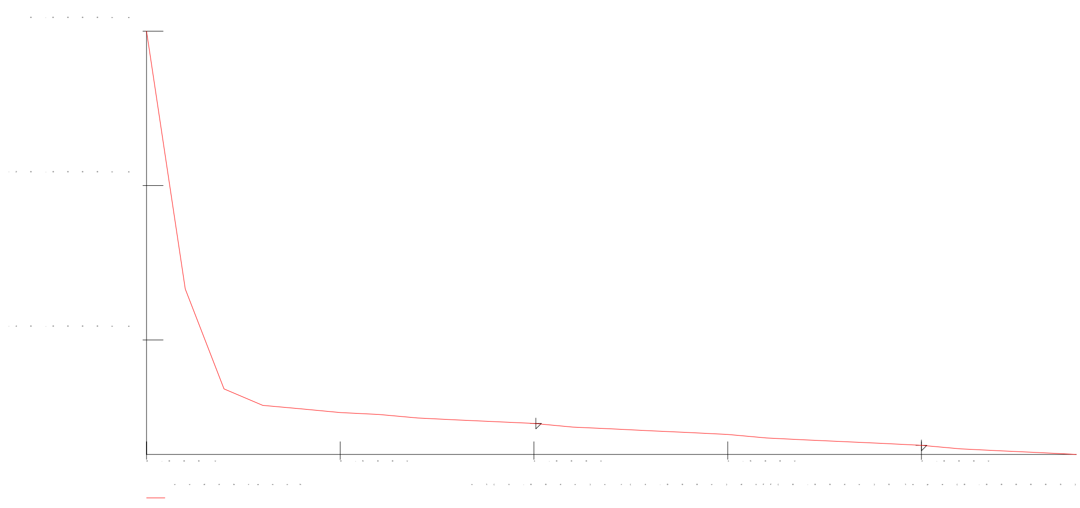
$\text{IDsatp}(20, 2, 1.009) = 6.009 \times 10^{-5}$

$\text{IDsatp}(20, 2, 1.497) = 1.957 \times 10^{-4}$

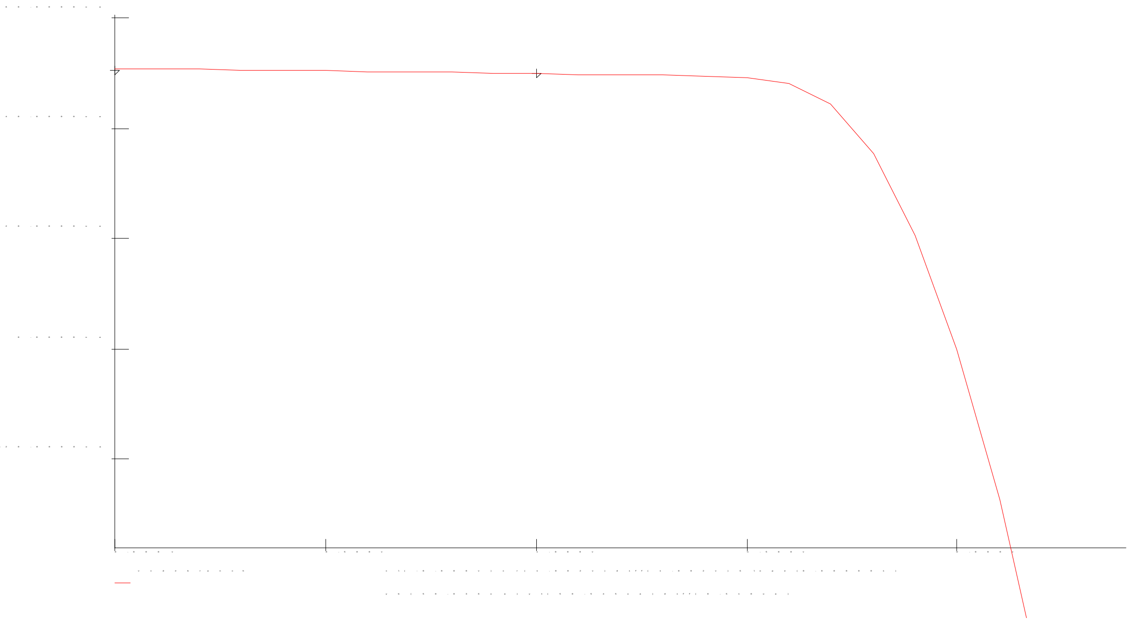
$\text{IDsatp}(20, 2, 2.004) = 4.19 \times 10^{-4}$

Now for Lambda for the N transistor...





$\frac{2.834}{52} = 0.055 \qquad \lambda n := 0.055$



$$\lambda p := \frac{0.510}{50} \qquad \lambda p = 0.01$$

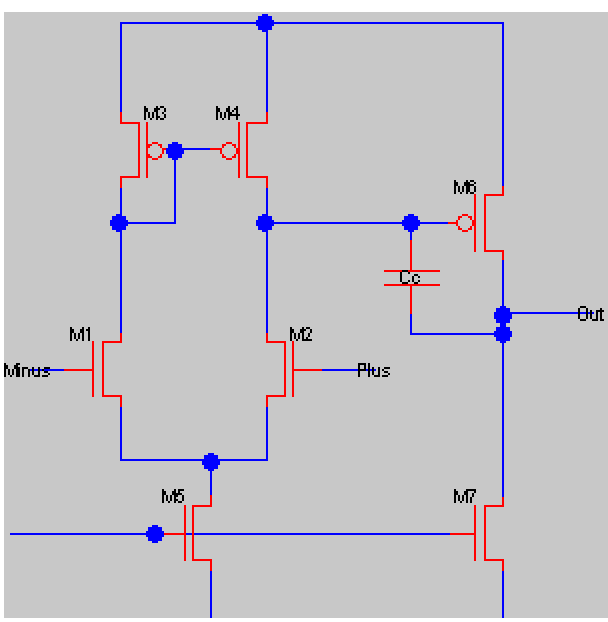
Some handy GM equations... We now have k'n, k'p, λn, and λp for this technology

$$GM(Beta, Id) := \sqrt{2 \cdot Beta \cdot Id}$$

$$bpn := 138 \cdot 10^{-6} \qquad bpp := 33 \cdot 10^{-6} \qquad bpn = 1.38 \times 10^{-4} \qquad bpp = 3.3 \times 10^{-5}$$

$$BetaN(W, L) := bpn \cdot \frac{W}{L} \qquad BP(W, L) := bpp \cdot \frac{W}{L}$$

Some OP Amp design equations for the following circuit...



Handy equations to help the design along...

Slew Rate $SR(I5, Cc) := \frac{I5}{Cc}$

First Stage Gain $Av1(Gm2, I5, \lambda2, \lambda5) := \frac{Gm2}{I5 \cdot (\lambda2 + \lambda5)}$

Second stage gain $Av2(Gm6, I6, \lambda6, \lambda7) := \frac{Gm6}{I6 \cdot (\lambda6 + \lambda7)}$

Gain Bandwidth $GB(Gm2, Cc) := \frac{Gm2}{Cc}$

Output Pole $P2(Gm6, Cl) := \frac{-Gm6}{Cl}$

Right Hand Pole $Z1(Gm6, Cc) := \frac{Gm6}{Cc}$

Saturation Voltage $Vdsat(Ids, B) := \sqrt{\frac{2 \cdot Ids}{B}}$

CC to CL $CC > 0.22 \cdot CL$

$$WL3(I5, Kpp, Vdd, Vinmax, Vtp, Vtn) := \frac{I5}{kpp \cdot (Vdd - Vinmax - |Vtp| + Vtn)^2}$$

$$VDS5(Vinmin, Vss, I5, B1, Vt1max) := Vinmin - \left(Vss - \sqrt{\frac{I5}{B1}}\right) - Vt1max$$

$$VDsat(Id, B) := \sqrt{2 \cdot \frac{B}{Id}}$$

$$WLGM(Gm, kp, Id) := \frac{Gm^2}{kp \cdot Id}$$

Settling time is approximatly 10X slew rate...

Shoot for a Cc of about 4pf (Just picked out of the air)

$Cc := 4 \cdot 10^{-12}$ $Cc = 4 \times 10^{-12}$

Assume the slew rate is .010V/us $SlewRate := \frac{1}{1 \cdot 10^{-5}}$ $SlewRate = 1 \times 10^{5}$

$SettlingTime := \frac{10}{SlewRate}$ $SettlingTime = 1 \times 10^{-4}$

$I5 := SR(Ix, Cc) = SlewRate \text{ solve}, Ix \rightarrow \frac{1}{2500000}$ $I5 = 4 \times 10^{-7}$

$wl3 := WL3(I5, kpp, 2.5, 2.0, .7, Vtn)$ $wl3 = 0.801$ $W3 := wl3 \cdot 2$ $W3 = 1.602$

Next, pick a gain bandwidth... I'll use 25KHz $GB := 55 \cdot 10^{4} \cdot 2 \cdot \pi$

$gm2 := GB \cdot Cc$ $gm2 = 1.382 \times 10^{-5}$

$wl2 := WLGM(gm2, I5, bpn)$ $wl2 = 3.462$ $W2 := wl2 \cdot 2$ $W2 = 6.923$

$vds5 := VDS5(1.0, 0, I5, bpn \cdot wl2, Vtn)$ $vds5 = 0.705$ It can work...

$wl5 := \frac{2 \cdot I5}{bpn \cdot vds5^{2}}$ $wl5 = 0.012$ $W5 := wl5 \cdot 40$ $W5 = 0.466$

Assume 1pf external load $Cl := 1 \cdot 10^{-12}$

$Gm6 := 2.2 \cdot gm2 \cdot \frac{Cl}{Cc}$ $Gm6 = 7.603 \times 10^{-6}$

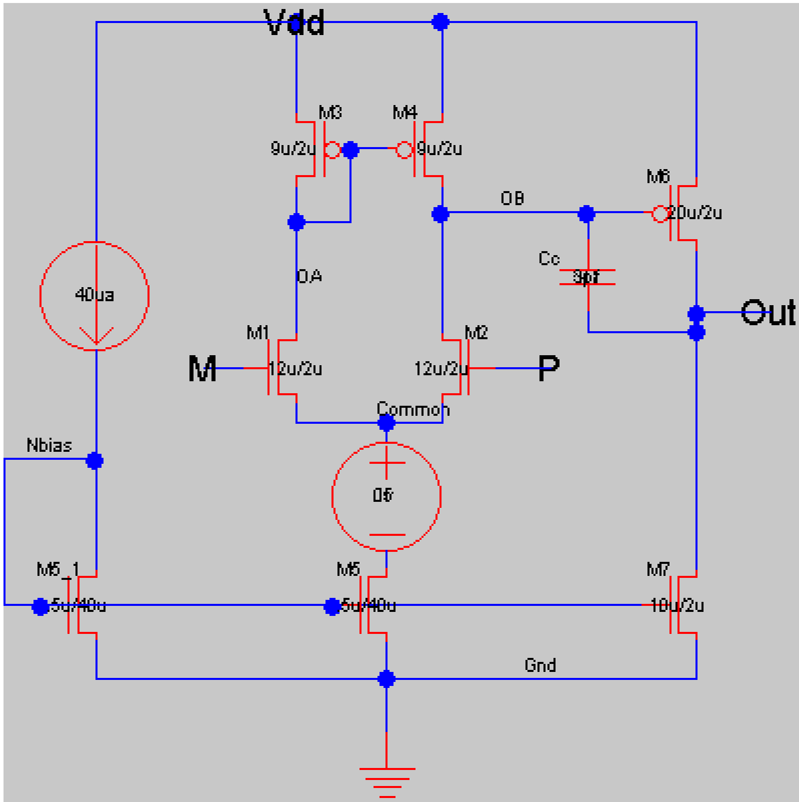
$wl6 := \frac{Gm6}{bpp \cdot Vtp}$ $wl6 = 0.572$ $W6 := wl6 \cdot 2$ $wl6 = 0.572$

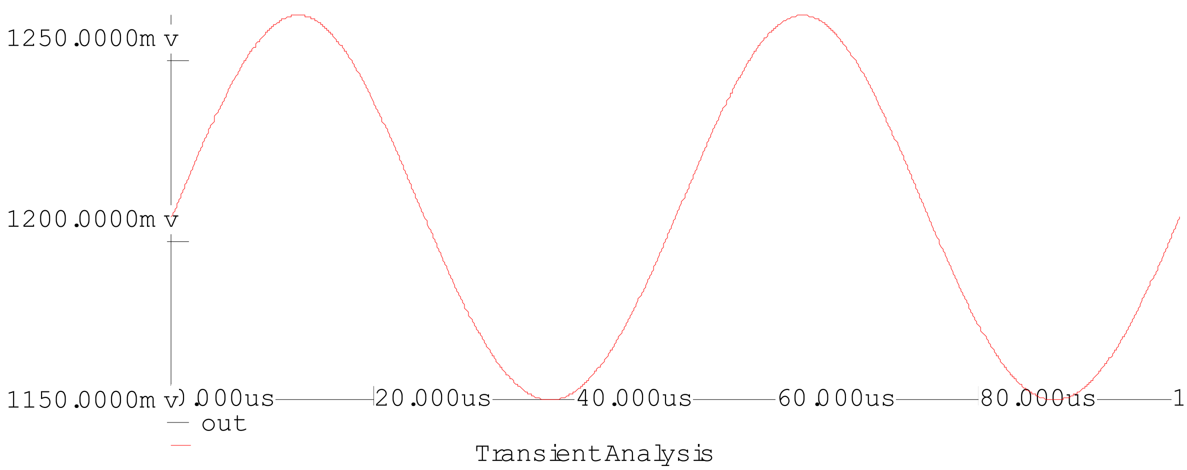
$I6 := \frac{wl6}{wl3} \cdot \frac{I5}{2}$ $I6 = 1.429 \times 10^{-7}$

$wl7 := wl5 \cdot \frac{I6}{I5}$ $wl7 = 4.163 \times 10^{-3}$ $W7 := wl7 \cdot 80$ $W7 = 0.333$

$Av := \frac{2 \cdot gm2 \cdot Gm6}{I5 \cdot (\lambda n + \lambda p) \cdot I6 \cdot (\lambda p + \lambda n)}$ $Av = 8.651 \times 10^{5}$

Build it, simulate it, and it doesnt work. Then move device sizes to get design points
Remember, Vt, moves... Equations are not powers of 2, (More like 1.5-1.7)...
This will be nice and slow... But should be stable...





Nice and smooth, but very slow....
This is a great op amp for a band gap reference. Some offset, but very little noise. It has low gain...

Now, do one seat of the pants..... No fancy formulas or other items

$Id := 50\cdot 10^{-6}$

$Gmi := 5 \times 10^{-4}$

$Wbp := GM(BP(Wxx,2),Id) = 10\cdot Gmi \text{ solve}, Wxx \rightarrow \frac{500000}{33}$ $Wbp = 1.515 \times 10^{4}$

$Wi := Gmi = GM(BetaN(Wx,2),Id) \text{ solve}, Wx \rightarrow \frac{2500}{69}$

$Wi = 36.232$ Differential Pair Size

$Gd := \frac{Gmi}{Gx} = 10 \text{ solve}, Gx \rightarrow \frac{1}{20000}$

$Gd = 5 \times 10^{-5}$

$Wl := Gd = GM(BP(Wd,2),Id) \text{ solve}, Wd \rightarrow \frac{50}{33}$

$Wl = 1.515$ Active Load size

$IDsatp(121,2,.72) = 9.961 \times 10^{-5}$ Voltage works out OK at .72V

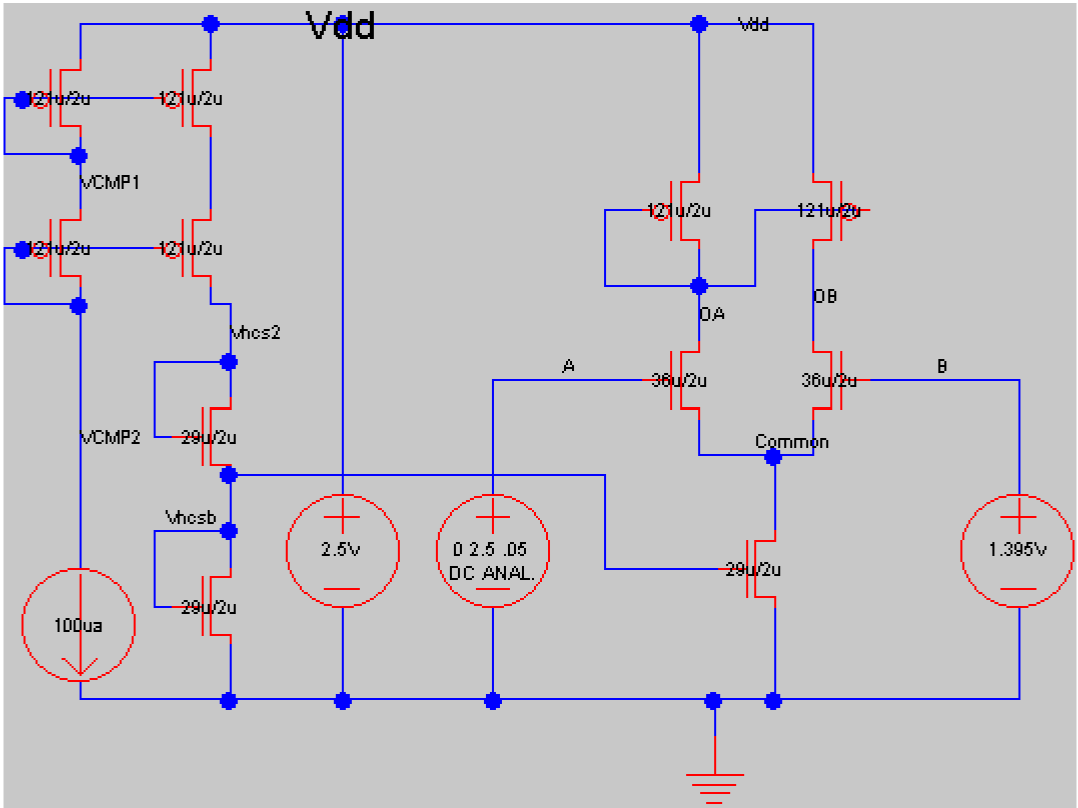
A first cut at the current source

$IDsatn(29,2,0.65) = 1.066 \times 10^{-4}$

The current Source transistor will be 29u/2u. Plug this into the design, and Set the amplifier up and check it out with a Simulation.

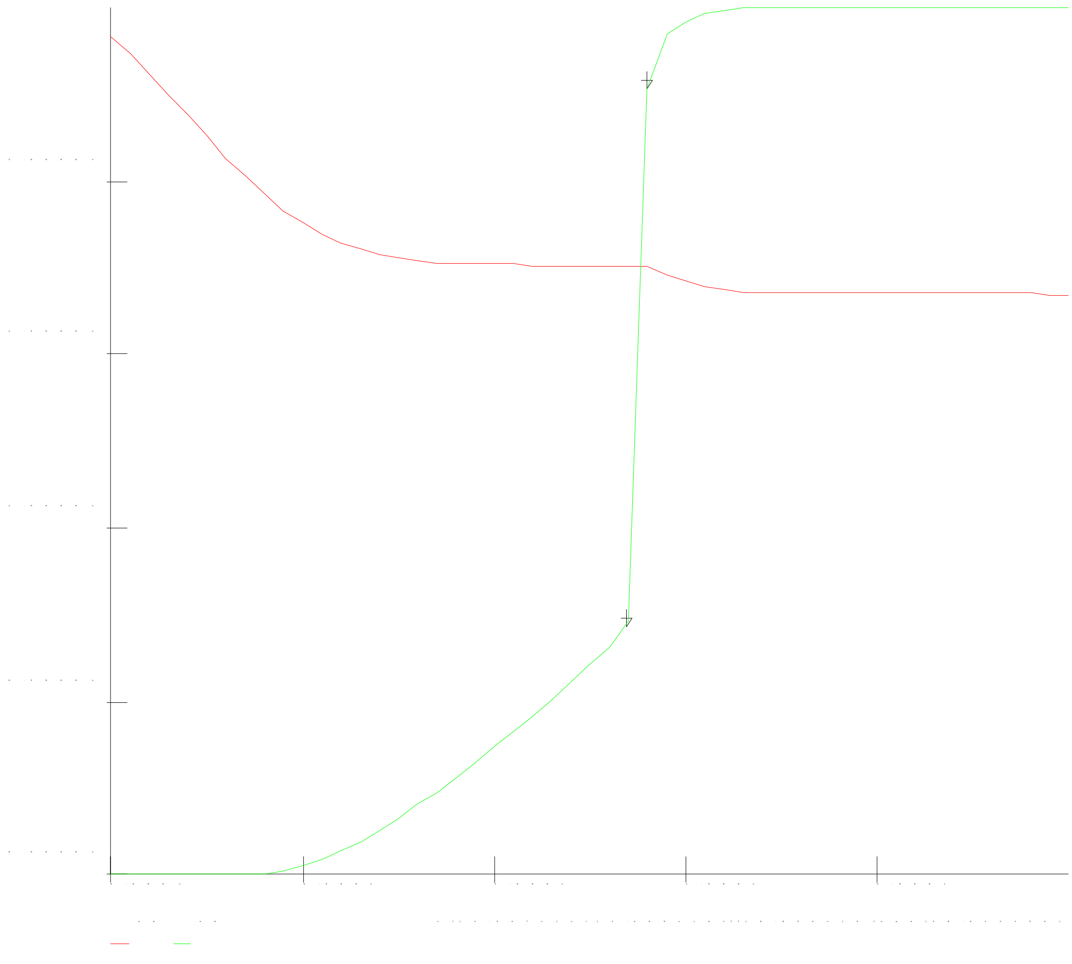
This gives the following OP amp circuit... I have used the same size transistors in the P current mirror as in the Op amp... (A little more voltage, but not too bad...

The following has problems...



The simulation response curves...
They show a higher gain than expected. This comes from the current sources being a little hotter than planned, and the poor fitting of the transistors. It is still a good amplifier.

(Chart on Next Page)



Create an output buffer, with some gain.

Using the existing transistor sizes...

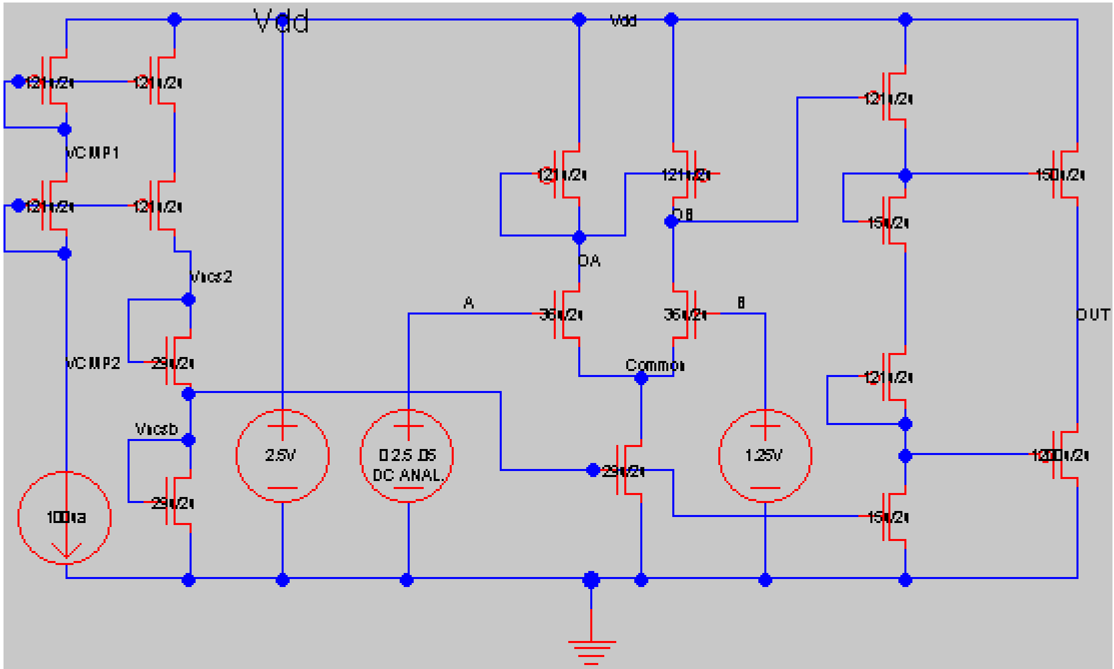
$$GM\left(BP(121,2),\frac{Id}{4}\right) = 2.234\times 10^{-4}$$

Using a current source load... Make it about 1/8 the size of N current source

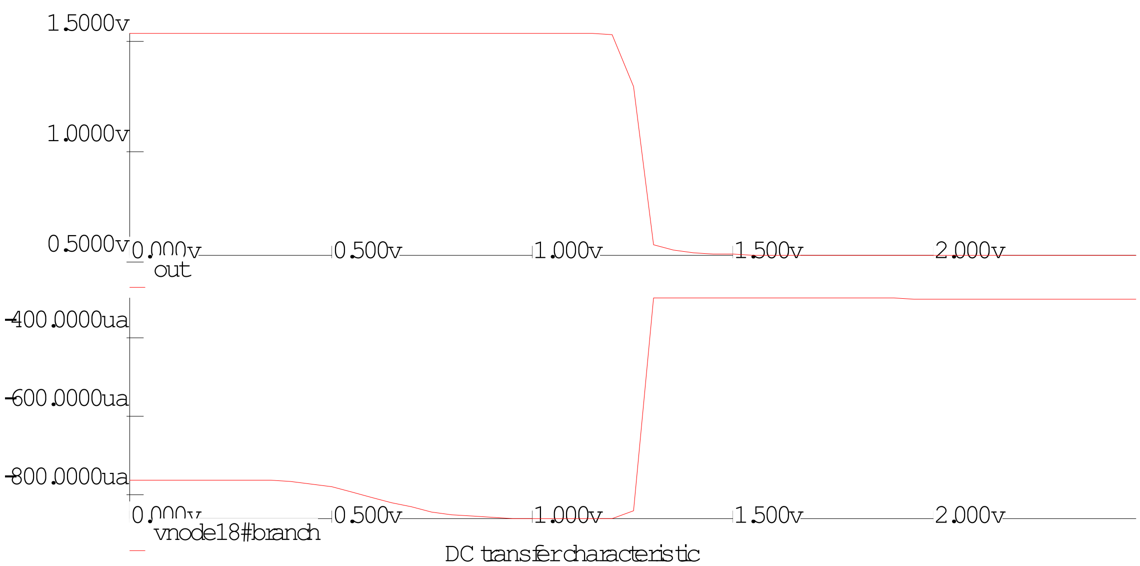
$$\frac{29}{4} = 7.25$$

I'll use 8 as a starting point.

Final Stage is a symmetrical Power amplifier

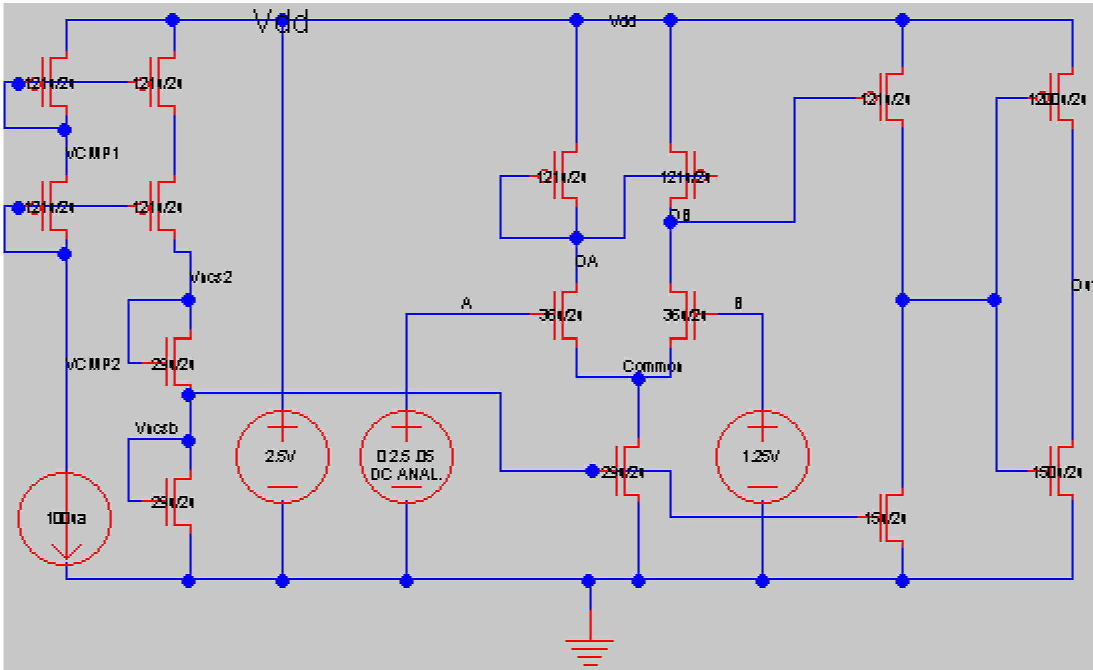


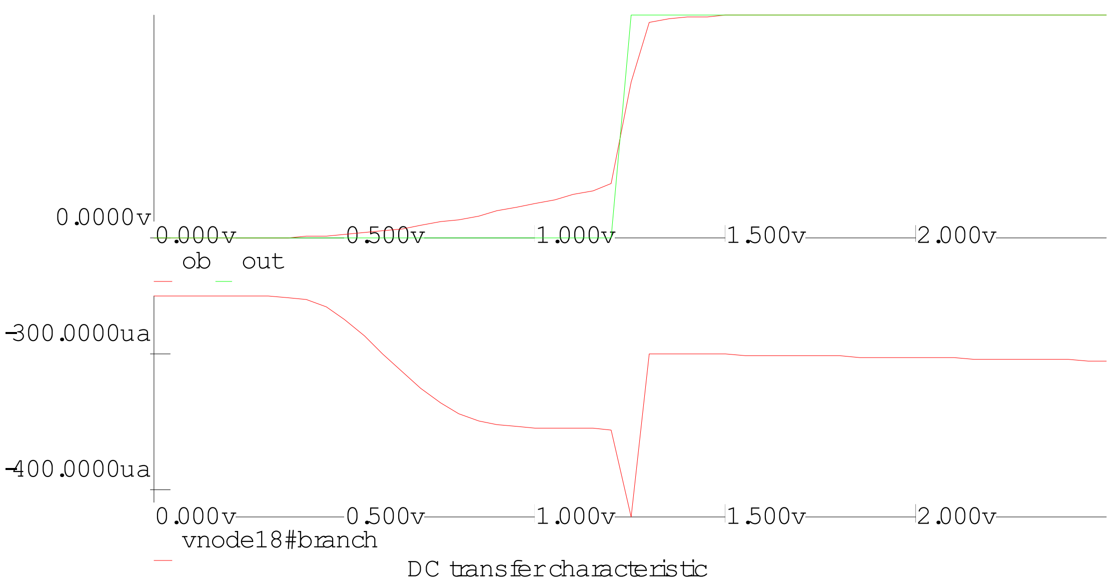
Book style schematics. No real gain from last stage. You lose Vtn+Vtp in output section.



We lost gain and headroom on the output section... I'll replace with a simple invertor...

Devices just 10x of the other transistors. (No real good reason...)

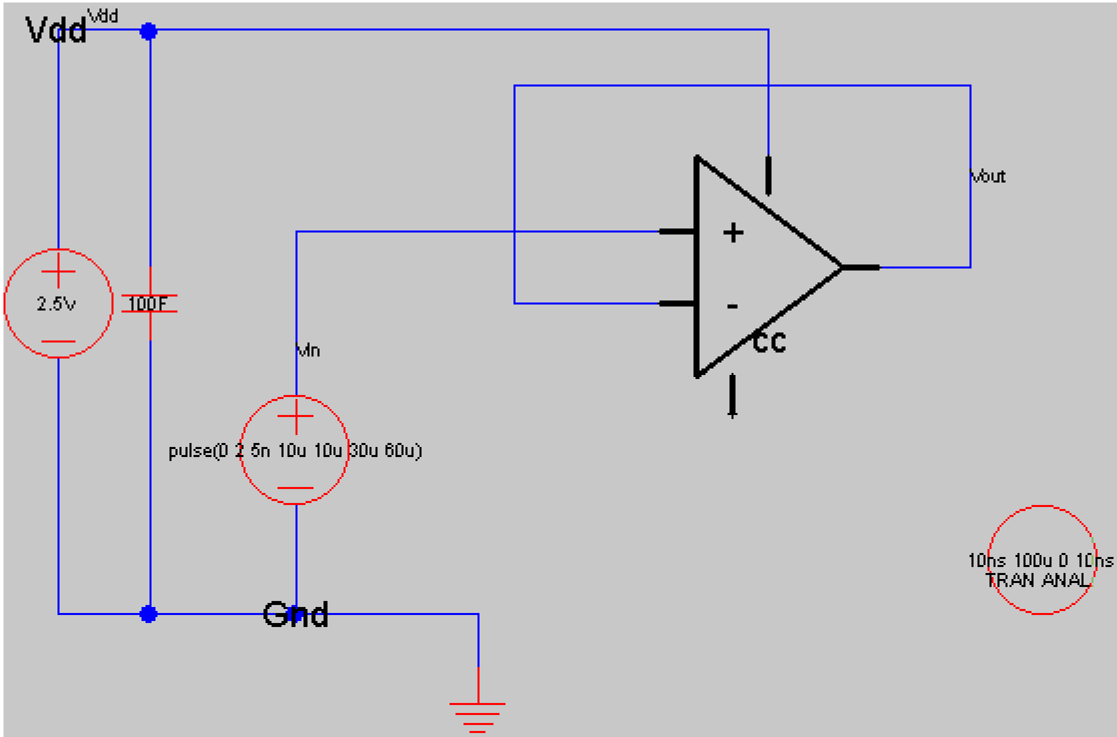




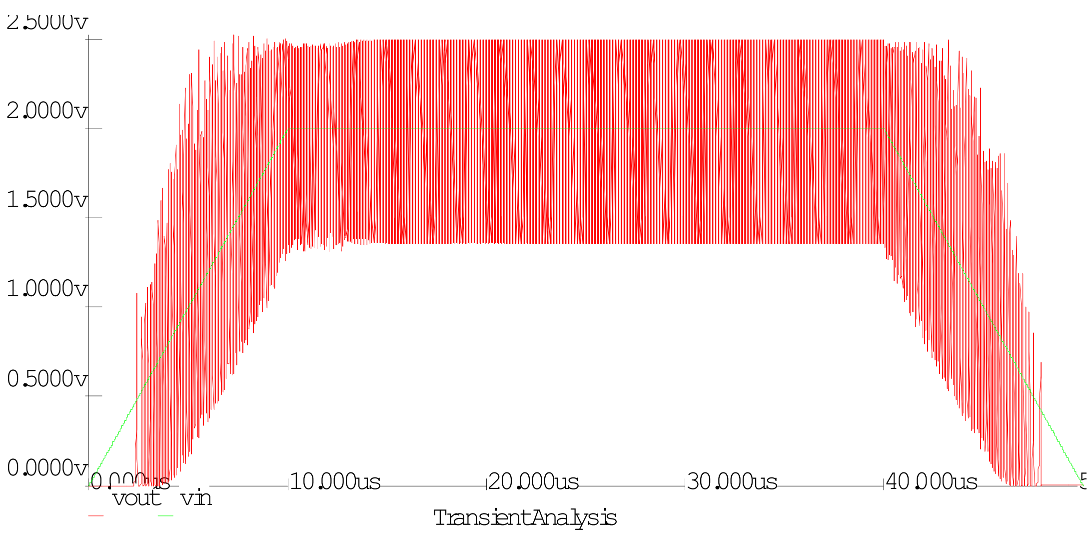
Power is no worse, and the gain is higher. The output is now going rail to rail, but it may not be real linear... The gain is quite a bit higher. (It has an inversion, switching + and - inputs).

Use this as a comparator, or to convert a small VCO signal to digital (Hint)

Now, Set up a test bench circuit of the amplifier as an OTA (No second buffer)...



How does it look. (Uncompensated)



It has a problem... It is not stable.

There is too much gain in the output stage... To be stable, Gm6 > 10Gm2 (buffer vrs diff pair)

$Gm6 := 10 \cdot Gmi$ $\qquad Gm6 = 5 \times 10^{-3}$

Just low pass it until it becomes stable...