Design of an Folded Cascode Operational Amplifier in High Voltage CMOS Technology

Benjamin LUTGEN
Wintersemester 2008/2009

Supervisor: Prof. Dr.-Ing. Andreas König

Overview

1. **Intoduction**
   - Given Objectives
   - Motivation
2. **Schematic Design**
   - Practical Version of the Amplifier
   - Schematic Description
   - Design Plan
     - Transistor groups
   - First Approach
   - Second Approach
     - Simulation Results
   - Final Solution
     - Final Schematic
     - Measurement Setup
     - Maximizing the Gain
     - Simulation results
     - Measuring the Characteristics
3. **Layout Design**
   - High Voltage Layouting
   - Final Layout
     - Functional Groups
   - LVS Log
4. **Summary and Conclusion**
   - Comparison Specification/Achieved Values
   - Discussion
   - Conclusion
   - References

1. Introduction

Given Objectives

Objective of the project:

- design of an **folded cascode operational amplifier**
- using a new **high voltage technology** („H35“ 20 V)

Meeting these specifications ➔

S. Nr	Characteristics	Specification values
1	Open loop Gain	> 100 dB
2	Gain Bandwidth	10 MHz
3	Phase margin	> 60 °
4	Settling Time	< 1 µs
5	Slew Rate	200 V/µs
6	Offset	5 µV
7	Input CMR	± 6 V
8	Output Swing	± 8 V
9	CMRR	> 100 dB
10	Power Dissipation	Minimum
11	Area Consumption	Minimum
12	Voltage Supply	20 V
13	Load Capacitance	10 pF
14	Load Resistance	100 kΩ

Motivation (1)

The used folded cascode topology offers the following properties:

- good common-mode range
- self compensation
- High gain
- Relatively low power-dissipation
- High output resistance

The special challenge of this project was the transfer of this circuit to a high voltage CMOS technology

Motivation (2)

The high voltage CMOS Technology H35 provides a high voltage capability **up to 50V**.

In the project, the symmetrical 20V variant with thick oxide is used („xMOS20HS“)

Disadvantage:

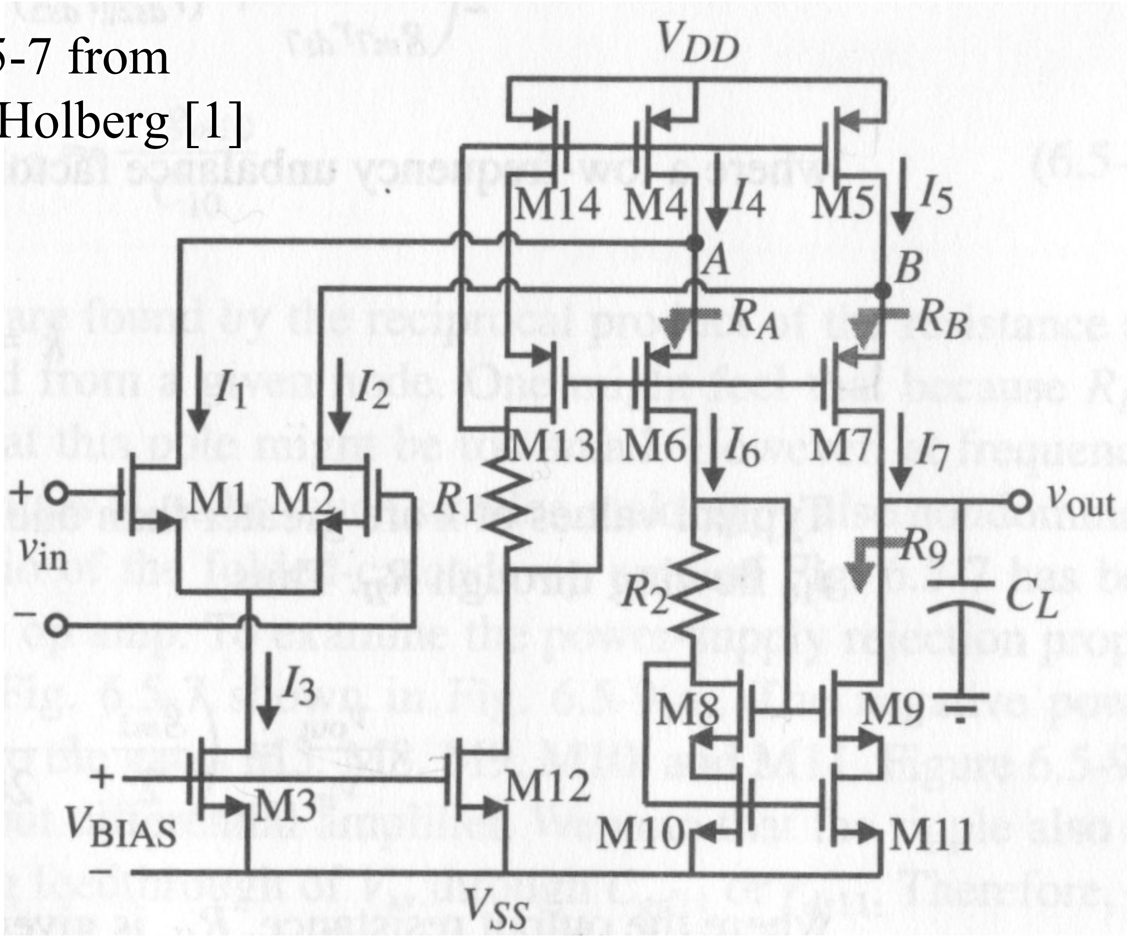
- **Less K'_n/K'_p as in 3.3V technology**

in µA/V²	**20V** Technology	**3.3V** Technology
K‘p	12	50
K‘n	35	110

2. Schematic Design

Practical Version of the Amplifier

Figure 6.5-7 from Allen/Holberg [1]

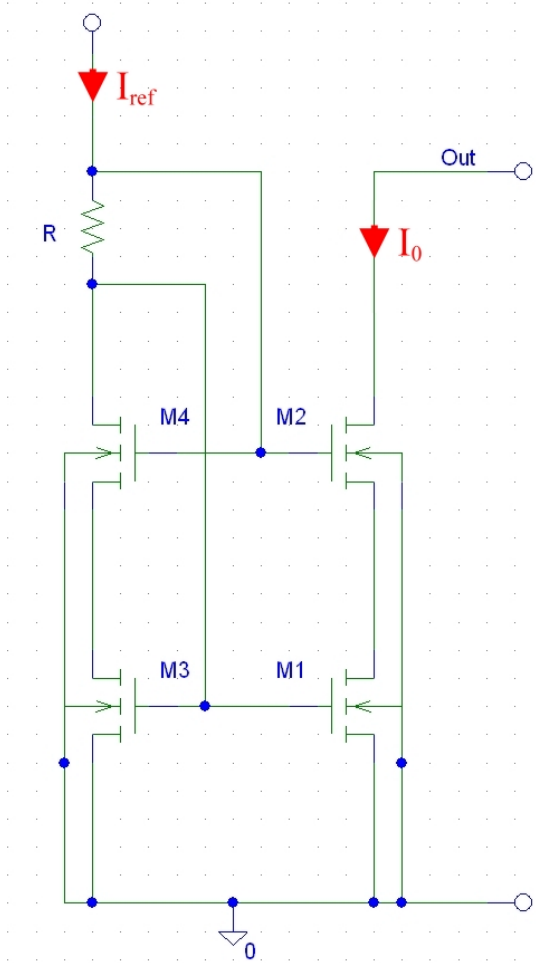


Schematic Description (1)

This is a **special current mirror sink**, with the following attributes:

- High output resistance
- Small saturation voltage
- Low power dissipation
- Self biasing
- High swing

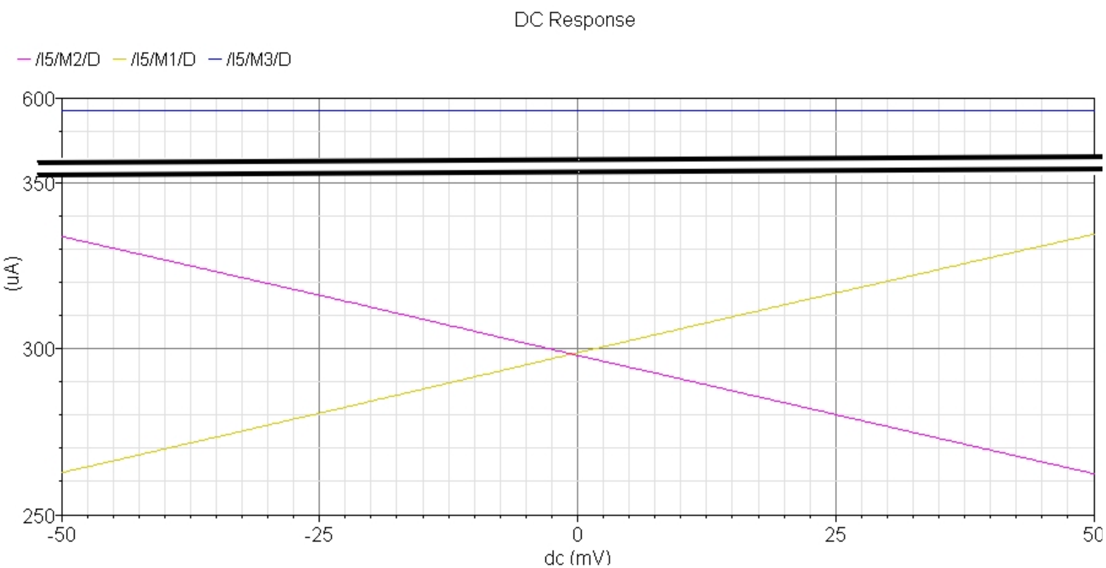
This **current mirror sink**, and the **current mirror source** are the basic modules of the folded cascode op amp.

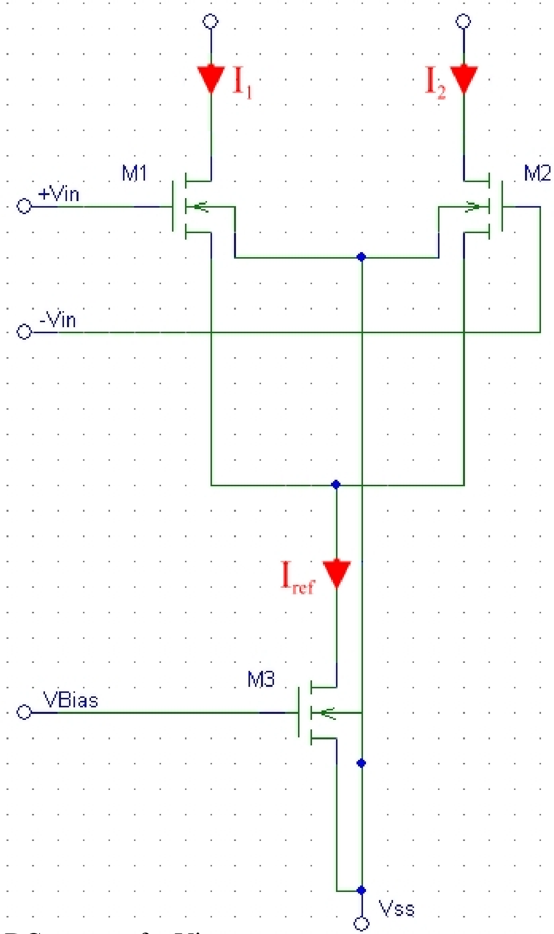


Schematic Description (2)

Another basic module:

- The **differential pair** with a constant common current.
- M3 works as current sink

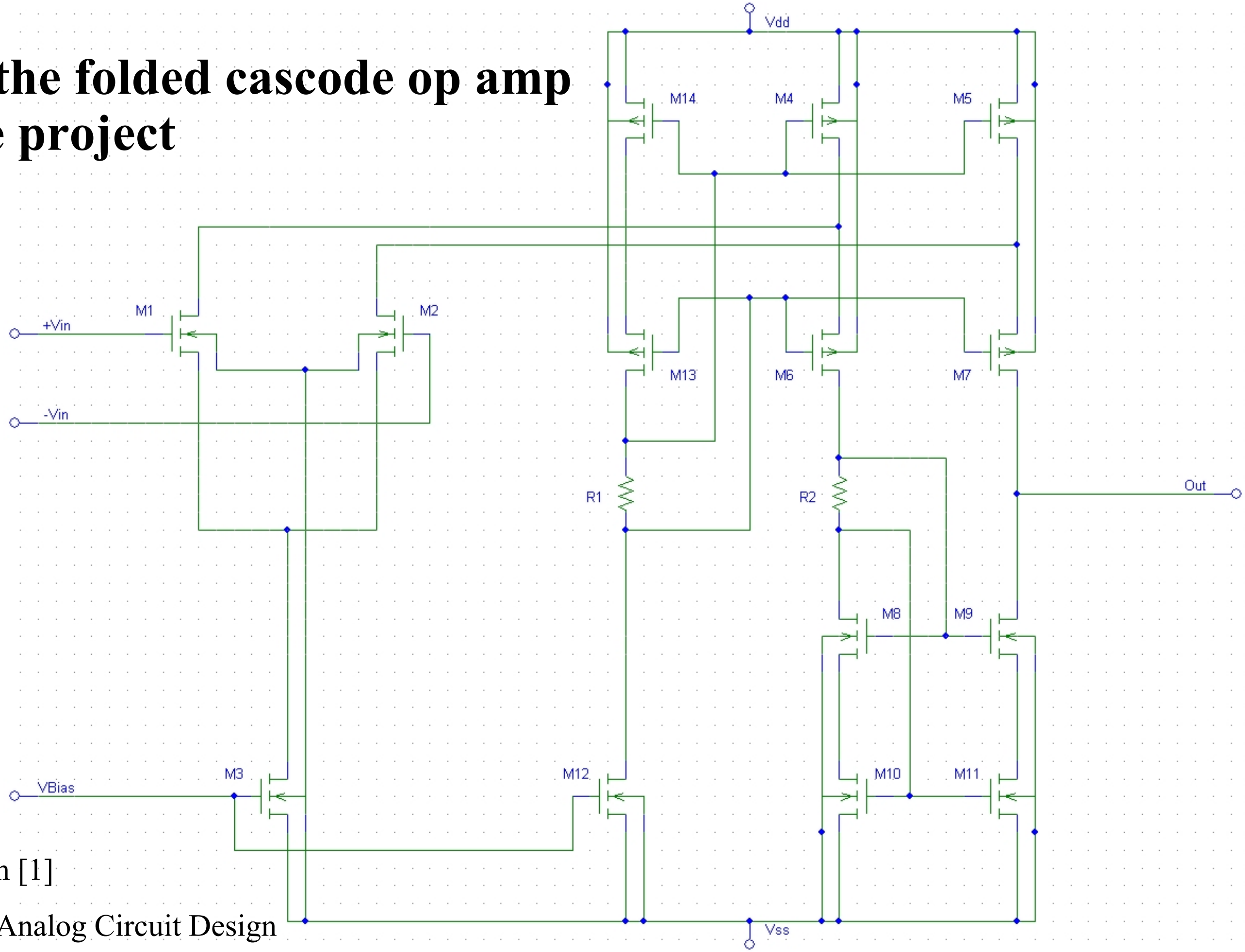




This are the currents of the pair, during a DC-sweep of +Vin

Schematic Description (3)

Schematic of the folded cascode op amp used in the project



Based on Schematic from [1]

Allen/Holberg – CMOS Analog Circuit Design

Design Plan (1)

Design plan from **Allen/Holberg - CMOS Analog Circuit Design [1]** was used for determining the values of the transistor and resistors

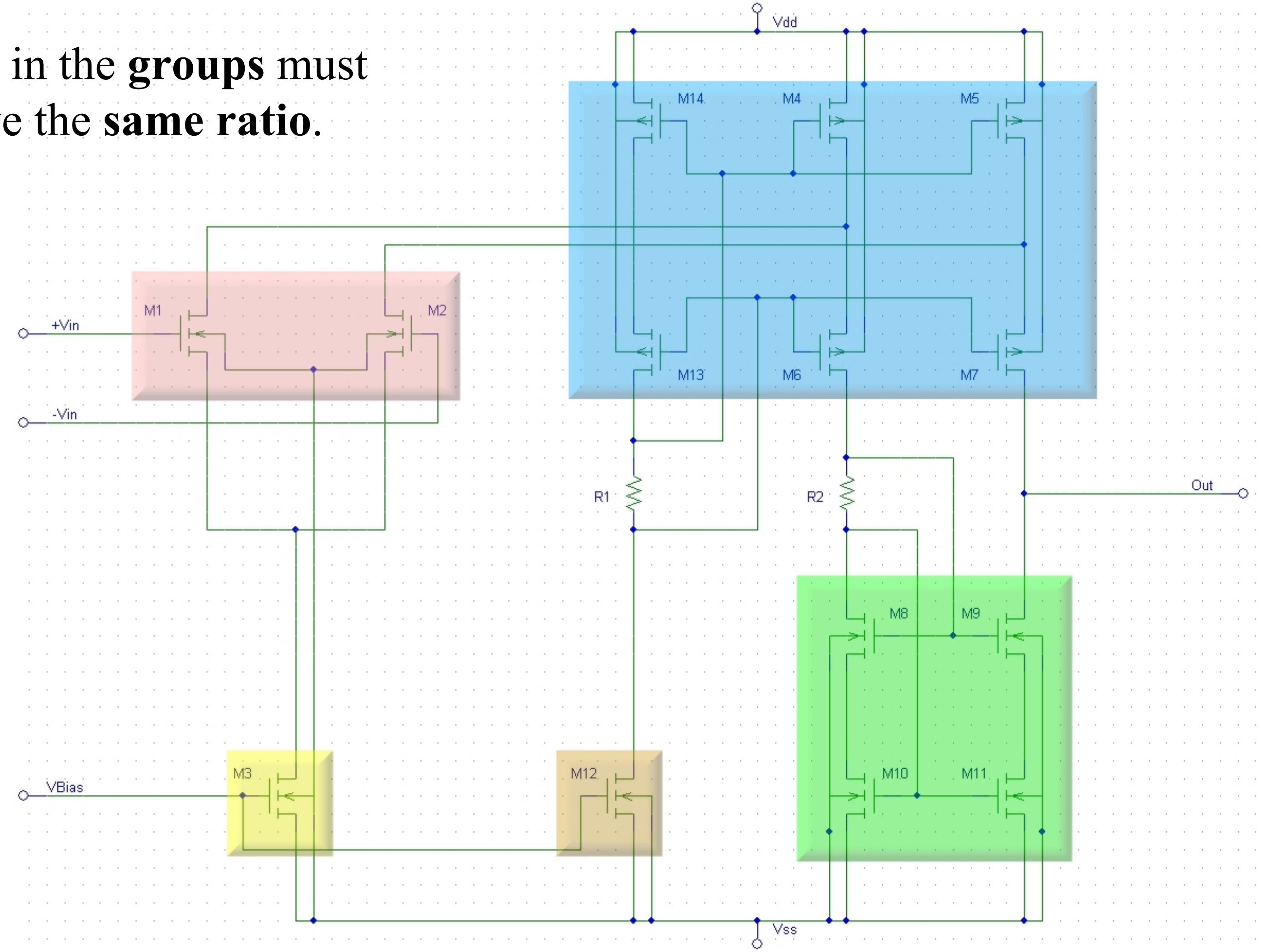
Table 6.5-3 Design Approach for the Folded-Cascode Op Amp

Step #	Relationship/ Requirement	Design Equation/Constraint	Comments
1	Slew rate	$I_3 = SR \cdot C_L$	
2	Bias currents in output cascodes	$I_4 = I_5 = 1.2I_3$ to $1.5I_3$	Avoid zero current in cascodes
3	Maximum output voltage, $v_{out}(max)$	$S_5 = \frac{2I_5}{K'_P V_{SD5}^2}$, $S_7 = \frac{2I_7}{K'_P V_{SD7}^2}$ Let $S_4 = S_{14} = S_5$ and $S_{13} = S_6 = S_7$	$V_{SD5}(sat) = V_{SD7}(sat) = \frac{V_{DD} - V_{out}(max)}{2}$
4	Minimum output voltage, $v_{out}(min)$	$S_{11} = \frac{2I_{11}}{K'_N V_{DS11}^2}$ $S_9 = \frac{2I_9}{K'_N V_{DS9}^2}$ Let $S_{10} = S_{11}$ and $S_8 = S_9$	$V_{DS9}(sat) = V_{DS11}(sat) = \frac{V_{out}(min) - \lvert V_{SS}\rvert}{2}$
5	Self-bias cascode	$R_1 = V_{SD13}(sat)/I_{12}$ and $R_2 = V_{DS8}(sat)/I_6$	
6	$GB = \frac{g_{m1}}{C_L}$	$S_1 = S_2 = \frac{g_{m1}^2}{K'_N I_3} = \frac{GB^2 C_L^2}{K'_N I_3}$	
7	Minimum input CM	$S_3 = \frac{2I_3}{K'_N\left[V_{in}(min) - V_{SS} - \sqrt{\frac{I_3}{K'_N S_1}} - V_{T1}\right]^2}$	
8	Maximum input CM	$S_4 = S_5 = \frac{2I_4}{K'_P (V_{DD} - V_{in}(max) + V_{T1})^2}$	S_4 and S_5 must meet or exceed the requirement of step 3
9	Differential voltage gain	Eq. (6.5-18)	
10	Power dissipation	$P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{12} + I_{10} + I_{11})$	

Design Plan (2) Transistor Groups

The transistors in the **groups** must always have the **same ratio**.

- $M_{1,2}$
- M_3
- $M_{4,5,6,7,13,14}$
- $M_{8,9,10,11}$
- M_{12}



Design Plan (3)

The calculations of the design plan were realized in an **Excel-Sheet**, providing **very fast recalculations**.

Given Specifications

Characteristics	Symbol		Specification Values	
Open loop Gain		>	100	dB
Gain Bandwidth	GB		1,00E+07	Hz
Phase Margin	PM	>	60	°
Settling Time		<	1,00E-06	s
Slew Rate	SR		2,00E+08	V/s
Offset			5,00E-06	V
Input CMR	V_{in}(max)		6	V
	V_{in}(min)		-6	V
Output Swing	V_{out}(max)		8	V
	V_{out}(min)		-8	V
CMRR		>	100	dB
Power Dissipation	P_{diss}		min	
Area Consumption			min	
Voltage Supply	V_{DD}		10	V
	V_{SS}		-10	V
Load Capacitance			1,00E-11	F
Load Resistance		=	1,00E+05	Ohm

Process Parameters

Characteristics	Symbol	Specification Values
Gain Factor	K'_n	3,90E-05 A/V^2
	K'_p	1,20E-05 A/V^2
Threshold Voltage	V_{T1n}	1,54 V
	V_{T1p}	-1,8 V

Design Plan

Step 1	I_3	=	2,00E-03 A	=	2,00 mA		
Step 2	Factor k			=	1,20		Ratio I_3 to $I_{4,5}$
	I_4	=	2,40E-03 A	=	2,40 mA		
	I_5	=	2,40E-03 A	=	2,40 mA		
Step 3	V_{SD5}	=	1 V				
	V_{SD7}	=	1 V				
	S_4	=	4,00E+02	=	400	NOK	max 249
	S_5	=	4,00E+02	=	400	NOK	max 249
	S_{14}	=	4,00E+02	=	400	NOK	max 249
	Factor i_{57}			=	1,00		Ratio I_5 to I_7
	S_6	=	4,00E+02	=	400	NOK	max 249
	S_7	=	4,00E+02	=	400	NOK	max 249
	S_{13}	=	4,00E+02	=	400	NOK	max 249
Step 4	V_{DS9}	=	1 V				
	V_{DS11}	=	1 V				
	Factor i_{79}			=	1,00		Ratio I_7 to I_9
	S_9	=	1,23E+02	=	123		
	S_8	=	1,23E+02	=	123		
	Factor i_{711}			=	1,00		Ratio I_7 to I_{11}
	S_{11}	=	1,23E+02	=	123		
	S_{10}	=	1,23E+02	=	123		
Step 5	R_1	=	4,17E+02	=	417,00 Ohm		
	R_2	=	4,17E+02	=	417,00 Ohm		
Step 6	S_1	=	1,28E-01	=	0	NOK	min 3
	S_2	=	1,28E-01	=	0	NOK	min 3
Step 7	S_3	=	3,33E-01	=	0	NOK	min 3
	S_{12}	=	4,17E-01	=	0	NOK	min 3
Step 8	S_4	=	82,6446281	=	83	OK	S4 and S5 have to
	S_5	=	82,6446281	=	83	OK	be bigger as here
Step 9							
Step 10	Pdiss	=	1,84E-01	=	184,00 mW		

Transistor ratios

Transistor widths

Transistor widths		
@ Length	2 µm	
Trans.	**Ratio**	**Width**
M_1	0	0 µm
M_2	0	0 µm
M_3	0	0 µm
M_4	400	800 µm
M_5	400	800 µm
M_6	400	800 µm
M_7	400	800 µm
M_8	123	246 µm
M_9	123	246 µm
M_{10}	123	246 µm
M_{11}	123	246 µm
M_{12}	0	0 µm
M_{13}	400	800 µm
M_{14}	400	800 µm

This shows only the first tentative

➢ Values not correct

First Approach

By entering the specifications into the design plan it became obvious, that the transistor-ratios were **not feasible**.

Given Specifications

Characteristics	Symbol		Specification Values	
Open loop Gain		>	100	dB
Gain Bandwidth	GB		1,00E+07	Hz
Phase Margin	PM	>	60	°
Settling Time		<	1,00E-06	s
Slew Rate	SR		2,00E+08	V/s
Offset			5,00E-06	V
Input CMR	V_{in}(max)		6	V
	V_{in}(min)		-6	V
Output Swing	V_{out}(max)		8	V
	V_{out}(min)		-8	V
CMRR		>	100	dB
Power Dissipation	P_{diss}		min	
Area Consumption			min	
Voltage Supply	V_{DD}		10	V
	V_{SS}		-10	V
Load Capacitance			1,00E-11	F
Load Resistance		=	1,00E+05	Ohm

Design Plan

Step 1	I_3	=	2,00E-03 A	=	2,00	mA		
Step 2			Factor k	=	1,20			Ratio I_3 to $I_{4,5}$
	I_4	=	2,40E-03 A	=	2,40	mA		
	I_5	=	2,40E-03 A	=	2,40	mA		
Step 3	V_{SD5}	=	1 V					
	V_{SD7}	=	1 V					
	S_4	=	4,00E+02	=	400		NOK	**max 249**
	S_5	=	4,00E+02	=	400		NOK	**max 249**
	S_{14}	=	4,00E+02	=	400		NOK	**max 249**
			Factor i_{57}	=	1,00			Ratio I_5 to I_7
	S_6	=	4,00E+02	=	400		NOK	**max 249**
	S_7	=	4,00E+02	=	400		NOK	**max 249**
	S_{13}	=	4,00E+02	=	400		NOK	**max 249**
Step 4	V_{DS9}	=	1 V					
	V_{DS11}	=	1 V					
			Factor i_{79}	=	1,00			Ratio I_7 to I_9
	S_9	=	1,23E+02	=	123			
	S_8	=	1,23E+02	=	123			
			Factor i_{711}	=	1,00			Ratio I_7 to I_{11}
	S_{11}	=	1,23E+02	=	123			
	S_{10}	=	1,23E+02	=	123			
Step 5	R_1	=	4,17E+02	=	417,00	Ohm		
	R_2	=	4,17E+02	=	417,00	Ohm		
Step 6	S_1	=	1,28E-01	=	0		NOK	**min 3**
	S_2	=	1,28E-01	=	0		NOK	**min 3**
Step 7	S_3	=	3,33E-01	=	0		NOK	**min 3**
	S_{12}	=	4,17E-01	=	0		NOK	**min 3**
Step 8	S_4	=	82,6446281	=	83		OK	S4 and S5 have to
	S_5	=	82,6446281	=	83		OK	be bigger as here
Step 9								
Step 10	Pdiss	=	1,84E-01	=	184,00	mW		

Second Approach

By **modifying the specifications** entered in the Design Plan, it was possible to achieve **feasible transistor-ratios**

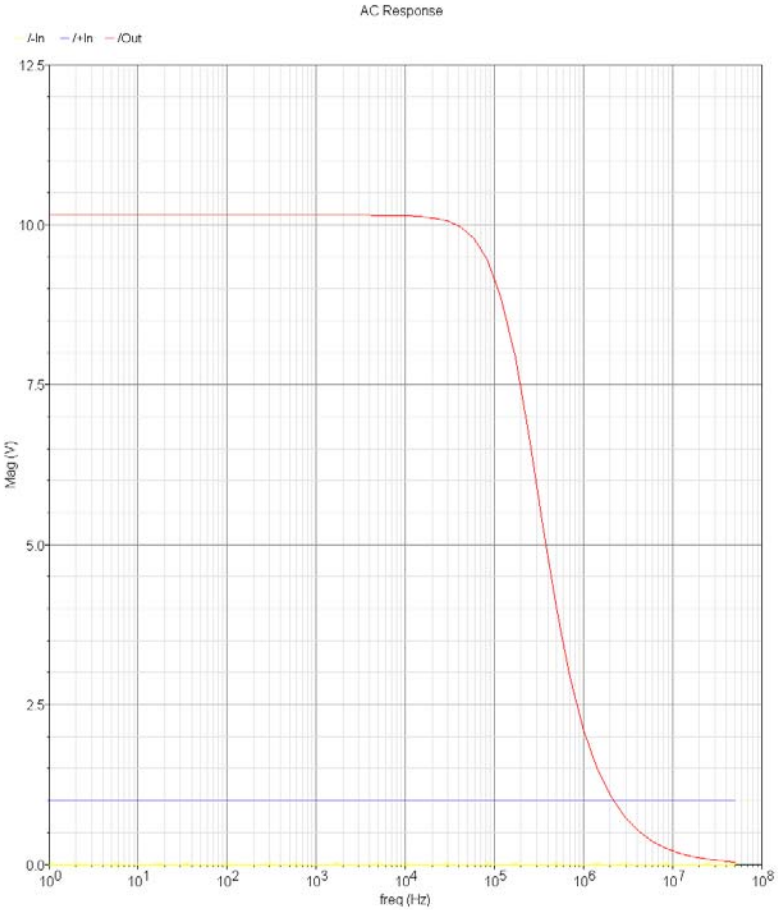
Given Specifications

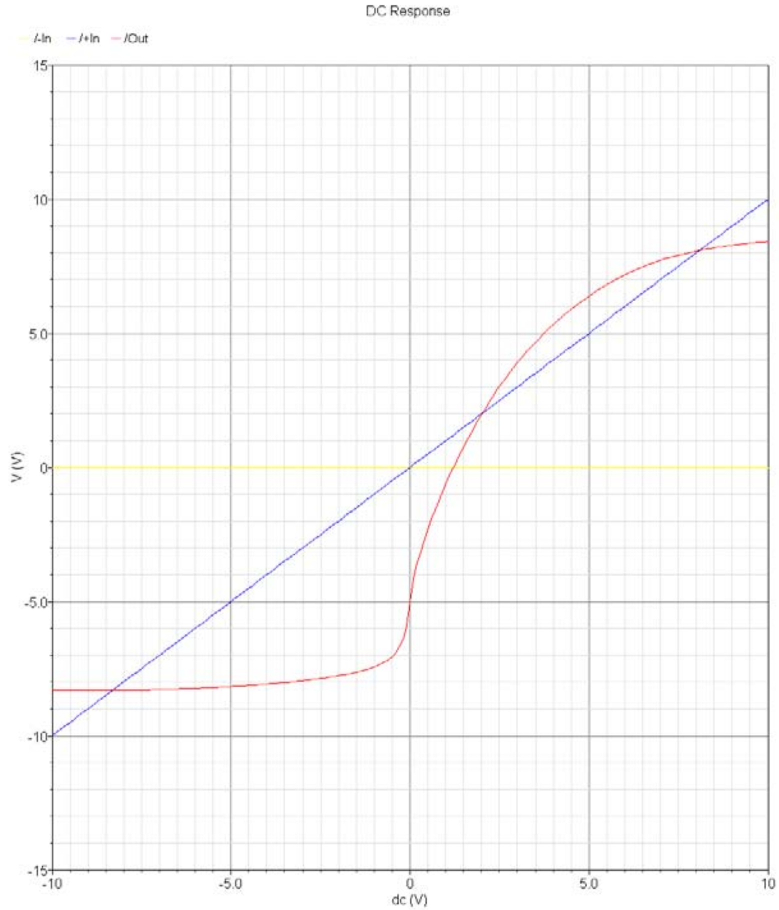
Characteristics	Symbol		Specification Values	
Open loop Gain		>	100	dB
Gain Bandwidth	GB		3,50E+07	Hz
Phase Margin	PM	>	60	°
Settling Time		<	1,00E-06	s
Slew Rate	SR		1,80E+08	V/s
Offset			5,00E-06	V
Input CMR	V_{in}(max)		6	V
	V_{in}(min)		-6	V
Output Swing	V_{out}(max)		7	V
	V_{out}(min)		-7	V
CMRR		>	100	dB
Power Dissipation	P_{diss}		min	
Area Consumption			min	
Voltage Supply	V_{DD}		10	V
	V_{SS}		-10	V
Load Capacitance			1,50E-11	F
Load Resistance		=	1,00E+05	Ohm

Design Plan

Step 1	I_3	=	2,70E-03 A	=	2,70	mA		
Step 2		Factor k		=	1,20			Ratio I_3 to $I_{4,5}$
	I_4	=	3,24E-03 A	=	3,24	mA		
	I_5	=	3,24E-03 A	=	3,24	mA		
Step 3	V_{SD5}	=	1,5 V					
	V_{SD7}	=	1,5 V					
	S_4	=	2,40E+02	=	240		OK	**max 249**
	S_5	=	2,40E+02	=	240		OK	**max 249**
	S_{14}	=	2,40E+02	=	240		OK	**max 249**
		Factor i_{57}		=	1,00			Ratio I_5 to I_7
	S_6	=	2,40E+02	=	240		OK	**max 249**
	S_7	=	2,40E+02	=	240		OK	**max 249**
	S_{13}	=	2,40E+02	=	240		OK	**max 249**
Step 4	V_{DS9}	=	1,5 V					
	V_{DS11}	=	1,5 V					
		Factor i_{79}		=	1,00			Ratio I_7 to I_9
	S_9	=	7,38E+01	=	74			
	S_8	=	7,38E+01	=	74			
		Factor i_{711}		=	1,00			Ratio I_7 to I_{11}
	S_{11}	=	7,38E+01	=	74			
	S_{10}	=	7,38E+01	=	74			
Step 5	R_1	=	4,63E+02	=	463,00	Ohm		
	R_2	=	4,63E+02	=	463,00	Ohm		
Step 6	S_1	=	2,62E+00	=	3		OK	**min 3**
	S_2	=	2,62E+00	=	3		OK	**min 3**
Step 7	S_3	=	1,92E+01	=	19		OK	**min 3**
	S_{12}	=	2,40E+01	=	24		OK	**min 3**
Step 8	S_4	=	111,5702479	=	112		OK	S4 and S5 have to
	S_5	=	111,5702479	=	112		OK	be bigger as here
Step 9								
Step 10	Pdiss	=	2,48E-01	=	248,40	mW		

Second Approach Simulation Results





Second Approach Conclusion

Due to the different characteristics of the H35 technology

- Very little amplification (~ 10)
- High offset (> 1 V)
- High power dissipation (> 400 mW)
- Non-linear

➔ **changing several input specifications for design-plan**

Final Solution

After several attempts a **promising design** was found:

- Low power dissipation
- Relatively small transistors

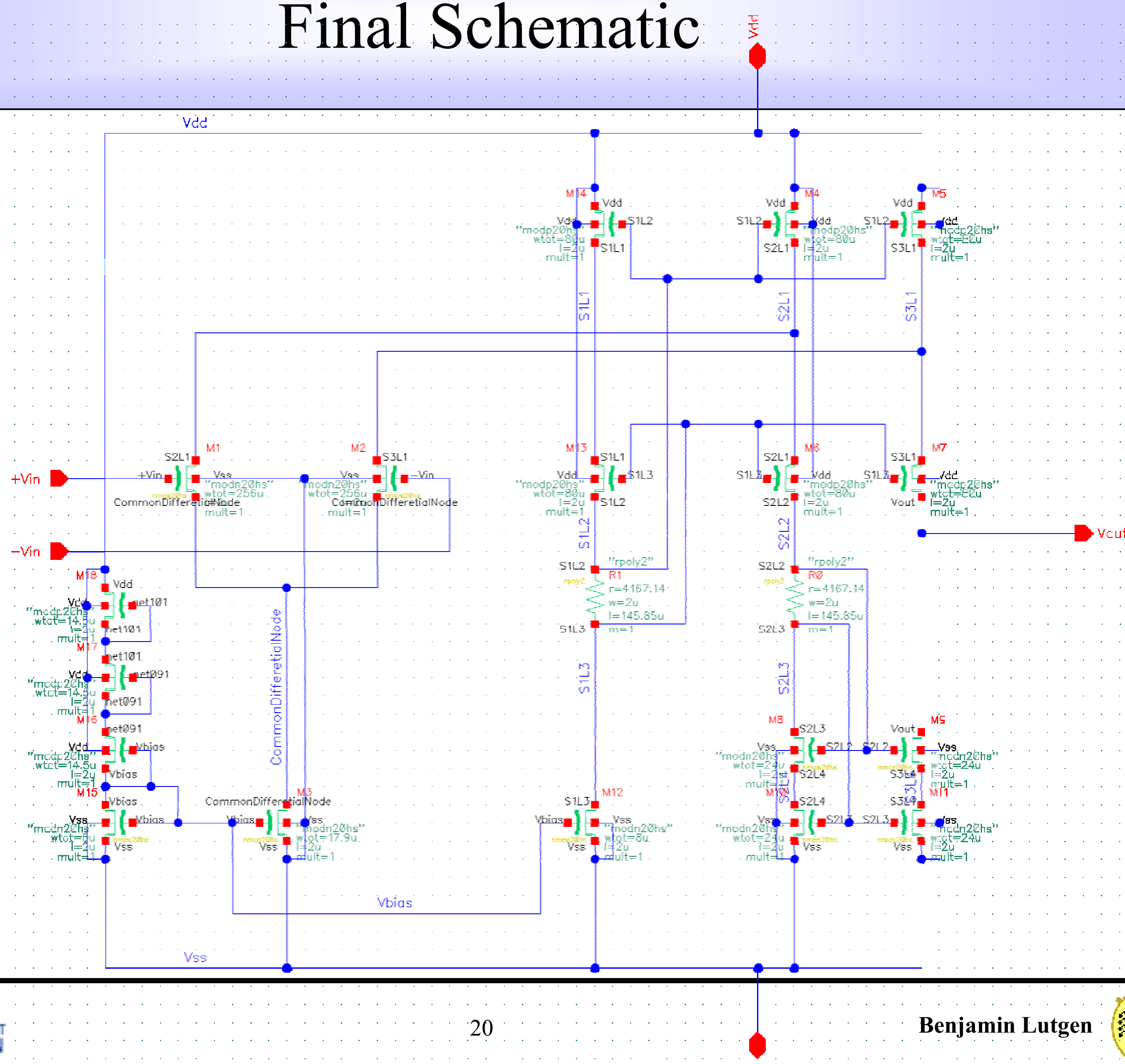
Given Specifications

Characteristics	Symbol		Specification Values	
Open loop Gain		>	100	dB
Gain Bandwidth	GB		1,00E+08	Hz
Phase Margin	PM	>	60	°
Settling Time		<	1,00E-06	s
Slew Rate	SR		2,00E+07	V/s
Offset			5,00E-06	V
Input CMR	V_{in}(max)		6,5	V
	V_{in}(min)		-6,5	V
Output Swing	V_{out}(max)		8	V
	V_{out}(min)		-8	V
CMRR		>	100	dB
Power Dissipation	P_{diss}		min	
Area Consumption			min	
Voltage Supply	V_{DD}		10	V
	V_{SS}		-10	V
Load Capacitance			1,00E-11	F
Load Resistance		=	1,00E+05	Ohm

Design Plan

Step 1	I_3	=	2,00E-04 A	=	0,20	mA	
Step 2	Factor k	=			1,20		Ratio I_3 to $I_{4,5}$
	I_4	=	2,40E-04 A	=	0,24	mA	
	I_5	=	2,40E-04 A	=	0,24	mA	
Step 3	V_{SD5}	=	1 V				
	V_{SD7}	=	1 V				
	S_4	=	4,00E+01	=	40	OK	**max 249**
	S_5	=	4,00E+01	=	40	OK	**max 249**
	S_{14}	=	4,00E+01	=	40	OK	**max 249**
	Factor i_{57}	=			1,00		Ratio I_5 to I_7
	S_6	=	4,00E+01	=	40	OK	**max 249**
	S_7	=	4,00E+01	=	40	OK	**max 249**
	S_{13}	=	4,00E+01	=	40	OK	**max 249**
Step 4	V_{DS9}	=	1 V				
	V_{DS11}	=	1 V				
	Factor i_{79}	=			1,00		Ratio I_7 to I_9
	S_9	=	1,23E+01	=	12		
	S_8	=	1,23E+01	=	12		
	Factor i_{711}	=			1,00		Ratio I_7 to I_{11}
	S_{11}	=	1,23E+01	=	12		
	S_{10}	=	1,23E+01	=	12		
Step 5	R_1	=	4,17E+03	=	4167,00	Ohm	
	R_2	=	4,17E+03	=	4167,00	Ohm	
Step 6	S_1	=	1,28E+02	=	128	OK	**min 3**
	S_2	=	1,28E+02	=	128	OK	**min 3**
Step 7	S_3	=	3,31E+00	=	3	OK	**min 3**
	S_{12}	=	4,14E+00	=	4	OK	**min 3**
Step 8	S_4	=	13,84083045	=	14	OK	S4 and S5 have to
	S_5	=	13,84083045	=	14	OK	be bigger as here
Step 9							
Step 10	Pdiss	=	1,84E-02	=	18,40	mW	

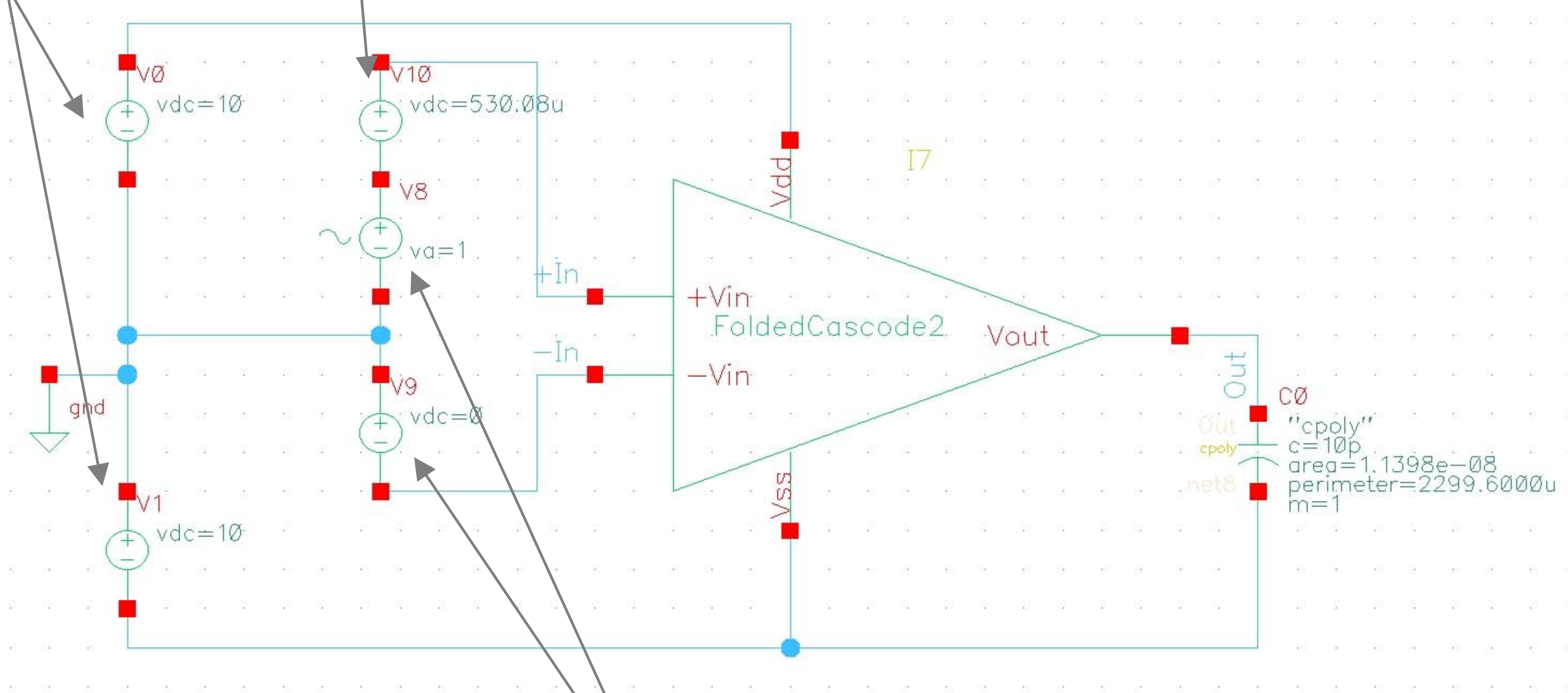
Final Schematic



Measurement Setup

- Offset compensation
- Supply Voltage

For AC and DC analysis



- Signal input

Final Solution Simulation Results (1)

Dependences

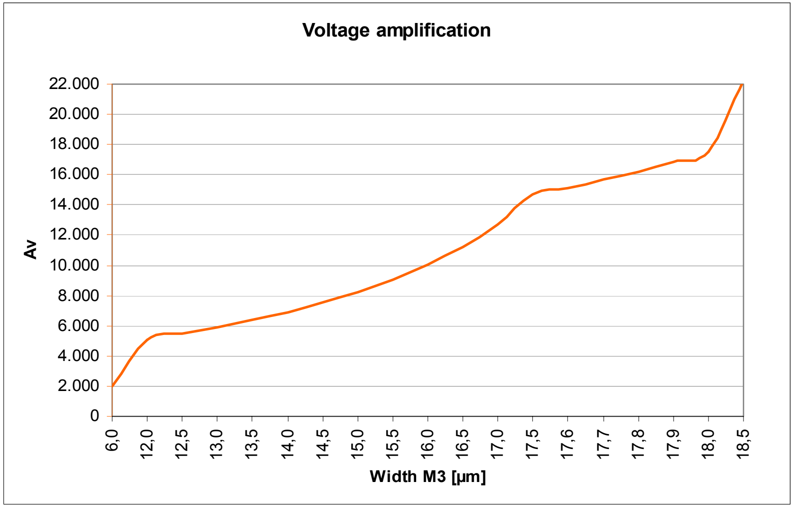
- For increasing the gain it showed out, that the best way was just **increasing M_3** in width, to get more current in the differential pair.
- Changing M_3 even **decreases the offset**

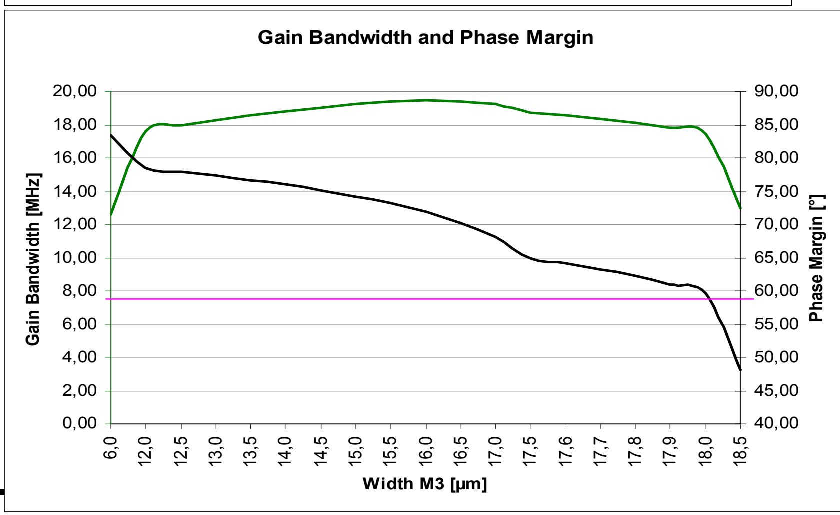
	$M_{1/2}$	M_3	M_{12}	R_1	R_2
Increase Gain	↑	**↑**	↓	↑	↑
Increase Phase Margin	↓	↓	⦸	⦸	⦸
Increase GBW	↑	⌅ ↓ ↑	⦸	⦸	⦸

<u>Legend</u>

↑	Make wider
↓	Make smaller
⌅	Has a maximum
⦸	Not measured

Maximizing Gain (1)



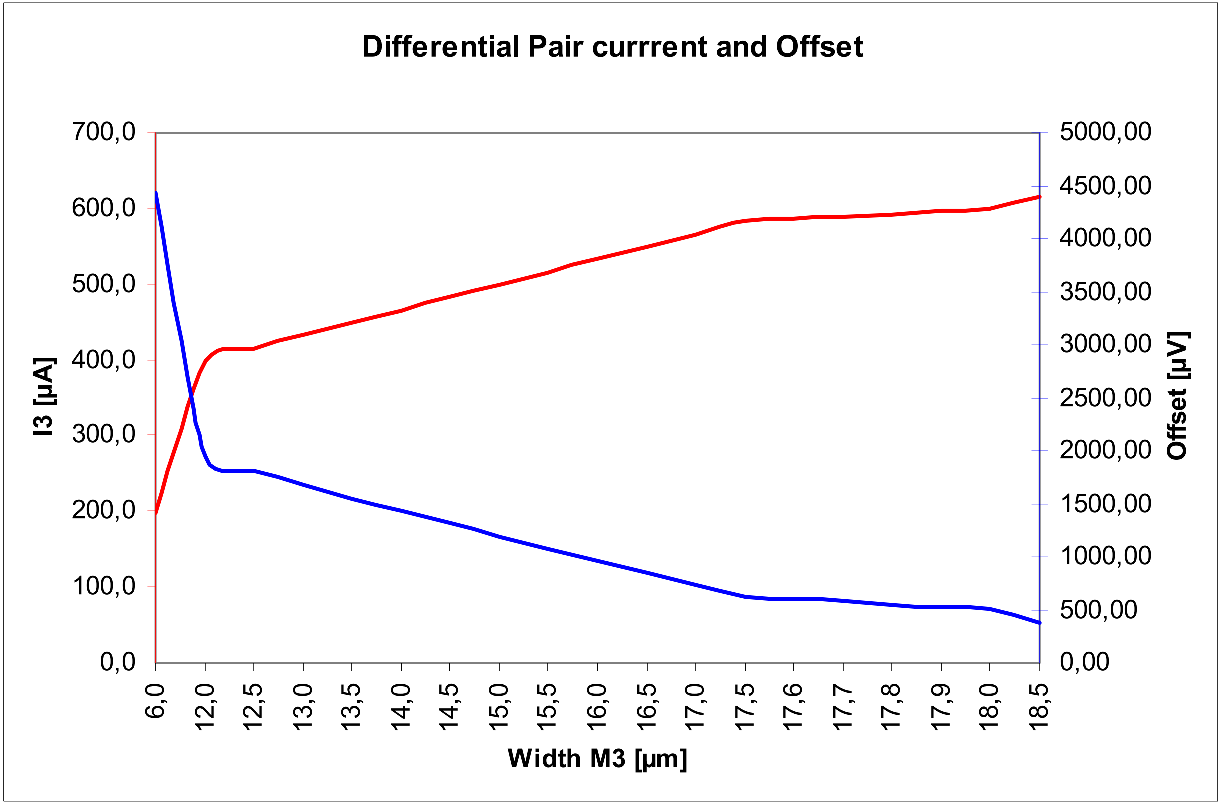


Finding the best width for M_3 with **maximum gain** and **PM > 60°**

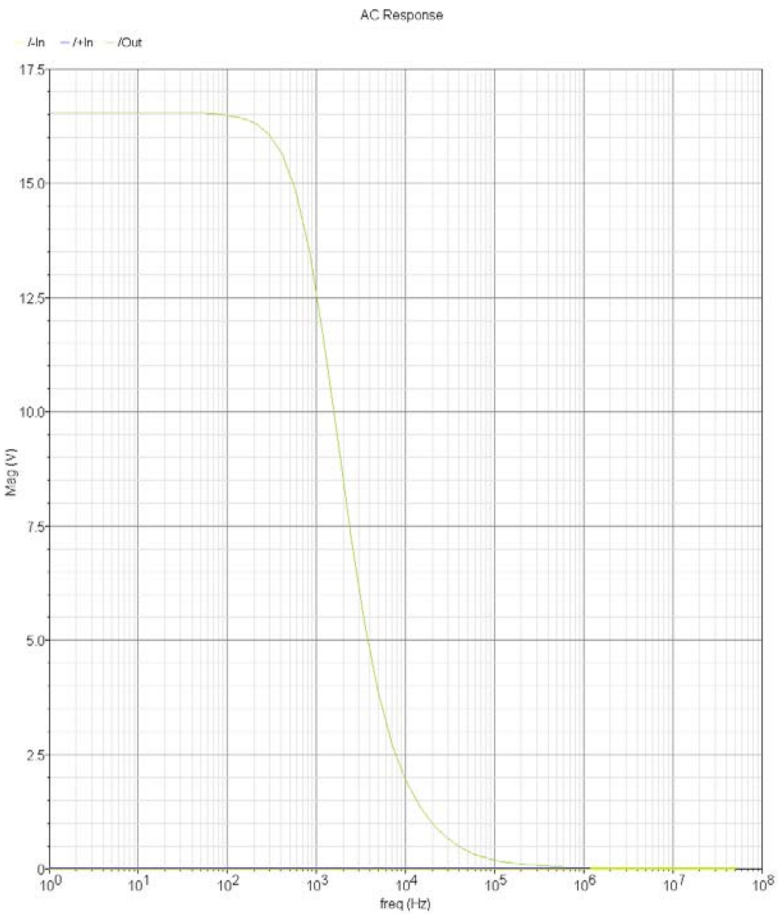
M3	M12	I3	Comp. Offset	Av	GBW	PM
6,0	8,0	198,4 µA	+ 4430,00 µV	2.018	12,59 MHz	83,38 °
12,0	8,0	398,7 µA	+ 1940,00 µV	5.060	17,62 MHz	78,49 °
12,5	8,0	415,5 µA	+ 1810,00 µV	5.440	17,96 MHz	77,94 °
13,0	8,0	432,2 µA	+ 1670,00 µV	5.900	18,28 MHz	77,34 °
13,5	8,0	448,9 µA	+ 1550,00 µV	6.370	18,56 MHz	76,69 °
14,0	8,0	465,6 µA	+ 1430,00 µV	6.910	18,82 MHz	75,97 °
14,5	8,0	482,4 µA	+ 1320,00 µV	7.520	19,04 MHz	75,15 °
15,0	8,0	499,1 µA	+ 1190,00 µV	8.228	19,23 MHz	74,22 °
15,5	8,0	515,8 µA	+ 1070,00 µV	9.060	19,36 MHz	73,14 °
16,0	8,0	532,5 µA	+ 962,38 µV	10.009	19,44 MHz	71,84 °
16,5	8,0	549,3 µA	+ 849,02 µV	11.191	19,41 MHz	70,23 °
17,0	8,0	566,0 µA	+ 735,94 µV	12.681	19,23 MHz	68,10 °
17,5	8,0	582,7 µA	+ 622,27 µV	14.659	18,74 MHz	65,00 °
17,6	8,0	586,0 µA	+ 598,93 µV	15.142	18,57 MHz	64,18 °
17,7	8,0	589,4 µA	+ 576,29 µV	15.658	18,36 MHz	63,26 °
17,8	8,0	592,7 µA	+ 553,38 µV	16.218	18,11 MHz	62,21 °
17,9	8,0	596,1 µA	+ 530,08 µV	16.829	17,80 MHz	60,99 °
18,0	8,0	599,4 µA	+ 506,24 µV	17.502	17,40 MHz	59,55 °
18,5	8,0	616,7 µA	+ 385,05 µV	22.210	12,98 MHz	48,20 °

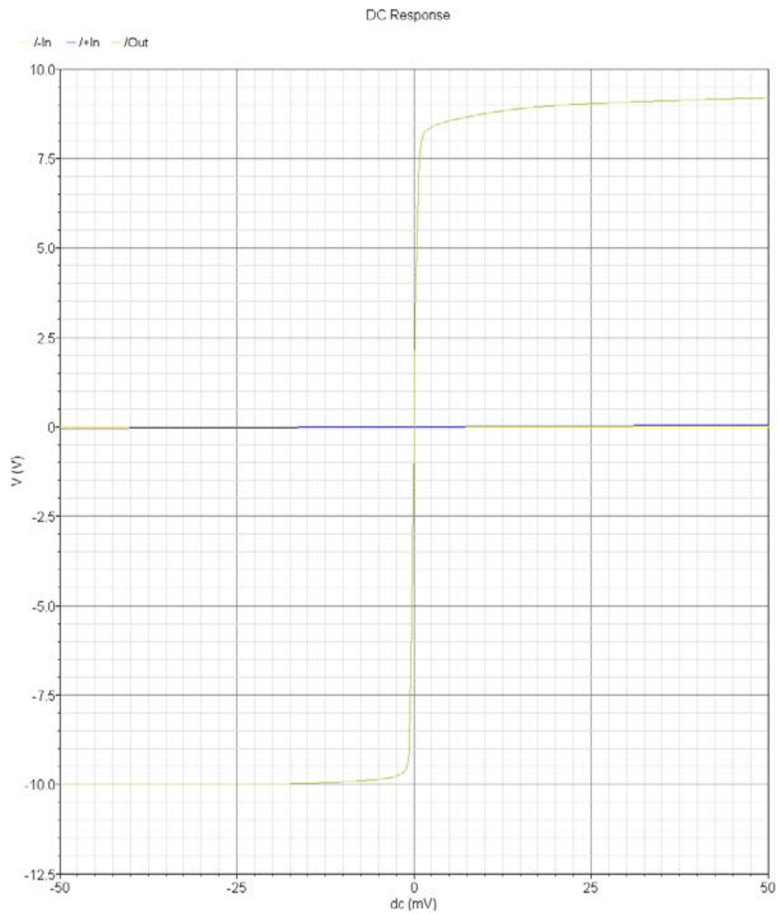
All other transistors according to the final solution values.

Maximizing Gain (2)

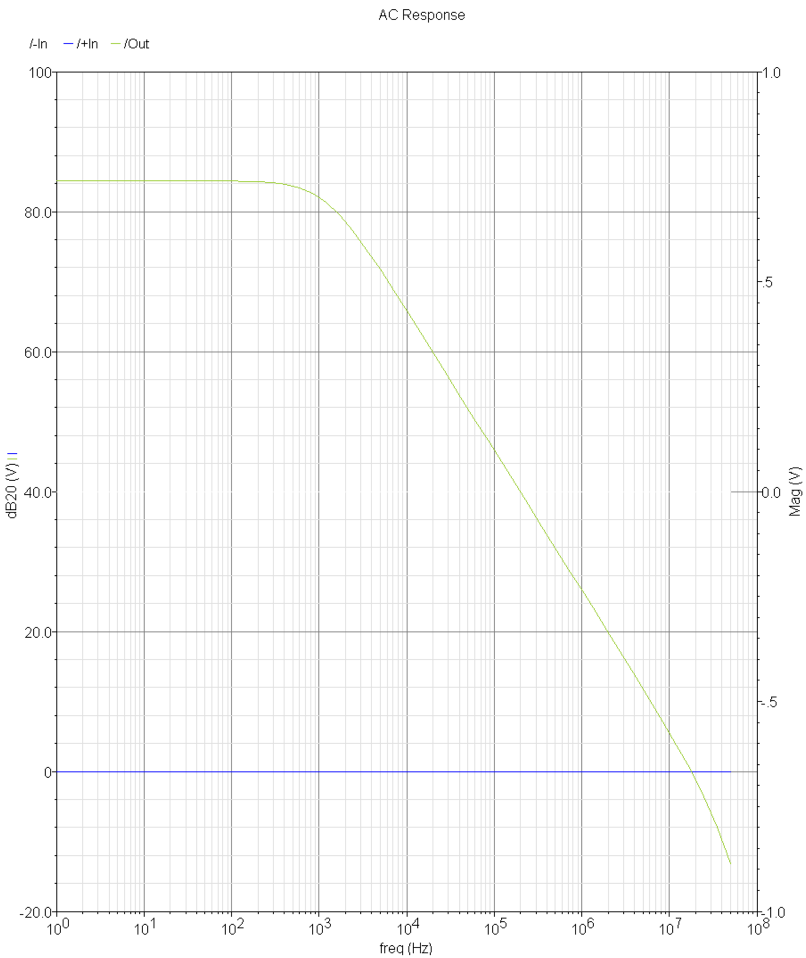


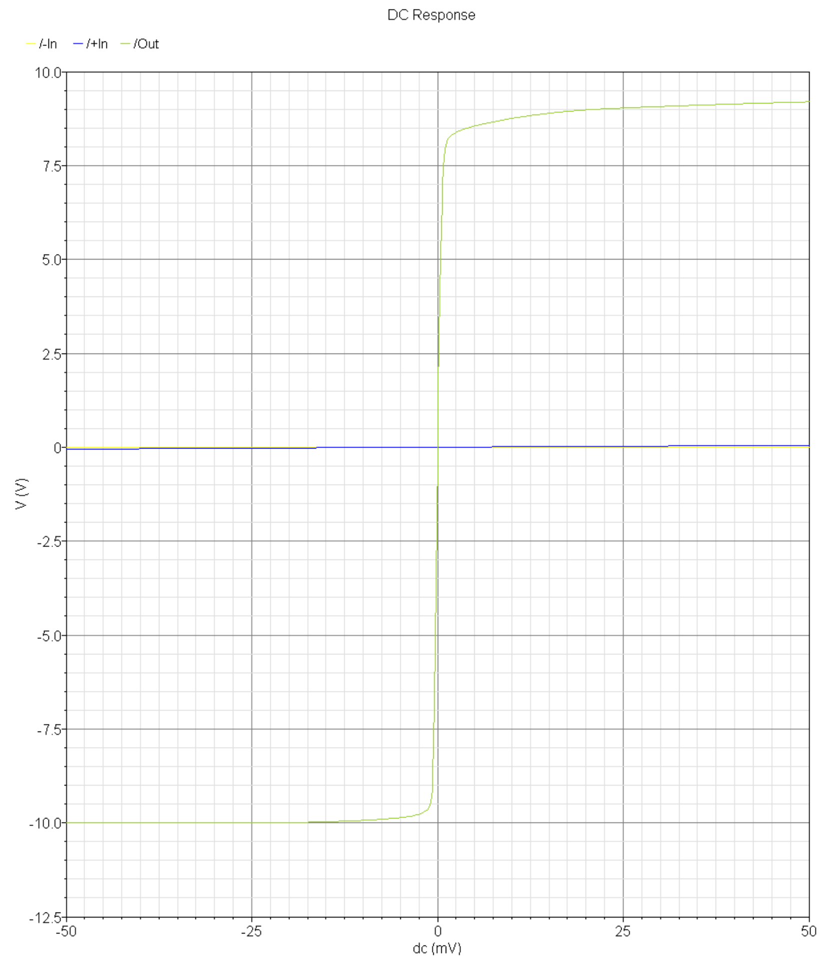
Final Approach Simulation Results (2)
AC Analysis (**linear**) / DC Analysis in Differential Mode



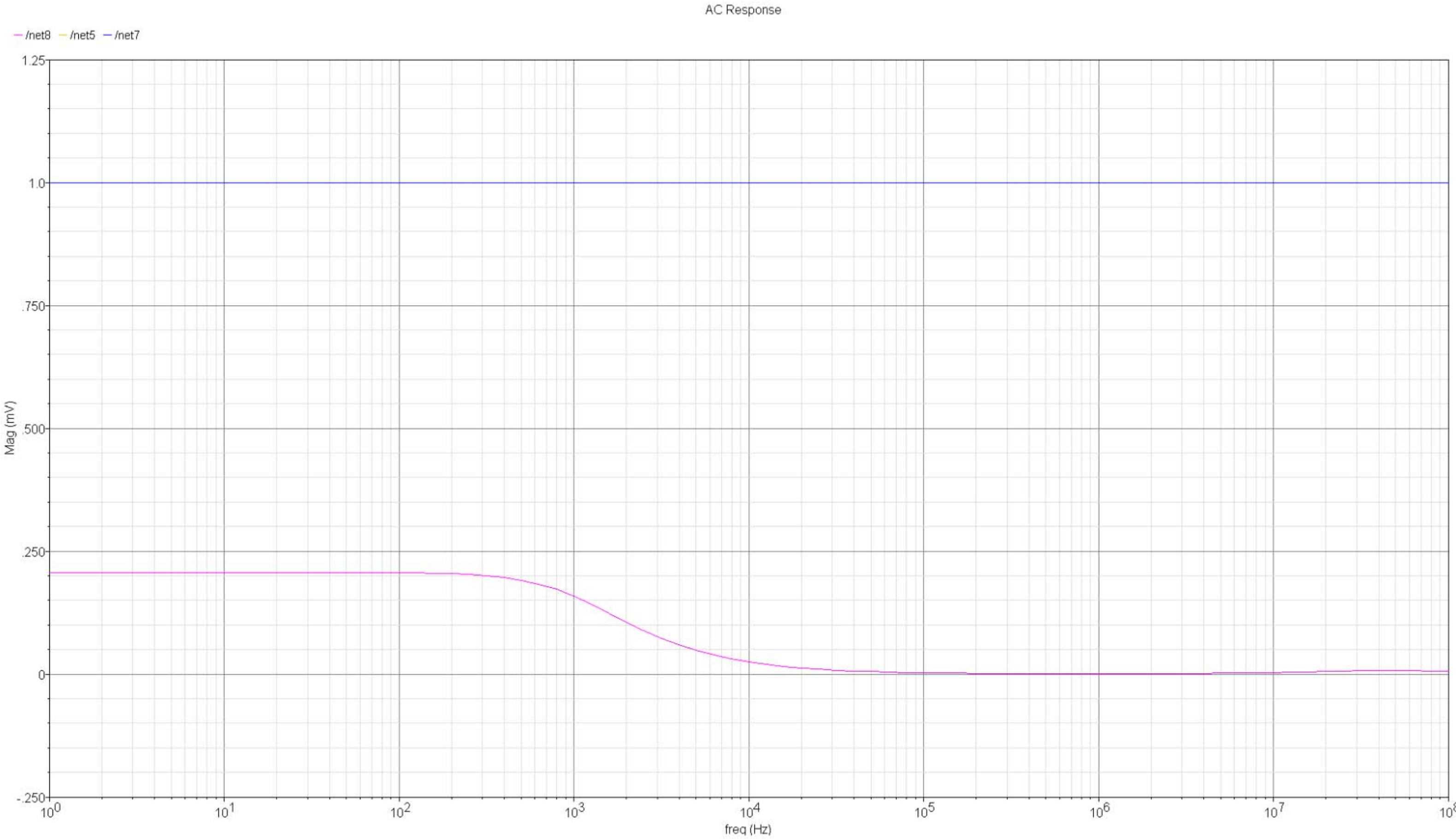


Final Approach Simulation Results (3)
AC Analysis (**dB**) / DC Analysis in Differential Mode





Final Approach Simulation Results (4)
AC Analysis (**linear**) in common mode



Measuring the Characteristics (1)

CMRR [input: sinus with 1 mV amplitude]

Differential mode output: 16829 mV

Common mode output: 0.213 mV

Measured on the plateau at low frequency

$$\frac{16829}{0.213} = 79009.38 \hat{=} \boxed{97.95dB}$$

P_{diss}

Max current in differential mode: 1,106 mA

$$1.106mA \cdot \underbrace{20V}_{V_{\text{supply}}} = \boxed{22.12mW}$$

Area

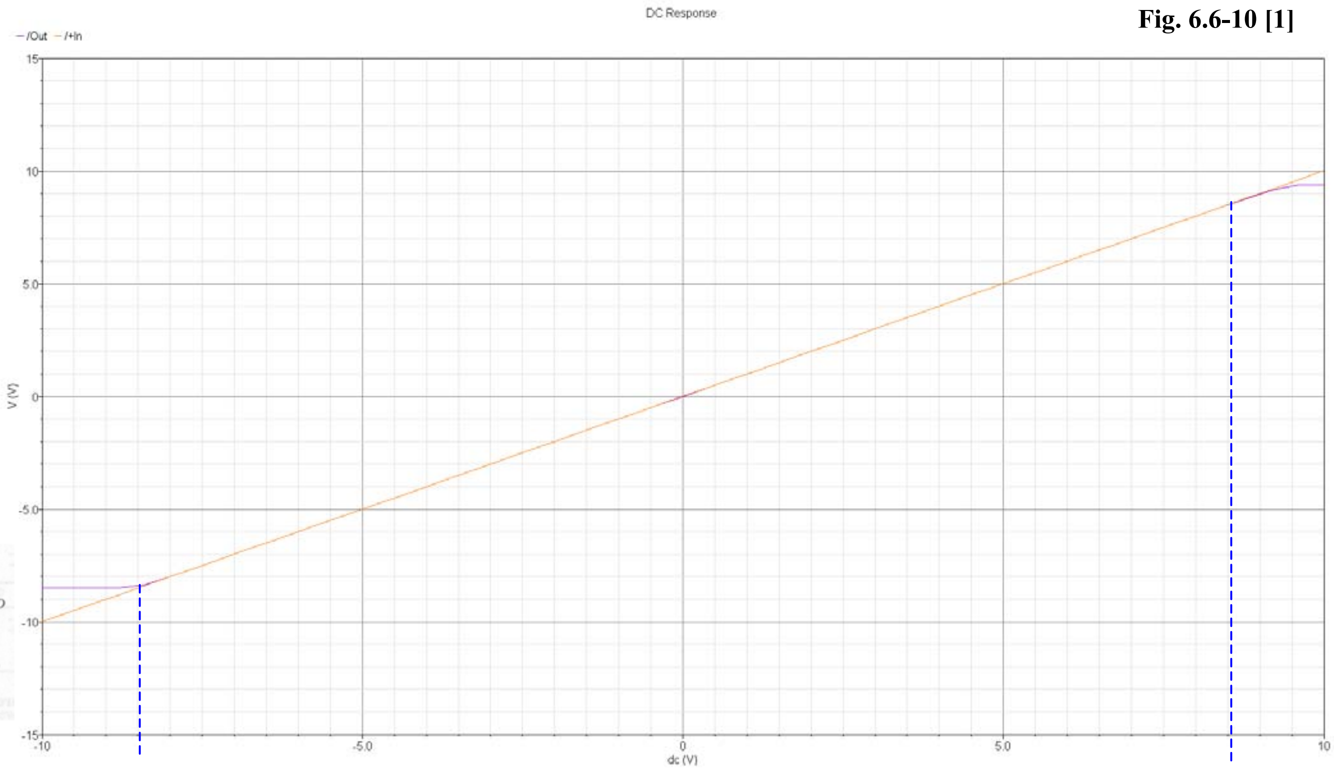
$$155\mu m \cdot 200\mu m = 31000\mu m^2 = \boxed{0.031mm^2}$$

Measuring the Characteristics (2)

ICMR

±8.5 V

Fig. 6.6-10 [1]



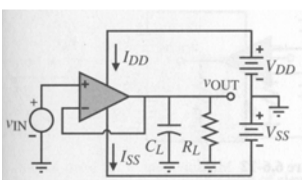


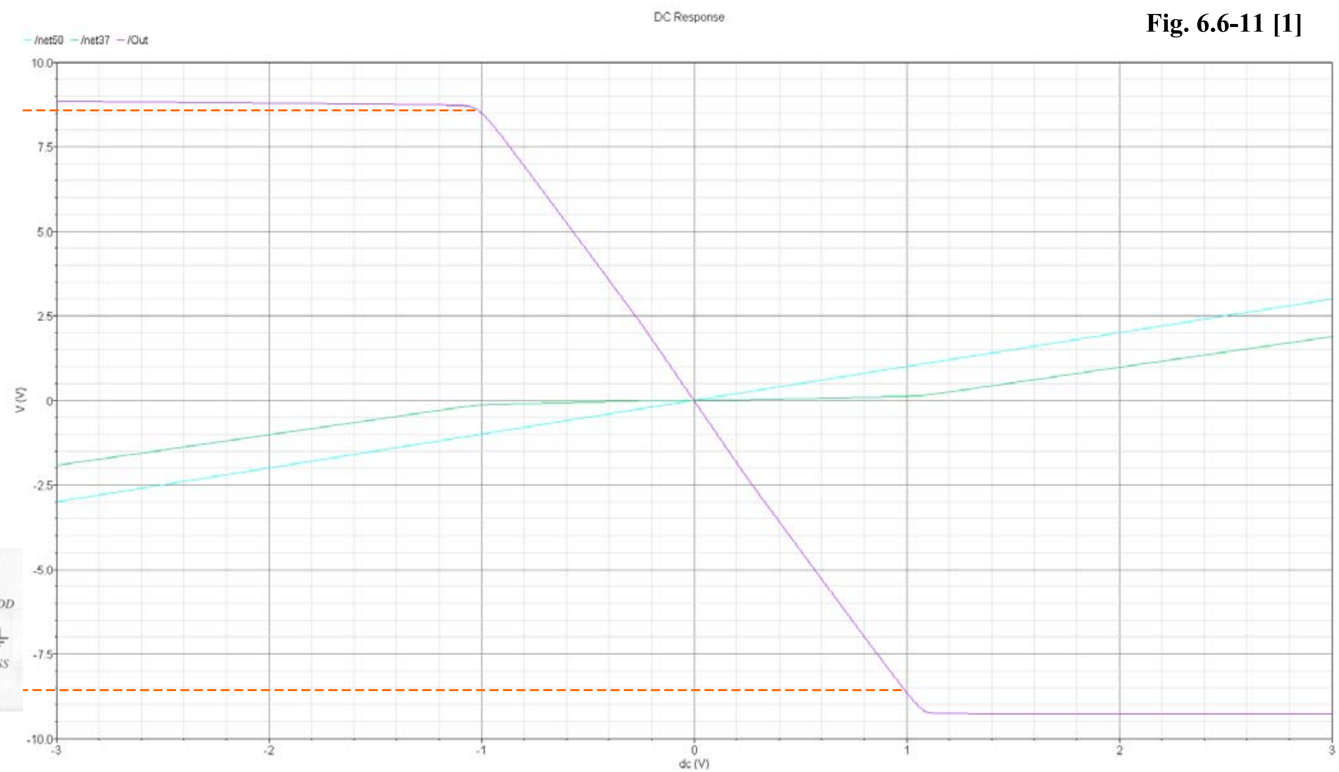
Fig. 6.6-10 [1]

Measuring the Characteristics (3)

Output Swing

±8.6 V

Fig. 6.6-11 [1]



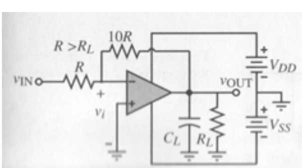


Fig. 6.6-11 [1]

Measuring the Characteristics (4)

Slew Rate

Rise: 27.052.69 V/µs Fall: 35.337 V/µs

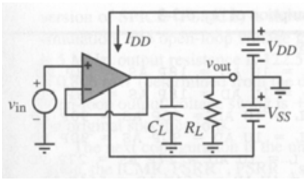
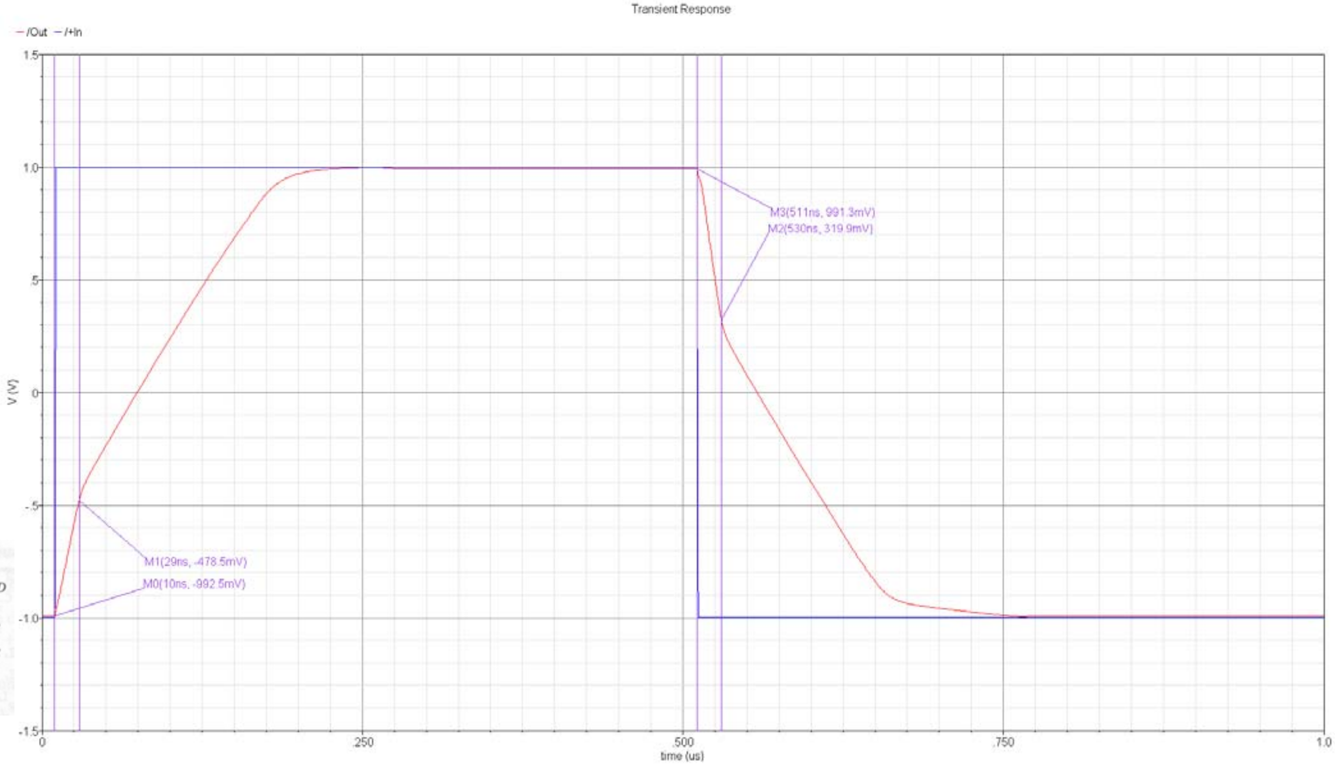


Fig. 6.6-14 [1]

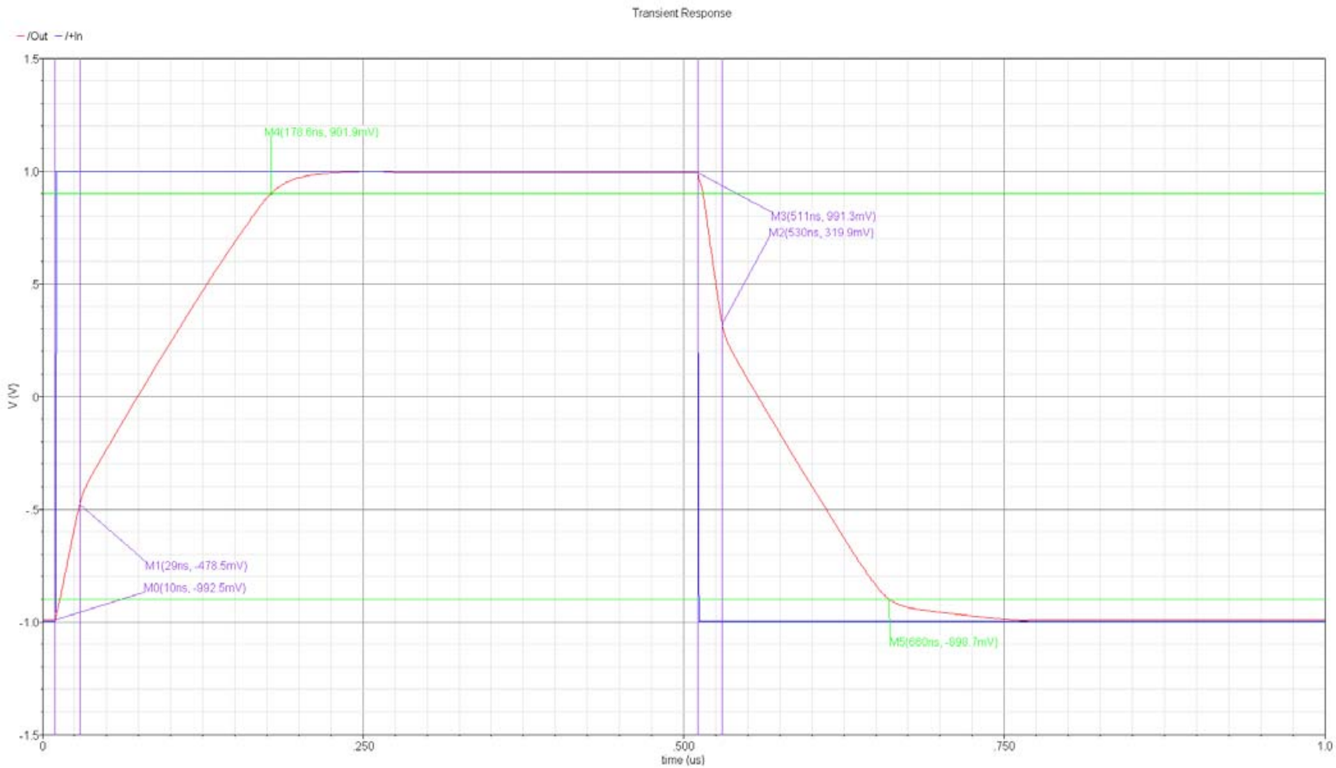


Measuring the Characteristics (5)

Settling Time

Rise: 168.6 ns

Fall: 149.0 ns

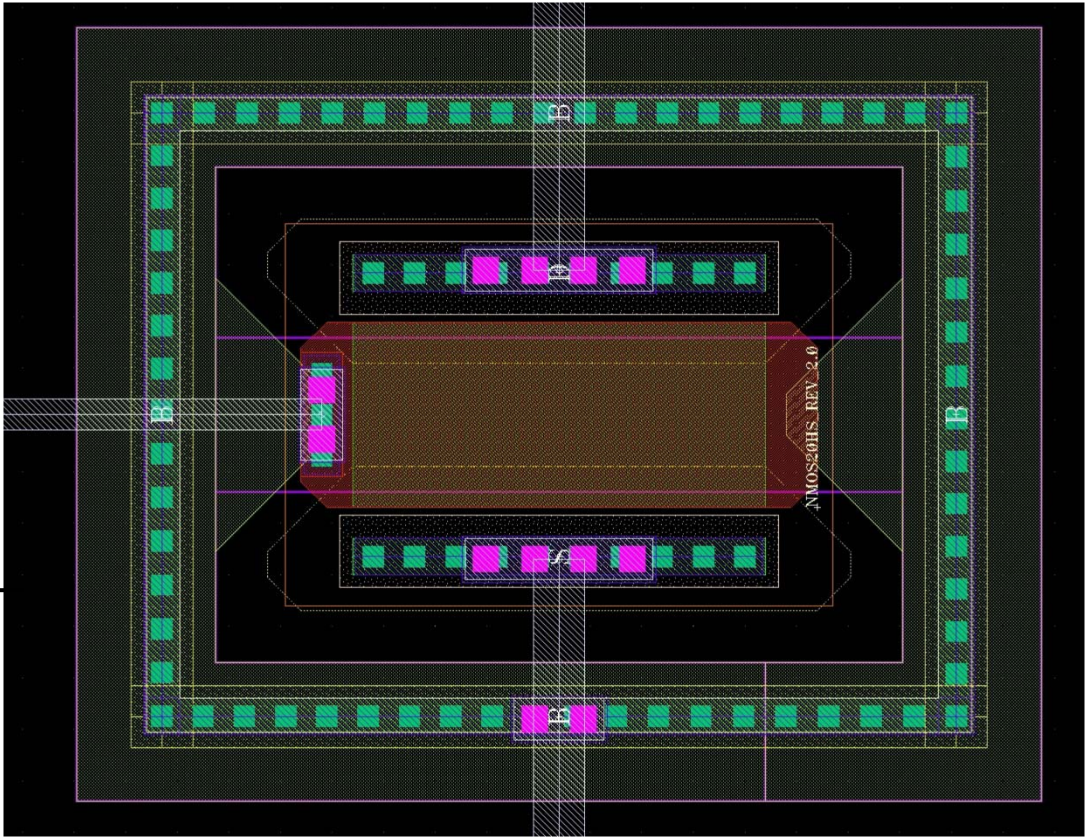


3. Layout Design

High Voltage Layouting (1)

Transistors from high voltage library:

- Many different layers (different doped TUBs)
- Very restrictive layout rules
- Protective structures



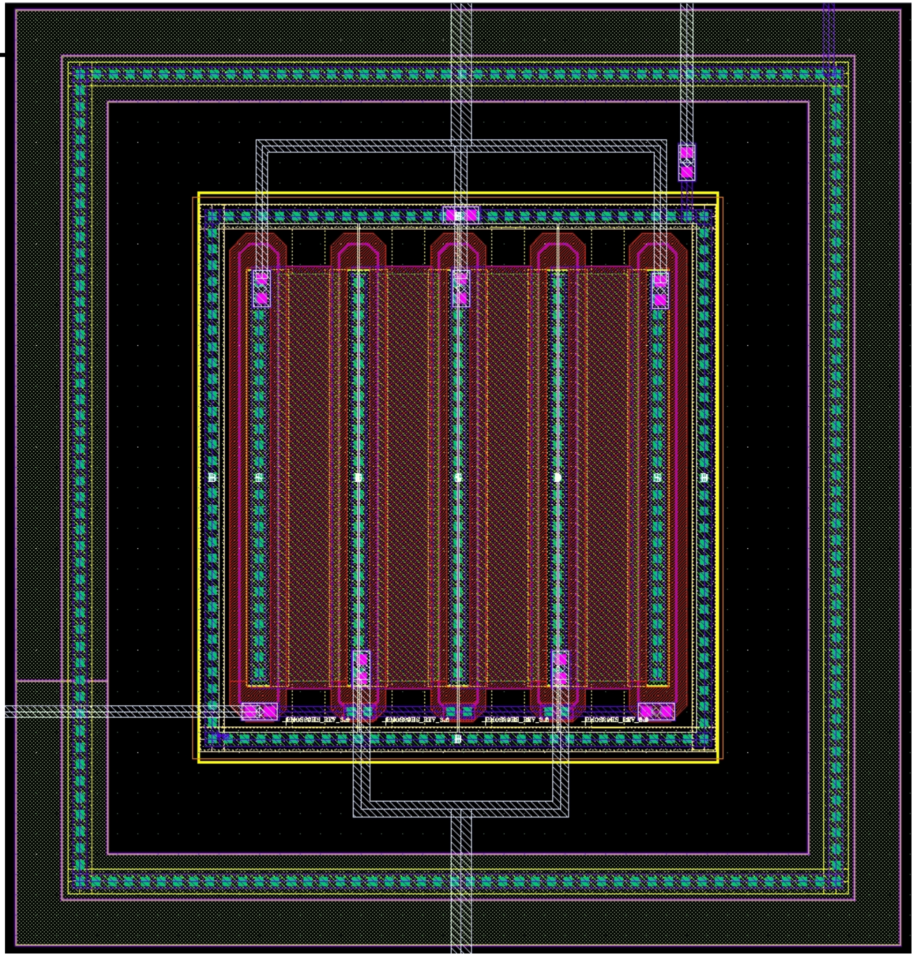
NMOS

- Guard ring (to Vdd)
- For folded Transistors -> multiple Gates

High Voltage Layouting (2)

PMOS

- Inner guard ring (to Vdd)
- Outer guard ring (to Vss)
- For folded Transistors -> common Gate
- Protective Metal1-Layer over the transistor

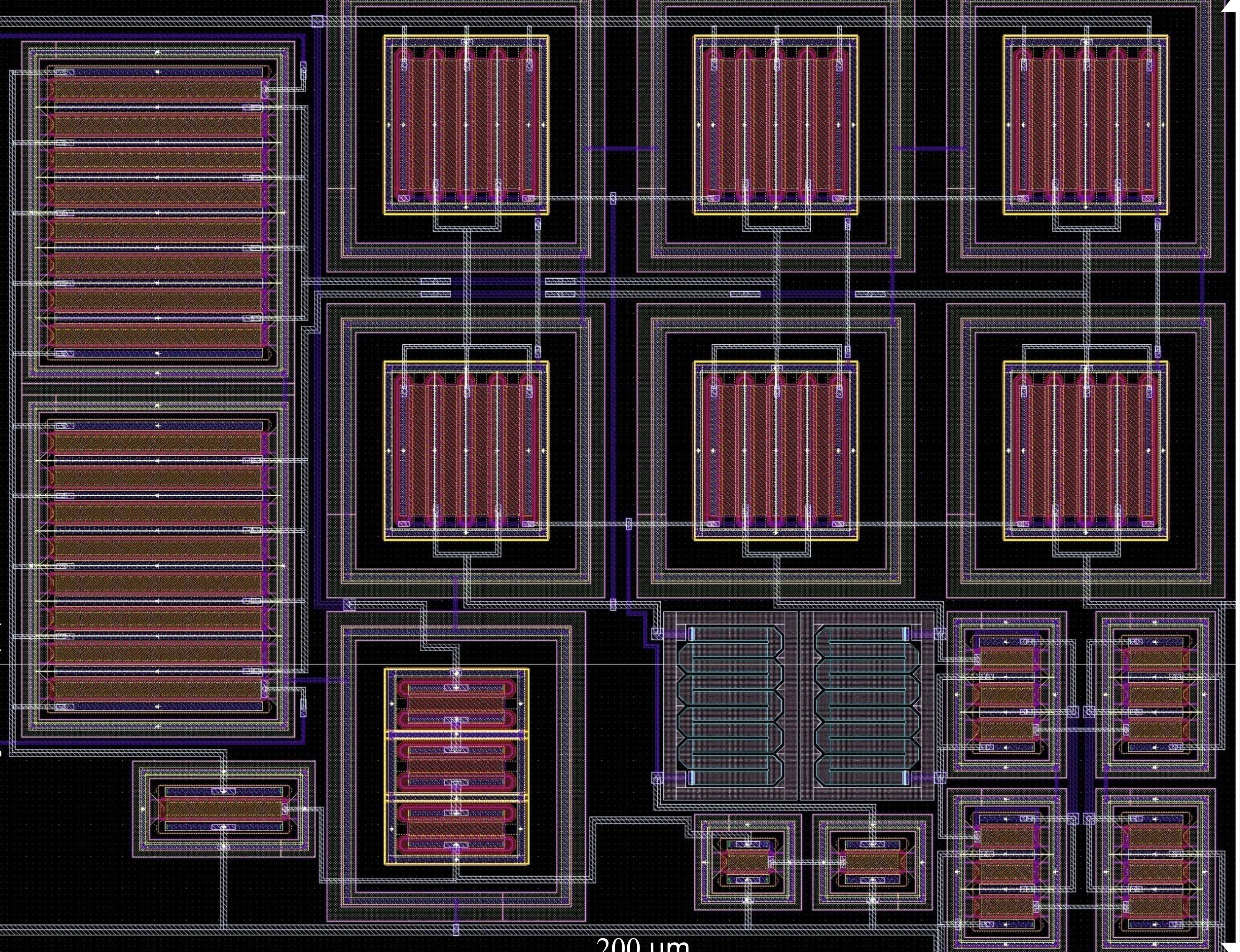


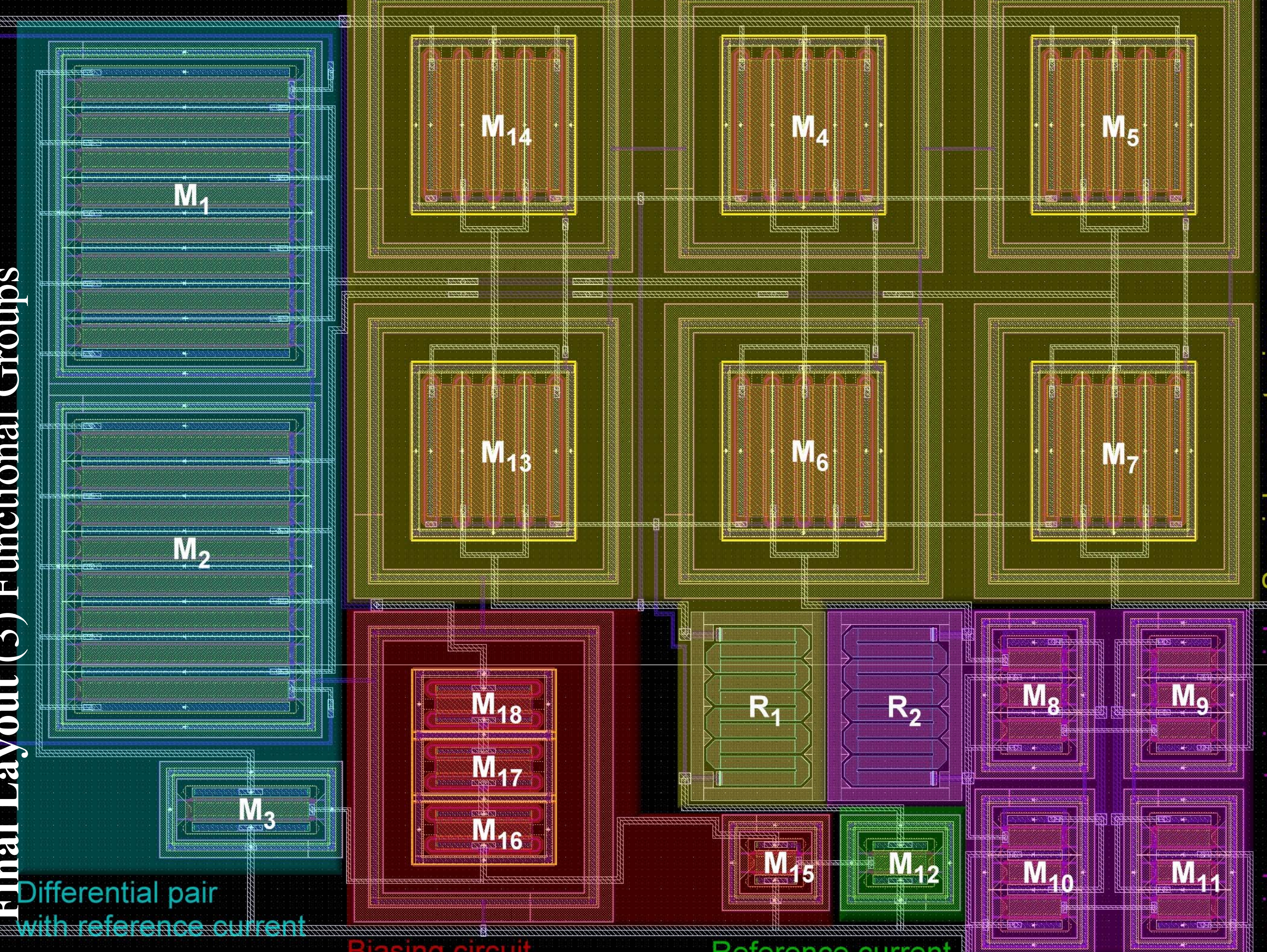
Final Layout (1)

The following layout is only principle

- ➢ Due to the time intensive design plan, there was not enough time to design a matched layout.
  - ➔The actual layout is very sensitive to process variations
- ➢ Matching of the layout is possible

Final Layout (2)




Final Layout (3) Functional Groups
M1
M2
M3
M14
M4
M5
M13
M6
M7
M18
M17
M16
R1
R2
M8
M9
M15
M12
M10
M11
Differential pair
with reference current

LVS Log

```
**************************************************************************************************
*******           FoldedCascode2 schematic TESYS_BL_P1  <vs>  FoldedCascode2 layout TESYS_BL_P1           *******
**************************************************************************************************

Filter/Reduce statistics only. Network matching was OK.

Pre-expand Statistics
======================                                                              Original
Cell/Device                                                                   schematic  layout      //comment for layout
(NMOS20HS) MOS                                                                        9       3*     //(M3, M12, M15)
(PMOS20HS) MOS                                                                        9       1*     //(M17) #
(RPOLY2) RES                                                                          2       0*     //
(_, nmos20hs layout PRIMLIB l="2u" mult="8"       w="  32u" wtot=" 256u") Cell        0       2*     //(M1, M2)
(_, nmos20hs layout PRIMLIB l="2u" mult="3"       w="   8u" wtot="  24u") Cell        0       4*     //(M8, M9, M10, M11)
(_, pmos20hs layout PRIMLIB l="2u" mult="4"       w="  20u" wtot="  80u") Cell        0       6*     //(M4, M5, M6, M7, M13, M14)
(_, pmos20hs layout PRIMLIB l="2u" subGuard=FALSE w="14.5u" wtot="14.5u") Cell        0       2*     //(M16, M18)
(_, rpoly2 layout PRIMLIB Bends=9 Dummy=TRUE l="145.85u" r="4167.14" w="2u") Cell     0       2*     //(R1, R2)
                                                                                 ------  ------
Total                                                                                20      20

Reduce Statistics
=================                                                                   Original            Reduced
Cell/Device                                                                   schematic  layout   schematic  layout
(NMOS20HS) MOS                                                                        9      31*          9       9
(PMOS20HS) MOS                                                                        9      27*          9       9
(RPOLY2) RES                                                                          2       2           2       2
                                                                                 ------  ------      ------  ------
Total                                                                                20      60          20      20

Schematic and Layout Match
```

//# M17 is created from PRIMLIB and then the substrate contacts are removed, to aviod DRC errors. Now M17 is regarded as drawn by user.

4. Summary and Conclusion

Comparison Specification/Achieved Values

S. Nr	Characteristics	Specification values	Values for the Design Plan	Mesured Values Schematic Simulation	Mesured Values Post-Layout Simulation
1	Open loop Gain	> 100 dB	100 dB	84.52 dB (*16829)	84.59 dB (*16954)
2	Gain Bandwidth	10 MHz	100 MHz	17.80 MHz	15.809 MHz
3	Phase margin	> 60 °	60 °	60,99 °	52.09 °
4	Settling Time	< 1 µs	1 µs	74.09 ns	-
5	Slew Rate	200 V/µs	20 V/µs	25.693 V/µs	-
6	Offset	5 µV	5 µV	530 µV	-
7	Input CMR	± 6 V	± 6.5 V	± 8.5 V	-
8	Output Swing	± 8 V	± 8 V	± 8.6 V	-
9	CMRR	> 100 dB	100 dB	97.95 dB	-
10	Power Dissipation	Minimum	Minimum	22.12 mV	-
11	Area Consumption	Minimum	Minimum	-	31000 μm^2
12	Voltage Supply	20 V	20 V	20 V	20 V
13	Load Capacitance	10 pF	10 pF	10 pF	10 pF
14	Load Resistance	100 kΩ	100 kΩ	100 kΩ	100 kΩ
	Comp. Offset	-	-	530.08 µV	2.634 mV

Discussion

- It was not possible to reach all the specifications, but also some specifications were exceeded.
- The **HV** design just reached a gain of **84.5 dB**, mostly limited by the lower K'-values . A **low voltage** folded cascode op amp should easily reach **more than 100 dB or even 120 dB**.
- The offset of the op amp is very high, and tentatively compensated by an external voltage source.
- The slew rate/settling time diagram shows an **unusual, non smooth characteristics**

Conclusion

- Analyzing, understanding the topology, getting good transistor values from the design plan [1] and get better gain and more stability was **very difficult and time intensive** because the HV-technology has **not the same behavior** than a low voltage technology.
- Assura (layout checking tool) had problems recognizing the pins during the LVS (**L**ayout **V**s **S**chematic) check
  - Solution: changing the rule-file “extract.rul” according to [4]
- The designed operation amplifier is not excellent, but on schematic level **good enough to be used in an application**.

References

[1] Allen/Holberg - **CMOS Analog Circuit Design** (Second ed. 2002) - Oxford University Press

[2] Prof. Andreas König - **Electronics II** Script - WS 07/08

[3] Prof. Andreas König - **TESYS** Script - SS 08

[4] Martin Hetterich - Untersuchung der Realisierbarkeit eines generisch rekonfigurierbaren Sensorelektronikbausteins in einer 0,35µm Hochvolt-CMOS-Technologie - 2009

Used Tools

- Sun Solaris 9.2
- Cadence HIT-Kit v3.72
- Assura v3.1
- Austriamicrosystems' high voltage transistor-technology (20V) **H35**

Thank You

END