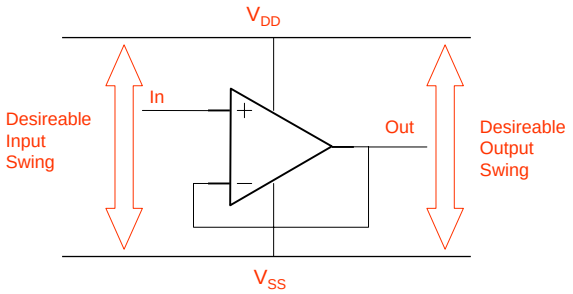
Rail-to-Rail Opamps

Andreas Kaiser
IEMN - ISEN

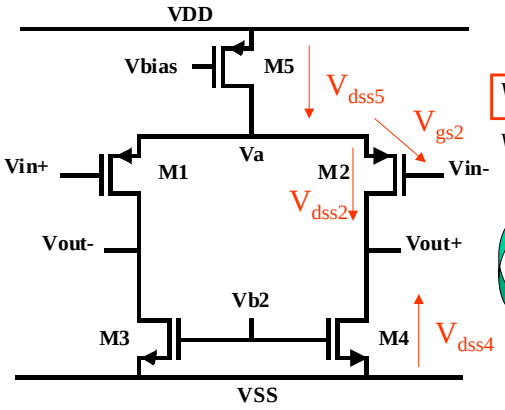
Low Voltage Design Goals



Input Common-Mode Voltage = Input Voltage

Optimize Performance { Rail-to-Rail Output Voltage; Rail-to-Rail Input Common-Mode Voltage

Opamp voltage limitations: PMOS Diff pair Input CM Voltage



$$V_{CM_{in\,max}} = V_{DD} + V_{DSS5} + V_{GS2}$$

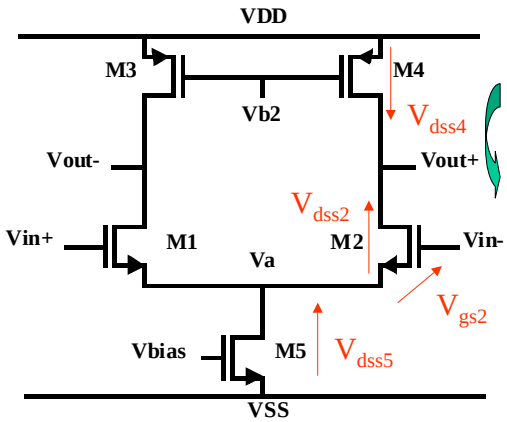
$$V_{CM_{in\,min}} = V_{SS} + V_{DSS4} - V_{DSS2} + V_{GS2}$$

$$V_{CM_{in\,min}} = V_{SS} + V_{DSS4} + V_{TP}$$

can be close to VSS or even below !

P-channel MOS differential pair

Opamp voltage limitations: NMOS Diff pair Input CM Voltage



can be close to VDD or even beyond !

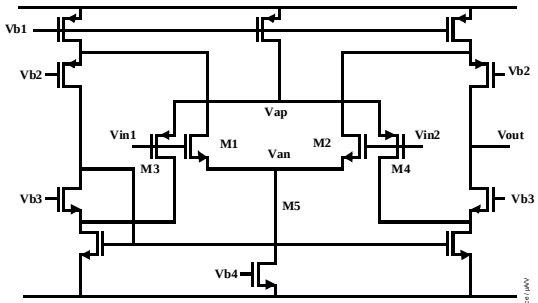
$$V_{CM_{in\,max}} = V_{DD} + V_{DSS4} - V_{DSS2} + V_{GS2}$$

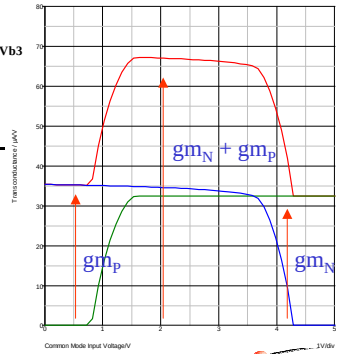
$$V_{CM_{in\,max}} = V_{DD} + V_{DSS4} + V_{TN}$$

$$V_{CM_{in\,min}} = V_{SS} + V_{DSS5} + V_{GS2}$$

N-channel MOS differential pair

Rail-to-Rail Input Stage (S.E.)



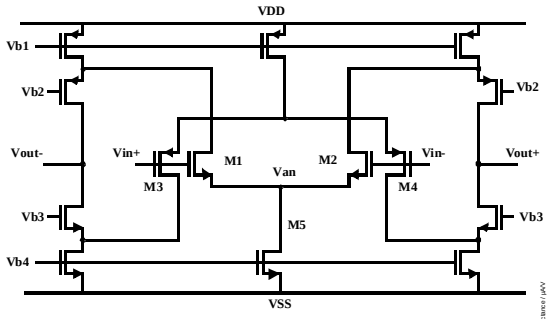


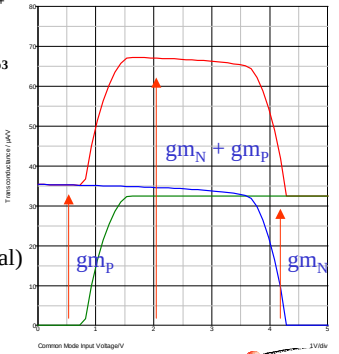
Combination of NMOS + PMOS Differential Pair

Here: folded cascode type amplifier structure (S.E.)

- Rail-to-Rail Input CM Range
- Non-constant Gm !!!

Rail-to-Rail Input Stage (diff.)



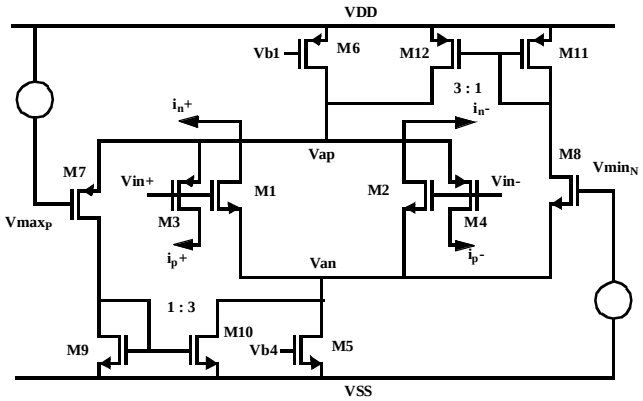


Combination of NMOS + PMOS Differential Pair

Here: folded cascode type amplifier structure (differential)

- Rail-to-Rail Input CM Range
- Non-constant Gm !!!

Constant Gm Input Stage

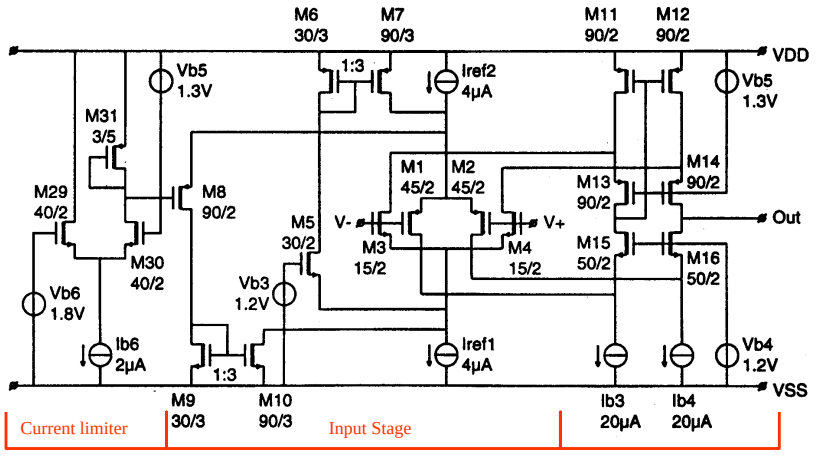


$V_{CM} > Vmax_p$: NMOS Diff pair, bias = 4 x I0

$Vmax_p > V_{CM} > Vmin_n$: NMOS Diff pair + PMOS Diff pair, bias = I0

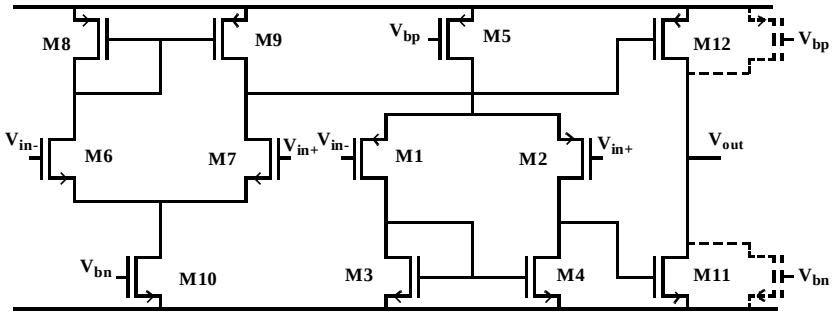
$V_{CM} < Vmin_n$: PMOS Diff pair, bias = 4 x I0

Constant Gm Cascode Amplifier



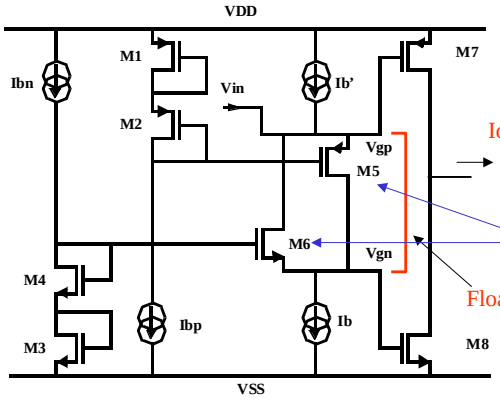
V_{DD} = 3.3V, 1.2µ CMOS Technology

2-stage Amplifier Rail-to-Rail Structure



Constant – Gm structure could be used as well !

Class A-B Gain stage



$Iout_{max}$ > Ibias

same gm !!

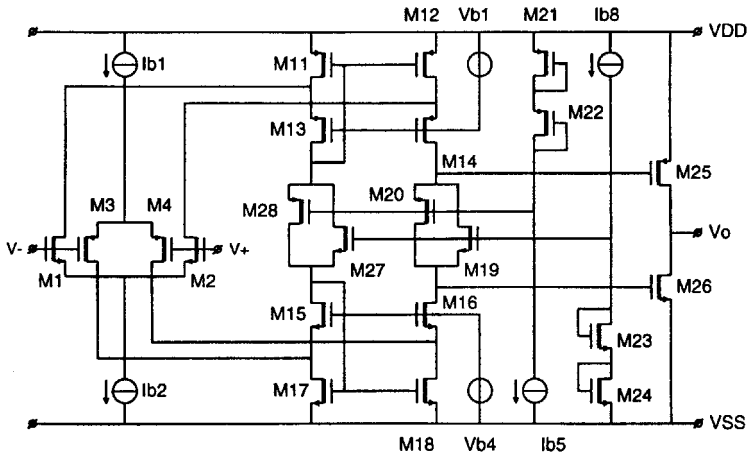
Floating Constant Voltage Source

Bias

Low quiescent power

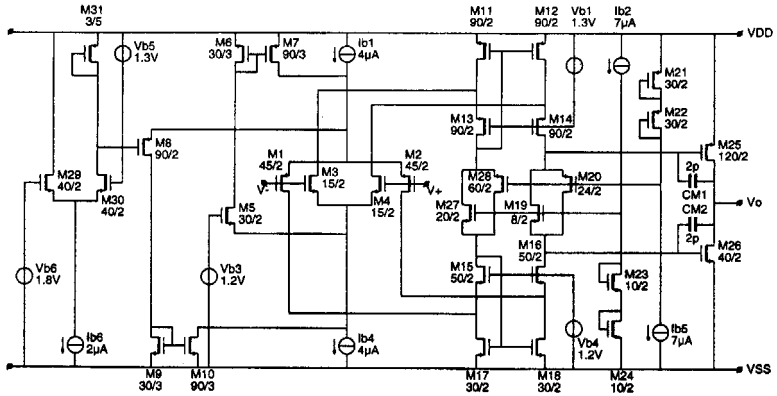
High slew rate (capacitive load)

Complete class A-B amplifier



Bias currents fixed by loops M21-M22-M28-M11 and M24-M23-M27-M17

Rail-to-Rail Class A-B Amplifier



Ron Hogervorst, John P. Tero, Ruud G. H. Eschauzier, Johan H. Huijsing;
A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries,
IEEE Journal of Solid-State Circuits, vol. 29, pp. 1505 - 1513, December 1994.

Opamp Performance

Parameter	opamp1	opamp2	
Die area	0.04	0.04	mm^2
Supply voltage range	2.5-6	2.5-6	V
Quiescent current	180	180	µA
Peak output current	3	3	mA
Common-mode input range V_{step}: from 3 V to 6V V_{step}: from 2.5 V to 2.9V	V_{SS}-.4 to V_{DD}+.5 V_{SS}-.4 to V_{DD}-1.4	V_{SS}-.4 to V_{DD}+.5 V_{SS}-.4 to V_{DD}-1.4	V
Output voltage swing	V_{SS}+0.1 to V_{DD}-0.2	V_{SS}+0.1 to V_{DD}-0.2	V
Offset voltage	4.0	5.0	mV
Input noise voltage@ 10 kHz	22	31	nV/√Hz
CMRR V_{common}: from V_{SS}-.4V to V_{SS}+1V and from: V_{SS}+1.3V to V_{DD}-1.3V and from V_{DD}-1V to V_{DD}+.5 V_{common}: from V_{SS}+1 V to V_{SS}+1.3V and from V_{DD}-1.3V to V_{DD}-1V	70 43	70 43	dB
Open-loop gain	85	87	dB
Unity-gain frequency	2.6	6.4	MHz
Unity-gain phase-margin	66	53	°
Slew-rate V_{common}: from V_{SS}+1.3V to V_{DD}-1.3V V_{common}: from V_{SS}-.4V to V_{SS}+1V and from V_{DD}-1V to V_{DD}+.5	2 4	4 8	V/µs
Large signal settling time (1%) V_{step}= 1V	440	275	ns
Small signal settling time (1%) V_{step}=100 mV	220	180	ns

TABLE I
MEASUREMENT RESULTS Vsupply = 3.3 V, Rload = 10 kΩ, Cload = 10 pf, TA = 27°C, UNLESS OTHERWISE STATED

Table I: Measurement results Vsupply=3.3V, Rload=10kΩ, Cload=10 pF, TA=27°C, unless otherwise stated

Opamp 1 refers to the compact opamp with Miller compensation

Opamp 2 refers to the compact opamp with cascoded Miller compensation