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Design of a MOS double folded cascode Op-Amp with 61dB of gain and 128 MHz of unity gain bandwidth for a Low-Pass Filter application

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***Abstract* -- This paper describes the design of a MOS operational amplifier with an Input Common-Mode Range between 1.25 V and 2.5 V, a gain greater than 50 dB and a unity gain bandwidth greater than 20 MHz. The Common-Mode Range and the high gain were achieved through a double folded cascode topology with NFETS as the input amplifiers.**

The purpose of this operational amplifier is to be used in a low pass filter, resulting in 20 dB of gain and a 1 MHz cutoff frequency.

Keywords- operational amplifier, op-amp, input common-mode range, differential gain, common mode gain, phase margin, common-mode rejection ratio (CMRR), double folded cascode, low pass filter (LPF).

I. INTRODUCTION

IN the design attempted, the goal was to have an operational amplifier (op-amp) meet predetermined specifications (table 1) using 0.13 μm SiGe technology. These specifications have to be maintained at 0 C, 27 C and 100 C of temperature, and at a voltage variation of +/-10% of the nominal supply voltage. Moreover, all bias currents have to be derived from a 100 μA reference current and V_{GS}, V_{GD} and V_{DS} in every MOS transistor may not exceed 1.2 V.

In order to accomplish these specifications, the op-amp is designed with three stages, shown in figure 2.

The first stage consists of an external 100 μA current source and an array of current mirrors. From this stage, the proper voltages and currents for the other two stages are derived. The second stage is the differential input stage, where input NMOS transistors, combined with the folding of the third stage, produce a high swing input voltage. And finally, the third stage shows the remaining part of the double folded cascode, which increases the gain in order to meet the desired specifications.

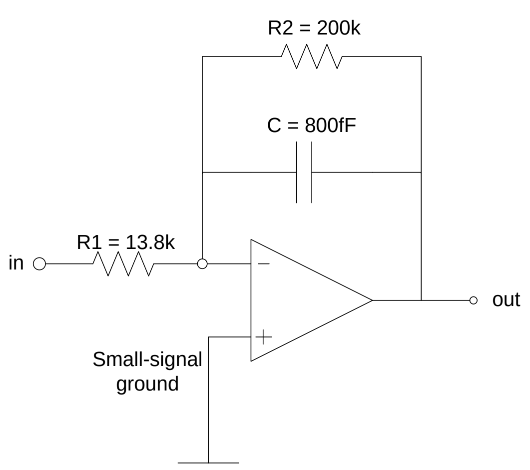

Fig. 1 - Low-pass filter schematic

After the operational amplifier was designed, the op-amp was tested in a Low-Pass Filter configuration, as shown in figure 1, with the final component values yielding 1 MHz of cutoff frequency and a 20 dB gain.

TABLE I
OPERATIONAL AMPLIFIER SPECIFICATIONS

Specification	Target	Final design
Gain	>50 dB	61 dB
Unity Gain Bandwidth	>20 MHz	128 MHz
Supply Voltage (V_{DD})	Pick one: 1.0 V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V	2.5V
Input Common-Mode Range	$V_{DD}/2<V_{INCM}<V_{DD}$	Range met
CMRR	>70 dB	92 dB
I_{REF}	100μA	--
Phase Margin	>45 degrees	64 degrees

II. CIRCUIT DESIGN

Before deciding that the double folded cascode was the correct design to accomplish the specifications, several other designs were tested. Among the designs simulated, the two-stage CMOS [1] and the wide-swing Current Mirror were fairly close, but the gain was not adequate and the input swing was limited. Therefore, the double folded cascode was chosen as the final design to provide enough gain and input swing.

In the schematic (figure 2), the left side, or biasing stage [2], is the one that provides the appropriate voltages for *vbias1*, *vbias2* and *vbias3*, and causes the PMOS transistors to be in saturation. In addition, the voltage at the drain of transistors T9 and T10, which depend on *vbias1*, has to be at most $V_{ICMmax}–V_{T<T9>}$ in order to permit the input voltage to swing up to V_{DD} [1].

$$V_{ICMmax} = V_{DD} – |Vov_{T9}|+ Vtn \tag{1}$$

$$V_{ICMmax} = |Vov_{T0}| + |Vov_{T9}| + Vtn \tag{2}$$

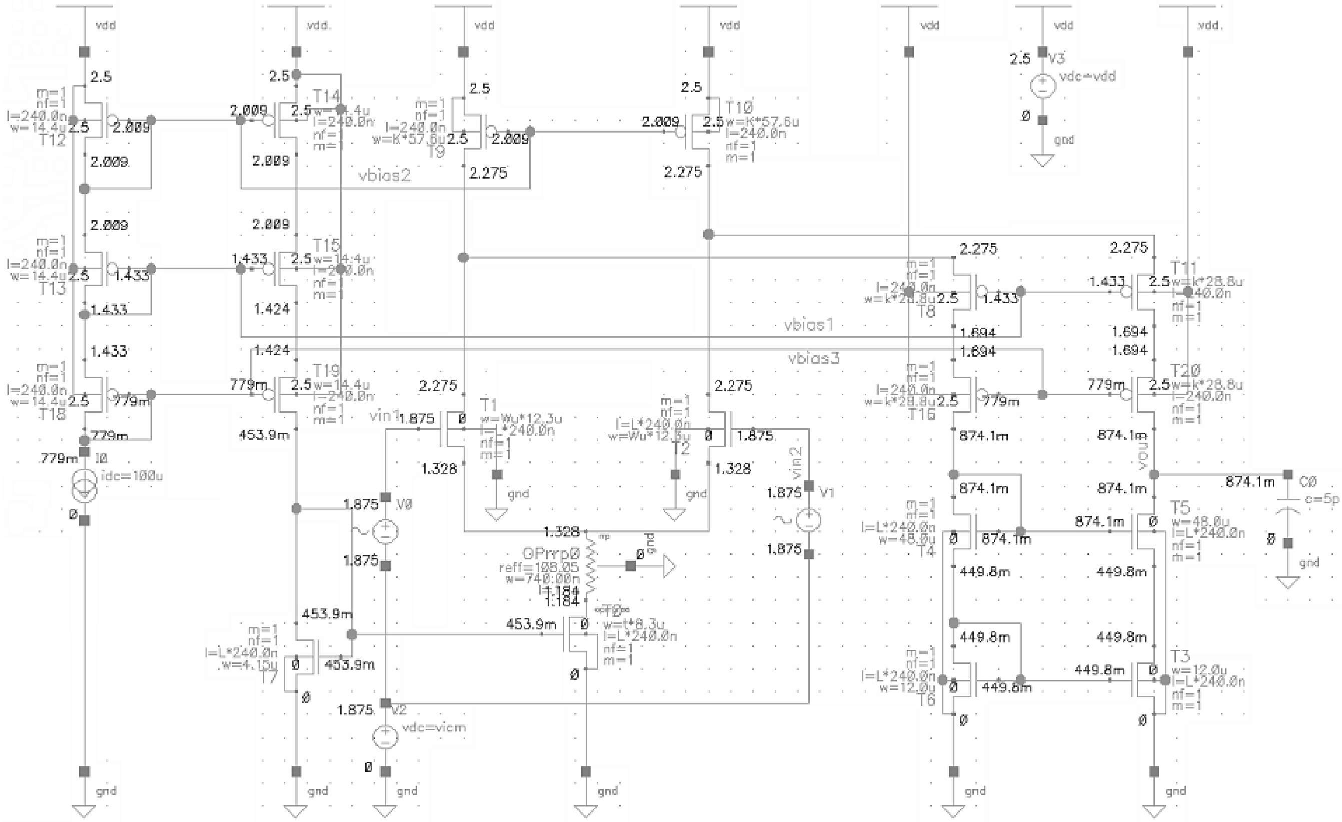

Figure 2 - Op-amp schematic. First two columns - biasing stage; Middle columns - diff. input stage; Last two columns - Double folded cascode

The differential input stage and a single cascode stage [1] design were also tested. This design is well-known to provide a wide input swing, a decent unity gain bandwidth and a relatively high gain. However, for this technology, it is difficult to uniformly achieve a gain over 50 dB across all the common-mode and temperature variations. Therefore, in order to increase the gain without affecting the unity gain bandwidth, an extra cascode stage was added. This is further understood with the expressions for the gain, the unit gain bandwidth and the dominant pole frequency for a double folded cascode:

$$\mathrm{Av} = g_{mT2} R_{OUT} \tag{3}$$

$$f_P = \frac{1}{2\pi C_L R_{OUT}} \tag{4}$$

$$f_T = \frac{g_{mT2}}{2\pi C_L} \tag{5}$$

where

$$R_{OUT} = \left(g_{mT5} r_{oT5} r_{oT3}\right) // \left(g_{mT20} r_{oT20} g_{mT11} r_{oT11} \left(r_{oT10} // r_{oT2}\right)\right) \tag{6}$$

Expressions (3) and (6) describe three important facts: The first fact is that the gain of a double folded cascode can increase up to $g_{mT11} r_{oT11}$ over the single folded cascode, as long as the transistors are sized correctly. The second fact is that the gain is directly dependent on g_{mT2} but not on r_{oT2}, which is in parallel with other r_o's. This yields an increase in the gain if the current through transistor T0, and consequently T1 and T2, is increased. And the third fact is that the gain is dependent on r_{oT3} and not g_{mT3}. Hence, increasing the length or decreasing the width on transistors T3 and T6 results in an increasing gain (of course, all these assumptions are only valid up to a certain limit).

In expression (4) and (5), it can be seen that the dominant pole frequency is reduced by the increased R_{OUT}, and then, the cutoff frequency of the op-amp is reduced. On the other hand, the unity gain bandwidth is independent from transistor T11. So, the double folded cascode does not increase the unity gain bandwidth, which yields the same unity gain bandwidth for both, the single and double folded cascodes.

Finally, in figure 2, a resistor was placed between the drain of T0 and the source of T1 and T2. This resistor effectively reduces the voltage through T0 to under 1.2 V. And, at the same time, does not affect the current flowing through T0, which depends only on transistor T7 (T7 acts as a current source for this branch of the circuit).

In order to get the values for the resistors and the capacitor in the LPF in figure 1, the expressions to be used are [1]:

$$CR_2 = \frac{1}{2\pi f} \tag{7}$$

$$DC_{Gain} = -\frac{R_2}{R_1} \tag{8}$$

Where by specification R_{IN}, which is equal to R_1, has to be greater than 5 kΩ.

III. SIMULATION RESULTS

Once the schematic was put together, the output of the circuit was connected with a 5 pF load capacitor (C_L), which represents the approximate capacitance perceived as the external circuit.

Then, a parametric analysis of six different common mode inputs was run, and the results shown in figure 3. In this parametric analysis, the gain is plotted against the temperature when the frequency is 0.1 Hz. This analysis demostrates that the circuit is over the 52.5 dB in the desired common mode input range and for the required temperature range. Furthermore, in figure 4, the performance of the circuit at 0C, 27C and 100C is observed at a V_{ICM} equal to 1.825V. Here, it is illustrated that a greater temperature diminishes the gain up to 56 dB and the unity gain bandwidth decreases up to 80 MHz.

For a variation of ±10% in the supply voltage (figure 5), the gain increases over 62 dB, while the unity gain bandwidth stays around 128 MHz and the phase margin around 64 degrees. Meanwhile, for a variation of 10% in the supply voltage, the gain decreases down to 56.3 dB, and the unity gain bandwidth and the phase margin stay nearly unchanged.

In figure 6, the differential gain, the common mode gain, the phase response and the CMRR are graphed for an optimal (calculated) V_{ICM} of 1.825V. The differential gain has a maximum gain of 61.41 dB, a cutoff frequency of 133.9 KHz, and a maximum unity gain bandwidth of 128.04 MHz. The Common Mode gain is -30.59 dB and as a result, the CMRR is 92 dB. Finally, the Phase Margin is 63.69 degrees, which yields a stable circuit.

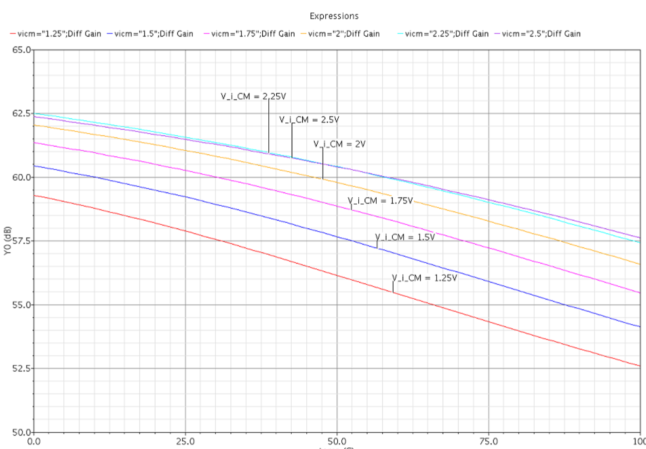

Fig. 3. Gain (dB) vs. Temperature (C) at different Common-Mode inputs

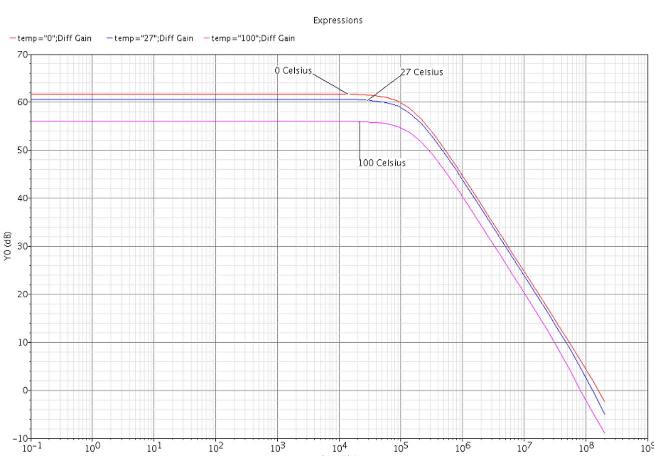

Fig. 4. Frequency Response at Vicm=1.825 V for 0C, 27C, 100C

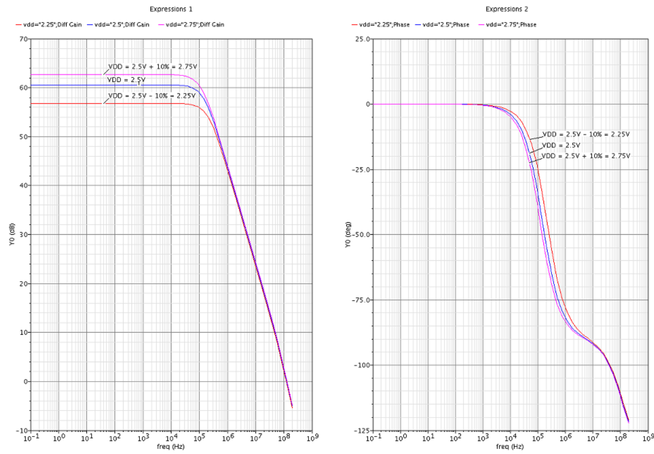

Fig. 5. Mag and Phase Response at Vicm=1.825 V for V_{DD}=2.5V +/-10%

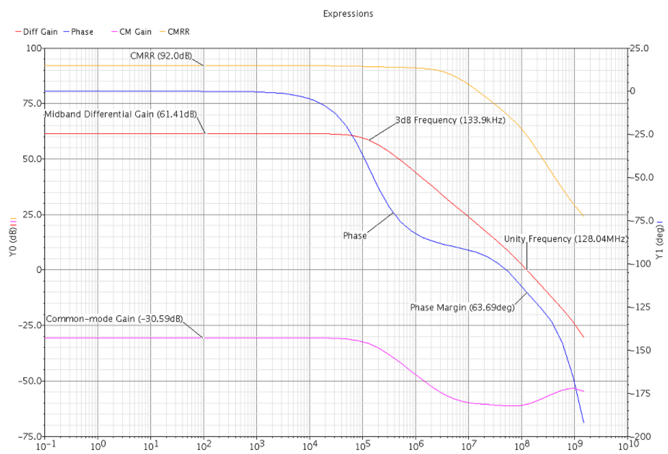

Fig. 6. Diff Gain, CM Gain, Phase response and CMRR at Vicm = 1.825 V

For the LPF (figure 1), expressions (7) and (8) were used to obtain an approximate of the values of R_2, R_1 and C. However, using the exact values computed with expression (7) and (8), the gain of the LPF was below 20 dB and the -3dB frequency of the LPF was at 1.33 MHZ, at V_{ICM} equal to 1.825 V. So, fixing C equal to 800 fF and R_2 to 200 kΩ , the value of R_1 is tuned until a value of 19.991 dB was reached. The same procedure can be applied, but now tuning C and getting closer to 1 MHz.

Figure 7 shows the impact of V_{ICM} in the different frequency responses in the LPF, where a greater V_{ICM} increases the gain and diminishes the cutoff frequency, and a lower V_{ICM} decreases the gain and increases the cutoff frequency.

IV. CONCLUSION

The design of a MOS operational amplifier and a LPF has been demonstrated. The double MOS folded cascode has been shown to be a good alternative when a high input swing and a high gain amplifier is desired. The NMOS transistors in the input allows to swing the common mode input up to V_T over the voltage at the drain of the NMOS. Furthermore, the double cascode provides an increased gain over the single folded cascode without affecting the unity gain bandwidth. Finally, the reduced functionality of this operational amplifier with

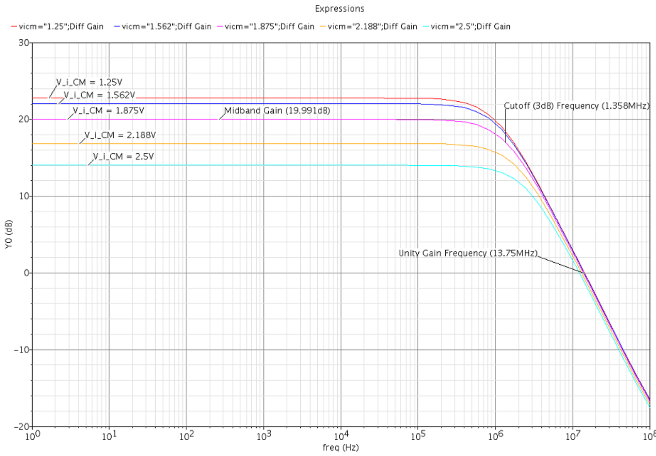

Fig. 7. Filter frequency response for 5 different V_{ICM}

respect to changes in the common mode voltage and the operating temperature are illustrated.

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REFERENCES

[1] A. Sedra and K.C. Smith, "*Microelectronic Circuits*" pp 883-890, 1099, 5th. Edition, Oxford University Press, 2004
[2] Sone, K. Yotsuyanagi, M. "Design Techniques for analogue BiCMOS circuits", Bipolar/BiCMOS Circuits and Technology Meeting, 1994.

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