A 1.8V SELF-BIASED COMPLEMENTARY FOLDED CASCODE AMPLIFIER

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Abstract

This paper describes a 1.8V self-biased complementary folded cascode(SB-CFC) amplifier. We propose a new self biasing scheme for the folded cascode amplifier, which eliminates 6 external bias voltages and related biasing circuits. The required minimum power supply voltage is reduced to 1.8V. And also the output voltage swings are increased. With our new self-biasing scheme the area and power overhead, susceptibility of the bias lines to noise and cross-talk, and design time are reduced.

¥ ºINTRODUCTION

The folded cascode(FC) amplifier is a good choice as a wide-band, fast settling operational amplifier in today's deep sub-micron CMOS technology. But the FC amplifier uses a large number of external bias voltages, and this results in numerous drawbacks, namely, an area and power overhead, susceptibility of the bias lines to noise and cross-talk, and high sensitivity of the bias point to process variations. In an FC amplifier each active devices should be properly biased to get high performance. For instance, most of the transistors should be biased in the saturation region of operation. But in this case determining the proper bias voltages becomes very time-consuming task.

There have been some efforts to overcome this biasing problem. In [1] self-biased CMOS OP-AMP's are proposed. But some of the transistors in these self-biased OP-AMP's are biased in their linear region of operation, which causes drastic reduction of some important a.c. performances, such as gain, CMRR and PSRR. And R. E. Vallee et al. introduced the complementary folded cascode(CFC) amplifier[2] shown in Fig. 1. This CFC amplifier was modified to SB-CFC amplifier in [3]. Though this SB-CFC amplifier doesn't need any external bias voltages, it has some drawbacks. The a.c. performance is degraded and the power supply voltage must be high as much as 6 or ¡ 8*V*.

¥ ±CIRCUIT DESCRIPTION

Fig. 2(a) shows the cascode current mirror. The voltage drop across M1 and M3 can be described as

$$V_{gs1} + V_{gs3} = 2(V_T + \Delta V), \qquad (1)$$

where ΔV is $\sqrt{2 I_{D1} / b}$

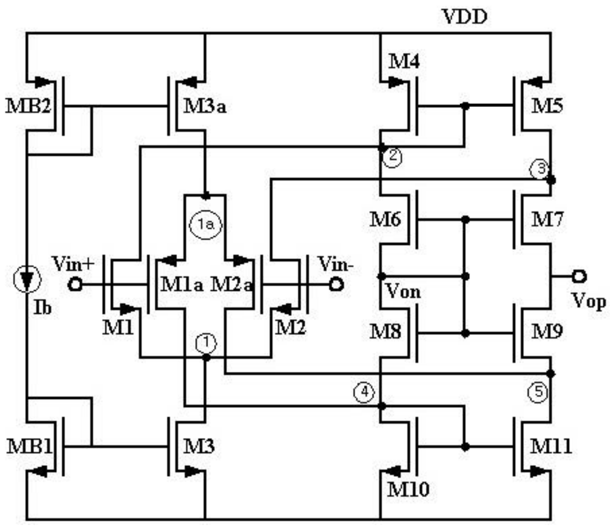
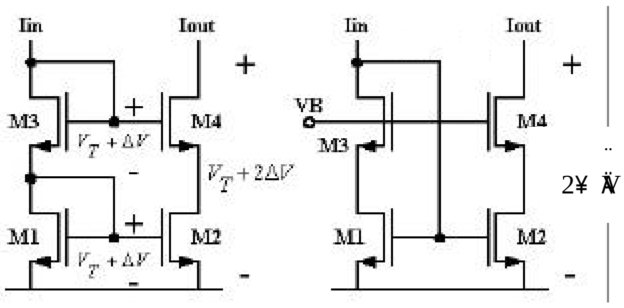


Fig. 1. The CFC amplifier schematic[3].

Its value reaches to 1.8 ~2.4*V* if we ignore the body effects and assume the typical values of V_T and *V* are as 0.8~0.9*V* and 0.1~0.3*V* respectively. Though I_{D8} and I_{D10} in Fig. 1 are different, M8,M9,M10 and M11 can be considered as a cascode current mirror for the convenience of understanding the operational characteristics of the output stage. The existing CFC amplifier contains two cascode current mirrors which are stacked serially. So the minimum required V_{DD} is 4.8*V*. The minimum output voltage of cascode current mirror, V_T +2 *V* is typically 1.5*V*. So the output voltage swings are limited to 1.5*V* from each power rail.

Fig. 2(b) shows the wide-swing cascode current mirror. The voltage drop across M1 and M3 can be described as

$$V_{gs1} + V_{gs3} = V_T + \Delta V \qquad (2)$$



(a) (b)

Fig. 2. (a) Cascode current mirror and (b) wide-swing cascode current mirror.

Its value is the half of (1) and it reaches to 0.9 ~1.2*V*. We propose a new SB-CFC which exploits the characteristics of the wide-swing cascode current mirror as shown in Fig.3.

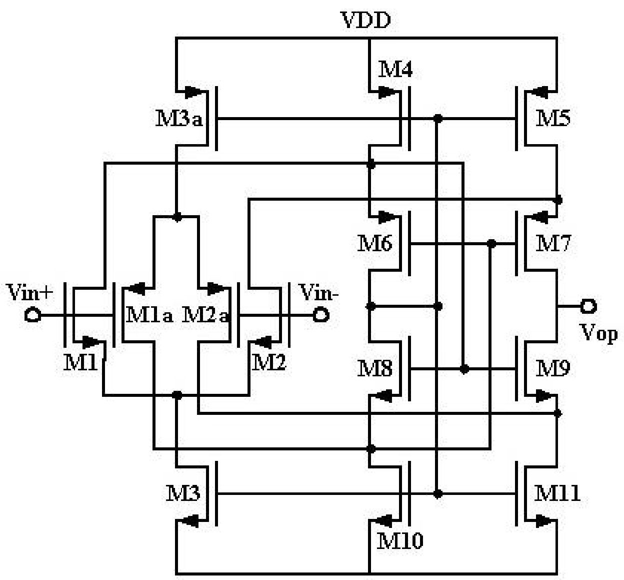


Fig. 3. Proposed low voltage SB-CFC amplifier.

Instead of cascode current mirror by making use of the wide-swing cascode current mirror, the required V_{DD} for the CFC amplifier is reduced by half. Also the minimum required output voltage of wide-swing cascode current mirror is reduced to 2 *V* while the output resistance is the same, that is, $g_m r_o^2$. The output voltage swings of our new CFC amplifier increase by one V_T toward each power rail compared with existing CFC amplifier.

In Fig.3 M4-M7 and M8-M11 construct p- and n-type wide-swing cascode current mirrors. At the same time they are complementarily self-biased in negative feedback-loop mode. If the drain node voltage of M6 is increased, V_{gs4} is decreased and the drain node voltage of M6 is decreased again because V_{ds4} is increased. Naturally all the transistors stay in their saturation region of operation. The self-biased OP-AMP requires only the two supply rails, V_{DD} and *GND*. Thus, the area and power overhead for biasing is eliminated. Further, the operating point is less sensitive to process variations since in this approach the bias point is determined by size ratios only.

The low frequency gain is given by

$$A_V = g_{mT} R_o \qquad (3)$$

where g_{mT} is the total transconductance of input stage, which is given by

$$g_{mT} = g_{mn} + g_{mp} = g_{m2} + g_{m2a} \qquad (4)$$

The R_o is the small signal resistance looking into the drain of M7 or M9 and is given by the parallel combination of $g_{m7} r_{o5} r_{o7}$ and $g_{m9} r_{o9} r_{o11}$. Then eq. (3) becomes

$$A_V = (g_{m2} + g_{m2a})(g_{m7} r_{o5} r_{o7} \parallel g_{m9} r_{o9} r_{o11}) \qquad (5)$$

Design and simulation results : We designed our proposed low supply voltage SB-CFC amplifier based on 0.6n-well CMOS process. Table 1 shows the summary of simulation results. The designed SB-CFC amplifier was targeted to the phase margin 60¢ ª at V_{DD} = 2.4*V* with the heavy load capacitor 20pF and was applied by the other supply voltages 1.8 and 3.3*V* respectively without the transistor resizing. At 2.4 *V* the power dissipation is 3.6 § Ñand the dc gain is 75.2 § ¼The unit gain frequency is 38 § Öand the phase margin is 60¢ ª The figures of performance show that proposed SB-CFC amplifier is superior to exixting CFC amplifier and useful for low voltage and high speed applications.

¥ : CONCLUSIONS

A novel self-biased complementary folded cascode amplifier is proposed. The key points of the proposed amplifier are the self biasing scheme and low supply voltage operation. The proposed biasing circuit eliminates the 6 external bias voltages and related circuits. Thus the area and power overhead for biasing is eliminated. Further the operating point is less sensitive to process variations. The required minimum supply voltage is reduced to 1.8*V* by exploiting the wide-swing cascode current mirror. Our proposed SB-CFC amplifier can used to compose the fully differential or gain boosting amplifiers with little architectual change. And it is a good choice as wide-band, fast settling and low voltage operational aplifier for today's deep submicron CMOS technology.

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Table 1. The summary of simulation results.

Technology	0.6¥ ìm CMOS		
Supply Voltage(V)	1.8	2.4	3.3
Load cap.(§ Ü)	20	20	20
Power Dissipation(§ Ñ)	0.24	3.6	22.1
Unity gain Frequency(§ Ö)	6.9	38	76
DC gain(§ ³)	80.8	75.2	61.3
Phase margin(¢ ª)	71	60	58
Slew rate(rise, fall) (V/§ Á)	2.2 1.7	19 30	100 110
Settling time(0.1%) (ns)	460	104	23.1
Output Swings (V)	0.2 - 1.6	0.3 - 2.1	0.4 - 2.8
PSRR @0Hz (§ ³) @1MHz	86.7 42.3	80.4 68.3	66.2 58.7