A Low-Power, High-Bandwidth LDO Voltage Regulator with No External Capacitor

by

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ABSTRACT

A low-dropout (LDO) voltage regulator for low-power applications is designed without an external capacitor for compensation. The regulator has two stages, the first a folded cascode amplifier and the second a large pass transistor acting as a common-source amplifier. To better explore the tradeoff between bandwidth and power supply rejection, transistor dimensions are modified to support three different bias current levels for the same topology. Tradeoffs involving phase margin and load capacitance are also explored. In simulation, the regulator provided an output of 1.3 V from an unregulated 1.8 V supply, using a 0.75 V reference. By exploiting the tradeoffs between PSRR, bandwidth, and power consumption, a PSRR between 40-60 dB is achieved with a bandwidth between 10 kHz-350 kHz while burning no more than 150 μA of current. The output voltage is stable for load currents between 18-174 mA.

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Chapter 1

Introduction

As demand rises for electronic devices to be smaller, faster, and more efficient, increasing importance is placed on well designed voltage regulators for power supplies. When space is limited, as in the case of portable devices, circuitry for multiple functions requires multiple voltage levels on the same chip. Voltage regulators are needed to protect the rest of the circuitry from fluctuations in the power supply, which can occur due to crosstalk or digital switching. Large variations in the power supply are extremely detrimental; voltages that are too high can damage sensitive semiconductor devices, while voltages that are too low may disrupt biasing or even prevent the circuitry from working at all. This chapter begins by describing the desirable properties of voltage regulators, and gives an overview of the state of the art. To conclude, the goals of this work are laid out in detail.

1.1 Design considerations for voltage regulators

Many factors must be considered when designing a voltage regulator. Minimizing power consumption is always desirable, particularly with portable consumer electronics. Less power consumption allows the device's battery to last longer, meaning the user needs to charge the battery less often. A related factor is efficiency, which is determined by the dropout voltage.

Dropout voltage is defined as the difference between the unregulated supply voltage and regulated output voltage [1]. Lowering the dropout voltage can lower the required voltage of the unregulated power supply, and this in turn lowers the power consumption of the regulator. A less power-hungry device may also use a smaller battery, leading to better portability.

Decreasing the area of a voltage regulator also improves portability. A device that uses several voltage regulators benefits greatly from a voltage regulator design that takes up minimal area, because the structure that houses the circuitry can be made smaller and hence easier to carry around. Smaller area also means that more devices will fit onto one wafer, decreasing the cost of manufacturing.

Bandwidth is another important specification in voltage regulator design. The higher the bandwidth of a regulator, the more quickly it can react to changes in input and power supply and keep the output voltage constant. High bandwidth also improves the power supply rejection ratio (PSRR) of the regulator, which is a measure of how well the regulator attenuates noise on the power supply. The better the power supply rejection, the less the output voltage changes in response to fluctuations in the supply. The PSRR can be characterized by the magnitude of attenuation as well as the range of frequencies over which the attenuation occurs. Usually PSRR is greatest at low frequencies and rolls off as the frequency increases.

Yet another factor to consider in voltage regulator design is stability. Since the purpose of a voltage regulator is to provide a steady voltage to other components, a regulator prone to oscillation is not desirable. Since stability varies with load conditions (such as output current and load capacitance), which may be incompletely specified or unknown, a regulator design that has good phase margin for a wide range of output loads is best. Associated with stability is load

regulation, the percentage change in output voltage in response to a change in the output current [2].

The importance of the numerous voltage regulator specifications vary widely depending on the application. It is generally desirable for a battery-powered portable device to consume less power than a device that will always remain in the same place and plugs into a wall outlet. Devices for audio applications require less bandwidth than RF devices. Circuits with very sensitive components like phase-locked loops (PLLs) and circuits that have both analog and digital components require especially high PSRR. Biomedical devices, such as pacemakers and hearing aids, are often implanted, so they must take up as little area and consume as little power as possible since surgical operations to replace dead batteries are expensive and inconvenient.

1.2 Types of voltage regulators

The basic function of a voltage regulator is to compare its output voltage with some fixed reference voltage, amplify the difference, and use feedback to make its output match the reference. The concept is rather simple, but implementations can be as varied as they are complex.

1.2.1 Switching regulators

The most efficient type of voltage regulator is the switching regulator [1]. A switching regulator takes in a DC voltage, converts it into a high-frequency voltage, then filters this AC voltage to convert it back into a DC voltage at the output. To perform the initial DC to AC conversion, a switch (usually a transistor) connecting the unregulated input voltage and a storage element (usually an inductor) is rapidly turned on and off. This causes an AC ripple at the output of the

storage element, which can then be low-pass filtered, usually by an LC network, to produce a DC voltage at the output.

Switching voltage regulators have been implemented with over 90% efficiency, even with the power lost during transistor "on" stages and the charge required to turn transistors on and off. Switching regulators also have the ability to output a voltage higher than the unregulated supply voltage, which other types of regulators cannot do without a charge pump. However, the intermediate DC to AC conversion causes high output voltage ripple, even after low pass filtering, so switching regulators cannot be used with circuits that are very sensitive to variations in supply voltage. Also, the inductors used in switching regulators are often too large to be integrated onto a chip, so they must be external and thus the regulator takes up more area.

1.2.2 Linear regulators

Linear regulators use a transistor operated in its linear region as a variable resistor in a voltage divider network to obtain the desired output voltage [1]. Linear regulators are less efficient than switching regulators because the transistor at the output, usually a PMOS, is always dissipating power in the form of heat. Charge pumps are sometimes used to increase efficiency, but they take up a lot of area and increase the complexity and power consumption of the circuit. However, linear regulators are stable with various loads since the transistor can be continuously adjusted. Also, because linear regulators do not use storage elements to convert between AC and DC voltage, output voltage ripple and noise is lower than in switching regulators. For the same reason, linear regulators respond faster than switching regulators to changes in the unregulated supply voltage and load current.

1.2.3 Cascaded regulators

Desirable characteristics of both switching and linear regulators can be obtained if the two architectures are cascaded. The switching regulator can set a rough DC level, above the original unregulated supply if needed. Because of its high output voltage ripple, the switching regulator usually comes first in the cascade. The linear regulator then reduces the switching regulator's output ripple and allows the regulator to be stable for a wide range of loads and react quickly to load changes [3]. With these benefits, however, come the drawbacks of increased area and power compared to a single stage regulator.

1.2.4 LDO regulators

A special class of linear regulators is the low dropout (LDO) regulator, named for the small difference between its required supply voltage and the desired output voltage. Most modern LDOs have a dropout voltage of less than one volt [4]-[7]. Like other linear regulators, LDOs use a transistor as a pass element, but unlike in other linear regulators, the transistor is not necessarily operated in the linear region. Feedback is used to modulate the gate voltage and control output impedance [1]. LDOs have low output voltage ripple and noise, like other linear regulators, but have a higher output impedance so they are less stable. LDOs often rely on large external capacitors for compensation, which increases the area and cost of these types of regulators. Stability is also affected by the equivalent series resistance (ESR) of the external capacitor, a value that is hard to control and characterize because of its temperature dependence.

1.3 Overview of the state of the art

The focus of this project will be on LDO regulator design, so it is helpful to examine some of the existing work in the field. Gupta and Rincon-Mora improved the PSRR of an LDO by cascoding an NMOS with the usual PMOS at the output, decoupling the output from fluctuations in the supply voltage [4]. To preserve low dropout performance, a charge pump was used to boost the gate voltage of the NMOS above the supply voltage. An RC filter was used to attenuate noise at the gate of the NMOS from the charge pump and supply voltage. Since no DC current ran through the filter, the resistor could be made very large, and PSRR could be further improved by placing a pole close to the dominant zero in the PSRR curve.

Hoon et al improved PSRR by inserting a voltage subtractor stage between the second high gain stage of the error amplifier and the PMOS pass transistor [5]. This fed supply noise directly into the feedback loop and modulated the pass PMOS gate with respect to its source terminal. The subtractor stage was a common source NMOS loaded by a diode-connected NMOS, which connected the supply voltage to the gate of pass transistor. The dominant pole of the system was at the output because of the low impedance at the gate of the pass transistor due to the diode-connected NMOS.

Wong and Evans designed an LDO with four gain stages, including the output PMOS [6]. The PMOS pass transistor was cascoded with a drain-extended PMOS (DEPMOS) to increase output impedance, which improved PSRR. Even with so many gain stages, compensation required just one Miller capacitor because the second and third gain stages were wideband stages, and the cascoded output devices reduced the parasitic gate capacitance that needed to be driven. The wideband stages also contributed to good PSRR over a wide range of frequencies. The system's dominant pole was at the output of first gain stage, and the second pole was at the

output of LDO. To decrease power consumption, the transistors in the first gain stage were biased in the subthreshold region to obtain maximum transconductance for the given bias currents. Subthreshold operation gives more gain for the same current increase compared to above threshold design because gain is proportional to the drain current in subthreshold, and to only the square root of the drain current above threshold.

To stabilize their three-stage LDO, Leung and Mok used an innovative method of compensation that combined pole-splitting with pole-zero cancellation [7]. For pole-splitting, they used damping-factor-control (DFC) compensation, implemented with a negative gain stage and two on-chip capacitors. The feedback network contained a capacitor in parallel with the feedback resistor, which formed a high-pass filter that created a mid-frequency zero to cancel one of the poles. All capacitors mentioned were small enough to integrate, and if an additional external capacitor was connected at the output, the LDO was stable for the full range of load current. Without an external capacitor, the LDO was stable only above a minimum load current. Because the transfer function of the system changed based on operating conditions, the power burned in pass transistor could be used to improve stability and bandwidth and hence PSRR.

1.4 Goals for this research

The purpose of this project is to design an LDO with the following constraints. The output voltage will be 1.3 V using a 1.8-V unregulated supply voltage and a 750-mV bandgap reference voltage. The LDO will consume no more than 150 microamperes of current, not including the load current, and have a phase margin of at least 45 degrees. The PSRR must be between 40 and 60 dB in band. In this project, the PSRR is defined to be the magnitude, in decibels, of the gain from the positive power supply to the LDO output for low frequencies. PSRR will be reported

and discussed as a positive value; for example, a PSRR of 40 dB means that fluctuations in the positive supply show up at the output attenuated by a factor of 100, and an increase in PSRR means more attenuation of supply noise at the output. The bandwidth of the LDO must be at least 10 kHz. For the purpose of this project, bandwidth is defined to be the frequency at which the magnitude of the power supply rejection falls to 3 dB below maximum value. The LDO will be stable for a load current of at least 50 mA and have a purely capacitive load.

There are many ways to improve an LDO design, but the primary focus of this project is to maximize the bandwidth and PSRR, and to do so without using an external capacitor. A design that can be fully integrated takes up less area and eliminates the possibility of oscillations due to parasitic bond wire inductance. If the regulator is packaged, the lack of an external capacitor saves a pin, or several pins if multiple regulators are needed, which reduces cost.

The remainder of this thesis is organized as follows. Chapter 2 details the topology, including biasing, of the voltage regulator, and Chapter 3 discusses the challenges and tradeoffs involved in the regulator design. Chapter 4 describes the results of testing the design in simulation. Chapter 5 summarizes the results, compares the design to the state of the art, and suggests directions for future research.

Chapter 2

System Architecture

The complete voltage regulator design is found in Figure 2-1. The design has only two stages, to simplify compensation. Both stages contribute to the gain of the system and are affected by fluctuations in the power supply. Biasing the devices in both stages requires careful consideration.

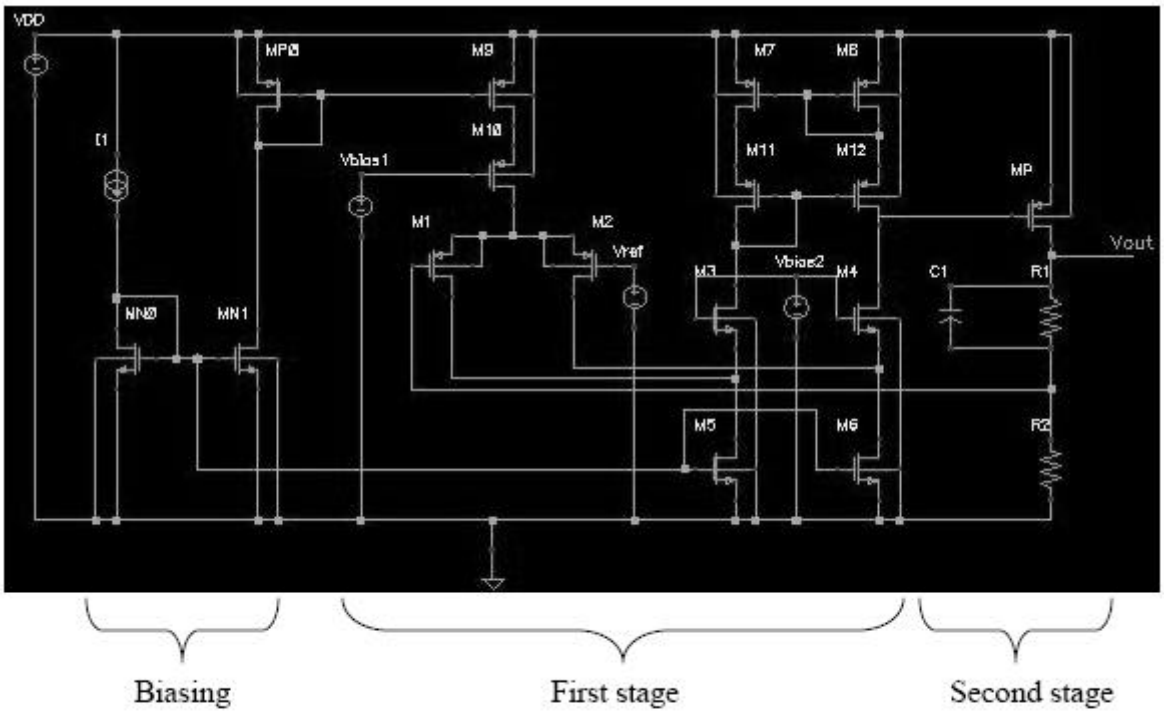


Figure 2-1 Voltage regulator schematic

2.1 Folded cascode

The first stage is a folded cascode, which allows a lot of gain to be obtained in a single stage. A folded cascode topology was chosen instead of a telescopic cascode because of the limited head room due to a low supply voltage. A folded cascode also has a higher output swing than a telescopic cascode [2]. PMOS transistors M1 and M2 are the inputs, with transistors M9 and M10 forming the cascoded tail current source, and NMOS transistors M3 and M4 are the “folded back” common gate transistors of the cascode. M5 and M6 provide the bias currents for M3 and M4, respectively.

The folded cascode is loaded by an improved Wilson current mirror, formed by M7, M8, M11, and M12. This type of mirror eliminates the systematic gain error of the conventional Wilson mirror by adding another transistor to input side (M7 and M11) to equalize the drain-source voltages of the two transistors closer to the power supply (M7 and M8) [2]. Loading the first stage with an improved Wilson mirror instead of a simple two-transistor mirror increases the output resistance of the stage and thus further increases the gain.

2.2 Pass transistor

The second stage of the LDO is merely the PMOS pass transistor MP. This device must be very wide so that it can source large load currents with a reasonable gate-source voltage. The length remains at the minimum value to keep the threshold voltage low. The output voltage of the LDO is at the drain of MP, and resistors R1 and R2 form a voltage divider to feed a fraction of the output voltage back to the input. R1 and R2 are made large so that very little current flows through them, minimizing the power consumption of the feedback path.

2.3 System gain

The output of the first stage is connected directly to the input of the second stage, which is the gate of MP. Because the impedance looking into the gate of a MOS device is very large, inter-stage loading does not need to be taken into account when approximating the gain of the LDO. The AC open loop gain is then merely the product of the gains of each stage. The gain of the first stage is the product of its transconductance, which is the g_m of M2, and its output resistance, which is the parallel combination looking up into the drain of M12 and looking down into the drain of M6. The gain of the second stage is the transconductance of MP multiplied by the output resistance of the LDO, which is the parallel combination looking up into the drain of MP and looking down at R1 and R2. Since the DC current in MP is very large, the r_o of MP is much smaller than the resistance of R1 and R2 in series. Therefore, R1 and R2 can be ignored when writing the gain expression for the second stage. The gain of both stages together can thus be approximated by $g_{m2}\{[2g_{m11}r_{o7}r_{o12}] \parallel [g_{m4}r_{o4}(r_{o6} \parallel r_{o2})]\}g_{mp}r_{op}$, where g_{m2}, g_{m11}, g_{m4}, and g_{mp} are the transconductances of M2, M11, M4, and MP respectively, and r_{o7}, r_{o12}, r_{o4}, r_{o6}, r_{o2}, and r_{op} are the output resistances of M7, M12, M4, M6, M2, and MP respectively. Since the output resistance of MP is small compared to the output resistance of the other devices, it can be clearly seen from the gain expression that most of the gain comes from the first stage, which is expected.

2.4 Power supply rejection

Fluctuations in the power supply affect the voltage output of the LDO through both stages. In the first stage, variations in the supply voltage are equivalent to a variation in the common-mode input voltage, since M9 and M10 together act as a current source. In the second stage, variations in the supply voltage modulate of the gate-source voltage of MP, which affects the output

voltage directly. Since the first stage is differential, it is less sensitive to power supply disturbances than the second stage, which is single-ended. The gate-source voltage of MP is the input of the second stage, so noise on the power supply is the same as noise at the input of the second stage, and we can model the signal path as shown in Figure 2-2. Applying Black's formula, we can approximate the PSRR of the LDO to be the magnitude of $20*\log[A_2/(1+A_1A_2Z)]$, where A_1 is the gain of the first stage, A_2 is the gain of the second stage, and Z is the feedback factor, which at DC is R2/(R1+R2).

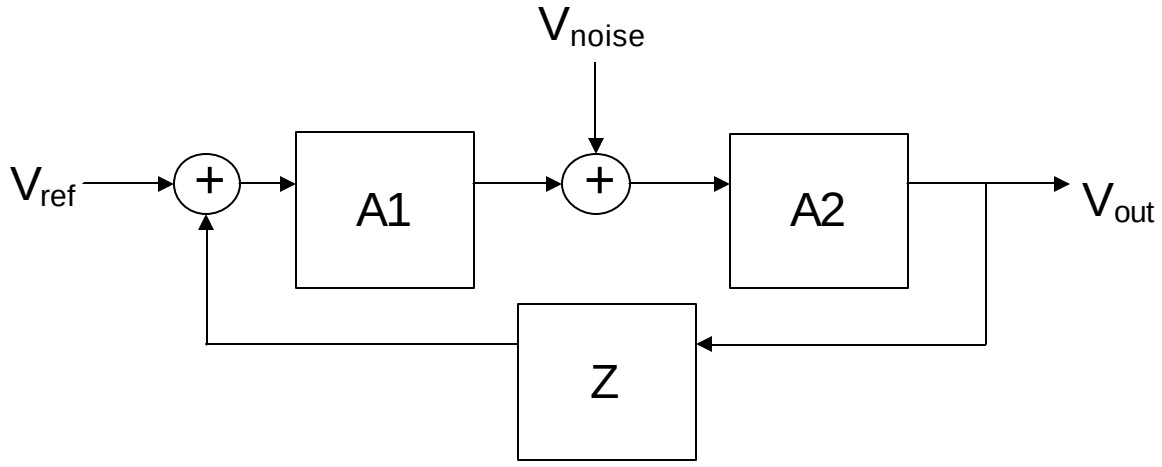


Figure 2-2 Block diagram for supply noise path

The bandwidth is improved by placing capacitor C1 in parallel with R1. As in the design by Leung and Mok, C1 generates a mid-frequency zero in the AC open-loop gain characteristic. This also improves the power supply rejection at higher frequencies.

2.5 Biasing

Several constraints must be considered when biasing the devices in the LDO. As seen in Figure 2-1, M5 sinks current from both M1 and M3, and M6 sinks current from both M2 and M4. The current in M9 is split evenly between M1 and M2. Therefore, M5 and M6 each need to have a

bias current that is more than half of the bias current in M9 so that M3 and M4 will have a nonzero bias current. The bias currents in M5 and M6 are set with an NMOS mirror whose input is set directly by ideal current source I1. An additional output is taken from this mirror to form the input of a PMOS mirror that gives M9 its bias current.

In order for transistors M8 and M12 of the improved Wilson mirror to stay in saturation, the magnitude of their gate-source voltage plus an overdrive voltage must be less than the magnitude of the gate-source voltage required by MP. The required voltage is depends on how much current MP must source, which in turn depends on the load current of the LDO. (MP must source slightly more than the load current because of the current through R1 and R2, but the current in the feedback network is only a small fraction of the load current.) Since M8 and M12 carry the same current as M4, the bias current of M4 must be set carefully. If it is too large, the gate-source voltage of M8 will be too large for M12 to stay in saturation because the source-drain voltage of M12 is the difference (in magnitude) between the gate-source voltage of MP and the gate-source (and thus drain-source) voltage of M8. Thus the bias current in M6 must be high enough for M4 to have enough bias current, but not so high that M12 is pushed out of saturation.

The bias voltages at the gates of M3, M4, and M10 must also be set carefully. If the voltage at the gates of M3 and M4 is too low, M5 and M6 will be pushed out of saturation because the drain-source voltage of M5 and M6 is the difference between gate voltage at M3 and M4 and the gate-source voltage required by the bias current of M3 and M4. If the gate voltage is too high, M3 and M4 will be pushed out of saturation because the voltage at their sources will be too close to the voltage at the gate of MP. The voltage at the gate of M10 must be set such that the gate-source voltage of M10 allows M9 enough drain-source voltage to keep it in saturation.

Chapter 3

Design Challenges and Tradeoffs

The design of an LDO to meet the stated goals posed many challenges and tradeoff decisions.

3.1 Open loop characteristic

The high load current required a very large pass transistor to keep the gate-source voltage at a reasonable value, but increasing the width of MP increased its parasitic gate-source capacitance. This large capacitance, together with the high output resistance of the folded cascode stage, formed a slow dominant pole that limited the bandwidth of the system. The second pole was at the output of the LDO. Because the system only had two poles before the unity-gain frequency, pole-splitting compensation would not have helped to increase the bandwidth because the first pole would have just been pushed to an even lower frequency. However, since there were only two main poles, the system did not need any additional compensation to attain a phase margin greater than 45°.

3.2 Tradeoff between PSRR and bandwidth

To increase the PSRR of the LDO, the gain of the first stage needed to be increased. This could be done by increasing the transconductance or the output resistance of the first stage. Decreasing

the widths of M5 and M6 was one way to increase the output resistance while keeping the transconductance constant. Since the width of M9 did not change, the bias currents of M1 and M2 stayed constant, leaving the transconductance of the first stage unchanged. However, decreasing the widths of M5 and M6 decreased their bias currents, so their output resistances increased. While this caused the PSRR to increase, it decreased the bandwidth because the increased output resistance lowered the frequency of the dominant pole. Conversely, increasing the widths of M5 and M6 increased the bandwidth of the LDO but decreased the PSRR. Changing the widths of M5 and M6 even slightly had significant impacts on the bandwidth and PSRR of the LDO.

Increasing the width of M9 also increased the PSRR. Widening M9 increased its bias current, which increased the bias currents through M1 and M2, which increased the transconductance of M2 and thus the transconductance of the first stage. Since the bias currents in M5 and M6 remained unchanged, increases in current through M1 and M2 corresponded one for one to decreases in current through M3 and M4, and thus through M7, M8, M11, and M12. Thus increasing the width of M9 increased the gain, and hence the PSRR, of the LDO by increasing both the transconductance and output resistance of the first stage. However, increasing the width of M9 also decreased the bandwidth because the increased output resistance decreased the dominant pole frequency.

Another way to increase PSRR was to increase the width of M10. When the width of M10 increased, its drain-source voltage decreased, which increased the drain-source voltage of M9. This increased the current through M9 slightly due to channel length modulation [2]. The increased bias current through M9 increased the PSRR and decreased the bandwidth in much the same manner as described above.

3.3 Overcoming the PSRR-bandwidth tradeoff

The effects of changing the widths of M5, M6, M9, and M10 demonstrate a clear tradeoff between bandwidth and PSRR. In order to increase bandwidth without sacrificing PSRR and vice-versa, the gain of the first stage must be increased without lowering the frequency of the dominant pole. Thus the LDO must burn more power to increase the transconductance without increasing the output resistance. This can be accomplished by increasing the widths of M5, M6, M9, and M10 simultaneously, which amounts to increasing all bias currents in the first stage.

3.4 Keeping all transistors in saturation

Changing the current in ideal current source I1 will change the bias current in all transistors except MP, whose bias current is determined by the current load. Significant changes in bias currents require changes in the dimensions of some devices in order to keep all devices in saturation. When M5 and M6 carry large bias currents, their drain-source voltages must be higher, decreasing the drain-source voltages of M3 and M4. The widths of M3 and M4 must be increased for them to stay in saturation, since increasing the width of a transistor decreases its drain-source and saturation voltages. Also, when the current in I1 increases, the bias currents in M7, M8, M11, and M12 increase, but the gate-source voltage of MP remains the same. In order for M7, M8, M11, and M12 to remain in saturation, their widths must be increased so that the magnitudes of their gate-source and drain-source voltages decrease.

3.5 Tradeoff between PSRR and phase margin

A tradeoff also exists between stability and PSRR. High PSRR requires high gain, and increasing the gain increases the unity-gain frequency, which decreases phase margin. Unlike the bandwidth-PSRR tradeoff, this tradeoff cannot be circumvented by burning more power. Increasing bias currents increases the transconductance of the first stage, which increases gain and decreases phase margin.

3.6 Tradeoff between load capacitance and phase margin

Although the chosen LDO design does not require an external capacitor for stability, the load capacitance of the LDO can affect its stability. Since the second pole of the system is formed by the output resistance of the LDO and any capacitance at the output, increasing the load capacitance will decrease the frequency of the second pole. This moves the two poles closer together, decreasing the phase margin.

Chapter 4

Measured Results

The LDO design was tested in simulation to see if the targeted constraints were met.

4.1 AC open loop gain

One simulation was set up with an input AC signal to find the AC open loop gain and phase margin of the LDO. To establish the appropriate operating conditions, the feedback loop needed to look closed for DC signals but open for AC signals. A large inductor placed in the feedback loop fulfilled these conditions. In addition, a very large capacitor, which looked like a short for AC but blocked DC, was connected between the AC source and the gate of M2 so that the input variation would only be seen at AC. The other input was connected to a 0.75-V source. An ideal 50-mA current source connected to the output of the LDO to represent the load current. This setup is illustrated in Figure 4-1.

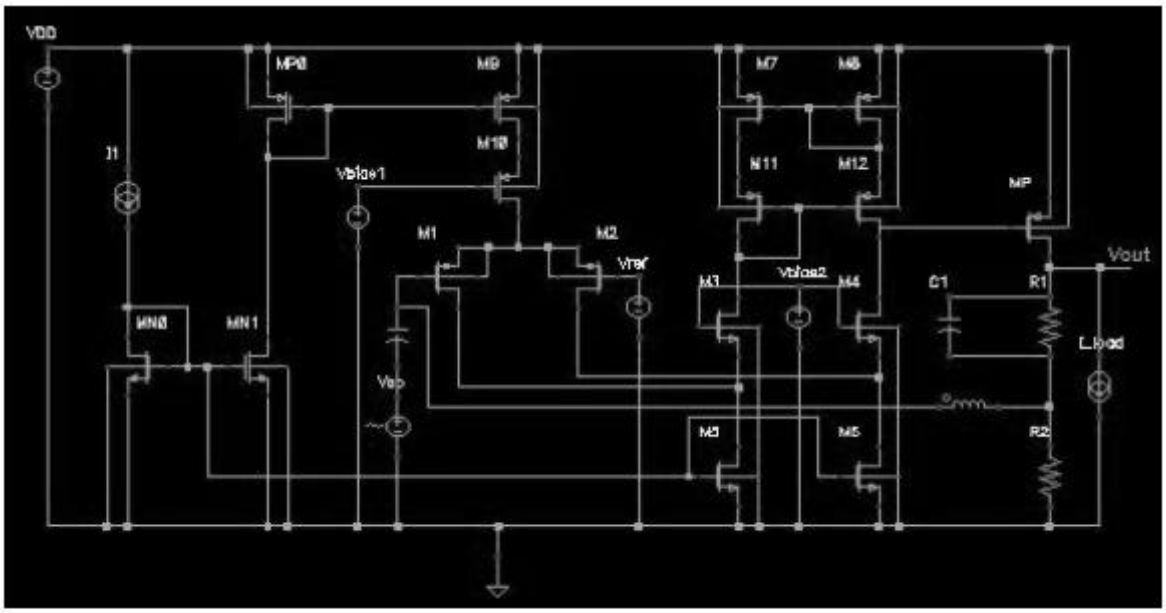


Figure 4-1 AC open loop gain simulation setup

4.2 PSRR and bandwidth

Another simulation was set up with an AC source in series with the DC supply voltage to find the PSRR and bandwidth. This simulation required no capacitor and inductor because there was no input variation, and the operating conditions were automatically set by the resistive feedback network. The AC output voltage was converted to decibels and then plotted versus frequency to find the PSRR. This graph was then used to determine the bandwidth by finding the frequency at which the magnitude of the output voltage dropped 3 dB below its maximum value. A sample plot is found in Figure 4-2. As in the previous simulation, an ideal 50-mA current source connected to the output of the LDO to represent the load current.

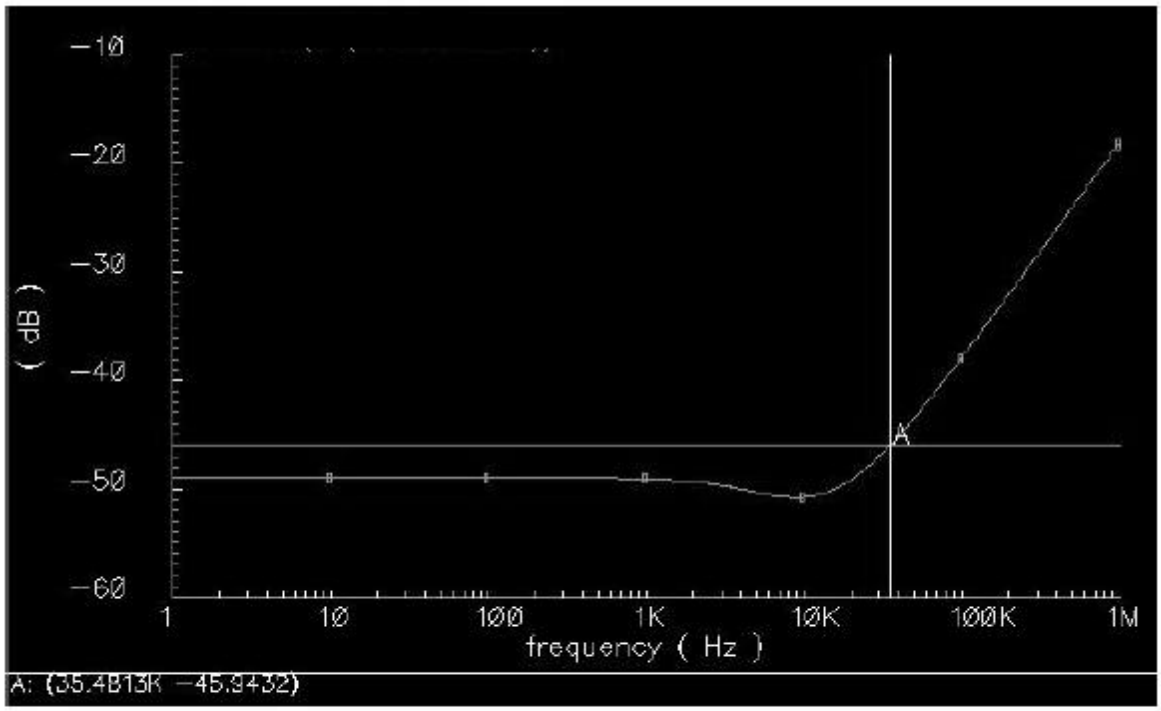


Figure 4-2 Sample power supply rejection curve. Here, the PSRR is 49 dB, and the bandwidth is 35.5 kHz.

4.3 Graphs

4.3.1 PSRR-bandwidth tradeoff and bias current levels

To demonstrate the tradeoffs between bandwidth, PSRR, and power consumption, three different values of current for ideal current source I1 were used: 1 μA, 10 μA, and 50 μA. Changing between these values caused significant changes in the bias currents of the devices in the first stage, so the dimensions of almost all of the devices needed to be changed to keep all transistors in saturation. Therefore, three different circuits, one for each current source value, were designed and simulated separately. For each design, small changes were made to various devices to obtain a range of PSRR values, and the bandwidth was measured for each value. As seen in Figure 4-3,

a clear inverse relationship exists between PSRR and bandwidth for the same value of I1. To obtain the same PSRR while increasing the bandwidth, or vice-versa, I1 must be increased.

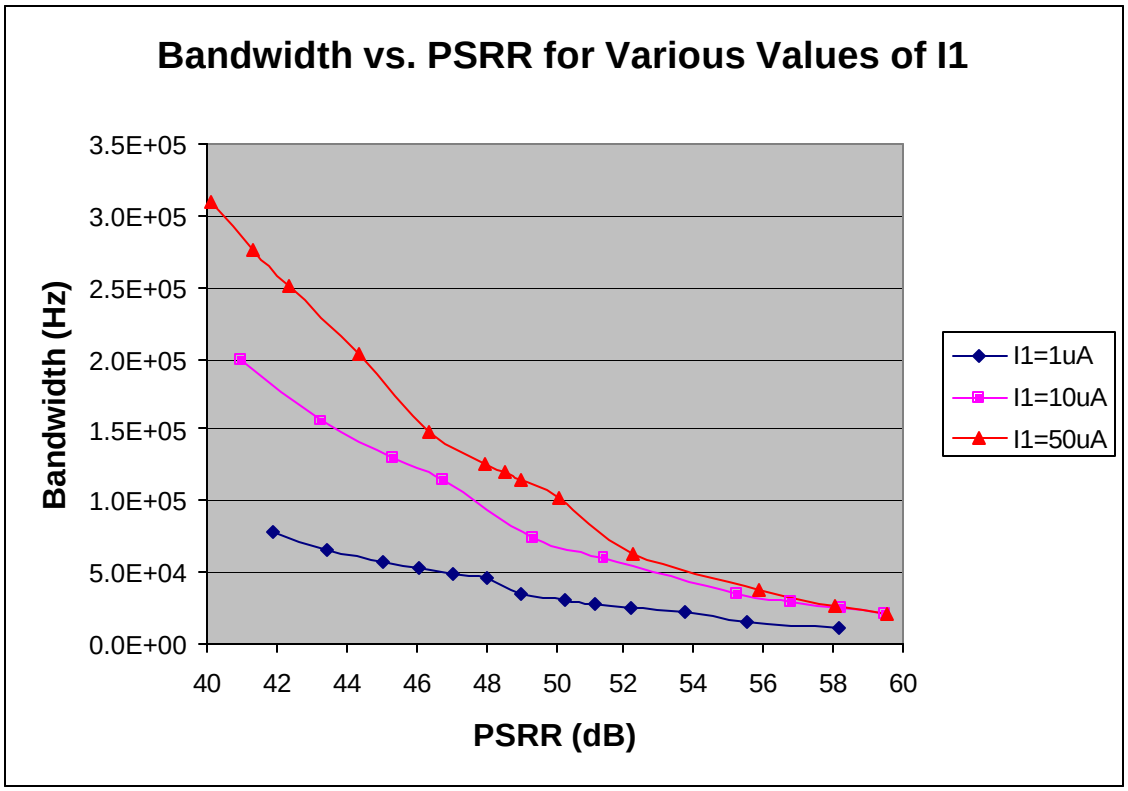


Figure 4-3 Plot of bandwidth vs. PSRR for various bias current levels

4.3.2 PSRR-phase margin tradeoff

Figure 4-4 illustrates the tradeoff between phase margin and PSRR for all three values of I1. As predicted by the direct relationships between bias current, transconductance, gain, and PSRR, increasing the power consumption of the LDO only makes the phase margin worse.

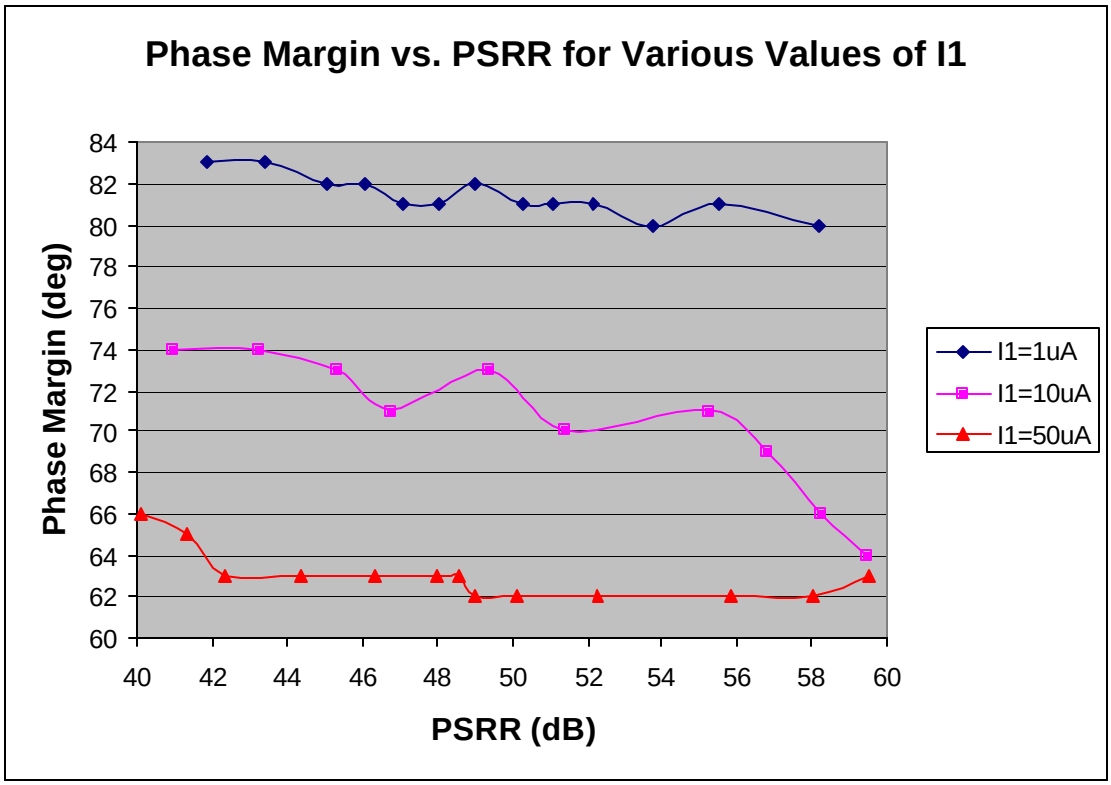


Figure 4-4 Plot of phase margin vs. PSRR for various bias current levels

4.3.3 Load capacitance-phase margin tradeoff

For the rest of the simulations, changes in PSRR were no longer of primary concern, so a single circuit could be used for each value of I1. A circuit with a PSRR around 50 dB was selected for each of the three I1 values. The number 50 was chosen because it is in the middle of the range given by the PSRR specification, but this decision was arbitrary; the trends exhibited would be the same for any of the circuits used in the previously mentioned graphs.

No specification was established for how much load capacitance the LDO needed to be able to drive, but it was important to find the maximum load capacitance. Figure 4-5 shows plots of phase margin versus load capacitance for all three ideal current source values. As long as the

LDO was stable, PSRR and bandwidth were not significantly affected by changes in the output capacitance because the output pole was always the second pole.

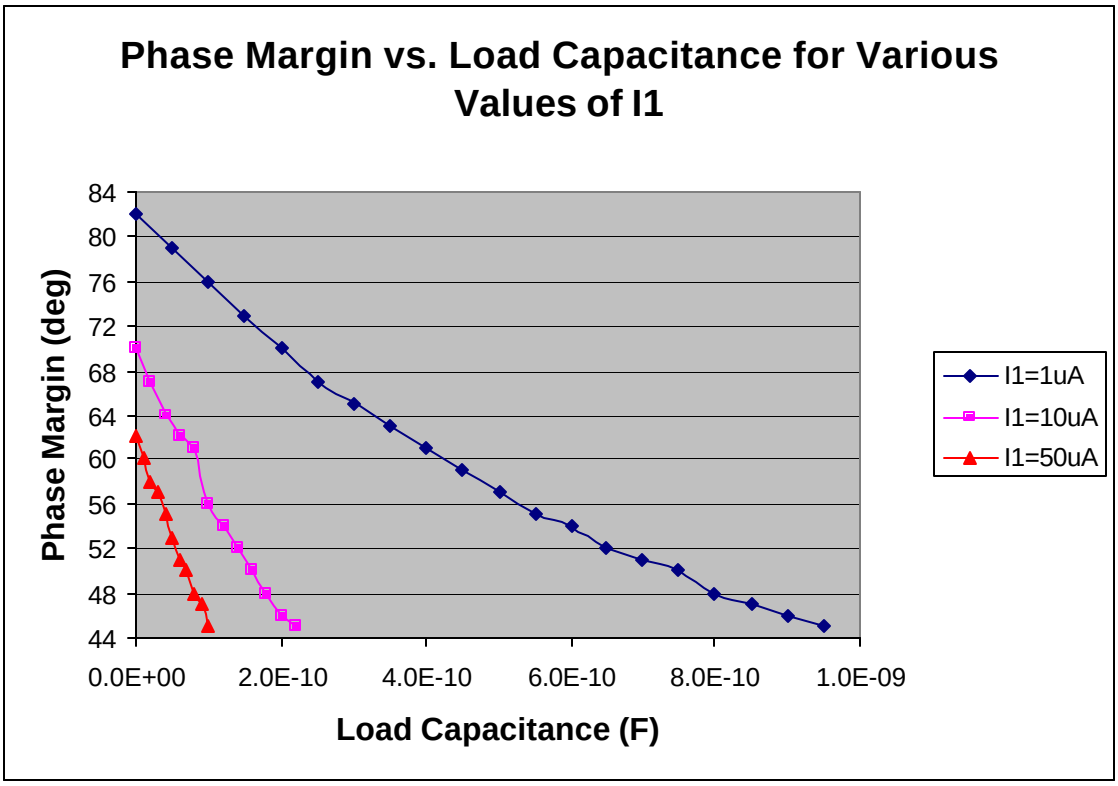
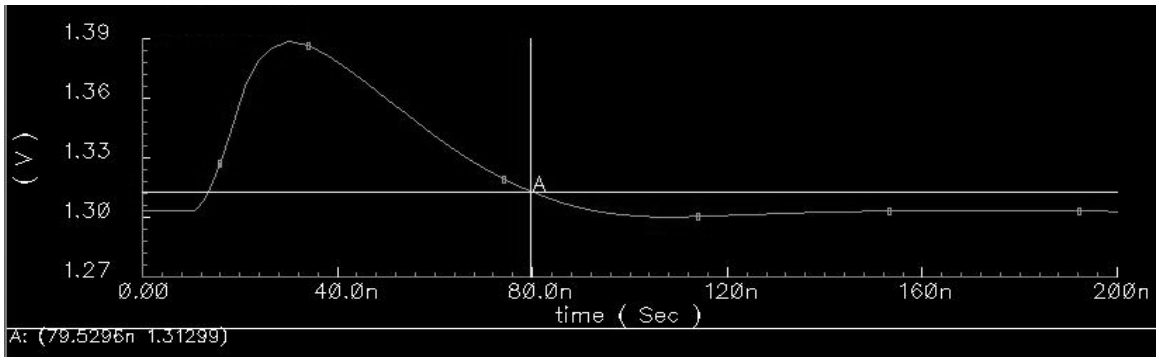


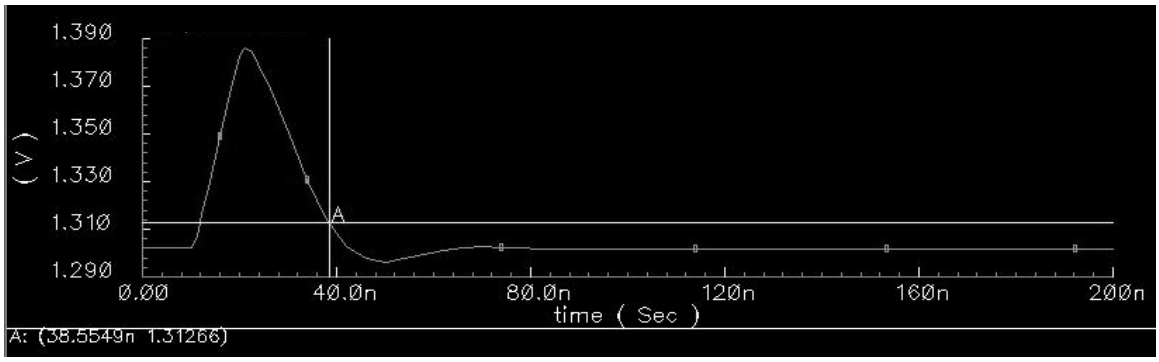
Figure 4-5 Plot of phase margin vs. load capacitance for various bias current levels

4.3.4 Transient behavior

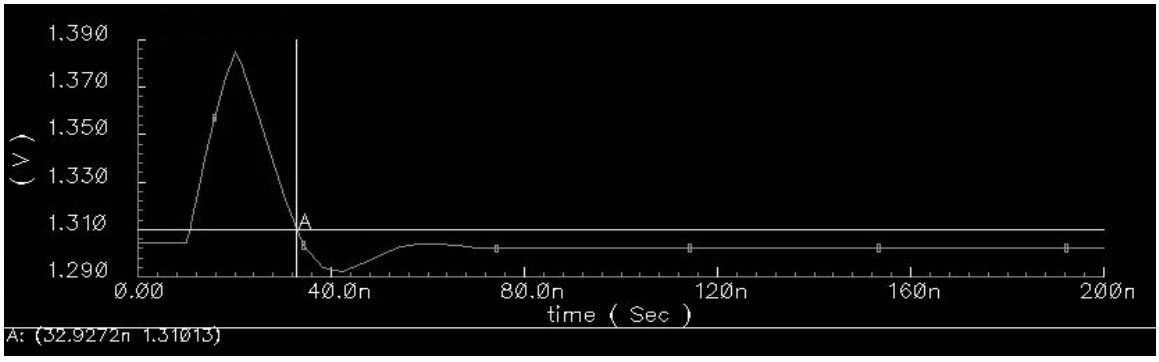
The transient behavior of the LDO was simulated by applying a voltage step to the power supply and plotting the voltage at the output (still with an ideal 50-mA load current). Since the phase margins of the systems for all three values of I1 were very good (a load capacitor was connected at the output of each circuit that gave the system about 60° of phase margin), there was no ringing in the output voltage in response to the step; the output just exhibited some overshoot and then settled to the desired output value of 1.3 V. As seen in Figure 4-6, the output voltage in all three circuits settled to within one percent of the final value within 80 ns.



(a)



(b)

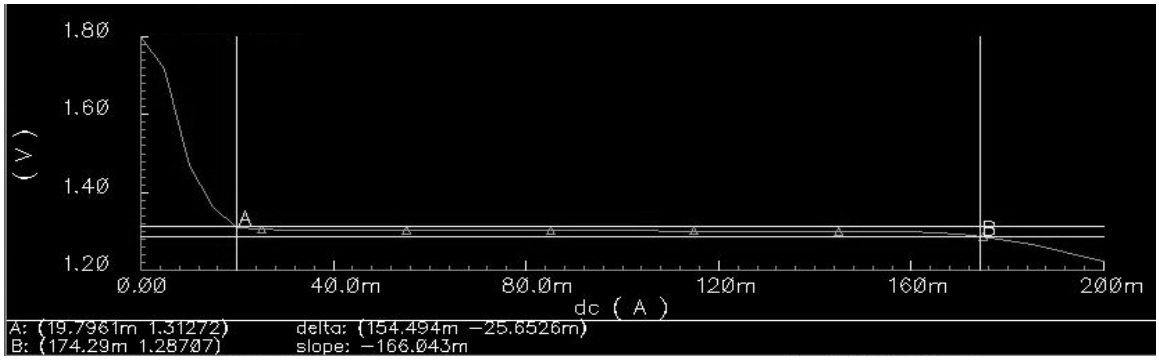


(c)

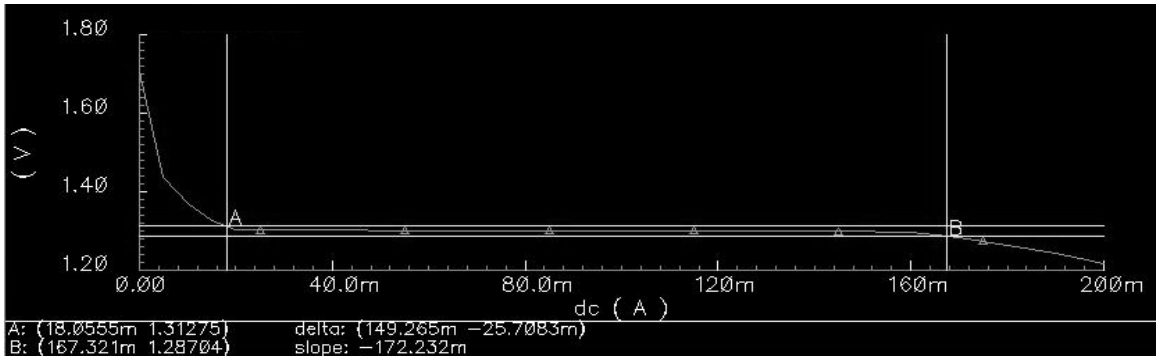
Figure 4-6 Transient response of output voltage to step in supply voltage at 10 ns. Marker indicates time at which output voltage is within 1% of final value. (a) I1 = 1 μA. (b) I1 = 10 μA. (c) I1 = 50 μA.

4.3.5 Load regulation

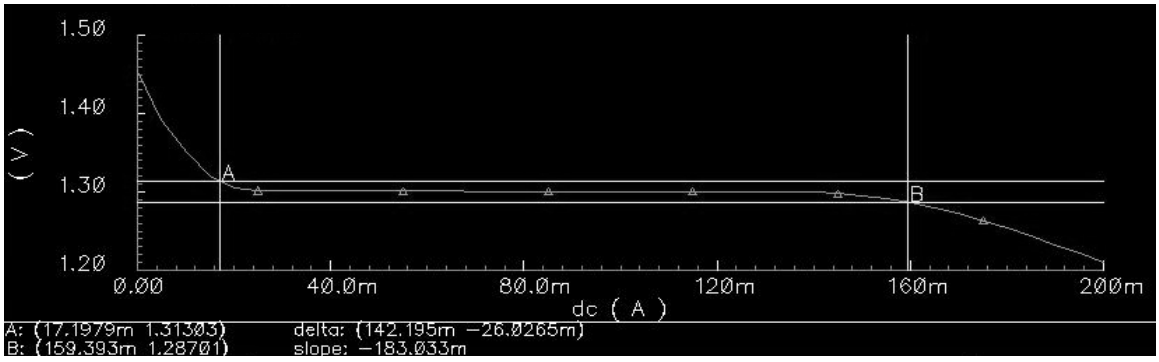
To test the load regulation of the LDO, the load current for each circuit was swept from 0 to 200 mA and the output voltage was plotted. The range of load current for which the output voltage was within one percent of the desired value was determined from these plots, which are found in Figure 4-7. For the circuit with I1=1 μA, the range was 19.8 mA to 174 mA. For the circuit with I1=10 μA, the range was 18.1 mA to 167 mA, and for the circuit with I1=50 μA, the range was 17.2 mA to 159 mA. Clearly, a minimum load current is needed for the LDO to be stable. This is because when the load current decreases, the output impedance of MP increases, lowering the frequency of the second pole and the decreasing the phase margin of the system. If the load current is too small, the second pole and the dominant pole will be too close together, causing the LDO to become unstable.



(a)



(b)

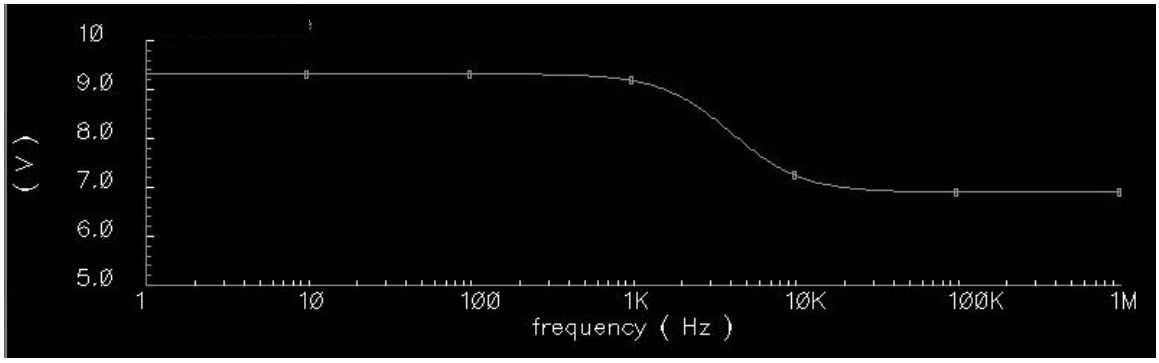


(c)

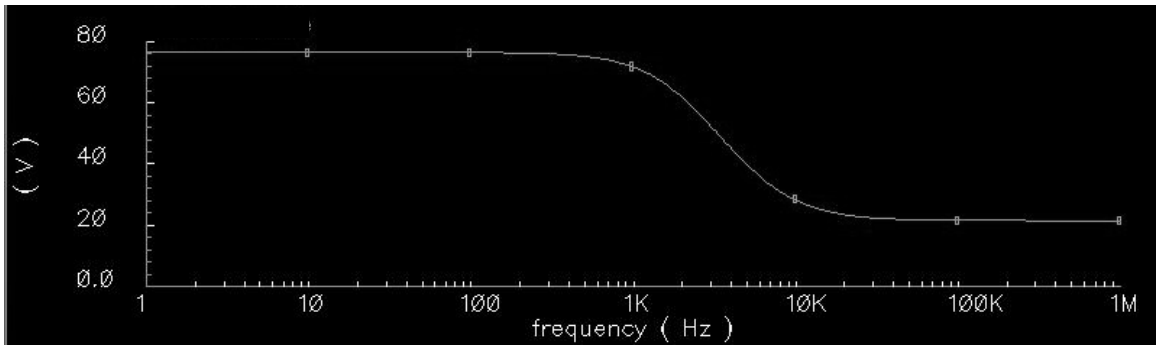
Figure 4-7 DC response of output voltage to sweep of load current from 0 to 200 mA. Points A and B mark off the range over which the output voltage is within 1% of 1.3 V. (a) I1 = 1 μA. (b) I1 = 10 μA. (c) I1 = 50 μA.

4.3.6 Output impedance

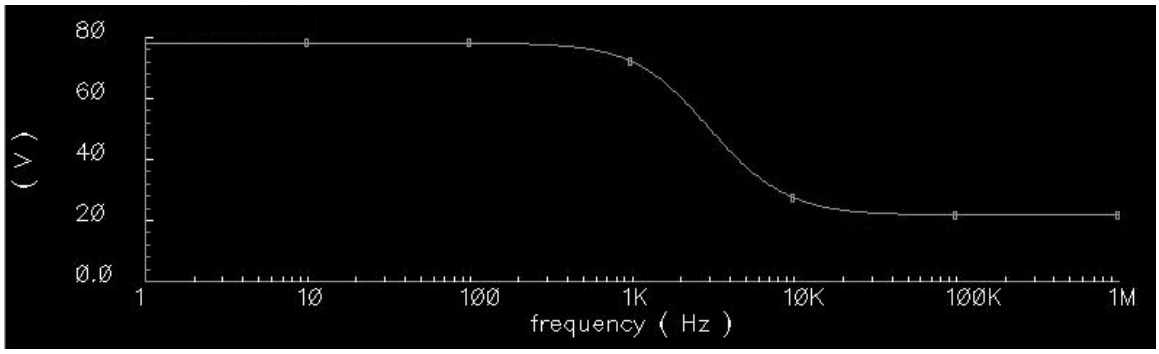
Plots of output impedance versus frequency were generated by putting a 1-A AC current source in series with the ideal 50-mA load current source, and plotting the AC output voltage as the frequency was swept. The magnitude of the output impedance was thus equal to the magnitude of the output voltage. As seen in Figure 4-8, the output impedance increased as the bias currents increased, which is the opposite of what one would normally expect. Higher current usually means higher gain, and higher gain usually means lower output impedance since R_o is divided by the loop gain, but the gain as well as the output impedance increased as the amount of current in I1 increased. This is because the dimensions of many transistors changed to keep devices in saturation as the bias currents increased, so the usual chain of reasoning breaks down. This also helps to explain why the maximum load capacitance decreased as the bias currents increased.



(a)



(b)



(c)

Figure 4-8 Plots of LDO output impedance vs. frequency. (a) I1 = 1 μA. (b) I1 = 10 μA. (c) I1 = 50 μA.

Chapter 5

Conclusion

A low-power two-stage LDO regulator was designed with good PSRR and good phase margin without the use of an external capacitor for compensation. By trading off PSRR with bandwidth and power, PSRR in the range of 40 to 60 dB was achieved. All circuits with a PSRR in this range had a bandwidth between 10 kHz and 350 kHz. Without a capacitive load, the phase margin ranged from 60° to 83°. The LDO, without the load current, consumed 150 μA of current or less under all conditions simulated. The dropout voltage was 500 mV, and the output voltage of 1.3 V could be sustained for a wide range of load currents above a certain minimum.

This project demonstrates the flexibility the designer has within a single topology. Small adjustments to various component values can allow the design to meet a wide range of specifications and loading conditions. To better understand the advantages and shortcomings of this design, it is compared with the designs discussed in Chapter 1. A summary of design characteristics discussed is found in Figure 5-1.

Designers	Supply voltage	Dropout voltage	PSRR	Current consumption	Max load current	External capacitor
Gupta, Rincon-Mora	1.6 V	600 mV	40 dB @ 10 MHz	not given	10 mA	none
Hoon et al	3.1 V	300 mV	60 dB @ 10 kHz	not given	50 mA	none
Wong and Evans	3.0 V	200 mV	67 dB @ 20 kHz, 40 dB @ 1 MHz	147 µA	150 mA	1 µF
Leung and Mok	1.5 V	200 mV	60 dB @ 1 kHz, 30 dB @ 1 MHz	38 µA	100 mA	none
Ha	1.8 V	500 mV	variable; 40-60 dB between 10 kHz and 350kHz	19 µA-150 µA	174 mA	none

Figure 5-1 Comparison of LDO designs of various authors

5.1 Comparison of design to the state of the art

Our design has a lower dropout voltage and higher maximum load current than that of Gupta and Rincon-Mora. Their design extends a good PSRR to much higher frequencies without an external capacitor, but it is not reported how much current their design used to do it. Also, it is likely that their design took up more area than ours because of the charge pump circuitry, the additional NMOS at the output, and the large resistor in the RC filter at the gate of this NMOS.

Our design has a higher dropout voltage but also a higher maximum load current than that of Hoon et al. Their design has a high PSRR up to 10 kHz without an external capacitor, but the power supply rejection at higher frequencies is not reported. This, combined with the lack of information about their design's power consumption, makes it difficult to compare the merits of their circuit with ours.

The LDO designed by Wong and Evans had a lower dropout voltage than our design, and a comparable maximum load current and current consumption. However, their supply voltage was higher, so their power consumption was higher. Their design had good PSRR up to 1 MHz, but it had the added help of a very large external capacitor, which our design did not.

Leung and Mok's LDO had a lower dropout voltage than our LDO, but also a lower maximum load current. Their design has very good PSRR at 1 kHz, which our design is able to accomplish with a comparable amount of current, but their design has good PSRR in the 1 MHz range, which ours does not. Their design is capable of good PSRR at high frequencies because of the added complexity of the DFC compensation scheme.

5.2 Summary of tradeoffs

Simulations of our LDO design demonstrated clear tradeoffs between several characteristics. For the same bias current, PSRR must decrease for bandwidth to increase, and vice-versa. To increase the bandwidth for a particular PSRR value, or to increase the PSRR while keeping the bandwidth constant, the LDO needed to burn more power. Another tradeoff involved PSRR and phase margin; increasing the PSRR decreased the phase margin, regardless of bias current. Driving a higher load capacitance also decreased the phase margin for all bias currents.

5.3 Future research

Our LDO design could be improved in several ways with future research. The bandwidth could be extended, perhaps using additional stages and a more complex feedback or compensation scheme. It would be interesting to find out if the same tradeoffs between PSRR, bandwidth, and power consumption exist with a more complicated circuit. The minimum load current required for stability could also be reduced so that the LDO would be able to be used for systems that require less current. These improvements would allow the LDO to be used in even more applications where low power and stability without an external capacitor are crucial.

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