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High PSRR Low Drop-out Voltage Regulator (LDO)

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Resumo

Os reguladores de tensão LDO são amplamente utilizados na actual indústria de electrónica, uma vez que fazem parte da unidade de alimentação. O aumento de produtos portáteis alimentados por bateria levou ao crescimento de soluções totalmente integradas num único circuito integrado, o que degrada o rendimento dos blocos analógicos que o constituem. Os LDO permitem proteger esses blocos do ruído injectado na alimentação dos mesmos. Para tal a sua capacidade de rejeição a esse ruído deve ser elevada. Além disso a baixa tensão de alimentação e corrente consumida é necessária, uma vez que as mesmas determinam a duração da bateria e estão associadas às soluções totalmente integradas.

Normalmente os LDOs têm a sua corrente de saída limitada, devido aos problemas de estabilidade associados. Numa tentativa de resolver esses problemas de estabilidade e aumentar o rendimento de PSRR dos mesmos, com elevado rendimento em termos de potência e baixo consumo de corrente. É apresentada uma nova técnica. A estabilidade é assegurada pela combinação de várias técnicas de realimentação e separação dos pólos, nomeadamente Nested Miller Compensation (NMC), Dynamic Miller Frequency Compensation (DMFC) e Single Miller Compensation (SMC). O baixo consumo de corrente é obtido pela topologia utilizada para o amplificador de erro. Contudo o PSRR encontra-se limitado pela mesma. Deste modo a polarização dinâmica é usasa para melhorar o PSRR e obter um elevado rendimento de potência.

O LDO foi implementado na tecnologia CMOS $SMIC\ 0.13\mu m$ e ocupa uma área menor do que $0.2\ mm^2$. Os resultados da simulação mostram que o LDO suporta uma transição da corrente de carga de $10\ \mu A$ para $300\ mA$ com uma queda de tensão entre a tensão alimentação e a tensão de saída inferior inferior a $200\ mV$. A estabilidade é assegurada para todas as correntes de carga. O tempo de estabelecimento é menor do que $25\ \mu s$ e as variações da tensão de saída relativamente ao seu valor nominal são inferiores a $75\ mV$. A corrente de consumo varia desde $15\ \mu A$ até $300\ \mu A$, o que permite atingir as especificações propostas para o PSRR de $-70\ dB\ @\ 1\ kHz$ e $-30\ dB\ @\ 1\ MHz$. Deste modo as técnicas apresentadas são adequadas para as soluções totalmente integradas num único circuito integrado e aplicações de baixa potência.

Palavras Chave

Circuitos integrados analógicos, PSRR, baixo consumo, tensão de referência, LDO.

Abstract

The Low Drop-out Voltage (LDO) regulators are widely used in present electronic industry, since they are one of the subsystems of the power management unit. The growing demand of mobile battery operated products and hand-held devices increases the use of System on Chip (SoC) solutions, which degrades the performance of the analog blocks. The LDO is used to protect the sensitive analog blocks from coupled supply noise, thus its Power Supply Rejection Ratio (PSRR) performance must be high. Moreover the low voltage supply and low quiescent current are a requirement, since they determine the battery life and are innate to SoC solutions.

Commonly the LDO have a limited operation range of load current due to their stability problem. In order to solve the stability problems and increase the PSRR performance of the LDO, with high power efficiency and ultra low quiescent current, a novel technique is presented. The stability is achieved by the use of combined pole-splitting and feedforward techniques, namely NMC, DMFC and SMC. The ultra low quiescent current is achieved by the use of a push-pull error amplifier architecture. However the high PSRR requirement is directly correlated with the performance of the error amplifier. Thus a dynamic biasing architecture is used to improve the PSRR performance, which also allows an high power efficiency.

The LDO was designed in $SMIC\ 0.13\mu m$ CMOS technology and occupies less than $0.2\ mm^2$. Simulation results show that the LDO provides a full load transient response from $10\ \mu A$ to $300\ mA$ with a low drop-out voltage of less than $200\ mV$. The settling time is less than $25\ \mu s$ and has overshoots and undershoots smaller than $75\ mV$. The quiescent current is variable in the range of $15\ \mu A$ to $300\ \mu A$. This allows to achieve the main proposal of the LDO, a high PSRR performance of $-70\ dB\ @\ 1\ kHz$ and $-30\ dB\ @\ 1\ MHz$. Thus the presented technique is suitable for SoC low power applications.

Keywords

Analog integrated circuits, PSRR, low quiescent consumption, voltage references, LDO.

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UGF Unitary Gain Frequency 4

LDO Low Drop-out Voltage vii

BJT Bipolar Junction Transistor 8

FET Field Effect Transistor 8

PSRR Power Supply Rejection Ratio vii

ESR Equivalent Series Resistance 4

GBW Gain Bandwidth Product 4

SoC System on Chip vii

CFC conventional Frequency Compensation 21

PCFC Pole Control Frequency Compensation 22

NMC Nested Miller Compensation v

SMC Single Miller Compensation v

DFCFC Damping Factor Control Frequency Compensation 22

PZTFC Pole-Zero Tracking Frequency Compensation 23

DMFC Dynamic Miller Frequency Compensation v

OTA Operational Transconductance Amplifier 26

1

Introduction

Contents

Power management has had an ever increasing role in the present electronic industry, this is, pushing toward a complete SoC, which allows less power consumption, a reduction of the area consumption and inherently costs, and also increasing the reliability of the system. This results from the increasing demand of mobile battery operated products and hand-held devices, such as cellular phones, pagers, PDA, camera recorders, and notebooks. The use of power management techniques to extend the life of the battery and consequently the operation life of the device is highly required. The design of this complex system (SoC) where the analog and digital blocks are fabricated in the same die, as shown in Figure (1.1), results in a dense digital circuitry in close proximity of sensitive analog blocks. Thus isolating the sensitive analog blocks from the noise caused by the switching of digital signals, RF blocks and DC-DC converters becomes a difficult task. Since the noise generated by these blocks can have amplitudes of the order of hundreds of millivolts and frequency range of tens of kilohertz to hundreds of megahertz, which can be propagated onto the supplies through crosstalk, deteriorating the performance of sensitive analog blocks.

A power management unit contains several subsystems including linear voltage regulators, switching regulators, and control logic. It is responsible for a correct and balanced distribution of energy in the integrated circuit, according to the needs of each block and operation modes. Thus the performance of the power management system is directly correlated with power efficiency and inherently the battery life.

Most systems incorporate several voltage regulators, which are fundamental building blocks that are used to supply a reference voltage to various subsystems and provide isolation among such subsystems. Absence of these power supplies can prove to be catastrophic in most high frequency and high performance circuit designs, since they can provide a constant voltage supply rail under all load conditions, since most hand-held and battery-powered electronics feature power-saving techniques to reduce power consumption and maximize the lifetime of the battery.

1.1 Motivation

The LDO is one of the fundamental building blocks of the Power Management Unit. Thus is widely used in many portable electronic systems, since a voltage independent of the state of battery charge is required. The LDO provides a stable voltage reference independent of the load impedance, input voltage variations, temperature and time. Thus it suitable for any equipment that needs constant and stable voltage, while reducing the wide fluctuations in upstream supply voltage and increasing the precision of the output voltage with few components.

The need of multiple on-chip voltage levels makes the voltage regulators a critical part of an electronic system design. The technology trend is forcing circuits to operate at lower power supply voltages driven by the market demand. Furthermore, high current efficiency has also become

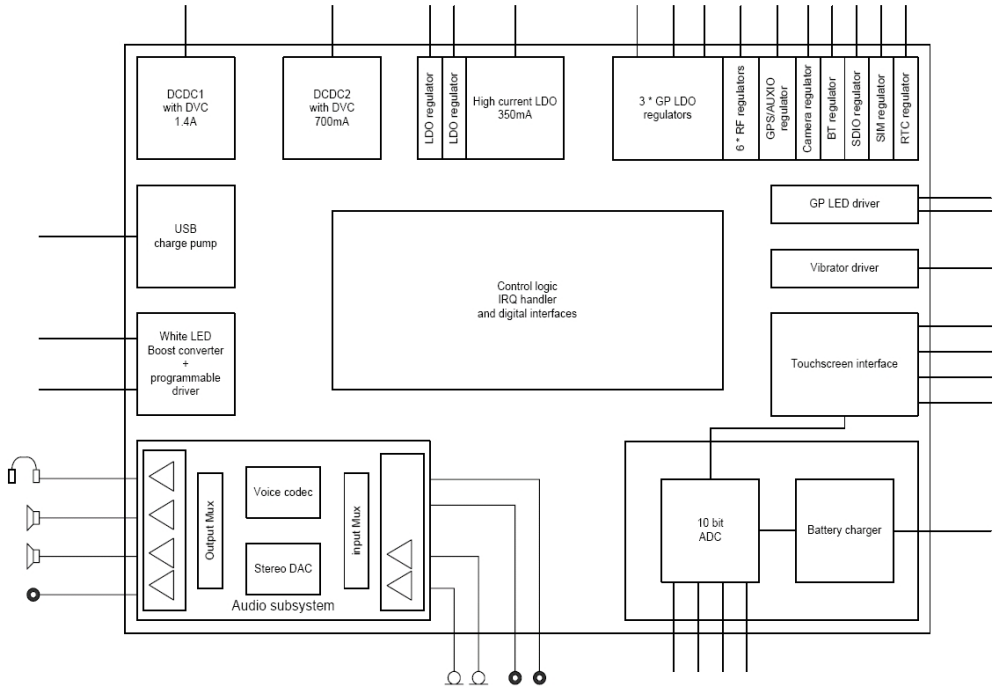


Figure 1.1: SoC architecture.

necessary to maximize the lifetime of the battery.

Moreover the on-chip and local LDOs are used to power up sub-blocks of the system individually, which can significantly reduce cross-talk, improve the voltage regulation and eliminate load-transient voltage spikes from the bonding wire inductances.

The dynamic range of analog blocks is largely affected by the use of a SoC system, since the use of low supply voltage and power consumption is required. The SoC system is plagued by the noise generated by the switching of digital circuitry, RF blocks and DC-DC converters. In such environment the linear voltage regulators are employed with the task of shielding the noise-sensitive blocks (i.e. analog blocks) from high frequency fluctuations in the power supply. Since the power supply noise directly translates to a degradation of in system performance. Therefore is imperative that LDOs have a good PSRR performance over a wide frequency range to improve the global performance of the system, this is commonly considered as the key figure of merit for a LDO voltage regulator. These are commonly placed after switching regulators to improve their efficiency.

1.2 Objectives

The scope of this work is focused on the realization of high efficiency current consumption, low dropout voltage and high PSRR LDO voltage regulator. Several techniques of the State-of-the-Art for this kind of circuit were employed in an attempt to improve the power efficiency of the system and the PSRR performance.

The research has been focused primarily on developing concepts that make high PSRR performance possible. However low voltage and low quiescent current consumption must be considered to obtain a LDO within the State-of-the-Art. The stability of the system is the major concern and must be ensured for all load current conditions.

The specification for current consumption of the circuit is $15\ \mu A$. Although this value is variable in a range of $15\ \mu A$ to $300\ \mu A$, is directly correlated with the load current consumption to ensure a high power efficiency of the system. The range of the battery supply voltage is from $3.6\ V$ to $2.6\ V$. The LDO circuit must supply a load current in the range of $10\ \mu A$ to $300\ mA$, with a stable output voltage (V_{out}) of $2.4\ V$. The drop-out voltage must be lower than $200\ mV$ for the load current range of $10\ \mu A$ to $300\ mA$. Since the value of the load current can yield the $300\ mA$, a $1\ \mu F$ off-chip capacitor is considered to ensure the stability of the system, with an Equivalent Series Resistance (ESR) that has a value between $0\ \Omega$ and $200\ m\Omega$.

The PSRR specification is $-70dB@1kHz$ and $-30dB@1MHz$. This as discussed previously a measure of the overall performance of the LDO. However this specifications limits the requirements of the error amplifier that compose the LDO circuit. Thus the error amplifier must ensure a high DC gain, a large Gain Bandwidth Product (GBW) and Unitary Gain Frequency (UGF) with a high output voltage swing.

The area occupied by the LDO is also a concern, thus the use of $MOScap$ is considered instead of the CVPP capacitor since it yields a better area consumption. However the CVPP capacitor is adopted where the linearity of the capacitance is a concern. The maximum occupied area is approximately $0.2mm^2$. The proposed LDO voltage regulator is designed in $SMIC\ 0.13\mu m$ CMOS technology.

1.3 Structure of the Work

The dissertation is organized in 7 chapters to reflect the necessary sequence of events that lead up to the complete design of a LDO system.

- **Chapter 2: Linear Voltage Regulators**
  This chapter provides the concepts behind linear voltage regulator systems and a brief description of blocks that that compose the LDO voltage regulator.

- **Chapter 3: Stability and PSRR**
  This chapter provides the concepts behind the stability and PSRR concerns of the system. It also contains the techniques of the State-of-the-Art used to improve the stability and PSRR of the LDO systems.

- **Chapter 4: System design**
  This chapter provides an overview through the design of different blocks that compose the LDO and the proposed strategy to achieve a low power consumption and high PSRR.

- **Chapter 5: Simulation results**
  This chapter provides illustrations of AC open-loop analysis, transient response, current limiter and PSRR performance of the proposed LDO strategy.

- **Chapter 6: Layout**
  This chapter provides an overview of the techniques that can be used to reduce design mismatch. An illustration of the complete floor plan of the proposed LDO circuit layout is also presented.

- **Chapter 7: Conclusions**
  This chapter is a summary of the contributions and major findings of this work for State-of-the-Art of LDO voltage regulator. It also includes a discussion of possible future work.

2

Linear Voltage Regulators

Contents

The main objective of a linear voltage regulator circuit is to provide a stable power supply voltage independent of load impedance, input voltage variations, temperature and current step variations of the load,

The alternatives for this generated voltage are DC-DC converters and switching regulators. However this kind of circuits are inherently more complex and expensive than linear regulators for low power realizations. The power supply voltage for a regulator is often obtained from a battery or a DC-DC converter. The linear voltage regulators have two main topologies: the conventional linear regulators and LDO voltage regulator [2]. The conventional linear regulators were the most widely used prior to the popularity of LDO voltage regulators, since conventional linear regulators are more stable for all loading conditions and do not require any capacitor at the output for stability purposes [3].

The conventional linear voltage regulator uses mainly a NPN Bipolar Junction Transistor (BJT) transistor as a pass element in emitter follower configuration, in either a single transistor realization or a Darlington configuration.

The LDO voltage regulators have gained popularity with the growth of battery powered equipment, since LDO voltage regulators can control their output voltage with much less headroom voltage, and therefore with small differences between supply voltage (V_{in})and load voltage (V_{out}). Most LDO regulator uses a $PMOS$ Field Effect Transistor (FET) transistor in common source configuration as a preferential pass element. The use of a PNP BJT transistor as a pass element has numerous disadvantages, since the use of a BiCMOS or BJT is limited by fabrication process compared with CMOS technology.

The two configuration options can be seen in Figure 2.1. The features of the pass element are important in design of the linear voltage regulators and are discussed in the follow of this work.

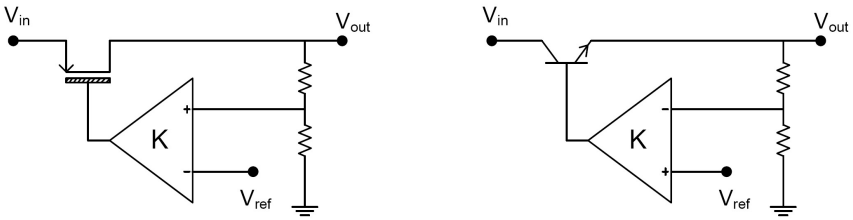


Figure 2.1: Two different main topologies of linear voltage regulators.

The design of linear voltage regulators has several issues to be considered on tradeoffs between stability and performance of the system. For example the demand to simultaneously achieve stability, high efficiency (i.e. low quiescent current consumption which is the current to drain), low drop-out voltage in low voltage environment (i.e. input/output voltage ratio must be as low as possible), high output voltage accuracy with short settling time, maximum output current

(load current) and high PSRR. This last characteristics is of a particular importance, since the linear voltages regulators in SoC solutions with digital circuits and RF blocks are commonly used and affects significantly the performance of the powered systems.

The linear voltage regulator topology shown in Figure (2.2) typically consists of a pass element, a error amplifier and a resistive feed-back network. The feedback network is a resistive voltage divider which scales output voltage (V_{out}) such that the scaled voltage is equal to the reference voltage when V_{out} is at its nominal value, this resistive network is internal to the LDO. The error amplifier has the function of comparing a scaled representation of V_{out} to the reference voltage (V_{ref}) and amplify that difference. The error amplifier output then drives the pass element to adjust V_{out}. The series pass element from incremental point of view, operates like a non-ideal gate to source voltage dependent current source with a transconductance value G_{mp} and a internal resistance r_{o-pass}, which as can be seen in the Figure 2.2 is connected between input voltage and the output voltage, The load resistance is given by the relationship between the V_{out} and the output current ($Iout$). The output capacitor C_{out} is located at the output of linear voltage regulator to improve the stability and varies with the specifications. Depending on the type of capacitor which can be solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors [4], it may have an internal ESR ranging between 10Ω and $10m\Omega$. The capacitance located at the output of error amplifier C_{par} appears due to the pass element and the input characteristics of the same. The R_{oa} is the equivalent output resistance of error amplifier.

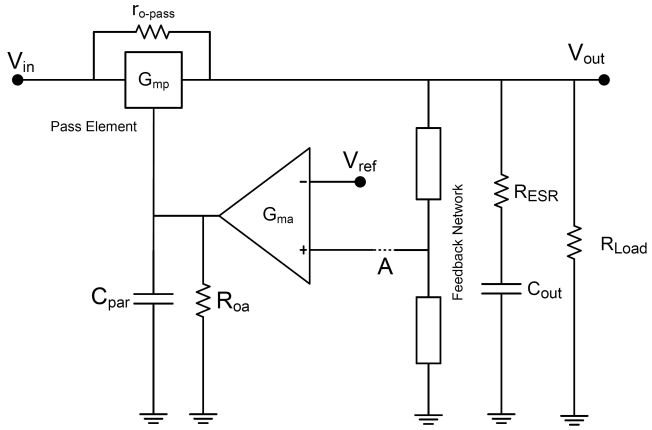


Figure 2.2: The typically linear voltage regulator topology

The important aspects of a LDO design can be resumed at three categories of specifications [5]:

1. The static-state specifications that include line and load regulations, as well as temperature coefficient.
2. Dynamic-state specifications that include the line and load transient responses resulting from transient load-current steps and the ripple rejection ration.

3. High frequency specifications which are characterized by PSRR and output noise.

The line regulation is characterized by the output variation ratio and results from a specific change in input voltage or in reference voltage, when the load circuit is open. It can be expressed by the equation(2.1),

$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{G_{mp} r_{o-pass}}{A_{ol}\beta} + \frac{1}{\beta} \cdot (\frac{\Delta V_{ref}}{\Delta V_{in}}) \tag{2.1}$$

where A_{ol} is the open-loop gain at low-frequency, G_{mp} and r_{o-pass} are the transconductance and output resistance respectively of pass element and β is the result of voltage divider feedback network. From the equation is possible to see that a high open-loop gain is required for a good LDO output voltage precision. However the stability of the system is sacrificed when the open loop gain is too increased. The stability problems will be analyzed more carefully in the Chapter (3).

Load Regulation is essentially the output resistance of the regulator, it a result from a sudden variations of load current. When the load current increases instantaneously the load capacitance supplies the extra current, and the capacitor voltage drops changing the output voltage. When the error amplifier detects the variation of output voltage scaled by feedback network, compensates this variation in attempt to maintain output voltage constant supplying more current from pass element. It is expressed by the ratio between output voltage and output current as can be seen in equation(2.2).

$$\text{Load Regulation} = \frac{\Delta V_{out}}{\Delta I_{load}} = \frac{r_{o-pass}}{1 + A_{ol}\beta} \tag{2.2}$$

As seen from equation(2.2), the performance of load regulation is improved as the open-loop gain is increased, however like line regulation the stability of the system is affected.

The analysis of static-state specifications can be concluded with the temperature coefficient analysis. This parameter is a result of the temperature dependency of the output voltage and measures the output variation due to temperature drift of the reference voltage, and the input offset voltage of the error amplifier. The temperature coefficient is given by the equation (2.3),

$$TC = \frac{1}{V_{out}} \cdot \frac{\partial V_{out}}{\partial \text{Temp}} \approx \frac{1}{V_{out}} \cdot \frac{\Delta V_{TC}}{\Delta \text{Temp}} = \frac{[\Delta V_{TC_{ref}} + \Delta V_{TC_{Vos}}] \frac{V_{out}}{V_{ref}}}{V_{out} \Delta \text{Temp}} \tag{2.3}$$

where ΔV_{TC} is the output voltage variation over the temperature range ΔTemp, $\Delta V_{TC_{ref}}$ and $\Delta V_{TC_{Vos}}$ are the voltage variations of the reference and input offset voltage of the error amplifier.

The dynamic-state specifications determines the capability of regulation of LDO voltage regulator, when the load current changes instantaneously or occurs a variation in the supply voltage. The LDO must respond quickly to the transients in attempt to reduce output voltage variations. This settling time is dominated by the closed-loop bandwidth of the the system, output capacitor,

ESR and load current. The worst case situation occurs when the load current suddenly steps from zero to its maximum specified value [6].

PSRR is an high frequency specification characterized by the ability of LDO voltage regulator reject the high frequency noise on the input voltage supply. Since the LDO on SoC with digital circuits and RF blocks is widely used, it is important to protect sensitive analog blocks from coupled supply noise that has amplitudes in order of hundreds of millivolts and frequency components in the range of tens of kilohertz to hundreds of megahertz. PSRR is a function of the pass transistor parasitic capacitance and is proportional to the reciprocal of the power supply gain as is shown in equation (2.4). The PSRR will be analyzed more carefully in the Chapter (3).

$$PSRR(\omega) = 20 \cdot \log \frac{A(\omega)}{A_{supply}(\omega)} \, [dB] \tag{2.4}$$

The effects of line and load regulation, temperature dependency and transient output voltage can be resumed into one specification that is accuracy [6]. Accuracy can be described by the absolute minimum and maximum output voltages (V_{o-min} and V_{o-max}) shown in follow equations:

$$V_{o-min} \leq \Delta V_{LDR} + \Delta V_{LNR} + \Delta V_{TC} + \Delta V_{tr} + V_{reference}(\frac{V_{out}}{V_{ref}}) \leq V_{o-max} \tag{2.5}$$

$$V_{reference} = V_{ref} + \Delta V_{TC_{ref}} + \Delta V_{LNR_{ref}} \pm V_{os} \tag{2.6}$$

$$Accuracy_{system} = \frac{V_{o-max} - V_{o-min}}{V_{out}} \tag{2.7}$$

where ΔV_{LDR}, ΔV_{LNR}, ΔV_{TC}, ΔV_{tr}, $\Delta V_{LNR_{ref}}$ and $\Delta V_{TC_{ref}}$ are absolute voltage variation resulting from load regulation, line regulation, temperature dependency and transient response respectively.

Along with higher power demands of low voltage environment in battery powered applications increases the demand of power efficiency of LDO voltage regulators. The main power issue in LDO is the battery life, which must maintain the required system voltage as the battery discharges. When the load current is low the quiescent (ground) current becomes a important factor in battery life. The quiescent current, load current and pass element voltage drop are the main parameters in efficiency of LDO voltage regulator. The power efficiency can be given by the equation (2.8) that is the relationship between the output power and power supply of the system.

$$Efficiency_{power} = \frac{V_{out} I_o}{(I_o + I_q) V_{in}} \leq \frac{V_{out}}{V_i n} \tag{2.8}$$

The influence of quiescent current in efficiency is increased when the output current is low, as is shown in the expression of current efficiency given by the equation (2.9), although when the load current increases the power efficiency becomes more pertinent since quiescent current is negligible compared with load current. The maximum power efficiency is defined by the ratio of the output and input voltages, as can be seen in equation (2.8).

$$Efficiency_{current} = \frac{I_o}{(I_o + I_q)} \tag{2.9}$$

Other characteristics that must be considered to achieve a high efficiency power of LDO is the dropout voltage, that is defined as the value of the input/output difference voltage, where the control loop stops regulating [6], this can be expressed on terms of switch ”on” resistance by the equation (2.10),

$$V_{drop-out} = I_{load} R_{on} \tag{2.10}$$

The value of $V_{drop-out}$ can range from 0.1V to 1.5V [6] when the transistor leaves the saturation and falls ino triode region, depending of pass element topology since R_{on} corresponds to r_{o-pass} in Figure (2.2). The power efficiency increases as the voltage difference between the output and input voltage decrease. Thus the value of $V_{drop-out}$ voltage must be as low possible to achieve a high power efficiency.

2.1 Pass element

The input voltage range, output current and $V_{drop-out}$ voltage directly affect the characteristic of the pass element on the regulator. As the maximum load current specification increases, the size of pass device necessarily increases and consequently the amplifiers load capacitance C_{par} increases, affecting the stability of the system as shown in Chapter (3). Hence most LDOs have limited operation range of load current due to their problem of stability. A variety of pass devices are available as can be seen in figure (2.3) with different tradeoffs between them.

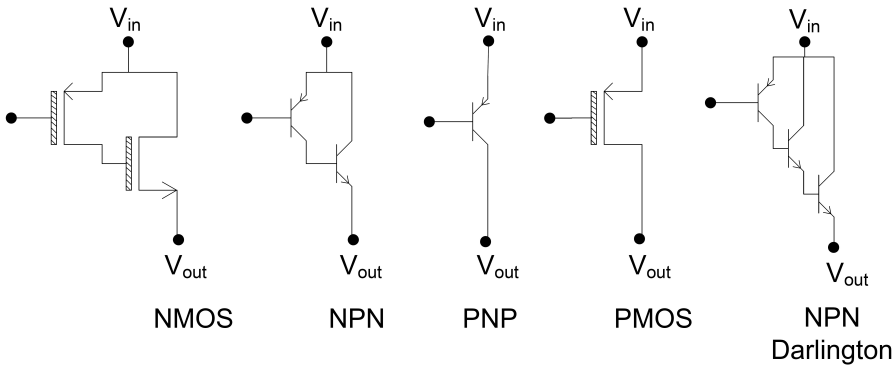


Figure 2.3: Pass device structures.

An important characteristic is the minimum permissible drop-out voltage, as seen before. This defines the maximum achievable efficiency to increase the battery life. Lowest drop-out voltage are achieved by $PMOS$ and PNP configuration as shown in Table 2.1, they are the pass element of LDO regulators. For this kind of device is approximately $0,1V$ and $0.4V$, for $NMOS$ and NPN

used in the conventional regulators the minimum drop-out voltage is respectively $0,8V$ and $1,2V$. A PNP is preferred to an NPN, because the base of PNP can be pulled to ground, fully saturating the transistor if necessary. The base of a NPN can only be pulled to supply voltage by an auxiliar PNP transistor limiting the minimum voltage drop ($V_{in} - V_{out}$). The use of BJT increases the $I_{quiescent}$ current because the error amplifier drives a bipolar pass element which sinks a relatively high base current during high-load current conditions, since the quiescent current becomes proportional to the output current, thus efficiency of LDO decreases for high loads. However the bipolar pass devices can deliver the highest output current, as can be seen in Table(2.1). Therefore, NPN, $NMOS$ and Darlington cannot provide dropout voltages below $1V$. The PNP and $PMOS$ allow the fully saturation, minimizing the $V_{drop-out}$ voltage and consequently the power dissipated. The $PMOS$ and $NMOS$ also allow quiescent current to be minimized.

Table 2.1: Comparison of pass device structures.

$Parameter$	$NMOS$	NPN	PNP	$PMOS$	$Darlington$
I_{o-max}	Medium	High	High	Medium	High
$I_{quiescent}$	Low	Medium	Large	Low	Medium
$V_{drop-out}$	$V_{sat} + V_{gs}$	$V_{sat} + V_{be}$	V_{ec-sat}	V_{sd-sat}	$V_{sat} + 2V_{be}$
$Speed$	Medium	Fast	Slow	Medium	Fast

Although a $PMOS$ does not have high drive capability, it must be large enough to meet the load current specifications as well as $V_{drop-out}$ voltage. Thus the gate capacitance is increased, which means that the error amplifier will have to supply a higher output current to drive the pass element [7]. As the supply voltage decreases the gate drive available for the $PMOS$ decreases, thus the aspect ratio of the pass device needs to be increased to provide acceptable levels of output current. Although $PMOS$ device is the better choice in compromise of drop-out voltage, $I_{quiescent}$ current flow, output current and speed, unfortunately is more difficult to make it stable.

2.2 Error Amplifier

The overall design of the error amplifier must be kept simple, since the specifications for a high efficiency power will impose a low quiescent current flow. The limiting factors for low quiescent current flow are amplifier's bandwidth and slew rate requirements. A tradeoff between performance and power dissipation is therefore necessary. The main aspects of error amplifier design are low output impedance (an important aspect to stabilize the system), high DC gain to ensure high loop gain for all loads, bandwidth, high output current slew-rate, output voltage swing with rail-to-rail output, since the error amplifier must turn off the pass device when the load turns off, internal poles at high frequency compared with the cross over loop frequency and low quiescent current. Load regulation as seen before is improved with an increase in open-loop gain that depends on the gain of error amplifier. Hence the design of GBW must be realized with caution, moreover the gain is limited by the UGF of amplifier and consequently the PSRR perfomance of

the system, as will be discussed in the Chapte(3). Thus the choice of error amplifier topology must consider the driving requirements of the pass device and the specifications of the system.

2.3 Feedback Network

The design of feedback network has two main topologies that can be used, resistive network voltage divider or two transistors (with the same size) as the configuration shown in Figure(2.4), with improvements and drawbacks between them.

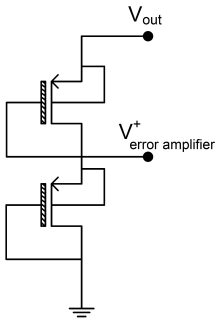


Figure 2.4: Feedback Network topology.

The use of the feedback network topology presented in Figure (2.4) allows a decrease of the area design and the quiescent current consumption, although the channel length of $PMOS$ transistors is largely increased in attempt to reduce current that flow through it. Consequently the capacitance between the output voltage and the scaled voltage to be used by the error amplifier increases. This imposes a slew rate which reduces the sensitivity of error amplifier to output voltages variations. The use of a resistor network increases the consumption of die area, since the resistor must be in order of hundreds of $k\Omega$. However allows lower quiescent current consumption and does not impose a slew rate when compared with transistor assembly.

2.4 Output Capacitor and ESR

The use of a huge pass device to supply a high load current increases the stability problems. Hence the use of an output capacitor is needed, this off-chip capacitor is the main obstacle to fully integrating of LDOs. The choice of the output capacitor has an ESR associated which can be critical for stability as will be discussed in Chapter (3).

Three types of output capacitor are suitable for LDO proposals and provided they meet the ESR requirements [4]:

1. The solid tantalum electrolytic capacitor.

2. The aluminum electrolytic capacitor.

3. The Multilayer ceramic capacitor.

The use of ceramic capacitors that typically have ESR values less then 0.05 improves the area of printed circuit board which allows a design more compact. Multilayer ceramic capacitors of the order of few microfarads are cheaper compared to tantalum alternative. However, most LDO voltage regulators oscillate with ceramic capacitor loads, hence their use is discouraged.

Low values of ESR are demanded for high PSRR performance at high frequencies and minimized transient output voltages variations, which allows a better load transient.

2.5 Summary

A brief description of Linear Voltage Regulators has been realized, with a simple analysis of several metrics that determines the system performance, and elements that are used to obtain a LDO voltage regulator system. In next chapter a careful analysis will be done, considering the use of a resistive network, a $PMOS$ pass device, and a error amplifier with two stages. As seen previously this configuration offers the best tradeoff between output current, drop-out voltage and speed. The main objective of all LDO proposals are enable a low voltage regulation, reduce the slew rate limit, improve load regulation and transient response with an increase in power efficiency of the LDO.

3

Stability and PSRR

Contents

3.1 Stability

Almost all LDO voltage regulators use a feedback loop to provide a constant output voltage independently of the load at output of the system. The location of the poles and zeros of the system depends on the high gain feedback loop. However the wide range of possible loads and the variability of the elements in the loop must be considered. For stability considerations each zero and pole contributes with $\pm 90^{\circ}$ of phase shift and $\pm 20\ dB/decade$ in gain, the stability of system can be measured by phase margin at UGF corresponding to $0dB$. The UGF is the frequency where the gain of the system is unitary, which corresponds at $0dB$ in scale logarithmic and indicates the highest usable frequency.

The analysis of stability of a LDO must be done considering all the components of the system, error amplifier, pass device, output capacitor, ESR and feedback network. As it is shown in the Figure (2.2) the pass device is in common-source configuration with a negative voltage gain,the feedback signal is connected to the positive input of the error amplifier in order to achieve a negative feedback loop. If a two inverting stage amplifier is used, the pass device is considered as the third gain stage, inverting the signal to guarantee negative feedback loop.

As discussed before, the output capacitor has a crucial rule in stability of LDO, the choice of this element depends on the output current specifications and inherently the aspect ratio of the pass device. Some authors [8] [4] [9] [10] consider the use of a second capacitor (bypass capacitor C_b), to improve the stability of LDO, which allows minimize the voltage variation resulting from sudden variations of current provided by C_o flowing through the ESR with less overshoots and undershoots during the load transient. Typically the C_b range is around $0.1\mu F$, hence their contribution for stability and output voltage variations is located at high frequencies. However the use of this second capacitor is discouraged, since it increases the area consumption and the final cost of LDO.

Sometimes the use of output capacitor is neglected, when the output current specifications does not require its use or a fully integrated LDO is required [5] [11] [12] [2]. The increase of aspect ratio of pass device that impose the slew rate and consequently the use of off-chip capacitor can be eliminated by the output current of error amplifier ability [13] directly correlated with quiescent current and performance of LDO.

By inspection of the basic topology of LDO that as can be seen in the Figure (2.2) two poles and one zero can be identified. For the AC analysis proposed, the feedback loop can be broken at point A in figure, assuming an infinitely large inductor as inserted at this point, which allows ”break” the AC contribution for the feedback loop. The small signal model of the basic topology proposed in Figure (2.2) is shown in Figure (3.1). The use of an error amplifier with two stages is considered.

From Figure (3.1), considering the voltage scaled by the feedback network (V_{fb}) and the volt-

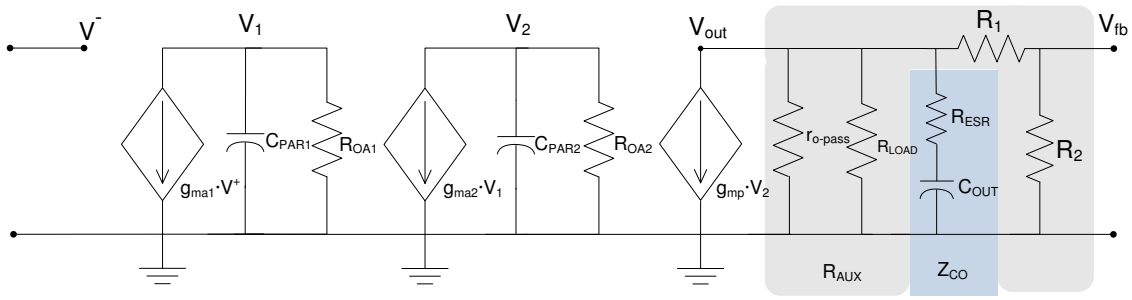


Figure 3.1: Small signal model of LDO basic topology.

age at positive terminal of the amplifier (V^+), as the output and input voltages respectively. The open loop transfer function (A_v) can be given by the Equation (3.1),

$$|A_v| = \frac{V_{fb}}{V^-} = G_{ma1}G_{ma2} \cdot \frac{R_{oa1}}{1 + sC_{par1}R_{oa1}} \cdot \frac{R_{oa2}}{1 + sC_{par2}R_{oa2}} \cdot G_{mp} \cdot Z_o \cdot \frac{R_1}{R_1 + R_2} \tag{3.1}$$

where the G_{ma1} and G_{ma2} are the transconductance of the error amplifier and G_{mp} are the transconductance of the pass device, R_{oa1} and R_{oa2} are the output resistance of first and second stage of the amplifier respectively. The C_{par1} is the parasitic impedance introduced by the second stage and C_{par2} is the parasitic impedance introduced the pass device. Z_o is the impedance seen by the output of the system and is given by the Equation (3.4),

$$Z_{co} = \frac{1 + sC_oR_{ESR}}{sC_o} \tag{3.2}$$

$$R_{aux} = R_{o-pass}||(R_1 + R_2)||R_{Load} \tag{3.3}$$

$$Z_o = R_{aux}||Z_{co} \tag{3.4}$$

where C_o and R_{ESR} are the capacitance and ESR of the output capacitor, R_{aux} represents the resistance at output of the system, where R_{o_pass} is the output resistance of the pass device. Thus from Equation (3.1) and Equations (3.2) (3.3) (3.4) is possible to rewrite the open loop transfer function as can be seen in Equation (3.5):

$$|A_v| = G_{ma1}G_{ma2} \cdot \frac{R_{oa}}{1 + sC_{par1}R_{oa1}} \cdot \frac{R_{oa}}{1 + sC_{par2}R_{oa2}} \cdot G_{mp} \cdot \frac{R_{aux}(1 + sC_oR_{ESR})}{1 + sC_o(R_{aux} + R_{ESR})} \cdot \frac{R_2}{R_1 + R_2} \tag{3.5}$$

For the majority of load-current (especially at high currents) R_{aux} can be simplified to R_{o-pass}, since $(R_1 + R_2)$ and R_{Load} are greater in magnitude. Thus the location of poles and zero can be approximated by the follow equations.

$$f_{P_1} = \frac{1}{2\pi \cdot C_o(R_{aux} + R_{ESR})} \approx \frac{1}{2\pi \cdot C_o(R_{o-pass} + R_{ESR})} \tag{3.6}$$

$$f_{P_2} = \frac{1}{2\pi \cdot C_{par1} R_{oa1}} \tag{3.7}$$

$$f_{P_3} = \frac{1}{2\pi \cdot C_{par2} R_{oa2}} \tag{3.8}$$

$$f_{Z_1} = \frac{1}{2\pi \cdot C_o R_{ESR}} \tag{3.9}$$

Other poles contributions due to the input stage parasitic capacitors are neglected since they are located at high frequencies below the loop's UGF. As can be seen in the Equations (3.6) and (3.9) the pole and zero depends on the output capacitor.

The DC open loop gain (K) can be given by the Equation (3.10), this is proportional to output resistance that is increased by a factor $G_{mp}R_{oa2}$ and consequently the gain increases [14]. The factor $G_{mp}R_{oa2}$ decreases with square root of the increasing current for an PMOS pass device $[\propto \frac{1}{\sqrt{I_{load}}}]$. As discussed before in Chapter (2) the DC gain is correlated with accuracy and performance of the system.

$$|K| = \frac{G_{ma1}G_{ma2}G_{mp}R_{oa1}R_{oa2}R_{aux}R_2}{R_1 + R_2} \tag{3.10}$$

The location of three poles and one zero can be seen in the Figure (3.2):

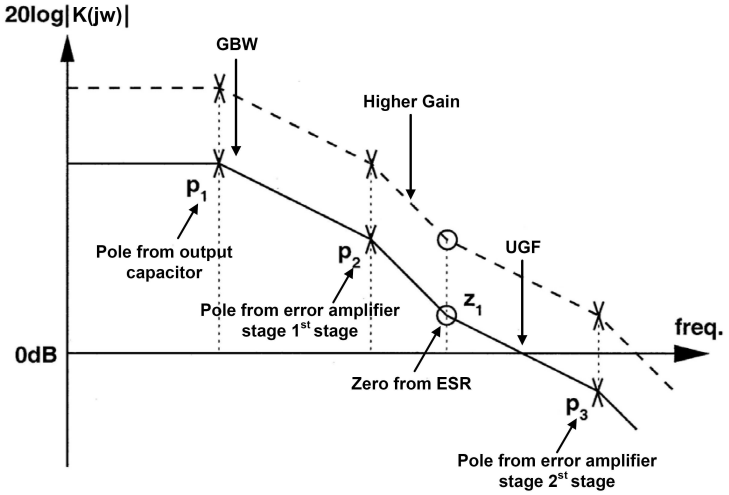


Figure 3.2: Typical LDO frequency response, location of poles and zero.

it is possible to see that the system is potential unstable due to the effects of two poles at low frequencies, which contribute with a 180^o gain phase shift to the UGF. To make selecting the appropriate output capacitor and the resistor placed in series with the capacitor easily solves the most stability issues. Therefore the range of values of ESR for a stable circuit is important and is

shown in Figure (3.3). The zero is formed by electrostatic resistance, the output capacitor, as can be seen in Figure (3.3), the stability is improved by smaller ESRs.

To improve phase margin and system stability the designer have to consider two main conditions:

1. the zero must be located below the loop's unity gain frequency.

2. all high frequency poles must be located at least three times the UGF.

The phase margin of the control loop at UGF always should be greater than zero to guarantee the system stability. The worst case for phase margin occurs for small load currents that corresponds to a very high load impedances and high R_{o-pass}. For this condition the zero maintain its value but the frequency of dominant pole decreases and consequently the unity-gain bandwidth of the open-loop response. This affects the performance of LDO in terms of dynamic response and PSRR at low loading conditions. Also for small load impedances that corresponded to a high load currents the closed-loop UGF increases and the parasitic poles become more important [3].Hence the stability of the system depends heavily on the load capacitance and the current in the output stage that limits it range. As shown in Figure (3.2) the position of first pole is located at very low frequency. To make the regulator stable a zero must be added to cancel one of the poles contribution, the feedback loop stability depends on the accuracy of the pole-zero cancellation. Other techniques can be used an will be discussed in next section.

However, if load current increases, the frequency of this pole shifts up. This frequency shift can be significant. In fact R_{o-pass} in Equation (3.6) decreases inversely proportional with the output current ($R_{o-pass} \propto \frac{1}{I_{load}}$) and the R_{load} must be included in the calculus of R_{aux}

3.1.1 State of the Art of the LDO compensation design

The state of the art of this kind of system is difficult to be defined, since it is dependent of system specifications. The output current, supply voltage and output capacitor are parameters that are directly correlated with the performance and stability of the system, although several techniques can be used to improve stability. The variable nature of load makes frequency compensation a difficult task.

The conventional Frequency Compensation (CFC) of LDO uses the zero generated by the ESR of output capacitor (Z_1) to cancel the contribution of P_2 to phase margin [4] [8] , since the poles are located at very low frequency the value of C_o need to be huge and have a very small ESR to create an appropriate ESR zero that ensures closed-loop stability. Furthermore this value depends on the fabrication process of output capacitor and this range can be too high or too small to generate the proper zero to cancel the pole and then the system will be unstable. In addition a

required high ESR introduces undesirable high overshoots and undershoots during load transient responses. Since LDO has wide output current range the poles change significantly with different load conditions, furthermore only one of the poles can be canceled by the ESR zero. Moreover the changes in the temperature will also affect the position of the poles and zero, which will be different since temperature coefficients of the output resistance of the gain stages and ESR are different. The relationship between the output capacitor, the ESR and the stability of the system is shown in Figure (3.3).

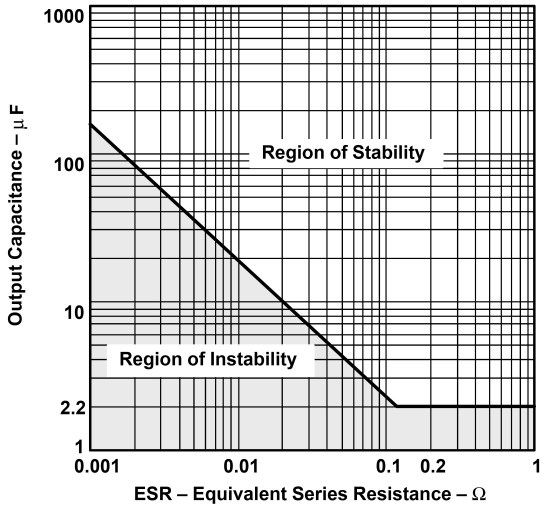


Figure 3.3: Relationship between C_o and ESR [1].

In order to solve this problem other techniques can be employed, the Pole Control Frequency Compensation (PCFC) can improve the LDO stability, independent changes in load current and temperature. Moreover is almost independent of ESR [11]. This technique is based on NMC [11] [15] [5] [3] [16] [17], that introduces a feedforward path for high frequencies through a compensation capacitor between the output of LDO and the second stage of the error amplifier as shown in Figure (3.4),

Another solution to the problem is Damping Factor Control Frequency Compensation (DFCFC) [5] [18] also based in NMC. The use of three stages in the design of the error amplifier allows a low-frequency, load independent dominant pole in the loop gain of transfer function, which increases the LDO stability. This approach allows high loop gain and excellent load regulation. However the drawback of NMC is present and the LDO is potentially unstable for low output current. Furthermore the complex circuits for DFCFC realization demand a high quiescent current that affects the power consumption of the system. This type of solution improves the PSRR performance.

The use of pole-splitting techniques (with the Miller capacitor across the gate and drain of the pass transistor) [10] to have one significant pole at any load can be used, the disadvantage of this technique is that the pole of first stage is pushed to low frequencies while the pole at the

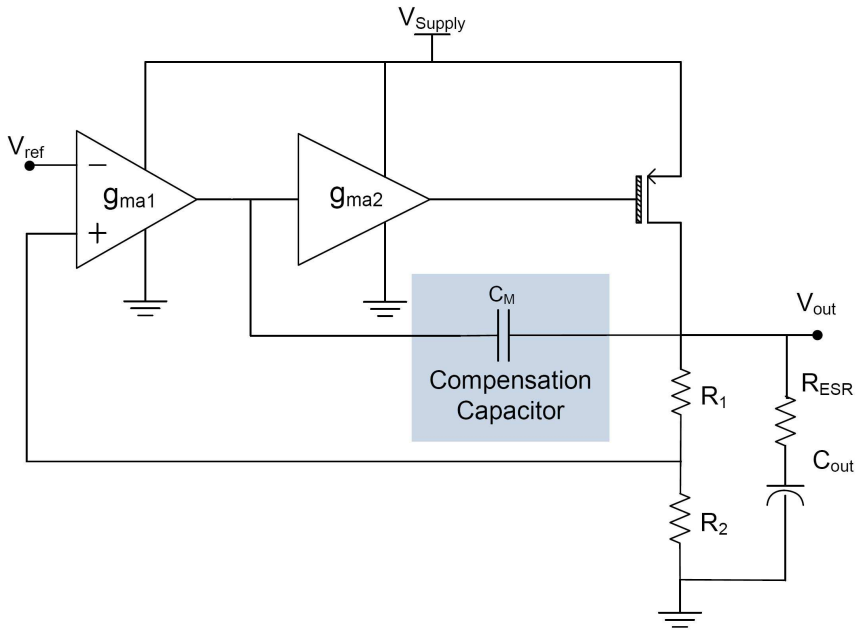


Figure 3.4: Example of Nested Miller Compensation.

LDO output goes to high frequencies, although such becomes a difficult task since the output impedance has a wide large variation and a large output capacitor can be used. Other drawback of this technique is that a huge capacitor is necessary so that pole-splitting can realized. The use of SMC on-chip capacitors at the output of the error amplifier have little effect on the first pole. The frequency of the second pole located at the output of the error amplifier is reduced for high values of R_{oa}. Thus the gain of the second stage is increased, since R_{oa} is proportional to the gain. However an increase in the load capacitance at the output of the error amplifier reduces both loop bandwidth and slew rate, furthermore more area is needed.

Another proposed solution is Pole-Zero Tracking Frequency Compensation (PZTFC) [19]. The proposed solution is based on moving the series RC network used for compensation into the output node of the error amplifier as shown in Figure (3.5), where the M_c transistor is in triode region and acts like a resistance.

If the resistance value can be controlled, the location of the generated zero can be adjusted. In order to have pole-zero cancellation, the position of dominant pole and zero should match with each other. However this is not optimal method to maintain stability, since the typical voltage regulator has a wide loading current range as discussed previously.

In CFC one of the problems is that only a zero is generated by ESR and only one of the poles can be canceled. However the ESR zero of the output capacitor can be replaced by a left-hand plane zero [3]. Thus the zero can be controlled and minimize overshoots, although the use of additional circuitry increases the complexity of the system and the power consumption. Other drawback of additional circuit is that PSRR performance is directly affected.

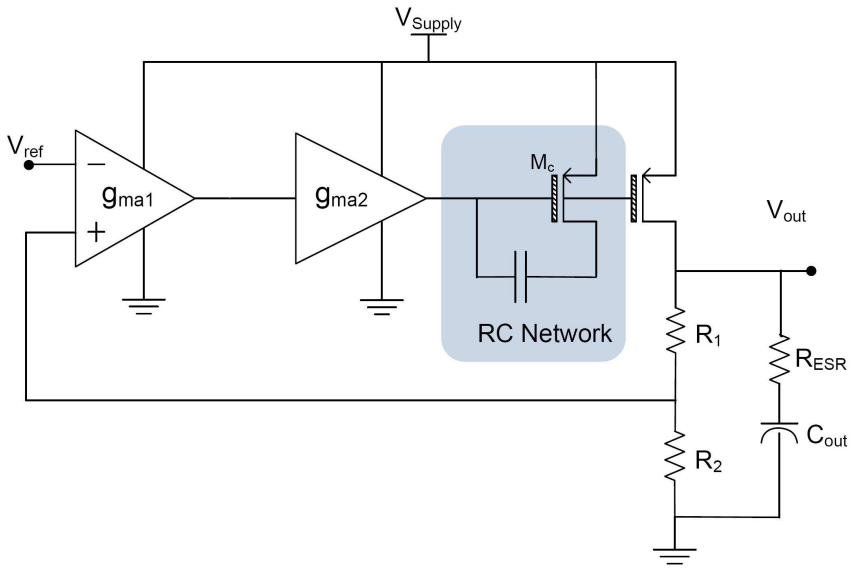


Figure 3.5: Example of Pole-Zero Tracking Frequency Compensation.

A dynamically biased voltage buffer has been proposed to improve the stability in [9] but a BiCMOS process is needed, which is limited by fabrication process. The use of error amplifier with a buffer stage cannot effectively turn off pass device during load transient, therefore it is discouraged.

Several of the methods described in this section can be used together in attempt to guarantee the stability. This strategy is also adopted by the presented dissertation. The DMFC [20] is a compensation technique that is based in PZTFC and NMC and increases the stability of the system. A RC network is introduced between the output of the error amplifier and the first stage as shown in in Figure (3.6), thus allows a Miller compensation, which can be controlled with the same technique used on PZTFC.

The stability of the system also can be ensured by the choice of pass device configuration as NPN or Darlington, since it tends to be insensitive to the output capacitive loading and provides a low-output impedance increasing the stability. However the use of charge pump is required which increase the circuit complexity. The characteristics of pass device as discussed better in Chapter (2).

The location of poles and zero in feedback loop must be suitable to achieve the stability proposal. Thus the slew rate imposed by the pass device must be considered, since the location of P_2 is associated with the parasitic capacitance generated by pass device. The ability of output of error amplifier to drive a high capacitance can improve the stability of the system. The use of a push-pull topology for the second stage of error amplifier [13] [12] helps improving stability of LDO without using any off-chip and on-chip compensation techniques, and the area efficiency of LDO is highly improved. Furthermore the power consumption can be improved since push-pull allows

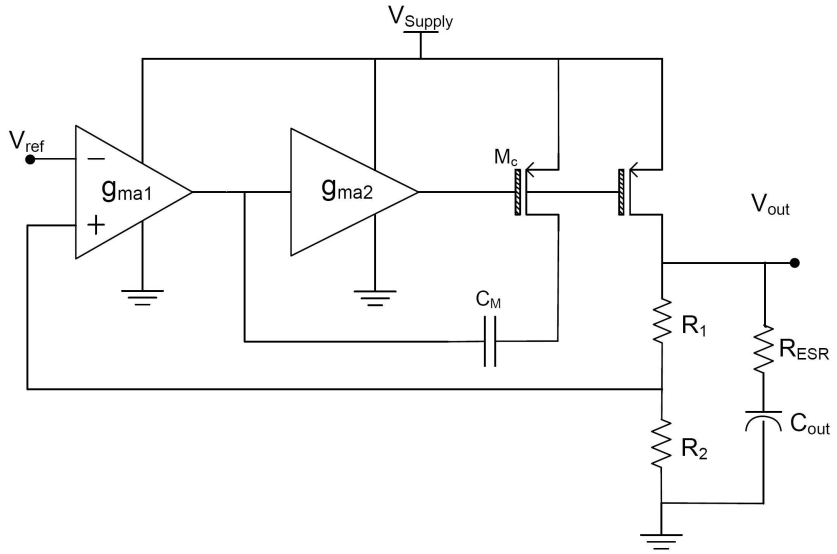


Figure 3.6: Example of Dynamic Miller Frequency Compensation.

the use of ultra-low quiescent current, with large GBW and wide rail to rail output voltage [21].

3.2 PSRR

The Power Supply Rejection Ratio has become an increasingly important parameter in modern SoC design as the level of integration increases. With large scale integration in attempt to reduce the cost and increase the area efficiency the analog and digital blocks are integrated on the same die, due to the demand for portable applications, such as cellular phones and Personal Digital Assistants (PDA)s, where radio-frequency blocks are commonly used.

Since SoC is widely used it is important to protect sensitive analog blocks from coupled supply noise generated by the switching of digital circuits, RF blocks and DC-DC converters, which has amplitudes in order of hundreds of millivolts and frequency components in the range of tens of kilohertz to hundreds of megahertz. Furthermore the high frequency noise that is generated by RF and digital circuits can be propagated onto supply rails through capacitive coupling.

Largely a linear voltage regulator is used with the task of shielding noise-sensitive blocks from high frequency fluctuations in power supply. Moreover the voltage reference used by LDO must be insensitive to noise [22] which yields a better performance of the system.

A general circuit has an input, an output and a power line as shown in Figure (3.7), thus transfer functions from any node to any other node are allowed. Moreover in order to calculate the PSRR of the total system, it can be divided into subcircuits or block diagrams, using control system theory [23]. Hence every node in the circuit can be expressed referring to another node in the circuit. However in many cases only the transfer function from input node (v_{in}) to the output

node (v_{out}) and from power supply node ($v_{powersupply}$) are important.

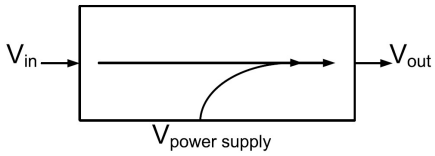


Figure 3.7: A block diagram of a general electrical circuit.

The PSRR is a function of ratio between transfer function of the power node to the output node ($A_{supply}(\omega)$) and the transfer function of the input node to output node is called the open-loop transfer function $A(\omega)$, as shown in Equation (5.21),

$$PSRR(\omega) = 20 \cdot \log \frac{A(\omega)}{A_{supply}(\omega)} \, [dB] \tag{3.11}$$

Where parameter $\frac{1}{A_{supply}(\omega)}$ is the reciprocal of the power supply gain commonly named as PSR, as distinct from PSRR. As can be seen in the Equation (5.21) the PSRR is proportional to $A(\omega)$ and inversely proportional to $A_{supply}(\omega)$, consequently if $A_{supply}(\omega)$ decreases the PSRR is increased. Thus from this equation can be seen that if the open-loop gain is increased the PSRR is improved. The main building blocks of analog cells are Operational Transconductance Amplifier (OTA), hence these analog cells must have high gain and high GBW to improve PSRR.

The equivalent mathematical equation for the output node as function of the v_{in} and of power supply node can be described by the superposition of the power supply gain and the open loop gain given by Equation (5.22) [23],

$$V_{out} = A_{powersupply} \cdot v_{powersupply} + A \cdot v_{in} \tag{3.12}$$

This type of analysis can be applied to LDO voltage regulators, where OTA is widely used as an error amplifier. The input voltage node is given by the reference voltage that is given by Equation (3.13), which is generally supplied by a bandgap reference which is supposed to present low noise characteristics and high immunity to power supply fluctuations.

$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_1}{R_2}\right) \tag{3.13}$$

Assuming that the contribution to supply noise of bandgap reference is negligible, the variations of v_{out} due to supply noise $v_{powersupply}$ for typical LDO of Figure (2.2), is given by Equation (3.14),

$$\begin{aligned} V_{out} &= A_{powersupply} \cdot v_{powersupply} + A_0\beta \cdot G_{mp} r_{o-pass} \cdot (-v_{out}) \\ \Leftrightarrow v_{out} &= \frac{A_{powersupply}}{1 + A_0\beta \cdot G_{mp} r_{o-pass}} \cdot v_{powersupply} \end{aligned} \tag{3.14}$$

where $A_{powersupply}$ is the power gain ($\frac{v_{out}}{v_{powersupply}}$), and A_o is the open-loop gain of the error amplifier, β is the feedback factor $R_2/(R_1+R_2)$, G_{mp} and r_{o-pass} are the transconductance and drain-to-source resistance of the pass device, respectively.

In order to improve the PSRR is necessary to increase the error amplifier gain or/and reduce the gain factor $\frac{1}{\beta}$ which is typically large for low quiescent current consumption. The aspect ratio of pass device and the current required for its operation also affect the PSRR and must be considered. The performance of PSRR is a key figure of merit for LDO voltage regulator, hence the LDO must be have high PSRR over a wide frequency range. The open-loop gain of the LDO feedback circuit is the dominant factor in PSRR for a defined range of frequencies. Increasing the gain with a high UGF is an alternative to improve the PSRR performance of the system. However makes it more difficult to stabilize. Is important have a good UGF so that the amplifier does not lose open-loop gain at relatively low frequencies [24].

The PSRR performance of LDO can be divided in three distinct regions [24], the first region at relatively low frequency between ($100Hz$-$1kHz$)is dominated by DC open-loop gain and bandgap PSRR. The second region extends from GBW of the regulator where PSRR is dominated by open-loop gain up to UGF where it is dominated by the error amplifier bandwidth of the system, at midband of frequencies. The third region is above the UGF at high frequency where the effects of feedback loop are neglected. In this region the output capacitor with ESR and any parasitic from $v_{powersupply}$ to v_{out} dominate, hence a larger output capacitor with less ESR will increases the PSRR in this region, although it can decrease the PSRR performance at some frequencies, since the capacitances at high frequencies have a behavior of shunt circuit. A model of equivalent circuit of LDO at high frequencies (i.e. in the third region) is presented in Figure (3.8).

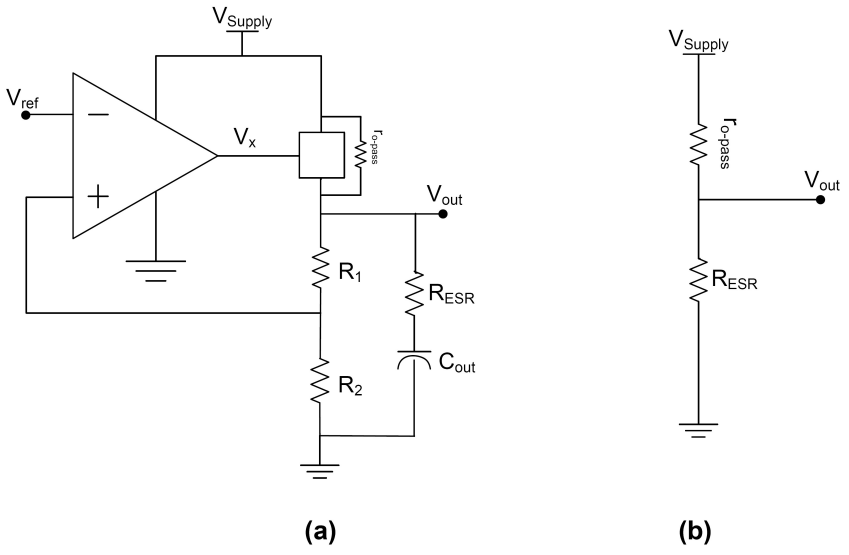


Figure 3.8: (a) - Typical topology of LDO. (b) Equivalent simplified circuit at high frequencies.

The PSRR of the circuit at high frequencies can be obtained by the Equation (3.15),

$$\text{PSRR} = \frac{\Delta V_{supply}}{\Delta V_{out}} \cdot \frac{V_{out}}{V_{ref}} = \frac{\Delta V_{supply}}{\Delta V_{out}} \cdot A(s) \approx \frac{r_{o-pass} + R_{ESR}}{R_{ESR}} \cdot A(s) \tag{3.15}$$

as can be seen by inspection of the Equation (3.15), low values of R_{ESR} improve the PSRR performance of the system. The use of large capacitors as mentioned previously in Chapter (2) lowers the UGF, which corresponds to the worst case of PSRR, typically in the range of ($1MHz$-$10MHz$), as shown in Figure (3.9). Is also is possible to distinguish the three region described before, and the influence of ESR at high frequency over the PSRR curve. Two curves are presented: the full line represents the PSRR curve without ESR and the doted line the PSRR curve with influence of ESR, where a zero is introduced.

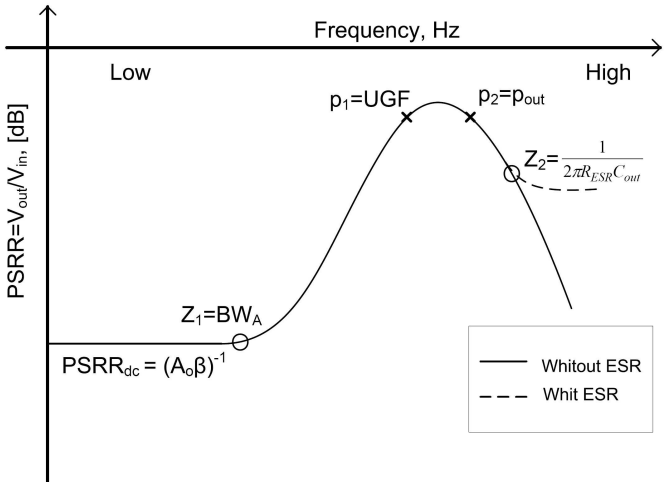


Figure 3.9: PSRR Curve of a linear voltage regulator.

The BW_A is characterized by R_{oa} and C_{par} the resistance and parasitic capacitance at the output of error amplifier respectively, and can be given by the Equation (3.16),

$$BW_A = \frac{1}{2\pi \cdot R_{oa} C_{par}} \tag{3.16}$$

since the choice of the topology of the error amplifier is crucial to obtain a good PSRR improvement [25], moreover the design of very symmetrical OTA helps this improvement. The C_{par} can be controlled with a Miller Compensation scheme, however the GBW of the system will be reduced and the use of on-chip capacitor increases the area consumption.

3.2.1 State of the Art of LDO PSRR design

Numerous techniques can be used to improve the PSRR of linear regulators. The simplest solution is to place an RC filter in line with the power supply to filter out fluctuations before they reach the regulator [22]. However,considering a low voltage integrated SoC solution, the high power losses and silicon area required, and reduction in voltage headroom caused by this resistor discourage the use of this approach.

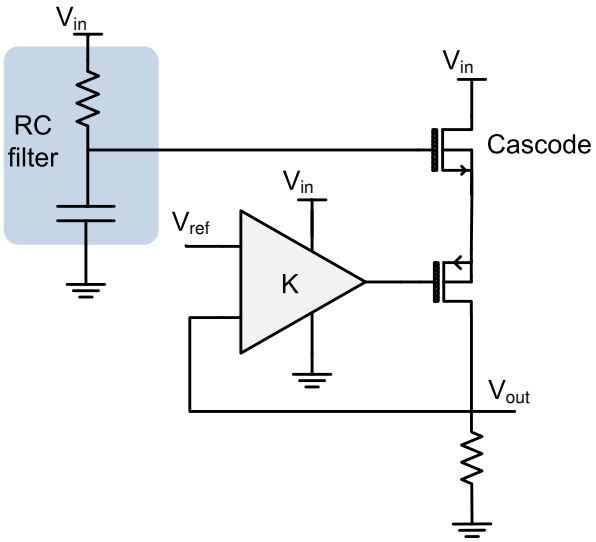
Another methodology that can be employed is the use of two linear regulators in series to effectively improve the PSRR. However this method has the disadvantage of increased power dissipation and voltage headroom, and a high PSRR over wide frequency range cannot be obtained since the two regulators have limitations in the third region as discussed previously.

In an attempt to isolate the power supply noise from LDO, a NMOS cascode can be used for the pass device as shown in Figure (3.10), thus the pass device is isolated from the supply line instead of being connected to it. A $NMOS$ configuration is used to do pass device. Since NMOS cascode is a source follower, it cannot be used with a gate voltage below the supply voltage, therefore the voltage at the gate must be boosted using a charge pump that generates a higher voltage. The error amplifier cannot be cascoded as conventionally as the pass device, in attempt to maintain a low dropout voltage as discussed before in Chapter (2) a charge pump must be used to boost the supply voltage of error amplifier as presented in Figure (3.10(b)), an RC filter is used to suppress fluctuations in the power supply line and fluctuations of charge pump. This solution leads to higher circuit complexity, with large power and area consumption.

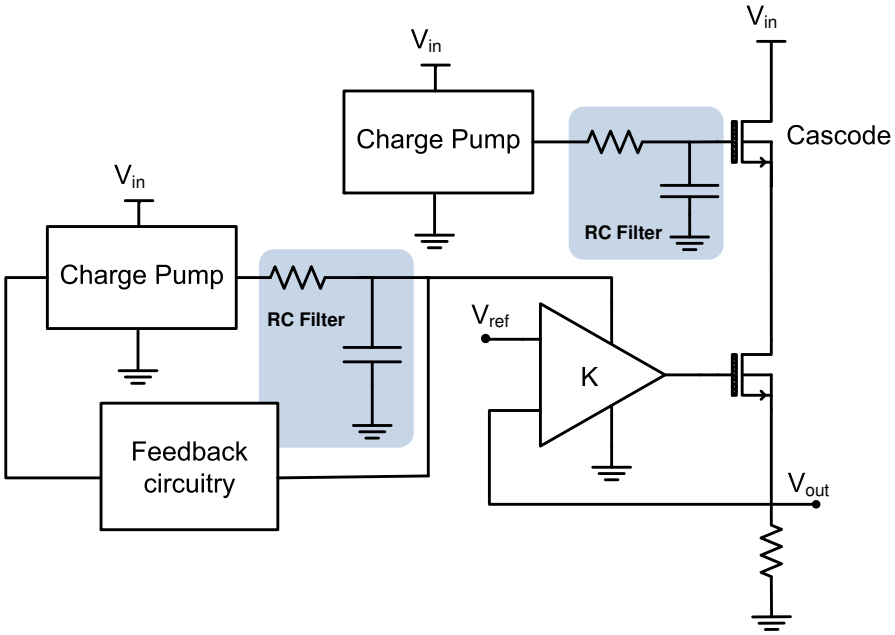
Alternatively the gate of $NMOS$ cascode can be biased through a RC filter due to relatively high voltage headroom, which allows to supply the error amplifier directly from power supply line as presented in Figure (3.10(a)). However as seen in the beginning of this section this technique has numerous drawbacks due to the use of RC filter.

The use of internal cascodes in error amplifier improves the PSRR [23], since their use increases the immunity of the gate of pass device from power supply fluctuations and consequently decreasing output voltage ripple, which improves the PSRR of the system. As mentioned before the general PSRR of the system is the result of the multiple stages. In an attempt to cancel the contribution of error amplifier to PSRR, it can be supplied by the output voltage of the LDO, which makes the PSRR only dependent of the differential DC voltage between input and output (i.e. dependent of pass device properties). However this technique only can be used in specific cases, since the error amplifier must be able to cut-off the pass device.

One technique to increase the PSRR over a midband frequencies is the use of current mirror technique for the error amplifier [26]. The use of Miller compensated circuits has the problem that for high frequency the compensation capacitor acts as a short circuit with unitary gain, which couples all the noise to the output. The PSRR of SMC could be improved, if there where another signal path that have gain -1 at the frequency of interest to cancel the first, according to the



(a) Simplified cascoding topology to assure PSRR improvement



(b) Two charge pumps topology to assure PSRR improvement.

Figure 3.10: State of the Art techniques to improve PSRR

superposition principle.

Another methodology that can be used consists in trying to design the error amplifier such that its gain will be unitary. For this to happen the voltage at the gate of the pass device needs to be close of V_{supply}. Thus the voltage at the gate of pass device tracks the voltage of the supply line in attempt to suppress fluctuations at output voltage. This technique is based on a subtractor stage [27] inserted between the pass device and the error amplifier as shown in Figure (3.11), which feeds the supply noise directly into feedback loop and modulates the pass device gate with respect to it.

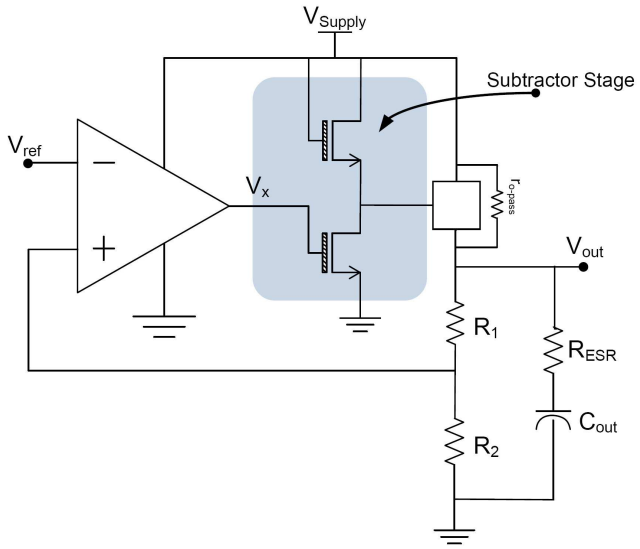


Figure 3.11: Subtractor stage technique to improve the PSRR.

3.3 Summary

In this Chapter the problem of Stability and PSRR in LDO is discussed. The two are inherently correlated, since the location of poles, the open-loop gain, the UGF and GBW of error amplifier affects the stability and PSRR of the system simultaneously. It is noticed that tradeoffs are inherently between the two, and the state of the art of this kind of system is difficult to be defined, since its dependent of specifications of the system. The voltage reference must be selected with the main proposal of the specifications, since it has an important role in PSRR performance of the system. The LDO is unstable by nature because it has three poles and only one zero. Nevertheless their location can be suitable to obtain the stability with a carefully design. In next chapter the design considerations of state of the art of stability and PSRR, are used to design a new LDO topology.

4

System Design

Contents

4.1 Motivation

The scope of this work is focused on the realization of high efficient current consumption, low dropout voltage and high PSRR LDO voltage regulator. These characteristics are driven by portable and supplied battery applications, such as cellular phones and PDA. These are important issues and are required in the present electronic industry, driven toward total chip integration (SoC) demanding that power supply circuits be included in every chip. LDOs are an essential part of any electrically powered system that require a reduction of the high input voltage of battery cells to the lower and more acceptable levels, shielding the reference voltages from fluctuations in power supply rails.

As a result, LDO regulators and other power supply circuits are always in high demand. Current efficiency is particularly important at low load-current conditions the life of the battery is adversely affected by low current efficiency. The summary of the LDO specifications are presented in Table (4.1).

Table 4.1: Summary of the LDO parameters specifications.

$ParametersDescription$	$Value$
V_{in}	$2.6V$ to $3.6V$
V_{out}	$2.4V$
I_{o-max}	$300mA$
I_{o-min}	10μ
$I_{quiescent}$	$15\mu A$ to $300\mu A$
$V_{drop-out}@I_{load} = 10\mu A - 300mA$	$\leq 200mV$
$Transient\ \Delta V_{o-for I_{load} step}$	$\leq 75mV$
$Temperature$	$-40^{o}Cto125^{o}C$
$OutputCapacitance$	$1\mu F$
ESR	0 to $200m\Omega$
$PSRR@1kHz$	$-70dB$
$PSRR@1MHz$	$-30dB$

From Table (4.1) we highlight several specification parameters such as current efficiency, since the quiescent current is extremely low, current boosting, which allows the range of output current to be between $10\mu A$ and $300mA$. As mentioned in Chapter 3 the frequency stability requirements are dependent on load-current, which leads to several considerations in the design of the LDO. The PSRR is a key figure of merit for LDO voltage regulators and is a major concern in the scope of this work and LDO design.

The techniques discussed previously in Chapter 3 will be adopted to design a LDO regulator that allows maximum use of currently existing techniques, which allow a suitable LDO realization with low drop-out voltage, and low quiescent current flow with a high PSRR. The advantages and drawbacks of the circuits used to realize these concepts will be discussed within the context of this Chapter. The design of LDO proposed strategy was designed in $SMIC\ 0.13\mu m$ CMOS technology.

4.2 Pass Element Design

The choice of the pass element is very important when high efficiency and low dropout voltage are required. Increasing the size of the pass transistor lowers the dropout voltage for a particular output current that has a range in order of milliampere. As load current specification increases, the pass transistor must be larger, however this results in an increase of the gate capacitance, which makes difficult to meet stability and slew rate requirements. Thus a higher output current of the error amplifier is required, moreover the current efficiency decreases due to the increase of the quiescent current consumption.

The design presented in this work uses a $PMOS$ pass transistor in common-source configuration as shown in Figure(4.1). A $PMOS$ pass transistor does not have a very high drive capability. It must be large enough to meet load current as well as drop-out voltage specification. The minimum channel length of the pass transistor is not used, since it makes the transistor output impedance unacceptably low at high load currents. Moreover the contribution of the pass transistor for improvement of the PSRR at high frequencies can be greatly affected if minimum channel length of the pass transistor is used.

The output impedance of the pass device is inversely proportional to the current flowing through it, which can change the position of the dominant pole. When the load-current is low the dominant pole frequency, is also low. This pole is determined by the output capacitor and the output impedance of the pass transistor, and is given by the Equation (4.1).

$$f_{P_1} = \frac{1}{2\pi \cdot C_o(R_{o-pass})} \approx \frac{\lambda I_{load}}{2\pi \cdot C_o} \tag{4.1}$$

Where λ is the channel length modulation parameter. As the load-current increases, the position of the dominant pole increases linearly and consequently so does the UGF. When the gate capacitance is increased, the location of the parasitic pole moves to lower frequencies. Consequently, the phase margin of the system is degraded and stability may be compromised.

The bulk of the power $PMOS$ transistor is shorted to the source to eliminate the substrate leakage and eliminates the commonly named bulk effect phenomenon as shown in Figure(4.1). The threshold voltage is described by the Equation (4.2).

$$|V_{th}| = |V_{t0}| + \gamma[\sqrt{2|\phi_f| - V_{SB}} - \sqrt{2|\phi_f|}] \tag{4.2}$$

The $PMOS$ pass transistor can operate in cut-off region for small load current, or operate in saturation region or even linear region to handle heavy load current. When the input voltage increases, the operating region of the power transistor changes from linear to saturation region.

The output current of power $PMOS$ transistor when it is operating in saturation region can be expressed by Equation (4.3).

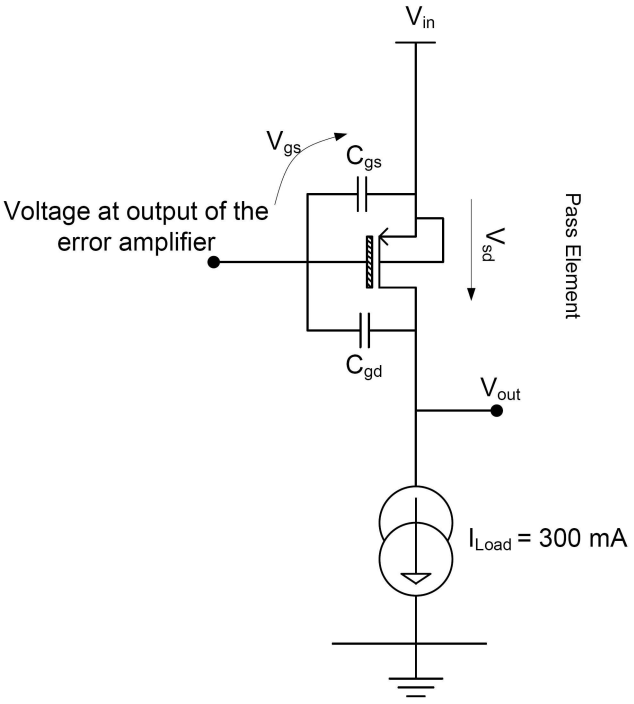


Figure 4.1: Pass element design.

$$I_{sd} \approx \frac{K_P}{2} \cdot \frac{W}{L}(V_{sg} - V_{th})^2 \tag{4.3}$$

Where K_P and $\frac{W}{L}$ are the transconductance parameter and aspect ratio of $PMOS$ transistor respectively. We suppose that $PMOS$ pass transistor operates in linear region at dropout voltage, and hence the required transistor size can be reduced significantly for the ease of integration and reduction of area consumption. The current relationship when the pass transistor is in triode and linear region is given by Equation (4.4).

$$\begin{aligned} I_{sd} &\approx \frac{K_P}{2} \cdot \frac{W}{L}[(V_{sg} - V_{th}) \cdot V_{sd} - V_{sd}^2] \\ &\approx \frac{K_P}{2} \cdot \frac{W}{L}[(V_{sg} - V_{th}) \cdot V_{sd}] \end{aligned} \tag{4.4}$$

The resistance of $PMOS$ pass transistor in triode region R_{on} is given by the relationship between the source drain voltage and the output current of $PMOS$ and is given by Equation (4.5).

$$R_{on} \approx \frac{V_{sd}}{I_{sd}} \approx \frac{2L}{K_P W} \cdot \frac{1}{(V_{sg} - V_{th})} \tag{4.5}$$

From Equation(4.5) is possible to write the dropout voltage $V_{drop-out}$ as a function of load current and R_{on} by the Equation(4.6).

$$\begin{aligned} V_{drop-out} &\approx I_{load} \cdot R_{on} \\ &\approx \frac{2L}{K_P W} \cdot \frac{I_{load}}{(V_{sg} - V_{th})} \end{aligned} \tag{4.6}$$

The output current I_{Load} has a large range between $10\mu A$ and $300mA$. The $PMOS$ will operate in cut-off region for small load current. Since the resistance of pass transistor $R_{o-pass} \propto \frac{1}{\sqrt{I_{load}}}$, the output current of the $PMOS$ in weak inversion is expressed by the Equation(4.7).

$$I_{sd} \approx I_{DO} \frac{W}{L} \cdot exp^{\frac{V_{gs}}{\frac{nKT}{q}}} \tag{4.7}$$

Hence, a $PMOS$ pass transistor with a very-large size is used in attempt to improve the PSRR of the LDO system and held the output current requirement. The large size results in a large gate capacitance, which imposes a large slew rate, and a large transconductance of the pass transistor (G_{mp}), thus increasing the gain of pass transistor. It should be noted that the gain of the $PMOS$ pass transistor may be less than the unity. However the product of the voltage gain of the error amplifier is greater than one and it is always verified in LDO design. The error amplifier will be discussed more carefully in Section 4.2, as designed with proposal of decrease the slew-rate imposed and high rail-to-rail output. As mentioned previously, when the loop gain increases, the LDO based on dominant-pole compensation may be unstable and this must be considered in overall design.

The parameters of the $PMOS$ pass transistor used in design of LDO proposal are shown in Table (4.2) and they satisfy the Equation (4.6) and the correspondent parameter specifications of Table (4.1)

Table 4.2: Parameters of the $PMOS$ Pass Transistor.

$Parameter$	$Value$
μpC_{ox}	37 $\mu A/V^2$
W	400 μm
L	431 μm

4.3 Error Amplifier Design

The error amplifier design demands careful attention to meet the required specifications, namely high DC gain to ensure good accuracy, load and line regulations, and high rail-to-rail output voltage to ensure the cutt-off of the $PMOS$ pass transistor, internal poles at significantly higher frequencies compared to the cross over loop frequency, low quiescent current and high output current, which allow a fast charging of the power device gate capacitance, reducing the slew rate and the settling time.

As discussed previously the performance of the error amplifier is directly correlated with the PSSR of the LDO system. The intuitive mode analysis of $PSRR$ discussed previously in Chapter 3 helps in the definition of error amplifier specifications. Since the PSRR specifications of the LDO system are $-70dB@1kHz$, the error amplifier must have a open-loop DC gain of $70dB$ for dropout voltage, with a GBW of $1kHz$. It is difficult to achieve a high DC gain with a single stage, therefore the use of two-stage-amplifier topology is mandatory for the gain specifications. However, the two-stage-amplifier topology is not optimum since the power transistor cannot function as a high-gain stage in dropout condition. Thus the pole-splitting effect is not effective and the output precision is also degraded. The power transistor will be considered as the third gain stage. The DC gain of error amplifier can be improved with the use of cascodes, which also improve the PSRR performance.

The first stage detects the difference between the reference voltage (V_{ref}) and the feedback signal (V_{fb}), to provide the error signal to the second stage. This stage must have high-swing with high rail-to-rail output voltage. The first stage of the error amplifier has a folded-cascode configuration, which limits the output swing of this stage, however a more suitable voltage can be provided by the second stage.

One of the major concerns of the error amplifier is the current consumption, hence its complexity must be low, since an increase in complexity has inherently an increase in quiescent current consumption. Thus appropriate design techniques must be used to ensure the $15\mu A$ of I_q.

In attempt to reduce the I_q at steady state, a push-pull configuration is used for the second stage of the error amplifier, it maintains a low static power consumption with capability to generate output currents greater than the output stage quiescent current. Thus the second stage is able to charge or discharge gate capacitance C_{par} quickly, which allows that both positive and negative direction slew-rates can be successfully enhanced, even if low quiescent current is used. Moreover the amplifier-output voltage is able to go from nearly zero to supply voltage of the error amplifier, thus an high rail-to-rail output voltage can be ensured. Which with other second stage topologies is difficult to achieve.

As mentioned in Chapter 3, in order to obtain good PSRR performance the gate of the power transistor should be referenced to the LDO input voltage and the error amplifier positive supply. This means that the power supply gain of the error amplifier should be unitary over a wide frequency range, and should also be considered to ensure PSRR requirements. This allows that the $PMOS$ power transistor can operate in three regions (i.e. triode region, saturation region and weak inversion).

The impedance between the two stages must be low to ensure that parasitic poles are located at high frequency, the UGF of the error amplifier is restricted by the location of the parasitic poles of the system. Moreover the GBW can be increased, which is a requirement of PSRR specifications.

The structure of the proposed scheme of the error amplifier is presented in Figure (4.2). This is

the basic LDO topology with the proposed error amplifier, the pass element discussed previously and the feedback network.

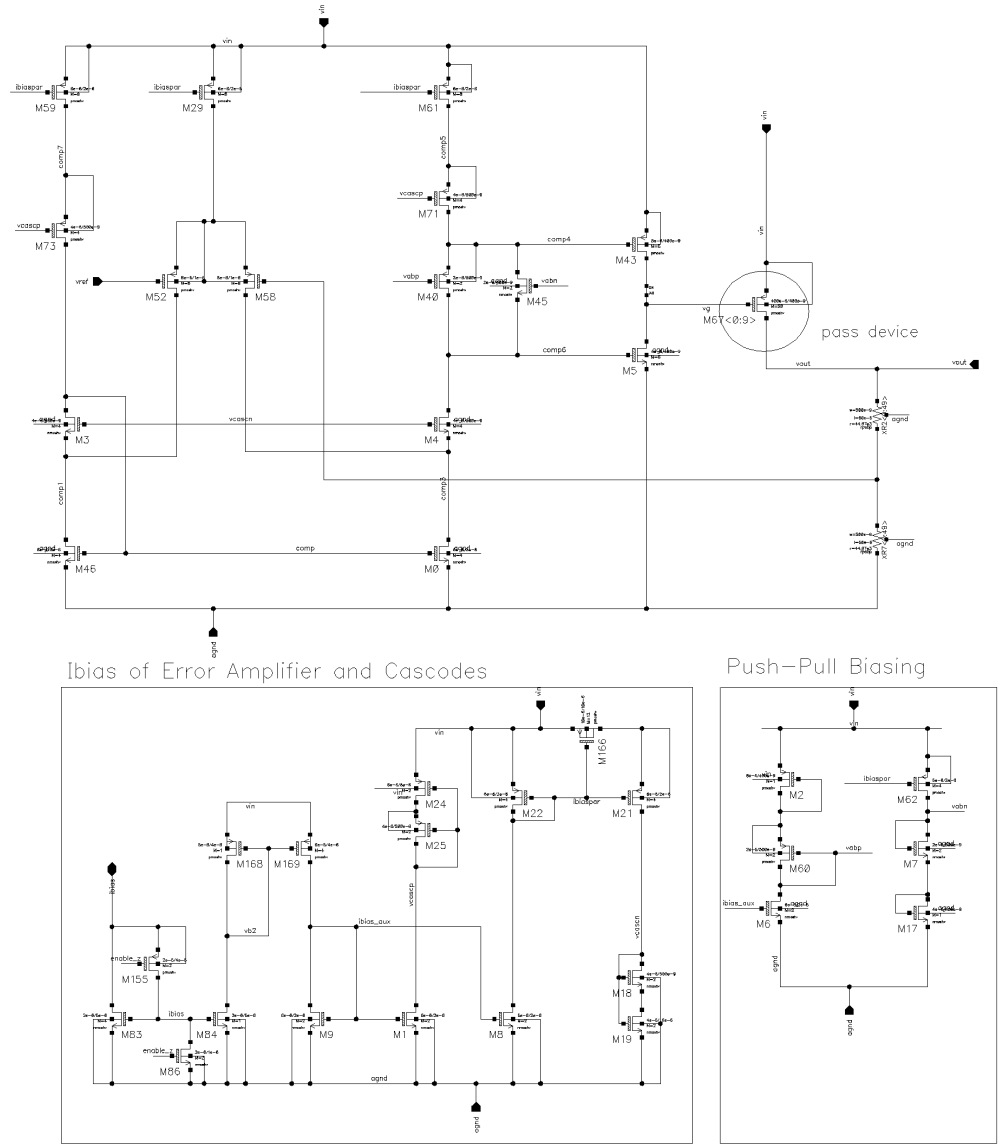


Figure 4.2: Error amplifier design.

The proposed scheme has a bias current I_{bias} input of $0.5\mu A$ to ensure low power consumption. The aspect ratio relationship between the transistors in Figure (4.2) is shown in Table 4.3.

The resulting structure can be viewed as a three-stage amplifier driving a large capacitive load, where the capacitive load is the output capacitor C_o, which has a large $1\mu F$ capacitance. Typically a high loop gain is required for all loads, however in this case power transistor cannot function as a high-gain stage in dropout condition, since its gain is inversely proportional to output current.

The transistors $M83$ $M84$ $M168$ $M169$ $M9$ $M1$ $M8$ $M6$ and $M22$ $M21$ $M62$ $M59$ $M29$ $M61$

Table 4.3: Relationship between the aspect ratio of transistors of the error amplifier and cascodes.

$Transistors$	$Ratio$
$M1 : M9 : M8 : M6, M21 : M22 : M62, M3 : M4 : M73 : M71$	1:1
$M40 : M45 : M7 : M60, M59 : M29 : M61, M52 : M58$	1:1
$M21 : M59, M18 : M3, M25 : M71$	1:2
$M84 : M83$ and $M168 : M169$	1:4
$M2 : M43$ and $M17 : M5$	1:6

forms the current mirror, which supplies the bias current to the error amplifier's first stage and cascodes. The transistors $M52$ and $M58$ form a single-stage differential amplifier. The $M3$, $M4$ and $M73$, $M71$ form the cascodes, which are biased by the $M18$ and $M25$ transistors respectively. The transistors $M24$ and $M35$ are in the triode region to provide a variable resistance, which will provide the voltage necessary to guarantee the biasing of cascodes. The push-pull amplifier stage is formed by the pairs $M45$ $M40$ and $M5$ $M43$. It is biased by the transistors $M7M60$ and $M17M2$ respectively. The design of current mirrors is critical for PSRR performance. In an attempt to reduce the contribution of parasitic capacitances at the pass device gate the transistors $M45$ $M40$ have the same aspect ratio. This will ensure that the disturbance at the pass transistor gate generated by power line and ground line noise is equal, which improves the PSRR performance of the system.

Moreover as can be seen in Figure (4.2) the class AB amplifier is symmetrical, which tends to distribute the line noise equally between the error amplifier and the output stage transistors.

The offset voltage due to the error amplifier should be minimized since the temperature and supply dependent offset voltage introduce additional errors to the LDO output voltage.

4.4 Current Limiter

In order to ensure that the current through the power transistor stays within a specified range, a current limiter was designed. This can prevent the destruction of the $PMOS$ pass device. When the load that is connected to the output of the LDO is suddenly disconnected a peak of current is generated which could result in damage or destruction of the device. The maximum power dissipation of the $PMOS$ power transistor occurs when the output is short-circuited to the ground.

The proposed configuration to the current limiter is presented in Figure (4.3). The $M170$ transistor acts as a sensor of the output current, mirroring the $PMOS$ pass transistor current. The $M88$ transistor is a current mirror that ensures a stable bias current for $M170$ transistor. When the output current changes suddenly the voltage at the gate of $M87$ transistor increases, and the voltage at the gate of the $M175$ transistor decreases. The drain of this transistor is connected to gate of the pass device.

Thus the gate of $PMOS$ pass transistor is pulled up to input voltage, preventing it from conducting a curren greater than the allowable limit. The drawback of this additional circuit is the

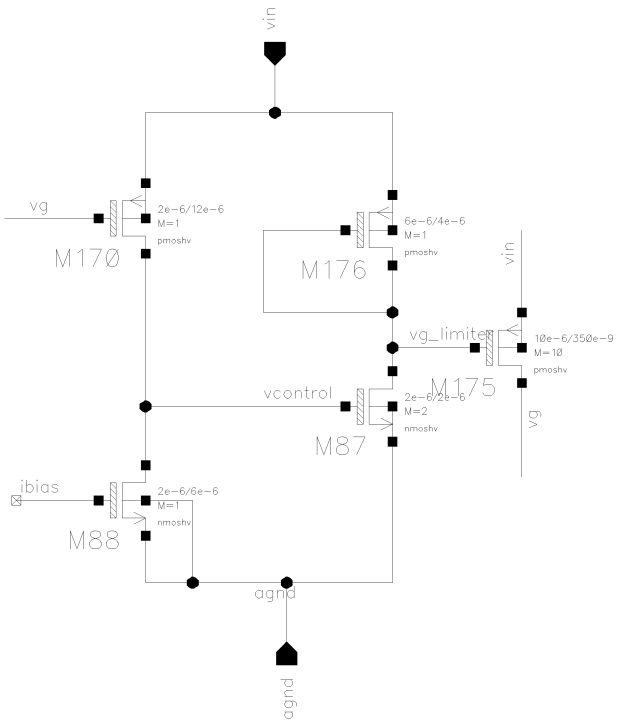


Figure 4.3: Proposed configuration of current limiter.

additional quiescent current flow and area consumption associated.

4.5 LDO design

The initial proposed topology for the LDO is presented in Figure (4.5). The LDO circuit is composed by the pass element and error amplifier that were discussed previously. A resistive feedback network is used instead of the configuration shown in Figure (2.4) in attempt to improve the start-up time, which can be affected by the slew rate imposed by the large aspect ratio of $PMOS$ configuration. The value of resistances used is $R_1 = 2.5M\Omega$ and $R_2 = 2.5M\Omega$. Their large value allows a low quiescent current and improves the PSRR at DC and low frequencies. The output capacitor and ESR are not presented in Figure (4.5), although they are considered for analysis and are located at the output of the circuit, as shown in Figure (4.4). The value of the output capacitor ESR is very low $R_{ESR} = 2m\Omega$. Since it has a low value, it helps to improve the PSRR at high frequencies and decreases the overshoots and undershoot. However a low ESR output capacitor decreases the stability of the system.

The load current transient was introduced with an active load current mirror as shown in Figure (4.4). The use of bonding wires in supply voltage rail is considered. It use improves the PSRR at high frequencies. Its equivalent model is presented in Annexe (B.1).

The voltage reference V_{ref} should be provided by a bandgap reference to improve the PSRR of the system. It is obtained from the output voltage and value is given by Equation (4.8). Thus

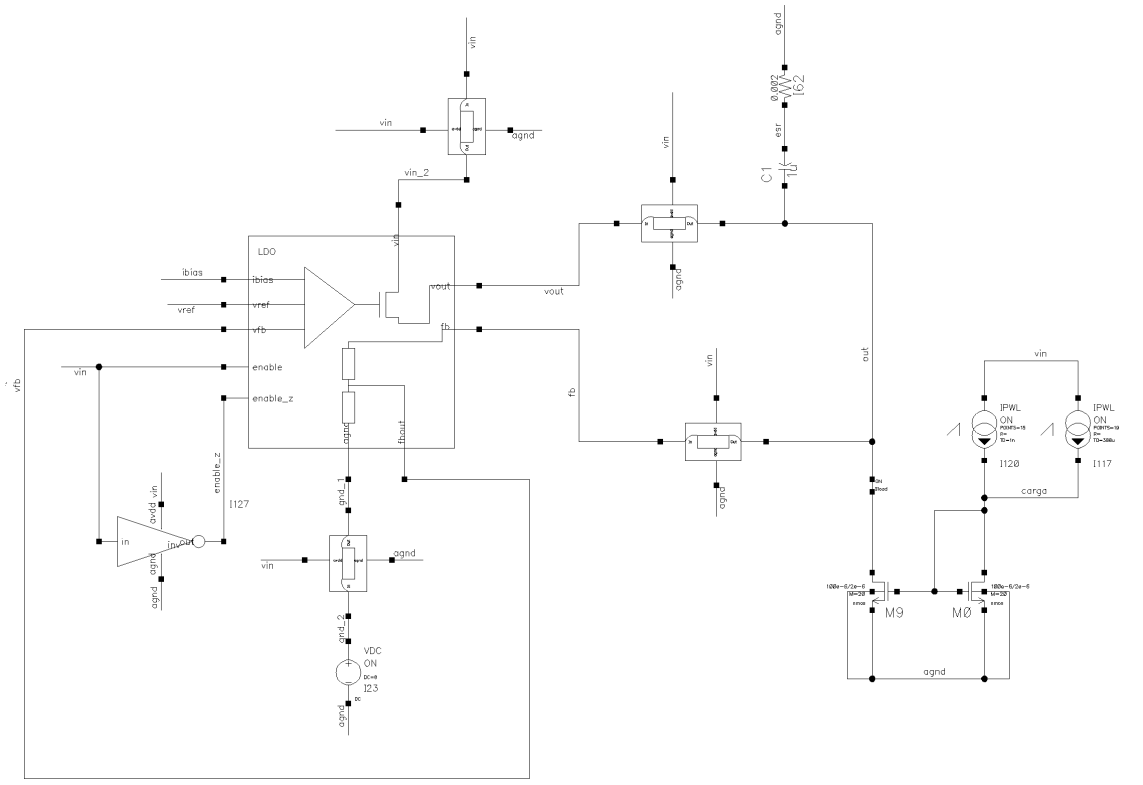


Figure 4.4: Close-loop LDO with load transient test circuit.

the voltage reference for the LDO proposal for $V_{out} = 2.4V$ is $1.2V$.

$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_1}{R_2}\right) \tag{4.8}$$

The stability of the system is ensured by the use of several techniques discussed in Chapter 3. Such is required since the use of only one technique have not allow to achieve the proposed specifications. The use of a low value for the ESR and a large capacitance for the output capacitor and the use of a very large $PMOS$ pass device transistor, increases the capacitance at output of the error amplifier discouraging the use of the CFC.

As mentioned previously the circuit architecture is based on a three-stage amplifier design driving a large capacitive load. In multistage amplifiers with a large capacitive load, the pole at the output is located at low frequency and is very close to the dominant pole. Thus the LDO has to be stabilized by removing the effect of the pole at the output. This can be done via pole-splitting using compensation capacitors or pole-zero cancellation using feedforward paths. The stability of the proposed LDO is not affected when the supply voltage increases from dropout voltage.

In order to achieve stability of the system the NMC technique with a null resistance is used to split the poles, allowing the pole-zero cancellation. This is done by the use of MOScap capacitors $M117$, $M114$ and $M152$ shown in Figure (4.5). Since the linearity of the capacitance is not a concern the MOScap can be used, otherwise a single capacitor solution must be considered. The

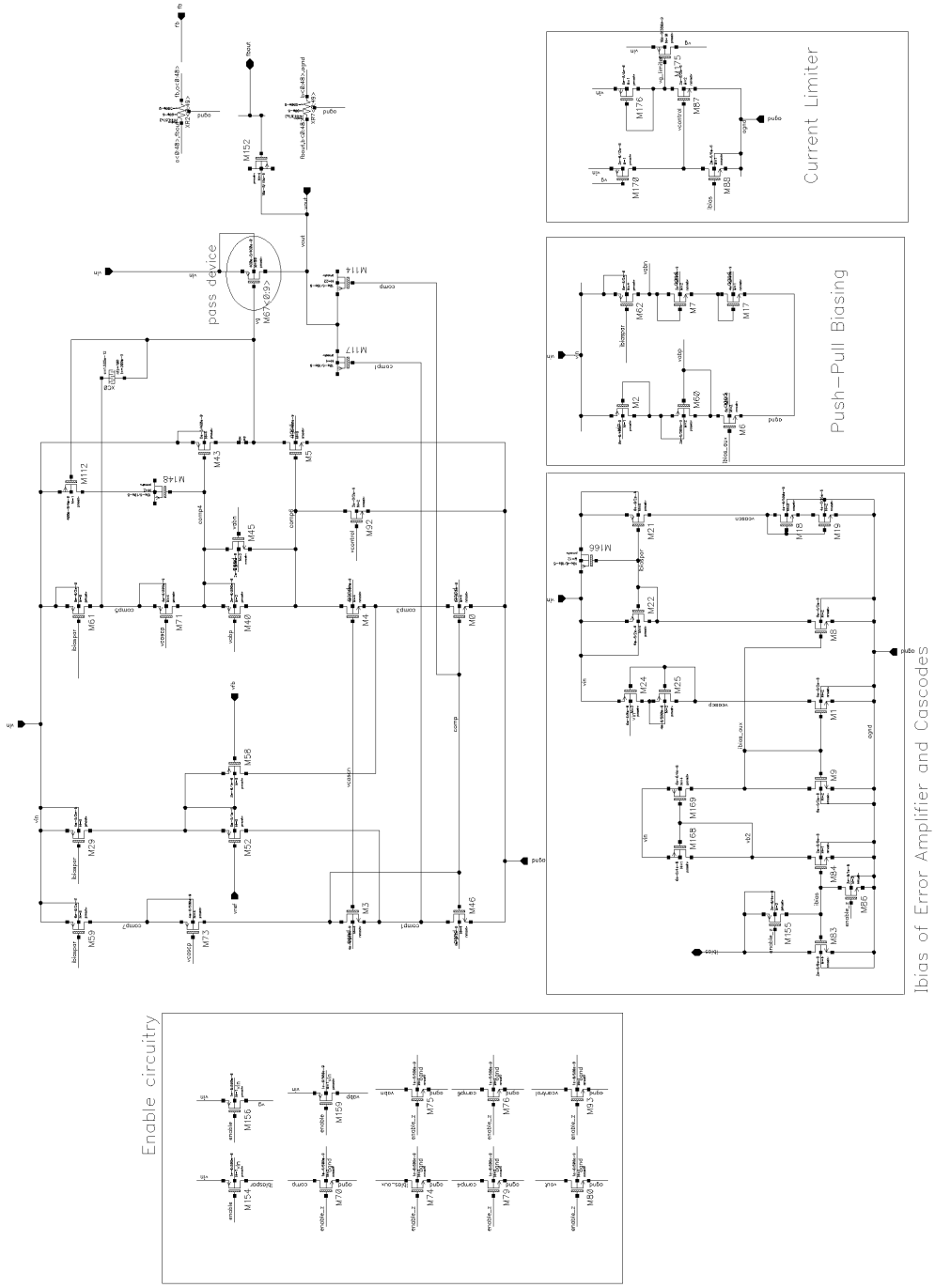


Figure 4.5: Initial topology of the proposed LDO.

generated feedforward path adds the AC signal current through a bypass path to the first-stage of the error amplifier, which increases the output conductance of the stage and pushes the pole at the output of the first stage to higher frequencies. However low-frequency pole-zero doublets can appear if the feed-forward path it not canceled properly. Which can affect the stability and the settling time of the amplifier, thus the design must be done carefully. The use of large capacitors is not considered since it increases the area consumption.

Another technique used to improve the stability is the DMFC, which is based in PZTFC [19]. The RC network is formed by the MOScap capacitor $M114$ and a $PMOS$ transistor in triode region $M112$, that acts like a resistance, as shown in Figure (4.5). The value of resistance associated with transistor $M112$ changes with voltage variations at the gate of the pass device and consequently the position of the generated zero will track the dominant pole.

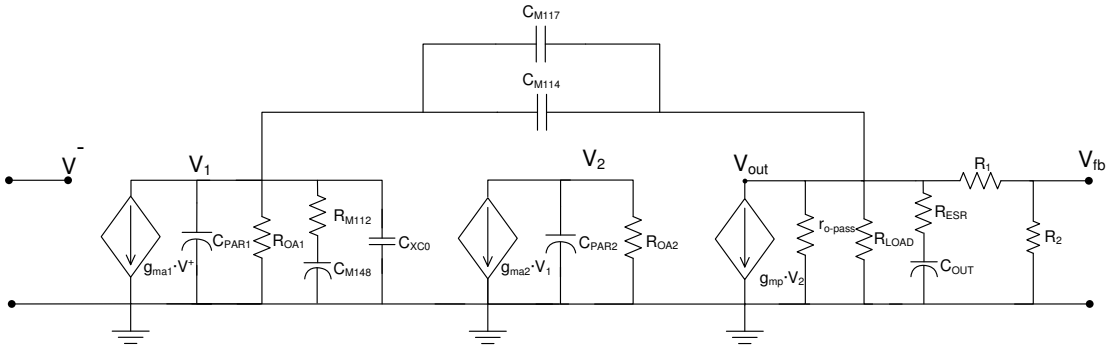


Figure 4.6: Equivalent small-signal circuit of the initial LDO proposal.

The use of single Miller pole-splitting technique is employed by the capacitor $XC0$. This reduce the GBW of the error amplifier, and therefore it must be designed carefully. The Miller capacitance between the gate and drain of the $PMOS$ pass device is not considered since its use does not affect the position of the pole and the error amplifier properties. When the load current increases significantly, the transconductance of pass device also increases significantly and the complex conjugated poles will shift to high frequencies.

The equivalent small-signal circuit of the initial LDO proposal depicted in Figure (4.5) is shown in Figure (4.6).

In order to analyze the frequency response of the initial proposed LDO the following assumptions are assumed. The C_M is the compensation capacitor that is equal to the global capacitance formed by the MOScap transistors $M117$, $M114$. The variable resistance composed by $PMOS$ transistor $M112$ working in the triode region is denoted as R_{M112} and the MOScap capacitor $M148$ as C_{M148}. The transconductance, output resistance and output parasitic capacitance of the first and second stages are denoted by $g_{ma(1-2)}$, $R_{oa(l-2)}$ and $C_{PAR(l-2)}$, respectively. The $PMOS$ pass transistor in the Figure (4.5) $M67$ operates in the linear region and is denoted by the transconductance g_{mp} and it source to drain resistance as r_{o-pass}. The value of the compensation

capacitors C_M and C_{OUT} is larger than $C_{PAR(l-2)}$ and C_{XC0}. Moreover $R_{ESR} \ll r_{o-pass}$, R_1, R_2, R_{Load} and R_{M112}. The parallel between r_{o-pass} and R_{Load} can be simplified to r_{o-pass} since the R_{Load} is greater in magnitude. The open-loop transfer function is expressed by the Equation (4.9).

$$\frac{V_{fb}}{V^-} = \frac{K \cdot (1 + \frac{s}{z_1})(1 + \frac{s}{z_2})}{(1 + sC_M R_{oa1} R_{oa2} R_{oa1} r_{o-pass} g_{ma2} g_{mp} + s^2 C_{M148} C_M R_{oa1} R_{M112})(1 + \frac{s}{p_3})(1 + \frac{s}{p_4})} \quad (4.9)$$

Where K is the DC open loop gain of the system and is given by the Equation (4.10). The poles p_1 and p_2 can be calculated solving the polynomial Equation (4.11).

$$|K| = \frac{g_{ma1} g_{ma2} g_{mp} R_{oa1} R_{oa2} R_{o-pass} R_2}{R_1 + R_2} \quad (4.10)$$

$$1 + sC_M R_{oa1} R_{oa2} r_{o-pass} g_{ma2} g_{mp} + s^2 C_{M148} C_M R_{oa1} R_{M112} = 0 \quad (4.11)$$

Therefore the poles and zeros of transfer function are given by the follow equations:

$$P_1 = \frac{1}{C_M R_{oa1} R_{oa2} r_{o-pass} g_{ma2} g_{mp}} \quad (4.12)$$

$$P_2 = \frac{R_{oa2} r_{o-pass} g_{ma2} g_{mp}}{C_{M148} R_{M112}} \quad (4.13)$$

$$P_3 = \frac{1}{R_{oa2} C_{PAR2}} \quad (4.14)$$

$$P_4 = \frac{1}{R_{o-pass} C_{OUT}} \quad (4.15)$$

$$Z_1 = \frac{1}{R_{ESR} C_{OUT}} \quad (4.16)$$

$$Z_2 = \frac{1}{R_{M112} C_{OUT}} \quad (4.17)$$

where the P_1 is the dominant pole and P_2 becomes a high frequency pole. The pole P_3 is located beyond the UGF, thus its contribution for a potential unstable system can be neglected.

As discussed previously the DC open loop gain of the system is inversely proportional to the output current. Thus when I_{Load} increases the open loop gain decreases and stability is improved (i.e. the phase margin increases), otherwise the gain increases and therefore the stability of the system decrease.

Both load and line transient responses improvement are achieved due to the fast and stable loop gain provided by compensation scheme. The amount of frequency shifting of the poles under the change of temperature is the same for all. Therefore, any increase in temperature only changes the UGF but not the stability of the LDO. The high and wide open-loop gain, and GBW of the error amplifier ensure that the PSRR specifications of $-70\ dB\ @\ 1\ kHz$ are achieved. At high frequencies the low value of ESR improves the PSRR. However the low quiescent current limits the UGF of the system as shown in Figure (4.7), which does not allow to achieve the specifications

of $-30\ dB$ to high frequencies. The variations of output current can be seen and also its effects on gain and stability of the system.

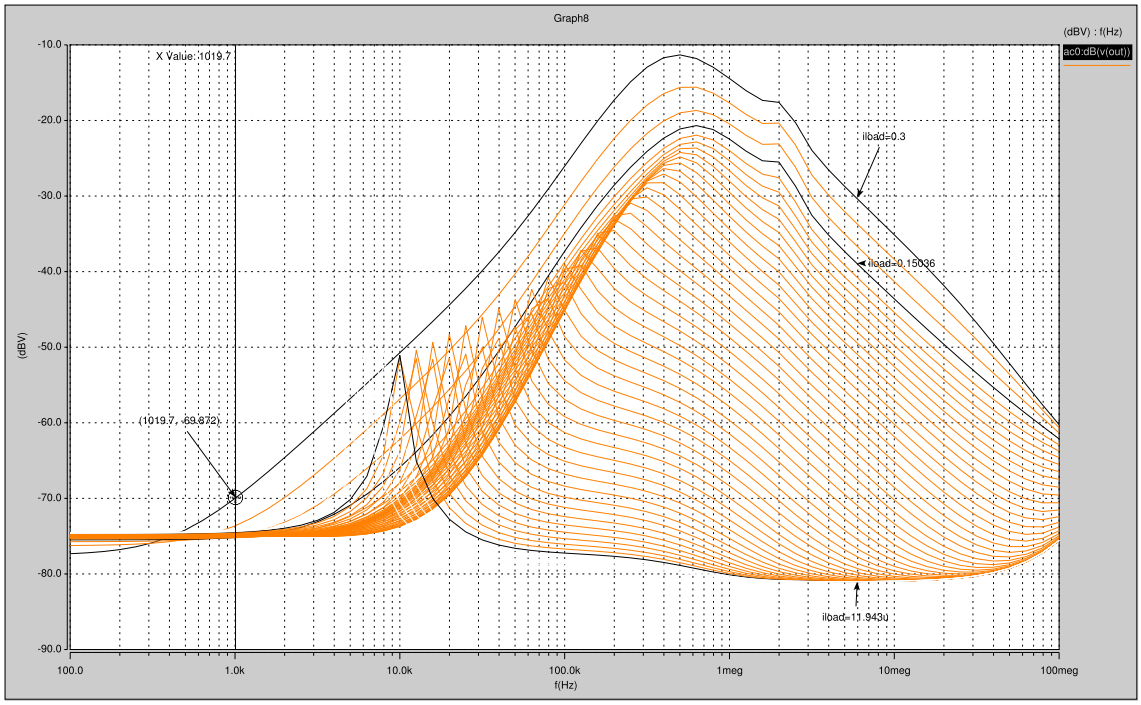


Figure 4.7: PSRR of the initial LDO proposal for all load currents.

In next section a proposed strategy will be discussed to improve the PSRR at high frequencies.

4.5.1 Power Down Mode

The power down mode allows to extend the battery life, when the system is operating in standby mode. This state is achieved by introducing a short-circuit between the gate and source of current mirror transistors by the $M155$ $M154$ $PMOS$ transistors and $M86$ $M159$ $M74$ $M75$ $NMOS$ transistors, as shown in Figure (4.5). This ensures that the current mirrors are inactive when the circuit is in power down mode ($enable = 0$). Moreover the $PMOS$ pass transistor and the transistors of the gain stages of the error amplifier must be in the cut-off region. This is ensured by the $M156$ $PMOS$ transistor and $M70$ $M79$ $M76$ $M80$ $M93$ $NMOS$ transistors as shown in Figure (4.5). Thus an inverter as shown in Figure (4.4) must be considered to ensure that all transistors are in the cutt-off region. Is topology is presented in Annexe (B.2). The achieved power consumption in power down mode has a quiescent current consumption less than $100nA$. The design of the enable signal must be done carefully since the time of system power-up and power-down is greatly affected by the performance of this circuit.

4.6 The PSRR Improvement Strategy

As mentioned previously the limitations imposed by low quiescent current limit the UGF of the error amplifier, and consequently the PSRR performance of LDO at high frequencies. Thus an increase in the low quiescent current allows a larger UGF, which improves the PSRR. Furthermore the open-loop gain will be increased, since the position of the poles as well as the UGF are directly proportional to the transconductance of the gain stages. Moreover as discussed in Chapter 2 the power efficiency of the system is not affected, since the quiescent current consumption increases proportionally to the output current.

The proposed strategy consists of changing the biasing conditions for the variations of the load current, increasing the bias current of the circuit, proportionally to the output current, through a dynamic biasing which senses the output current as shown in Figure (4.8).

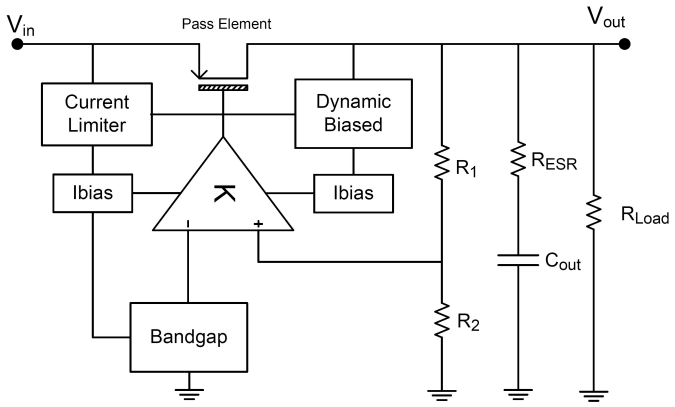


Figure 4.8: System diagram of the proposed strategy.

The LDO needs a large biasing current for the large UGF of the error amplifier, especially when the load current is high, since this represents the worst case of PSRR. It would be advantageous if the bias current of the LDO was adaptive to the load current variations, specially for low load current conditions, since for this conditions the power efficiency is greatly affected by the quiescent current consumption. The bias current would be low, and at high load the bias current would be high enough to ensure a large UGF, and a high speed of the error amplifier, also improving the settling time of the system. Thus a current sensing of the output current is used to change dynamically the bias current of the circuit as shown in the Figure (4.10).

However low-frequency pole-zero doublets can appear due to the generated feed forward path, thus a delay in the feed forward must be considered to improve the stability. This can be designed with a RC network, as can be seen in Figure (4.10), where the $M146$ transistor acts like a variable resistance, since it is in the triode region and $M167$ is the MOScap capacitor. The output current sensing is designed through a mirror of $PMOS$ pass transistor by the $M164$ transistor, which scales the output current. The $M158$ $M157$ $M163$ $M81$ $M77$ $M82$ $M78$ transistors form

the current mirror of scaled I_{Load}. Although its complexity increases the I_q of the circuit, other techniques can be used to sense the output current as shown in [18], decreasing however the PSRR performance, since a feed forward path is created between the output voltage and the voltage of the bias circuit, yielding that fluctuations in the output voltage are introduced in all elements that compose the LDO.

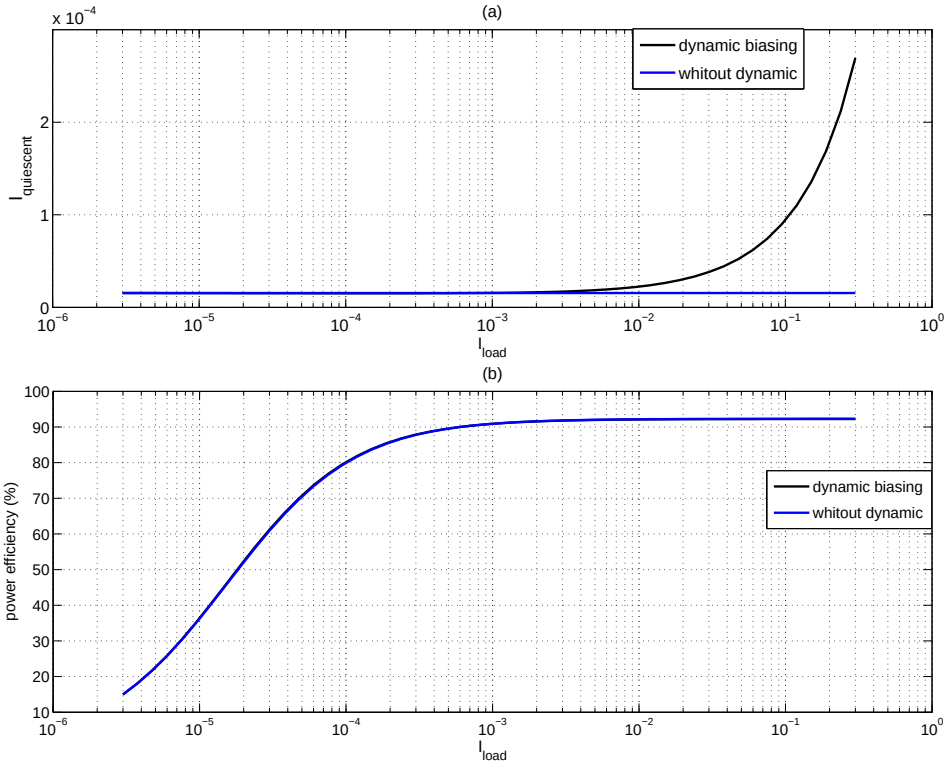


Figure 4.9: The I_q consumption and the power efficiency of the initially proposed and proposed LDO topology.

The scaled output current is inserted in the bias circuit of the error amplifier by the current mirror composed by $M160$ $M165$ transistors, increasing is quiescent current, and changing the position of the poles and UGF, as mentioned before. The small signal model shown in Figure (4.6) is maintained, since the position of all poles and zeros only changes proportionally to I_q. Therefore a careful design is required, since the transistors that compose the system will have to work in the saturation or weak inversion regions resulting from changes in their bias current. Thus the stability of the system is not affected leading to an increase of the UGF and GBW of the error amplifier and a low value of ESR allowing the achievement of a high PSRR at high frequencies.

As mentioned previously in Chapter 2 the contribution of the quiescent current to the power efficiency of the LDO can be neglected for high load currents, thus the dynamic biasing is suitable to the system requirements, since it allows a high PSRR at high frequencies without affecting the power efficiency. The relationship between the I_q consumption and the power efficiency of the

initial proposal and proposed LDO topology is presented in Figure (4.9).

As can be seen from Figure (4.9), the power efficiency of the system is improved with the increase of the load current, which can be verified by the Equation (4.18). The power efficiency for low load current is equal for the two topologies due to the use of dynamic biasing, which ensures that the quiescent current consumption is the minimum for low load current condition, thus the battery life can be extended.

$$Efficiency_{power} = \frac{V_{out}I_o}{(I_o + I_q)V_{in}} \leq \frac{V_{out}}{V_i n} \tag{4.18}$$

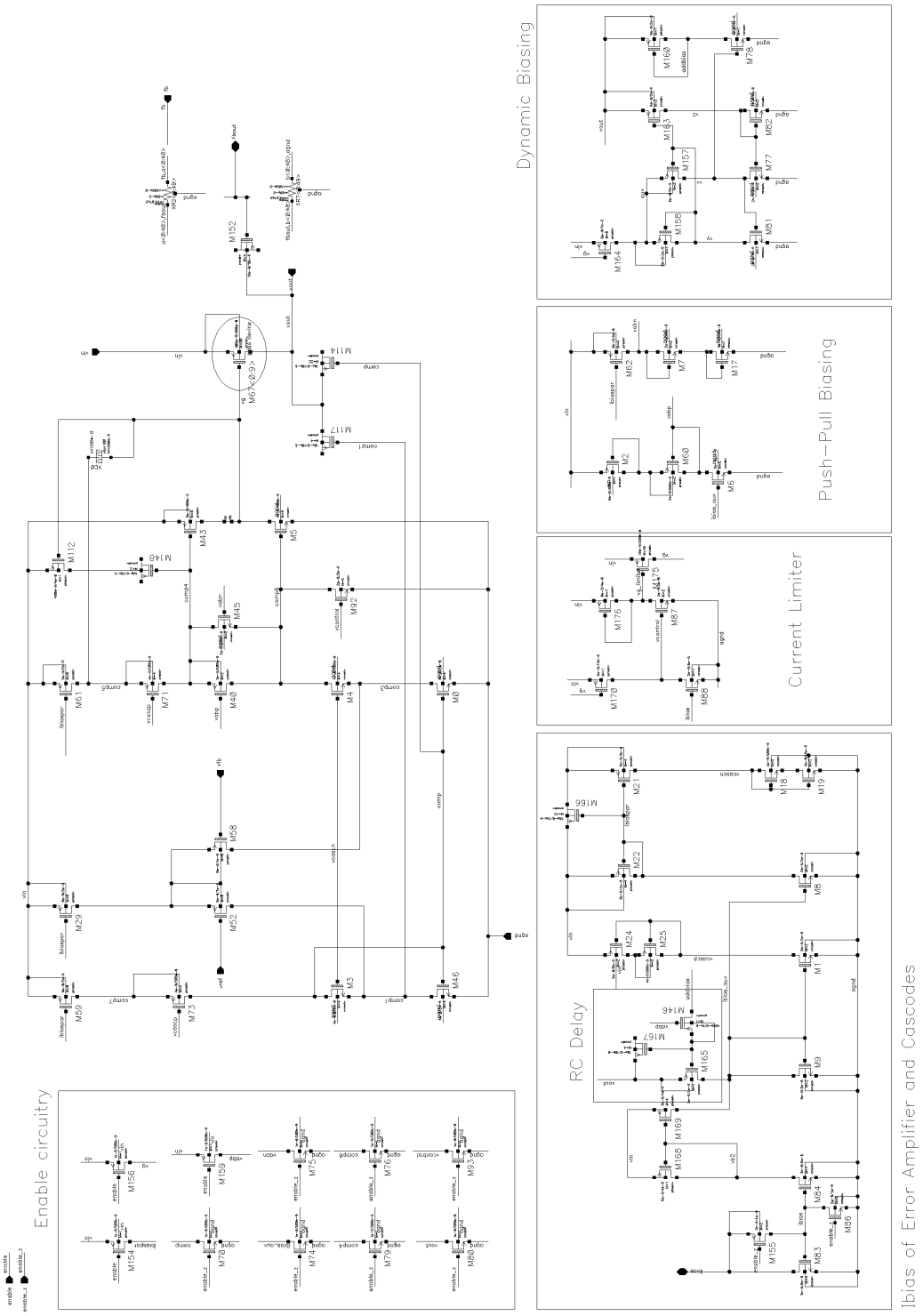


Figure 4.10: Topology of the proposed LDO.

5

Simulation Results

Contents

The simulations results that characterize the proposed LDO topology will be presented in the the follow of this Chapter. The schematics were implemented using the schematic editor from the Cadence® Custom IC Design tools and $SMIC\ 0.13\ \mu m$ CMOS technology. Its characterization has be done with variations in several parameters, such as the supply voltage, the bias current, temperature, resistance, capacitance and MOS parameters as presented in Table 5.1. The MOS parameters are dependent of fabrication process variations (e.g. V_{th}, thin oxide and transistor capacitance) and can be $Fast$ or $Slow$. The combination of the two concerns to the $PMOS$ transistors and $NMOS$ transistors respectively. Thus the combination of $FastSlow$ and $SlowFast$ is also considered for simulation results, although is not presented in Table 5.1.

Table 5.1: Corner identification.

Corner	I_{bias} (%)	Supply voltage (V)	Temperature (^oC)	Resistance (%)	MOS
Best	+20 %	3.6	-40	-10 %	FastFast
Typical	-	2.6	50 (ROOM)	-	Typ
Worst	-20%	2.6	125	+10%	SlowSlow

The variations of I_{bias} resistance and capacitance (10%) parameters are in percentage from is nominal value. All these variations are combined to produce a total of 128 corners.

5.1 AC Open-Loop Analysis

The schematic of the AC Open-Loop Analysis is presented in Annexe (A.3). For the DC analysis proposed, the feedback loop can be broken through a $CUTAC$, which allows to ”break” the AC contribution for the feedback loop. It is noted that the DC open-loop gain is a function of the load current as discussed previously in Chapter 3. The variation of the DC open-loop gain and phase-margin of the LDO system is presented in Figure (5.1). As can be seen the stability is improved with the increase of the load current, it behaves poorly for $I_{load} = 10\ \mu A$ with a phase-margin of approximately 1.85^o, however this value can ensure the stability of the system. The greater value of the phase-margin is 56^o and is achieved at $I_{load} = 25\ mA$, when $I_{load} = 300\ mA$ the value of the phase-margin is 33^o.

The gain of the system is higher at lower output currents, which results from variations of the R_{o-pass} resistance of the $PMOS$ pass device, as shown by the Equation (4.10).

The Figure (5.1) shows all variations of the load current from $I_{load} = 10\mu A$ to $I_{load} = 300\ mA$, thus the stability of the proposed LDO is fully tested under all load current. This is done by variation of the load resistance R_{load} at output of the LDO as can be seen in in Annexe (A.3). As can be seen the a phase-margin greater than zero is ensured for all load load current condition.

The AC Open-Loop Analysis for all alters conditions was realized and is presented in Figure (5.2) for $I_{load} = 300\ mA$, Figure (5.3) for $I_{load} = 150\ mA$ and Figure (5.4) for $I_{load} = 10\ \mu A$.

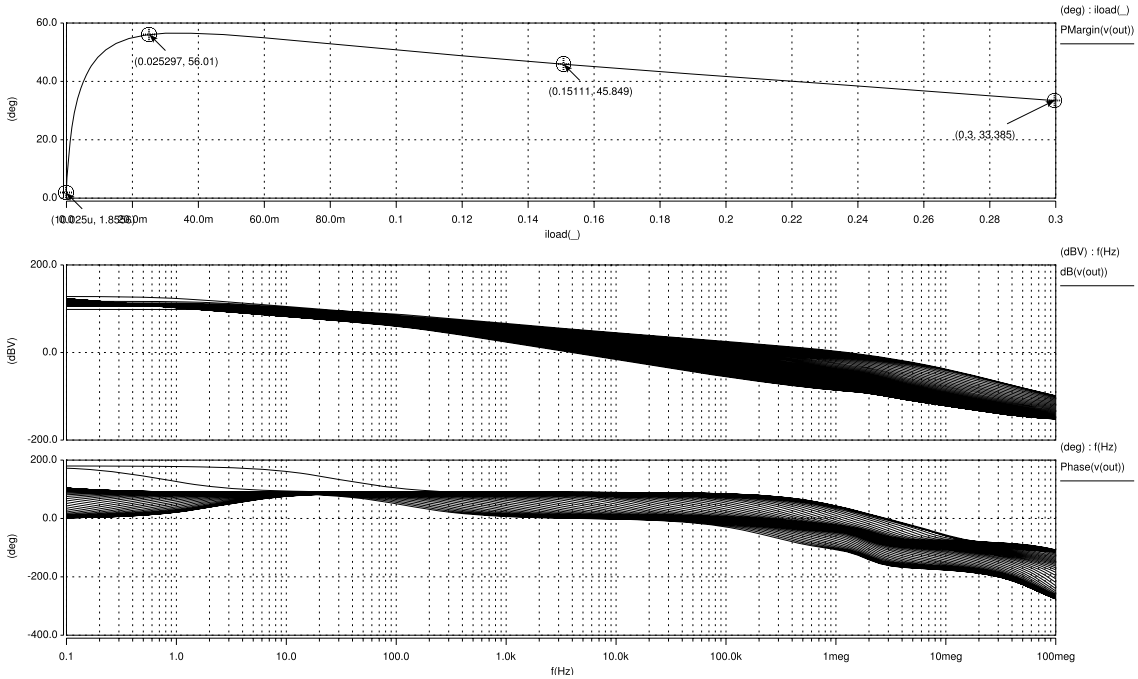


Figure 5.1: AC open-loop analysis for all load conditions of the proposed LDO topology, under typical condition.

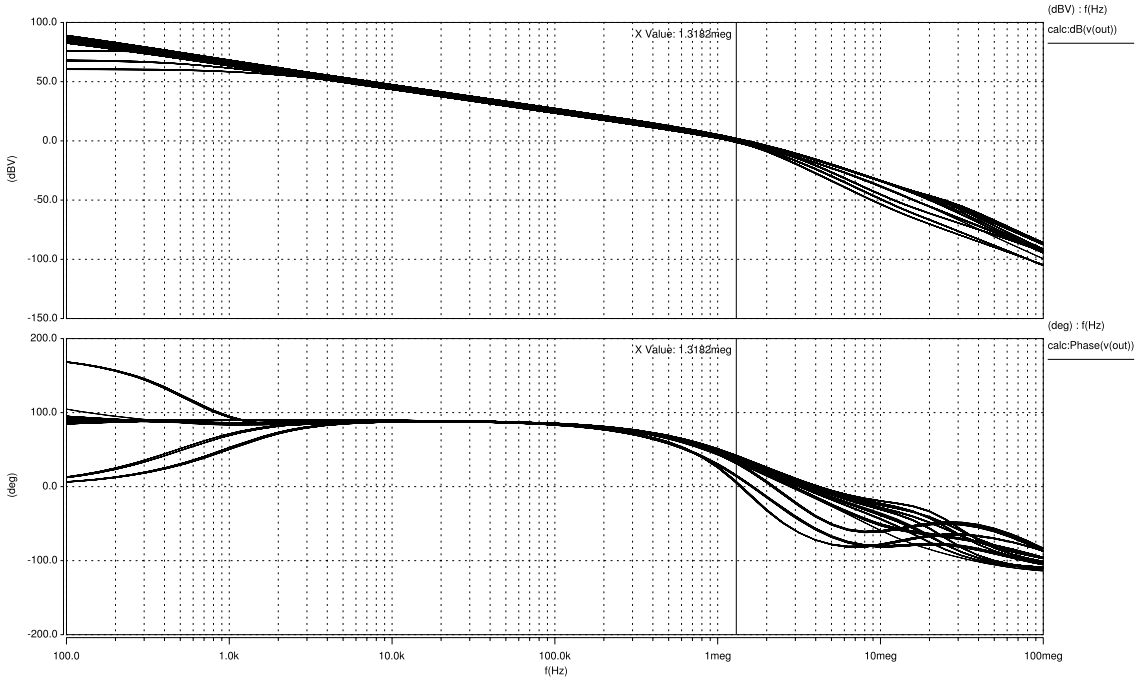


Figure 5.2: AC Open-Loop Analysis for all alters condition with $I_{load} = 300\ mA$.

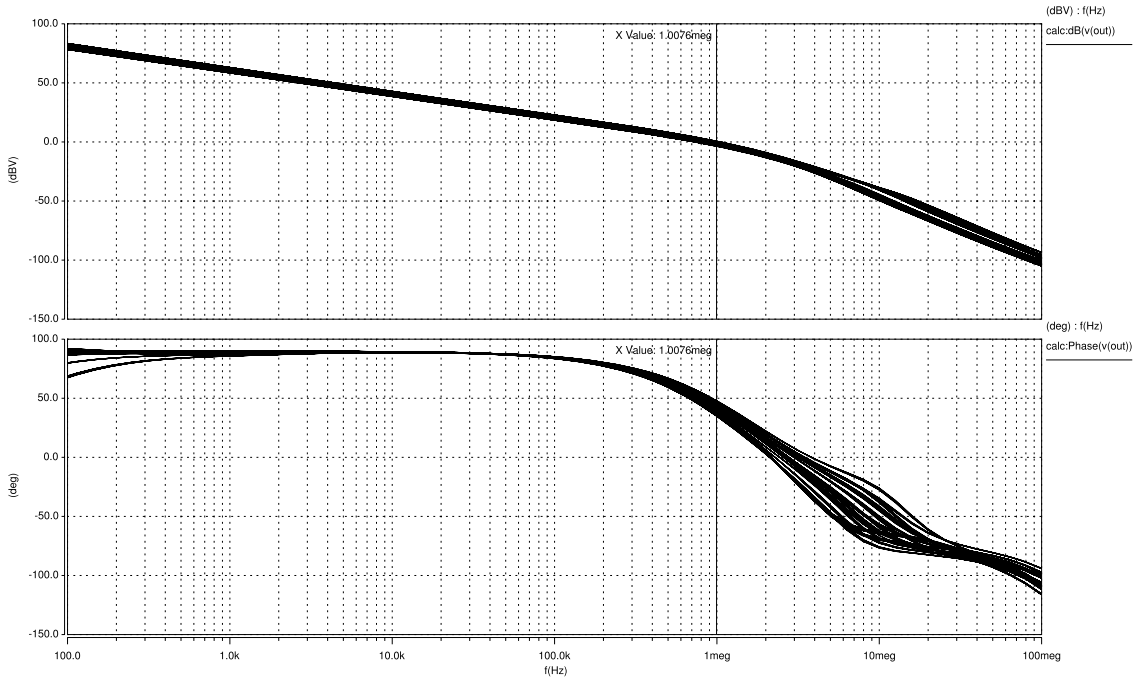


Figure 5.3: AC Open-Loop Analysis for all alters condition with $I_{load} = 150\ mA$.

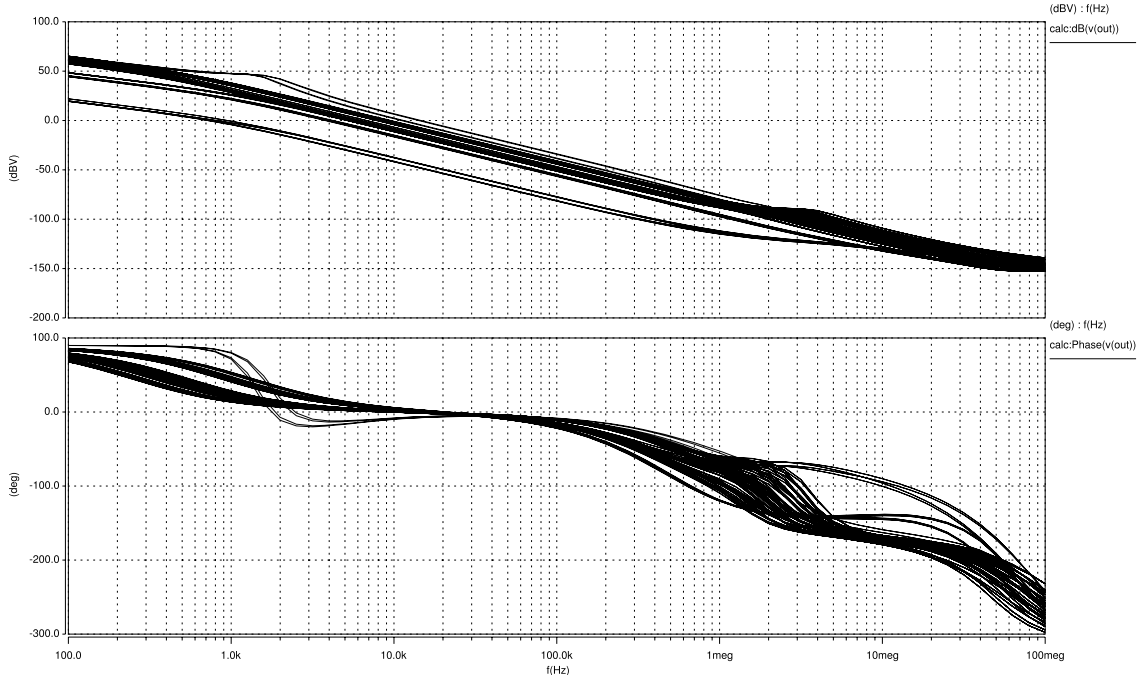


Figure 5.4: AC Open-Loop Analysis for all alters condition with $I_{load} = 10\ \mu A$.

5.2 Transient Response

The schematic of the transient response of the proposed LDO is presented in Annexe (A.2). To ensure a good load transient a current mirror is used as shown in Figure (4.4) to simulate the changes of the load current.

The analysis of the measurement results is realized by applying different current pulses at the output of the regulator and observing the output voltage, as presented in Figure (5.5), where all alters condition are considered.

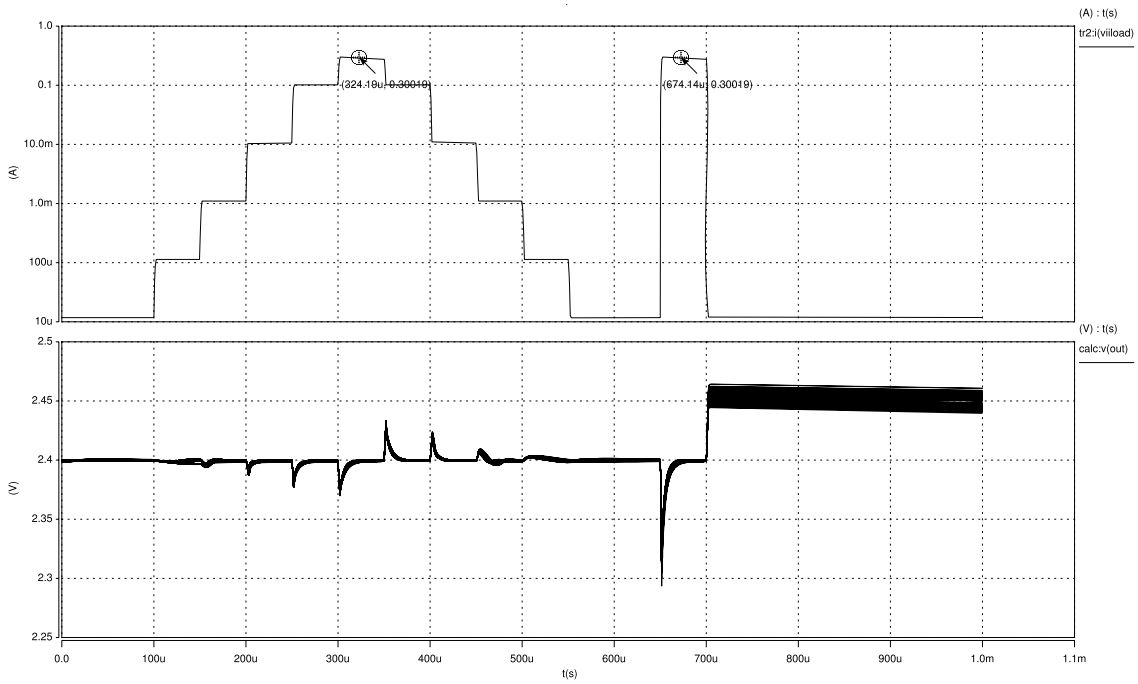


Figure 5.5: Transient response of the proposed LDO topology under all alters condition.

The feedback loop responds to drops in output voltage and the proposed LDO topology adjusts to the new loading conditions, with the output voltage coming back to the nominal voltage of $2.4\,V$.

The worst case response time corresponds to the maximum output voltage variation as shown in Figure (5.6) and is less than $25\ \mu s$. This time limitation is determined by the closed-loop bandwidth of the system and the output slew-rate current of the error amplifier, that has a high slew-rate improvement since a push-pull topology is used and yields a better settling time. This is affected by the output capacitor discharging through feedback resistors, however the large output capacitor improves the stability of the system.

An important specification is the maximum allowable output voltage change (i.e. overshoot and undershoot) for a full range transient load-current step. If the regulator is used to provide power to digital circuits which inherently have high noise margins, this specification can be relatively relaxed, however this is not the case for many analog applications. The worst case of overshoot and undershoot voltage corresponds to a load-current transition from its minimum value to its

maximum value and the inversely case as can be seen in Figure (5.5).

Settling time is not as important as maximum overshoot because the overall accuracy is not affected. Settling time could only become an issue when considering noise injection as a result of a sudden load-current change.

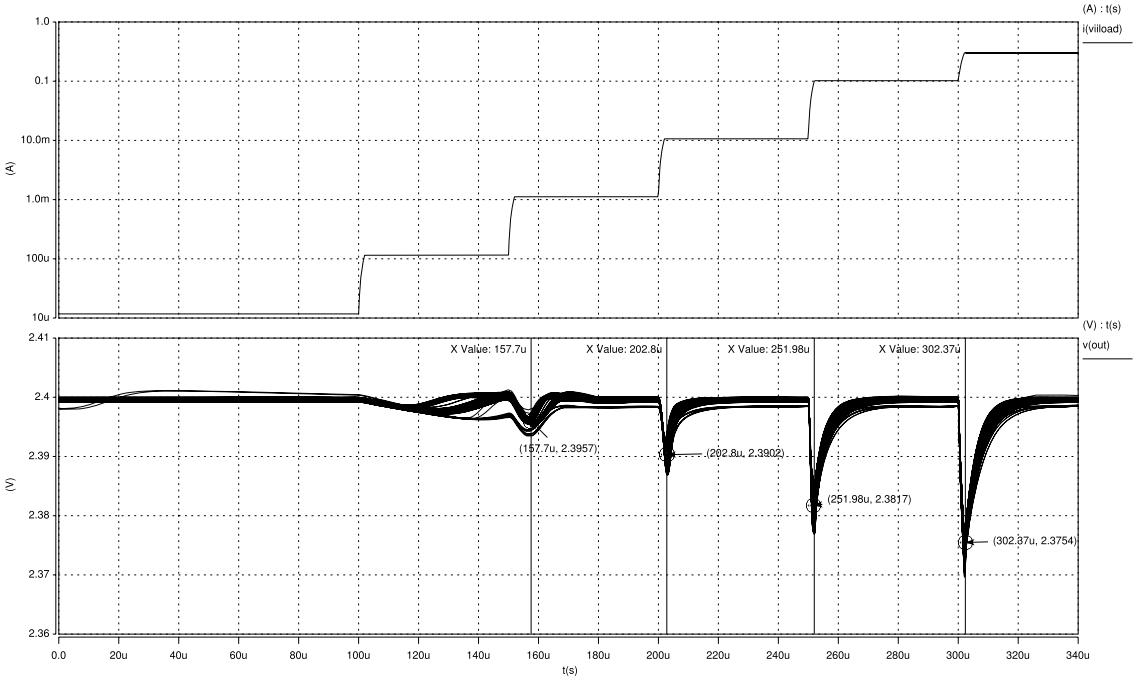


Figure 5.6: Transient response of the proposed LDO topology for variation step of the I_{load} from $10\ \mu A$ to $300\ mA$ under all alters condition.

As previously presented in Figures, the system can ensure the good regulation of the output voltage to $2.4\ V$. The worst case corresponds to the low load current. This results from poor phase margin for this load condition as mentioned previously and shown in Figure (5.1), which causes sustained oscillations resulting from the decrease of the stability of the system.

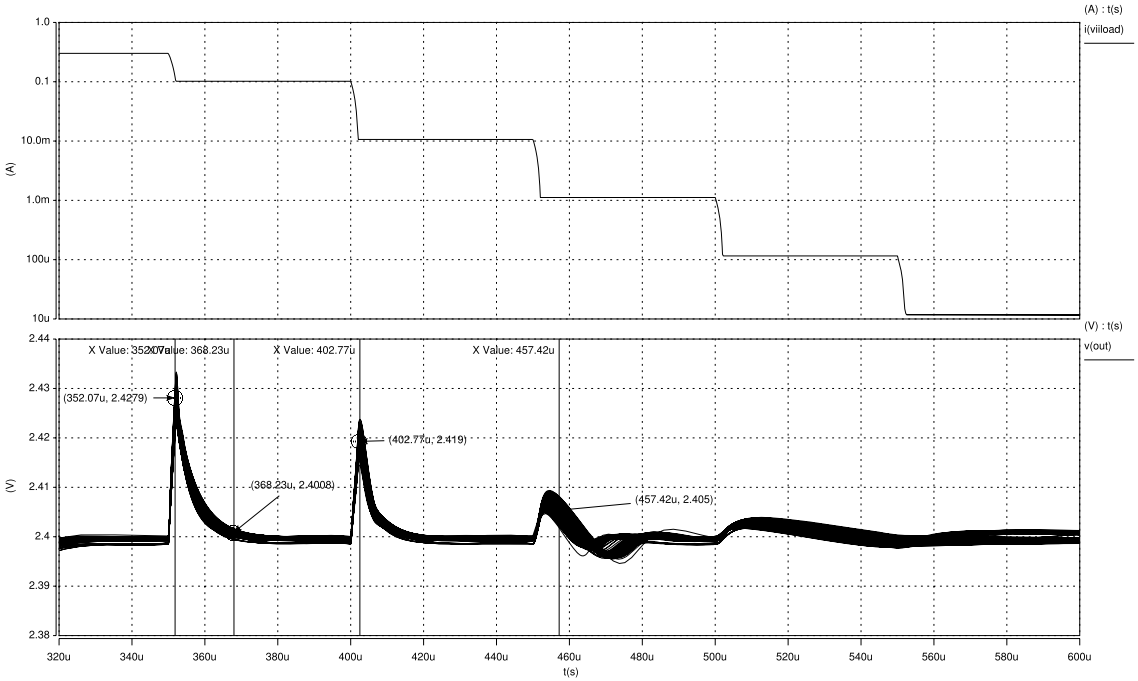


Figure 5.7: Transient response of the proposed LDO topology for variation step of the I_{load} from $300\ mA$ to $10\ \mu A$ under all alters condition.

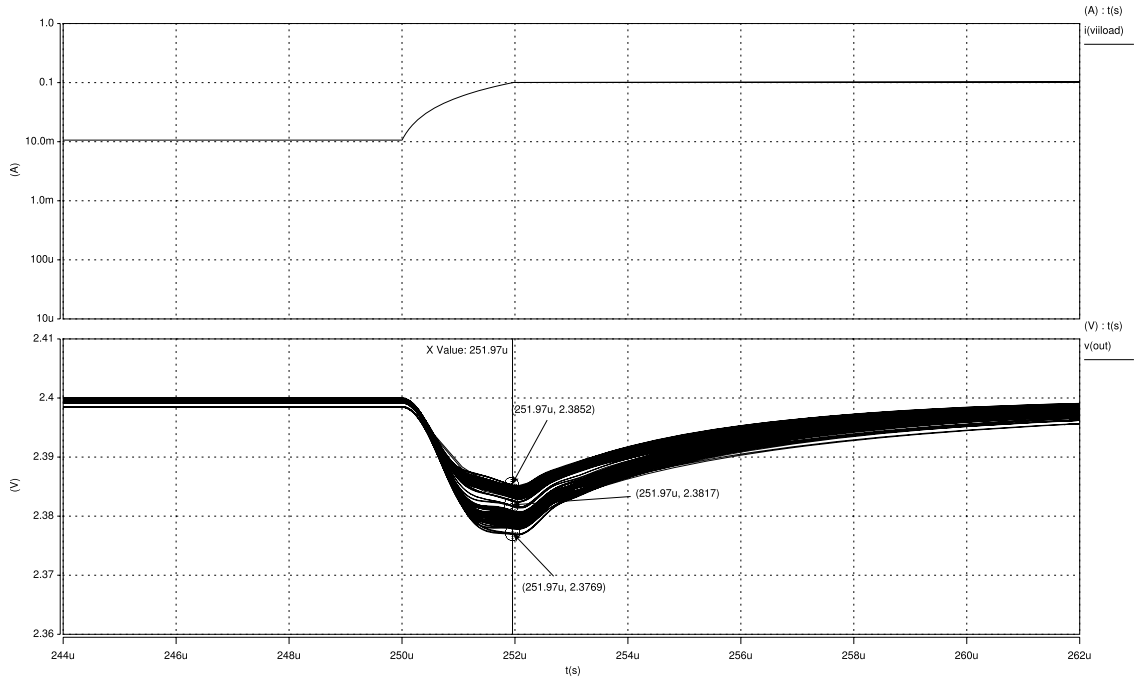


Figure 5.8: Transient response of the proposed LDO topology for variation of I_{load} from $10\ mA$ to $100\ mA$ under all alters condition.

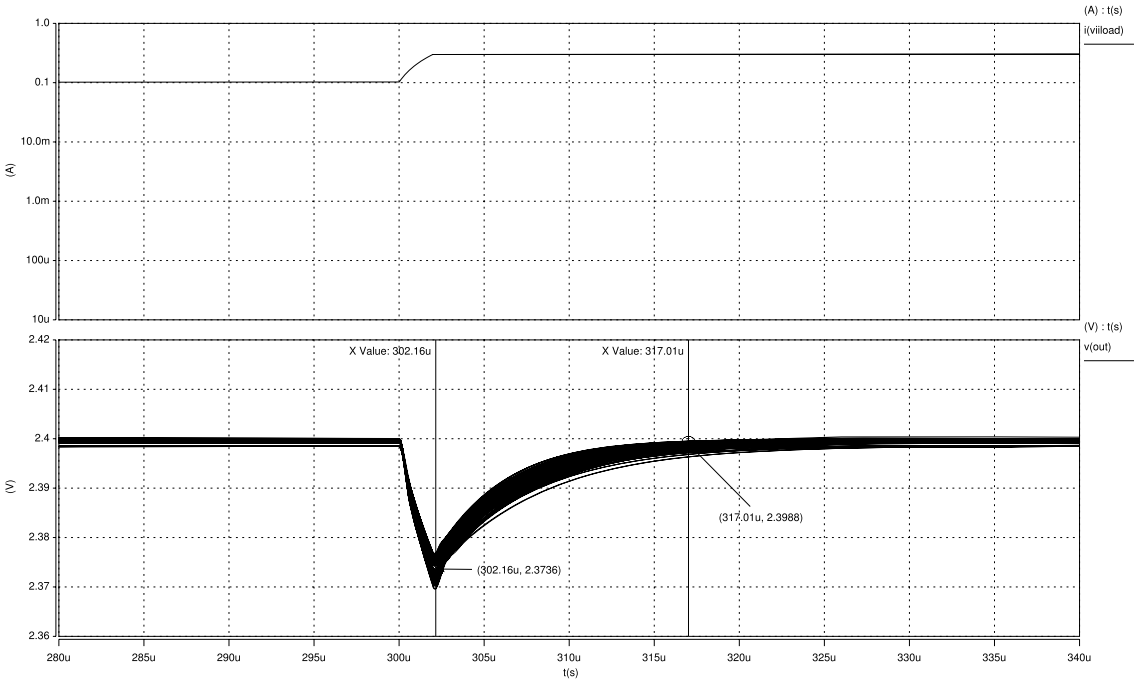


Figure 5.9: Transient response of the proposed LDO topology for variation of I_{load} from $100\ mA$ to $300\ mA$ under all alters condition.

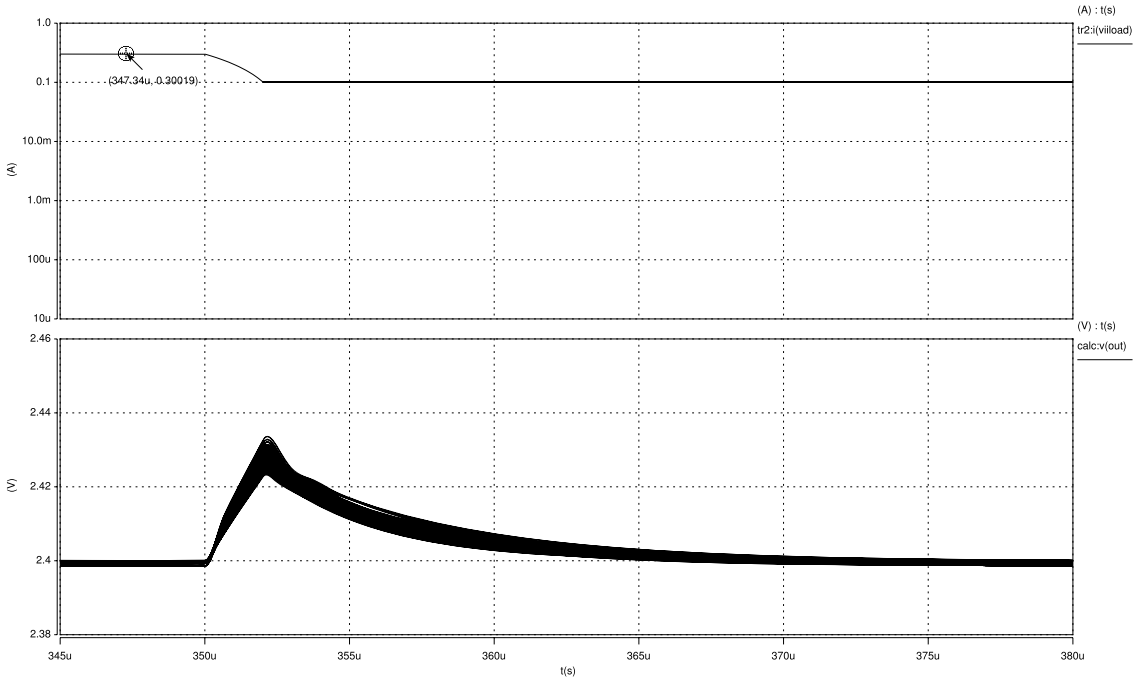


Figure 5.10: Transient response of the proposed LDO topology for variation of I_{load} from $300mA$ to $100mA$ under all alters condition.

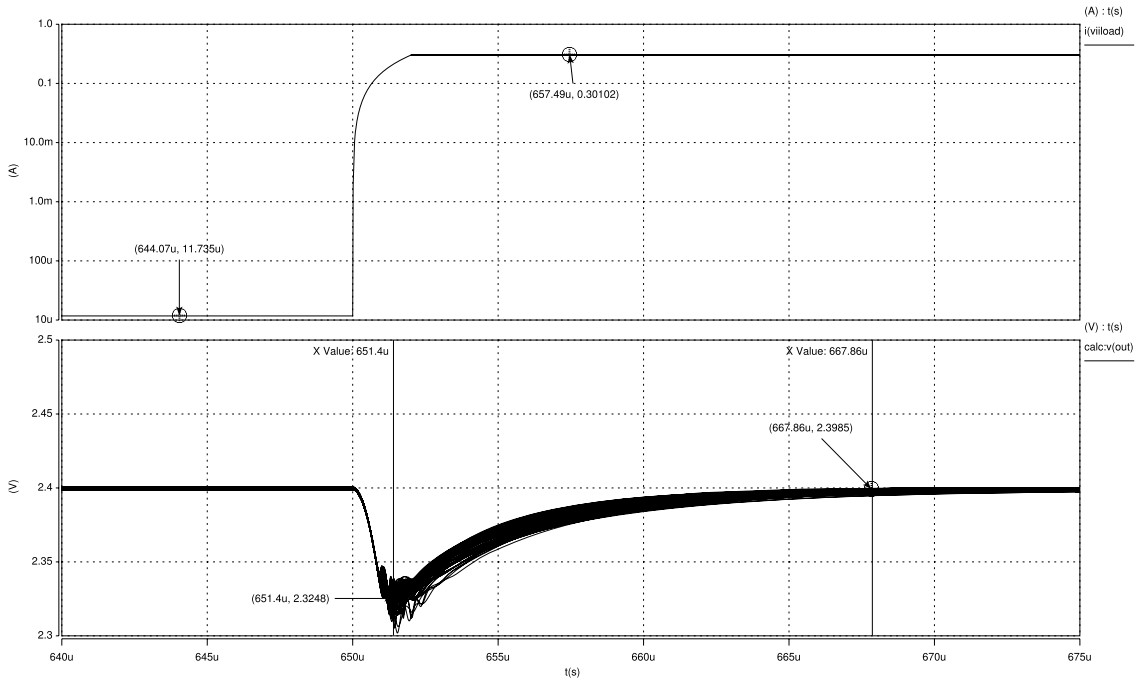


Figure 5.11: Transient response of the proposed LDO topology for variation of I_{load} from $10\mu A$ to $300mA$ under all alters condition.

5.2.1 Load Regulation

The load regulation of the proposed LDO is presented in Figure (5.12) and Figure (5.13). This is a measure of the output voltage variation from change in the load current. It is greatly affected by the open-loop gain of the LDO system as discussed previously in Chapter 2. As can be seen in Figure (5.12), the output voltage of $2.4\ V$ is ensured for a range of load current from $10\ \mu A$ to $350\ mA$. The use of a current limiter circuit limits the range of the load regulation, without this circuit the range of the load current for a good load regulation can be extended up to $400\ mA$, since the large size of the $PMOS$ pass transistor allows a large output current much greater than $400\ mA$.

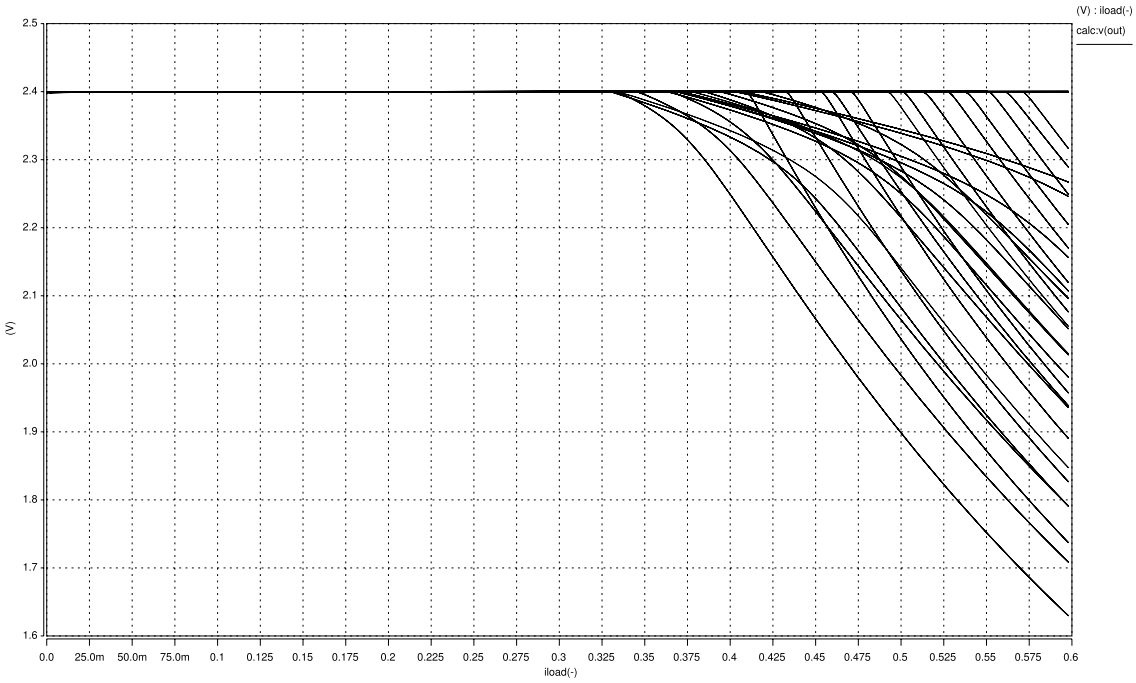


Figure 5.12: Load regulation of the proposed LDO topology over all alters condition.

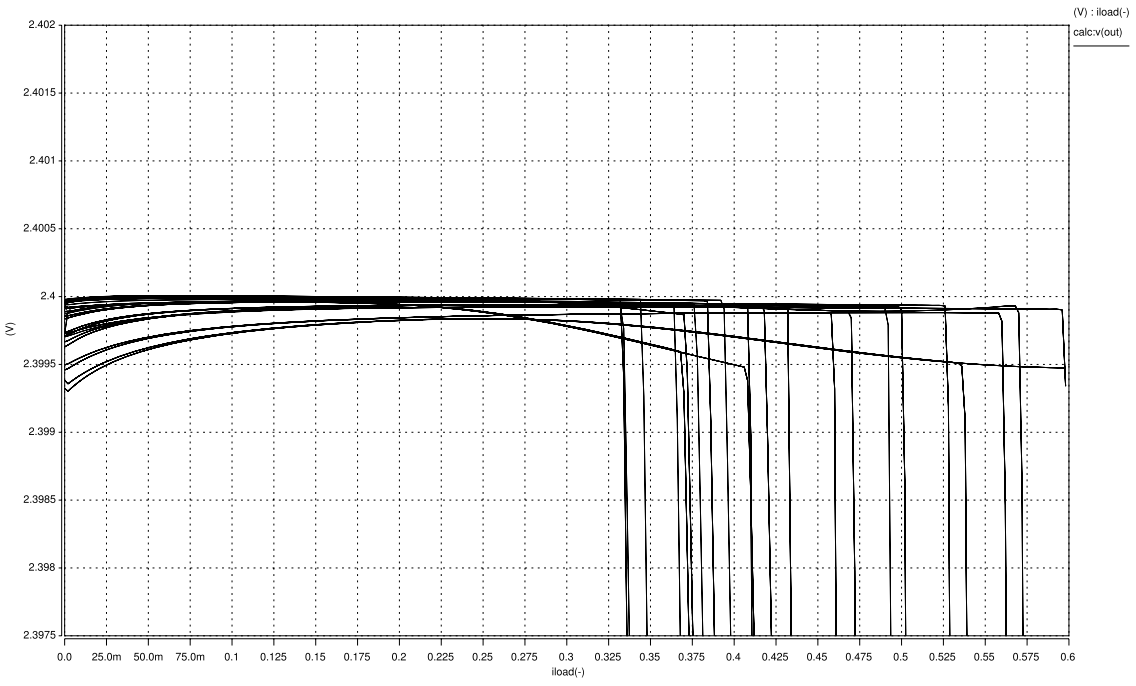


Figure 5.13: Load regulation of the proposed LDO topology over all alters condition.

5.2.2 Line Regulation

The line regulation of the proposed LDO is presented in Figure (5.14).As can be seen the analysis was realized for three load current ranges of the proposed LDO, $10\ \mu A$, $150\ mA$ and $300\ mA$. The line regulation is improved by the high DC open-loop gain of the proposed system as discussed previously in Chapter 2. The line regulation tends to be worst for small load currents as shown in in Figure (5.14), since for these conditions the zero is closer to the loop unity gain frequency which reduces the bandwidth of the system.

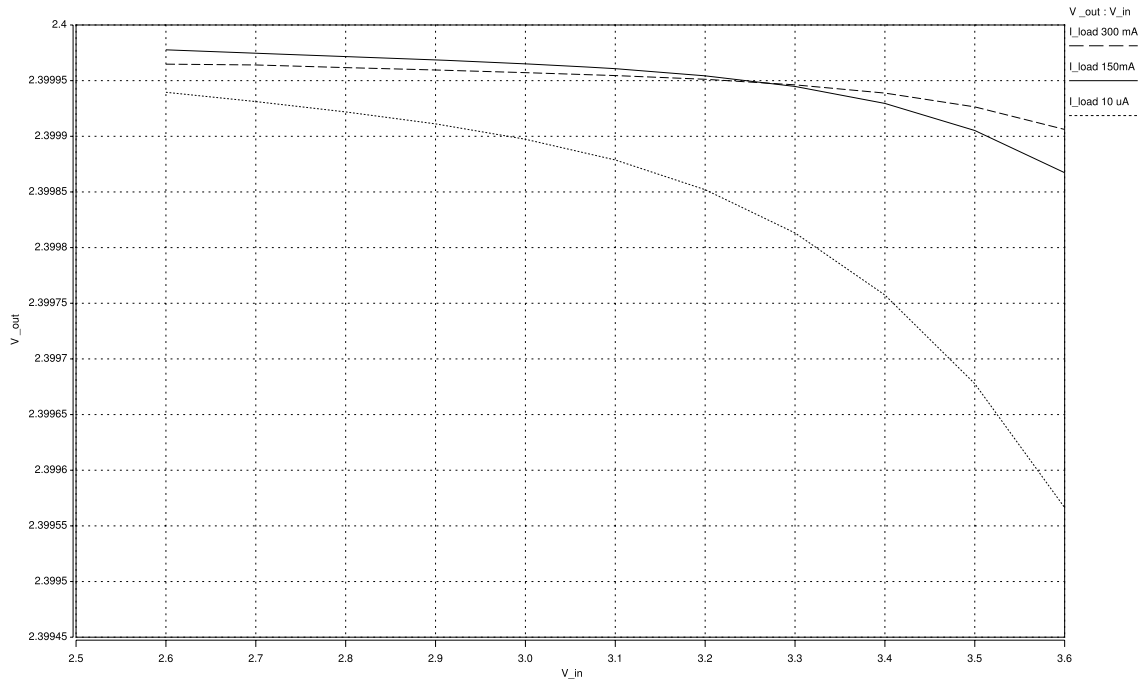


Figure 5.14: Line regulation of the proposed LDO topology.

5.3 Current Limiter

The simulation results of the current limiter circuit presented in Figure (4.3) are shown in Figure (5.15) for all alters condition. The typical corner is identified as $run = 0.0$ and has a value of $574mA$, with this value preventing the destruction of the $PMOS$ pass transistor. Although the large size of the $PMOS$ pass transistor can yield a greater value of current than the considered. The values of maximum allowable current changes with alters condition range from $450\ mA$ to $742\ mA$, which corresponds to a variation of 30% over the nominal value.

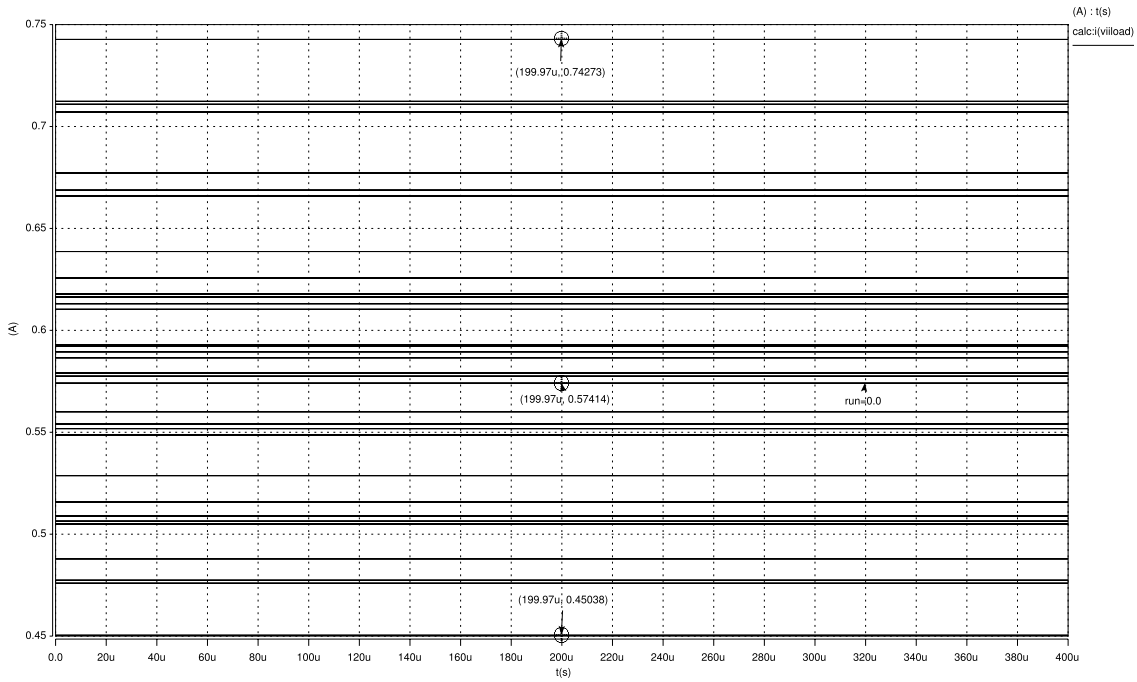


Figure 5.15: Current Limiter Performance of the proposed current limiter topology over all alters condition.

5.4 Power-Down Mode

The performance of the power-down mode is extremely important for the applications where power circuit frequently needs to turn the regulator on and off. Assuming that the power supply is ramped up with a rise time of a few microseconds. The response time of the proposed LDO topology is presented in Figure (5.16) over all alters condition. A more accurate view of rise time and fall time is shown in Figure (5.17) and Figure (5.18) respectively. The ($enable$) voltage is given by the supply voltage, thus the ($enable$) signal varies from $2.6\ V$ to $3.6\ V$ as shown by the figures mentioned previously.

The achieved power consumption in power down mode has a quiescent current consumption less than $100\ nA$. The worst case of the power consumption occurs during the power-down, that is correlated with a peak of the quiescent current consumption as shown in Figure (5.19).

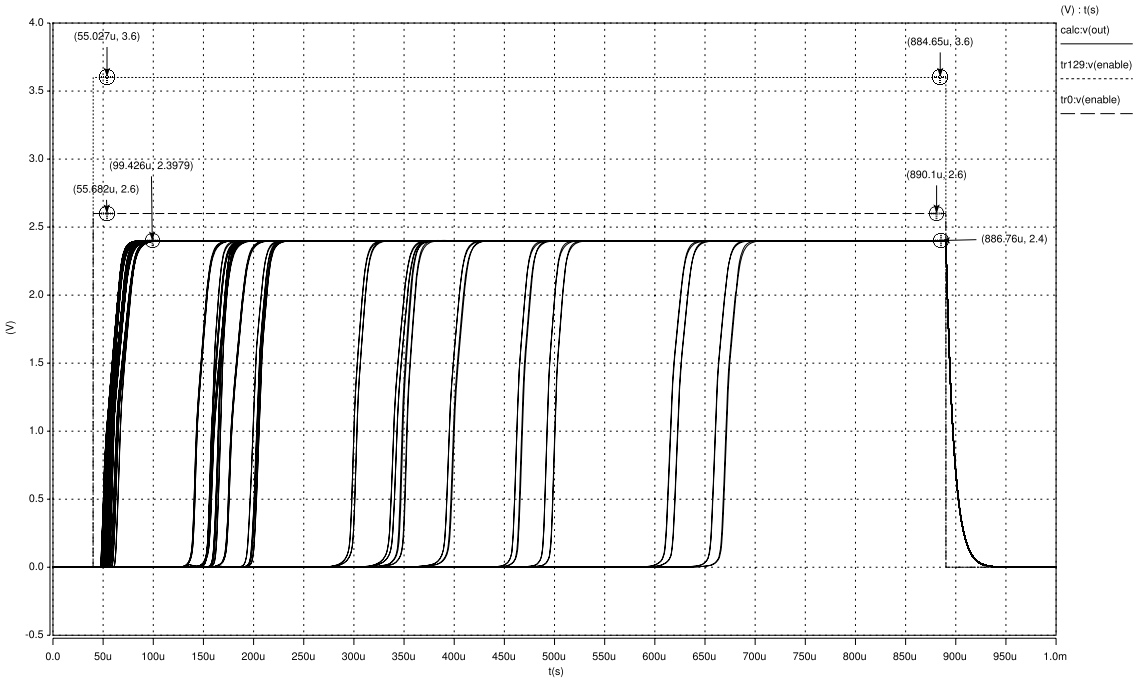


Figure 5.16: Power-Down mode performance of the proposed LDO topology over all alters condition.

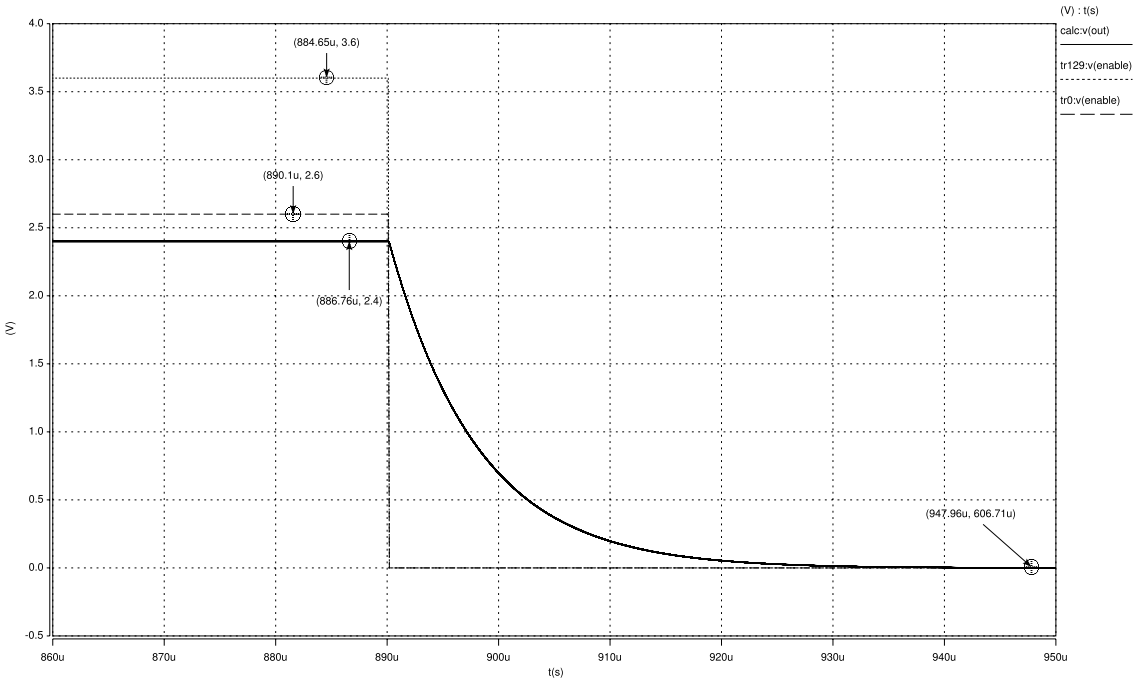


Figure 5.17: Fall time response of the proposed LDO topology over all alters condition.

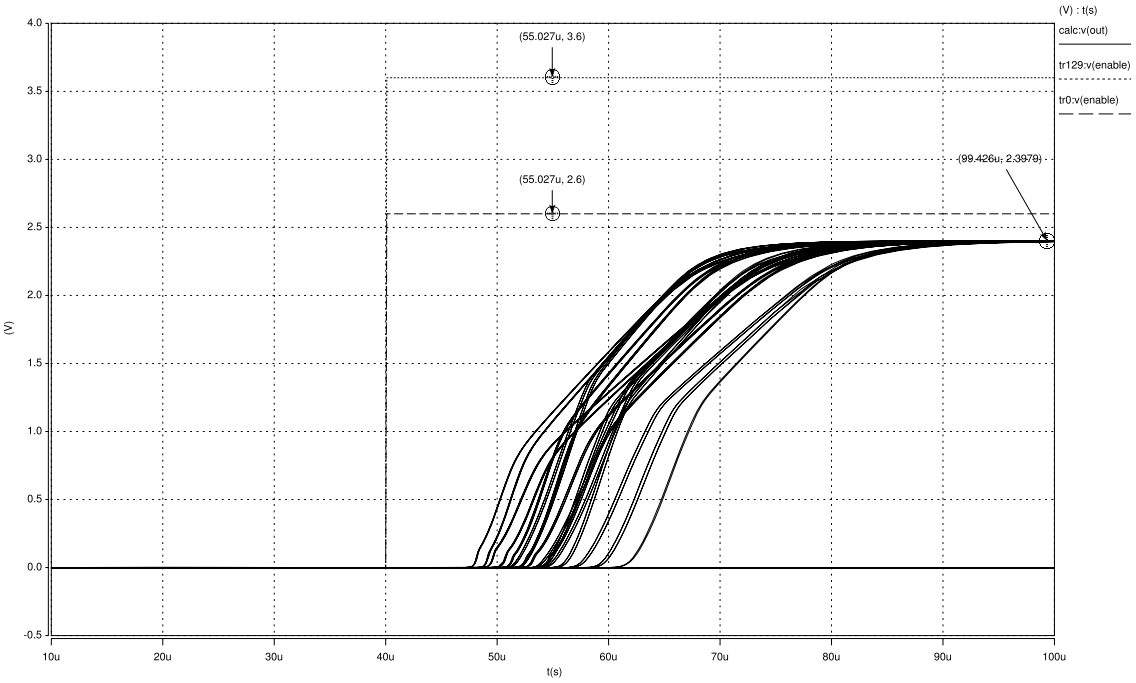


Figure 5.18: Rise time response of the proposed LDO topology over all alters condition.

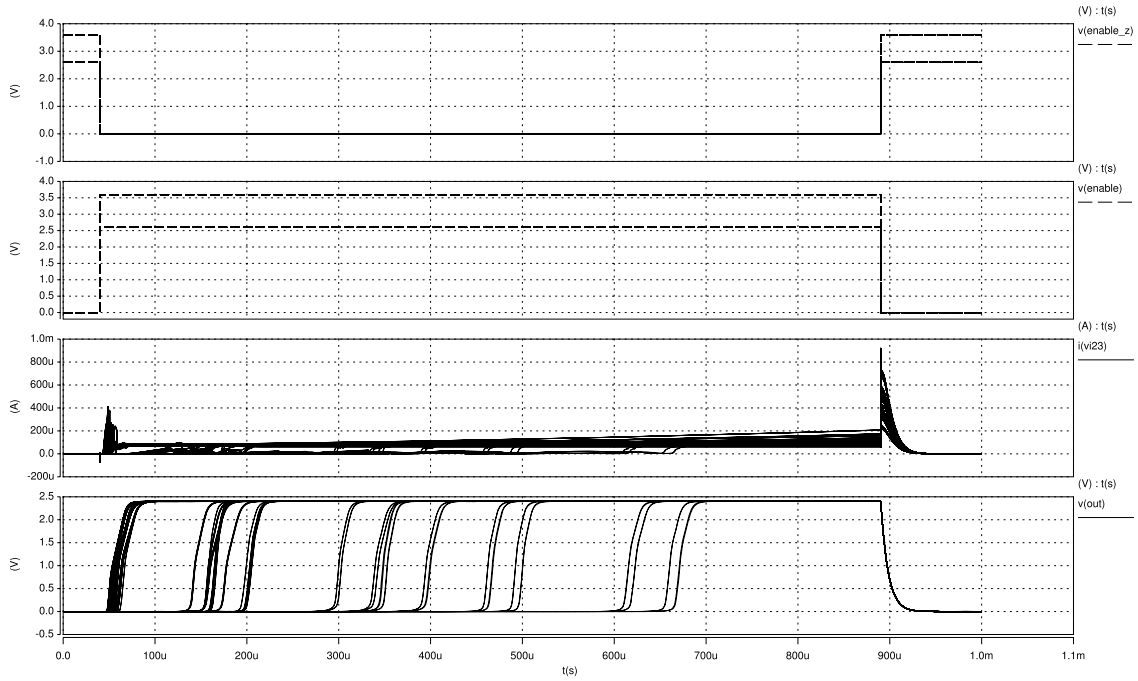


Figure 5.19: Power-Consumption performance of the power-down mode over all alters condition.

5.5 PSRR Performance

In this section is presented the PSRR analysis. The achieved PSRR performance of the proposed LDO topology for all load current condition from $10\mu A$ to $300mA$ is presented in Figure (5.20). As can be seen by inspection of the Figure(4.7) and Figure(5.20), the proposed strategy allows a large improvement of the PSRR when compared to the initial proposal. Furthermore this improvement can be obtained without an increase of the feed-back loops and complexity of the circuit, although the quiescent current consumption is increased to yield this PSRR performance. However as mentioned in Chapter 4 this increase does not have a significant impact in power consumption of the regulator. Otherwise the presented PSRR result could not have been achieved, since as discussed previously in Chapter 3, the PSRR performance is highly correlated with UGF and GBW of the error amplifier.

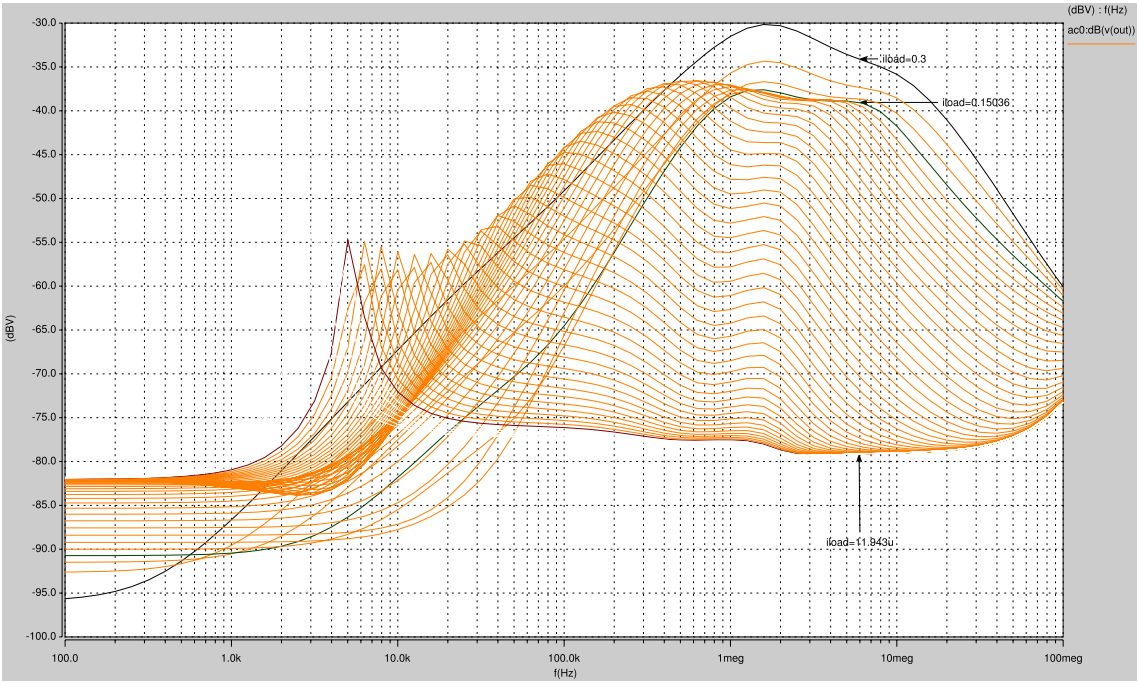


Figure 5.20: PSRR response of the proposed LDO topology for all load currents condition.

The PSRR response of the regulator circuit for $I_{load} = 300\ mA$ and $I_{load} = 150\ mA$ is presented in Figure(5.21) and Figure(5.22) respectively. The system achieves a better PSRR performance for the low load current. As can be seen in Figure(5.21) the system has $-82dB@1kHz$ and less than $-30\ dB$ at $1\ Mhz$, for the typical corner line in black in Figure (5.20), thus the proposed objectives are achieved.

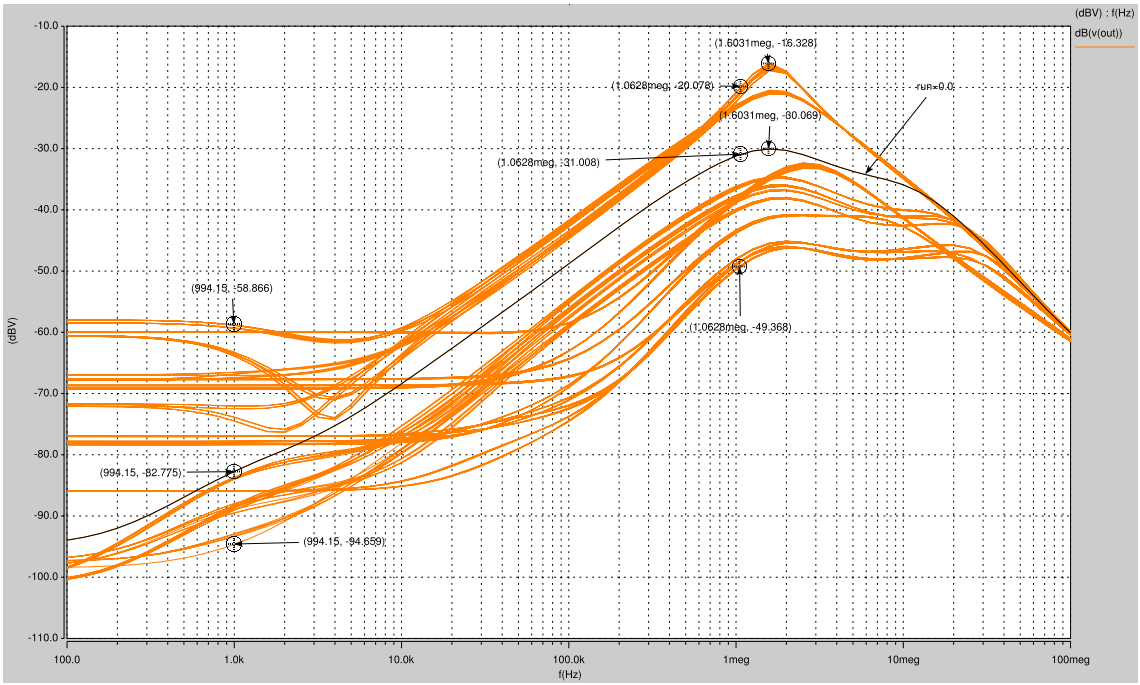


Figure 5.21: PSRR response of the proposed LDO topology for $I_{load} = 300\ mA$ over all alters condition.

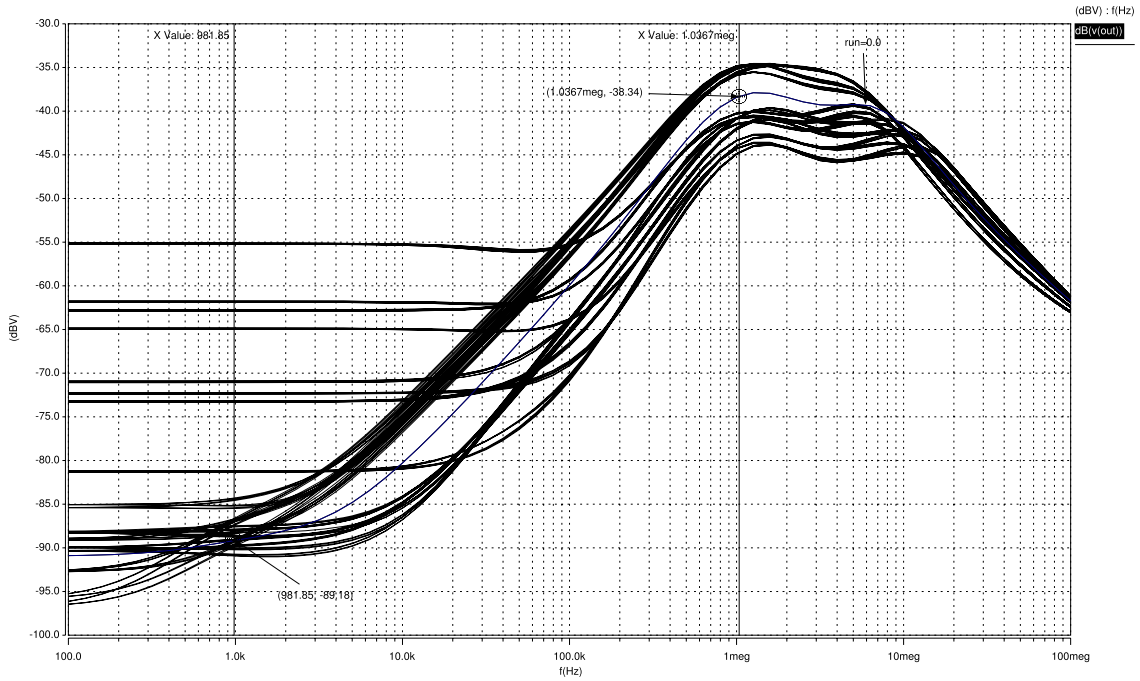


Figure 5.22: PSRR response of the proposed LDO topology for $I_{load} = 150\ mA$ over all alters condition.

6

Layout

The layout is an important concern for the global performance of any LDO circuit. It is highly affected by the mismatch that occurs during the process fabrication between the parameters of an equally group designed. The mismatch not only affects the DC performance, where it causes nonzero offset voltage, but also affects high frequencies reducing the PSRR performance.

Moreover the interconnect crossovers in the amplifier design can produce parasitic or undesired capacitance. This problem can be solved with a careful design and shielding of the amplifier inputs with metal lines connected to the ground [14]. Moreover the design of transistors with translational symmetry (i.e. each transistor is a copy of the other without rotation), reduces the capacitance.

The mismatch of the input transistors of the amplifier can be reduced with methods commonly used in conventional amplifier design, such as placing these input transistors with common-centroid method and designing them in large width.

The Figure (6.1) shows the complete floor plan of the proposed LDO circuit layout. The large size of the $PMOS$ pass transistor is greatly denoted (on the top of the figure), since it has the ability to supply high load current. The resistors (red part on bottom of the figure) would be made of the most highly resistive layer in attempt to decrease the area consumption, hence the resistive poly-resistor is considered. The implementation of the capacitors is done by $MOScap$ transistors, since the linearity is not a concern and yields better area consumption than CVPP capacitor (yellow part on bottom of the figure).

The $PMOS$ pass transistor, capacitors and resistances occupy most of the area of the proposed LDO circuit. The total area is approximately $0.2\ mm^2$. The high load current consumption must be considered for design of the supply rails, thus it large size is a must. This can be reduced by driving the current through different levels of metal.

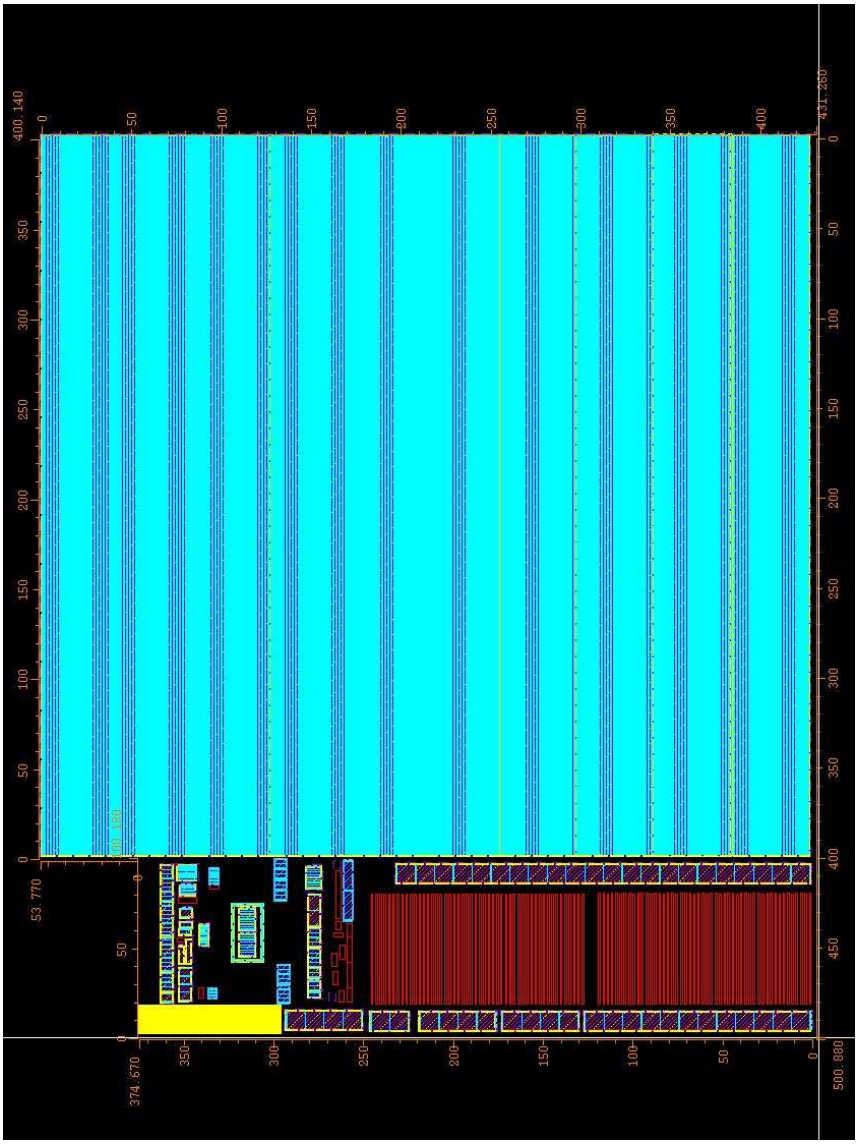


Figure 6.1: Layout Floor Plan of the proposed LDO.

7

Conclusions

Contents

The design and limitations of the LDO voltage regulators were analyzed in this work, different LDO voltage regulator topologies were studied, in order to obtain a simple and robust circuit that has potential to accomplish the proposed specifications.

The use of several techniques to improve the stability and the PSRR performance of the LDO were considered. Within the scope of the low quiescent current consumption required by the initial specifications a folded cascode and push-pull topology were employed in the error amplifier design for the first and second stages respectively. These topologies allow a low current consumption and provide a high DC gain with high GBW and UGF, which are required for a high PSRR performance. Moreover the use of a push-pull topology allows an enhance of the slew-rate imposed by the large $PMOS$ pass transistor. This was designed to obtain a low drop-out voltage less, than $200\ mV$ for all the load current conditions.

A new compensation scheme is presented that provides both a fast transient response and full range AC stability from $10\ \mu A$ to $300\ mA$ of the load current. It is composed by the use of the NMC technique, DMFC which is based in PZTFC and SMC pole-splitting. Thus the stability of the system is ensured for all the load current conditions. However the PSRR performance was limited by the specifications of the current consumption, since it is correlated with the performance of the error amplifier.

In order to solve the problem of GBW and UGF of the error amplifier and consequently improve the PSRR performance of the system over a wide frequency range, dynamic biasing was considered. Since the majority of the applications demand low load-currents for the majority of the time, while high load currents are only demanded briefly. The use of this technique as shown does not affect the power efficiency of the LDO voltage regulator, and the stability can be ensured by the use of a RC delay. The use of this technique allows to achieve a PSRR performance of $-30dB@1MHz$, which is an improvement in State-of-the-Art of this kind of circuit.

The compensation techniques have been developed and verified in $SMIC\ 0.13\mu m$ CMOS technology at Chipidea®and permit a practical realization of the LDO voltage regulator. It is also less sensitive to process variations and load conditions, which can work in a battery operated environment, thus being suitable for SoC solutions.

7.1 Future Work

The proposed LDO topology represents an improvement on the State-of-the-Art of this kind of circuit. Although the area consumption can be reduced with the use of the other CMOS processes, which implies smaller chip area and cost reduction.

The reduction of threshold voltages allow an increase in DC performance of the LDO voltage regulators. Although is not expected to decrease below $0,5\ V$ or $0,6\ V$, since this is characteristic imposed by digital circuits. The consequence of lower breakdown voltages in future technologies

will force regulator design to work with lower input voltages. This is aggravated by the growing demand for single, low voltage battery cell operation.

The use of $BiCMOS$ technology can increase significantly the performance of the LDO voltage regulators. The addition of a p-base layer to a CMOS process offers the capability of vertical bipolar devices, which enhance the frequency response and the circuit topology characteristics of the LDO, however it implementation is still expensive and difficult. The use of MOS technology yields a better low quiescent current flow.

The SoC and mixed-signal products are the result of complete circuit integration. A simultaneous coexistence between analog and digital circuits is possible in a purely CMOS environment but with degraded analog performance. This type of environment demands a high PSRR performance of the LDO, a low drop-out voltage and less occupied chip area. These are requirements that are driven by the market demand. Furthermore, quiescent current flow and drop-out voltage will be demanded to decrease as well.

The main concerns can be resumed in fast transient response, stability, low power consumption, area consumption and PSRR. In an attempt to improve the stability and PSRR of the system, other compensation techniques can be correlated and error amplifier topologies can be used, in an attempt to achieve a better LDO voltage regulator.

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A

Testbenches

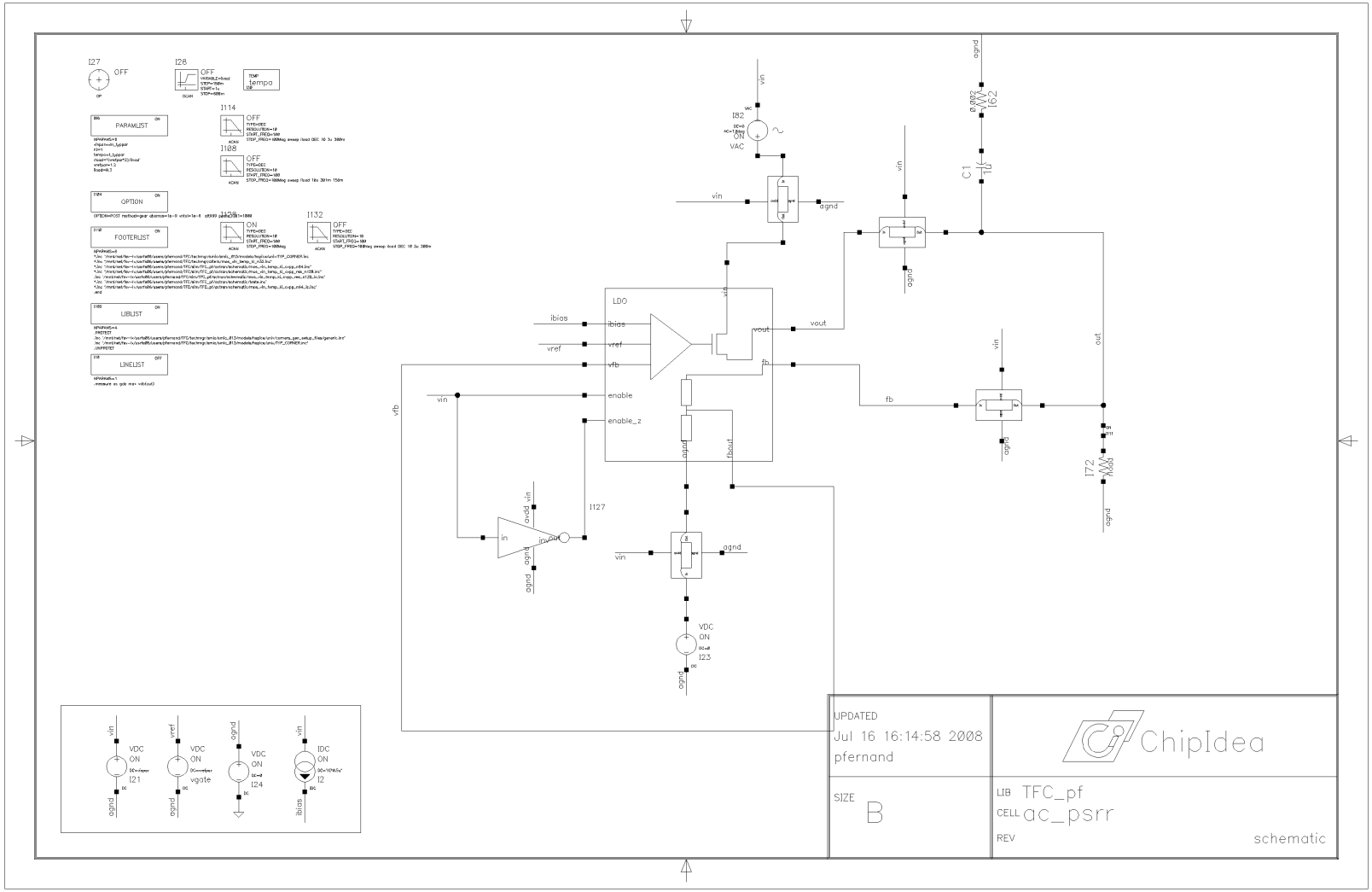

Figure A.1: Testbench used to evaluate the psrr performance of the proposed LDO topology.

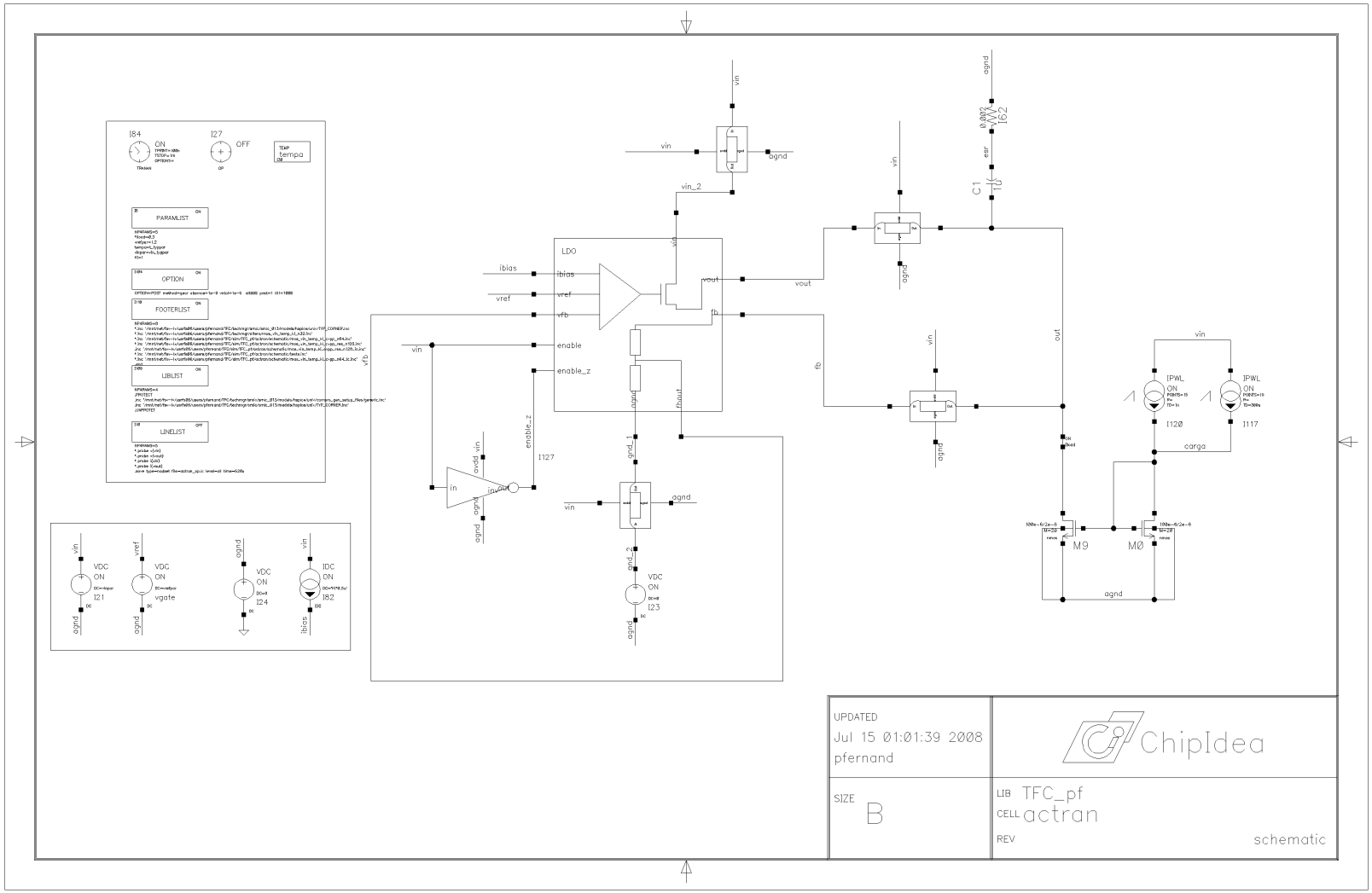

Figure A.2: Testbench used to evaluate the transient response performance of the proposed LDO topology.

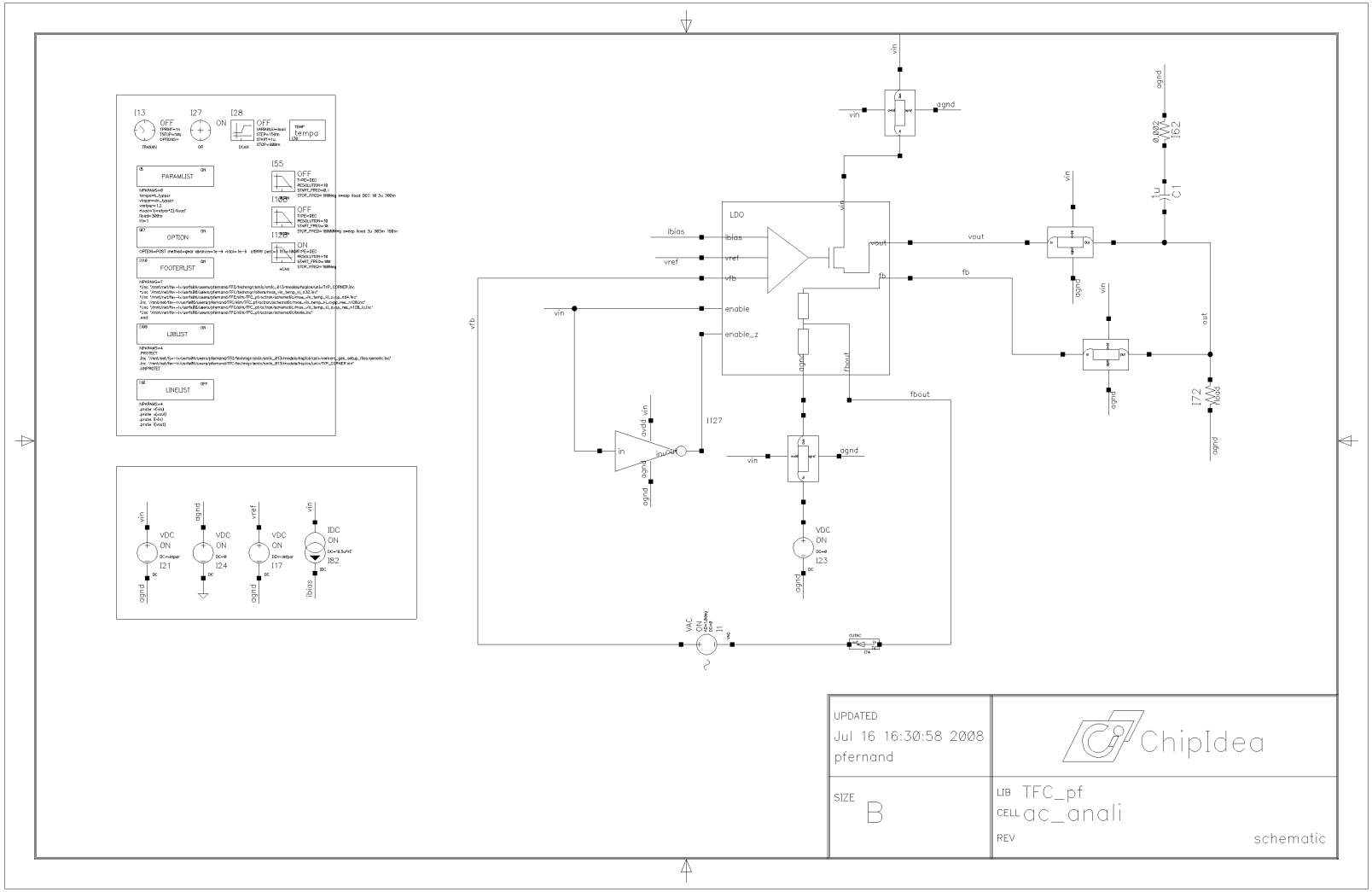

Figure A.3: Testbench used to evaluate the AC open-loop performance of the proposed LDO topology.

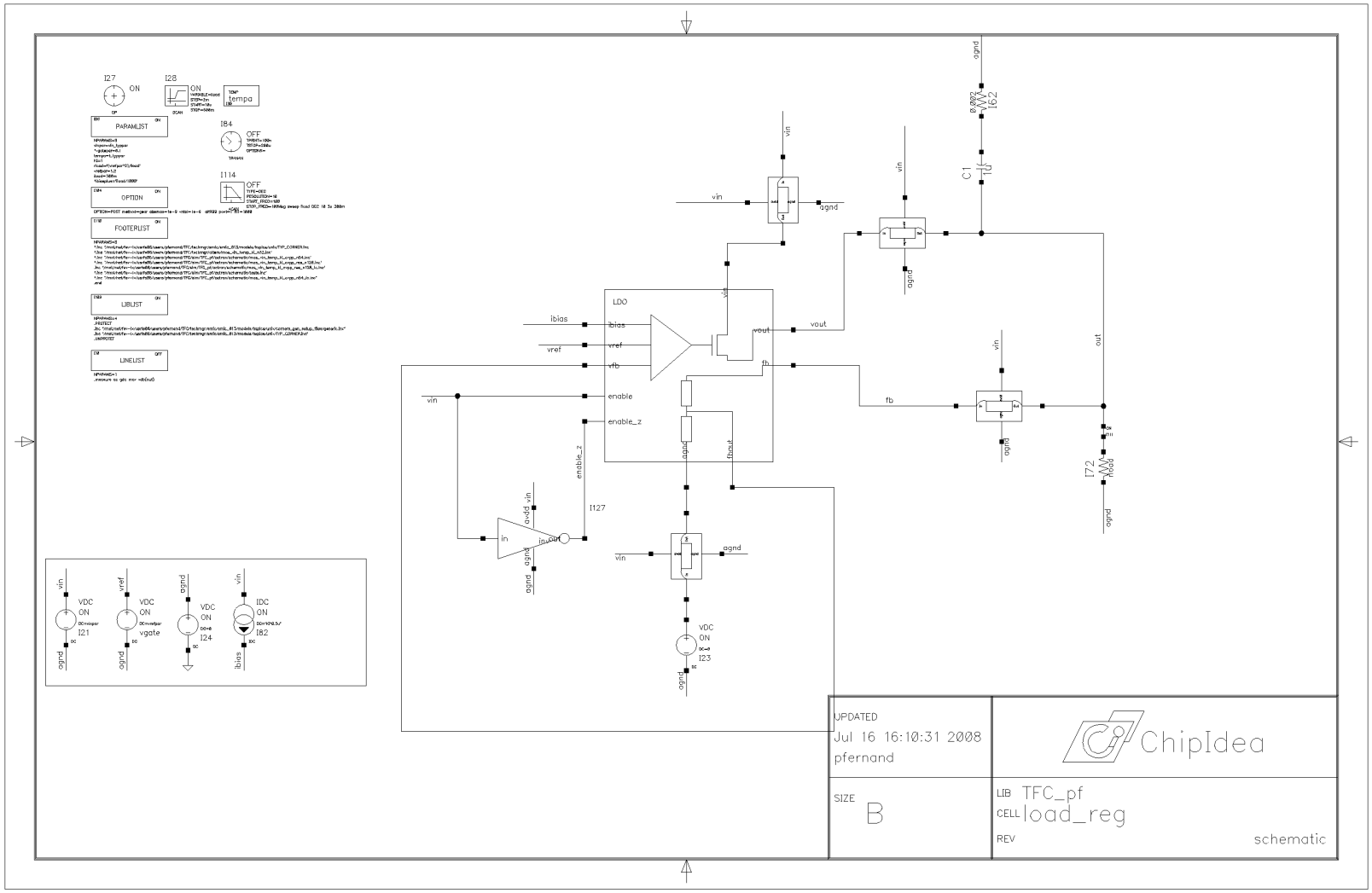

Figure A.4: Testbench used to evaluate the load regulation performance of the proposed LDO topology.

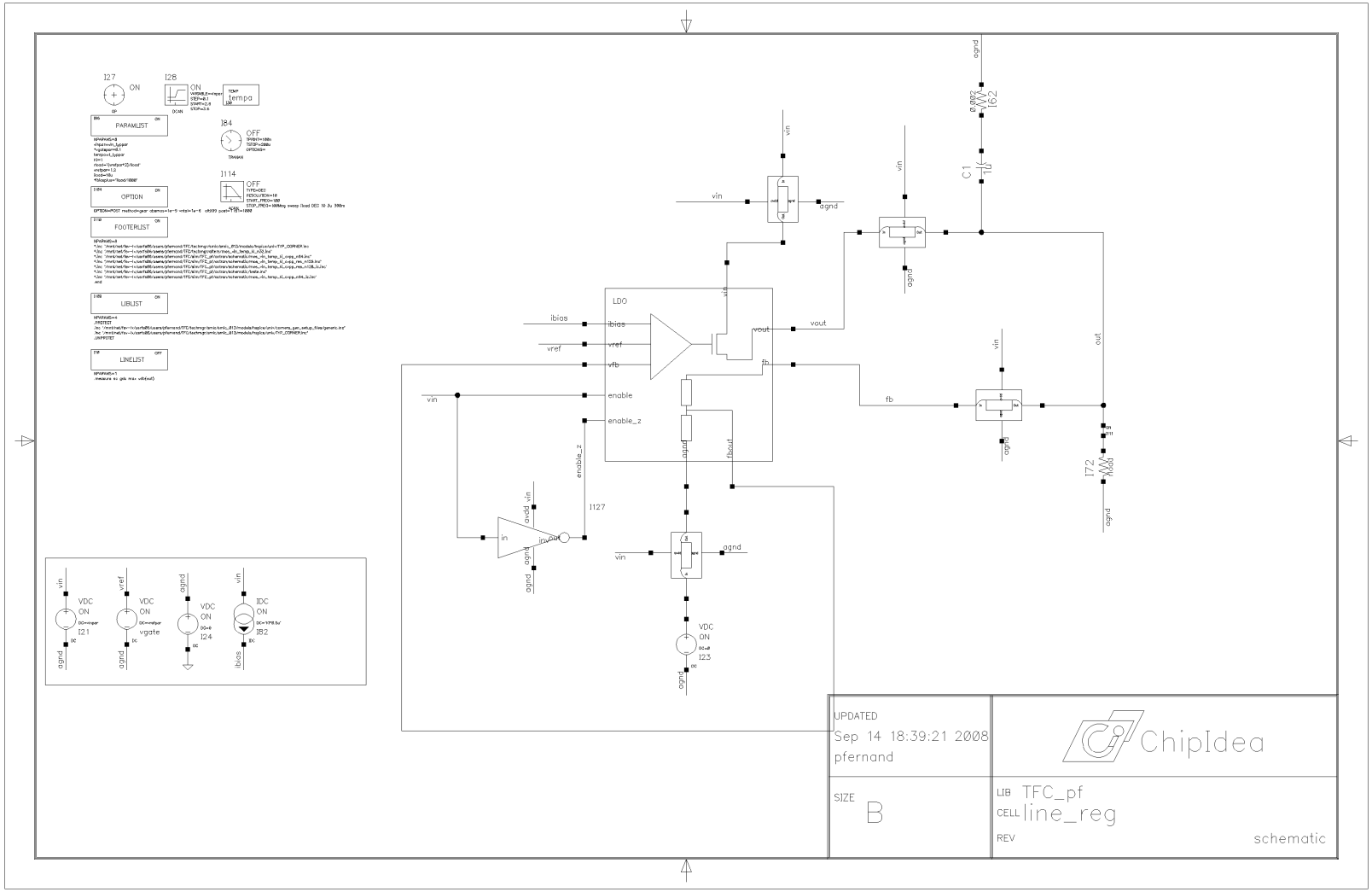

Figure A.5: Testbench used to evaluate the line regulation performance of the proposed LDO topology.

B

Schematics

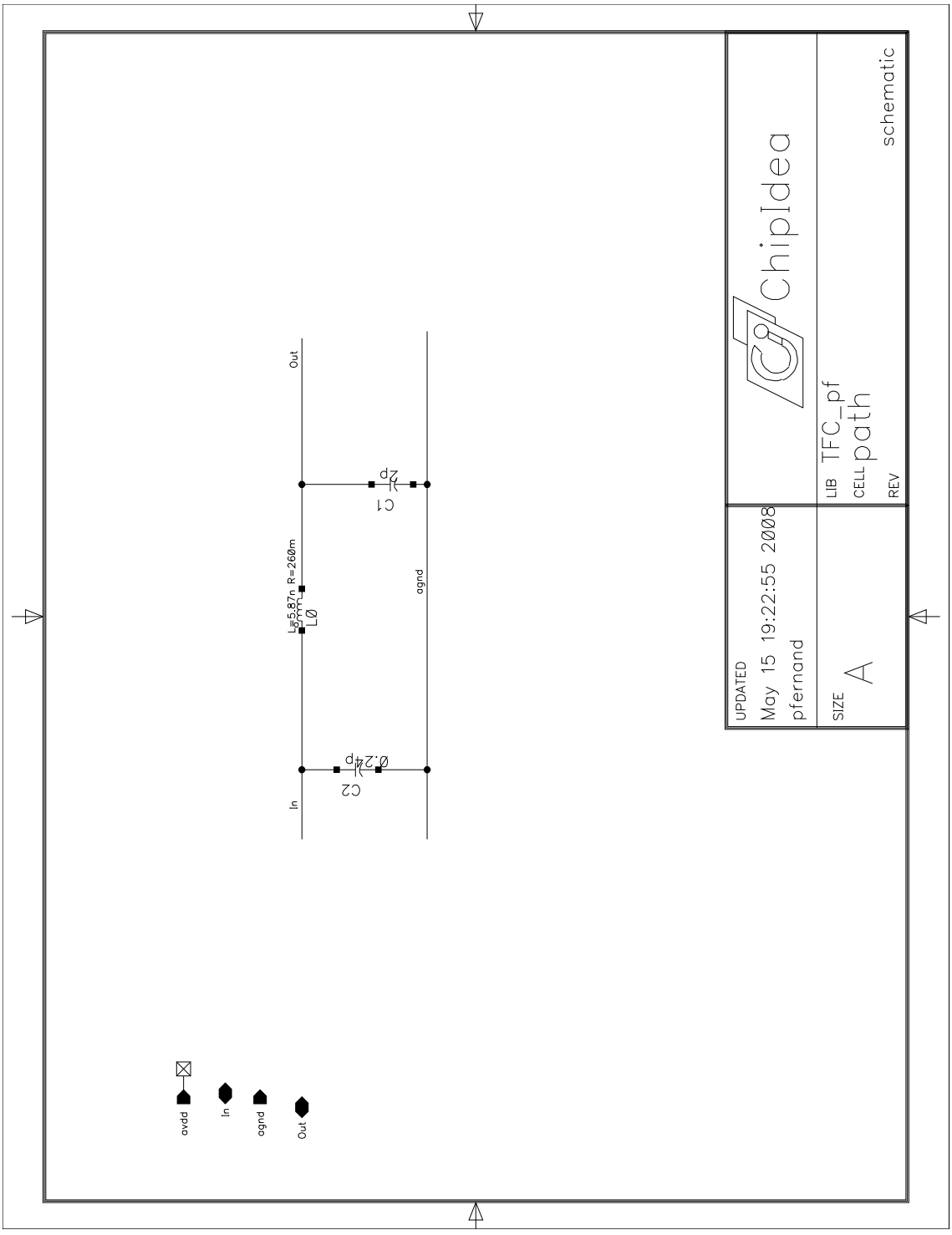

Figure B.1: Schematic of the equivalent circuit of the bonding wire.

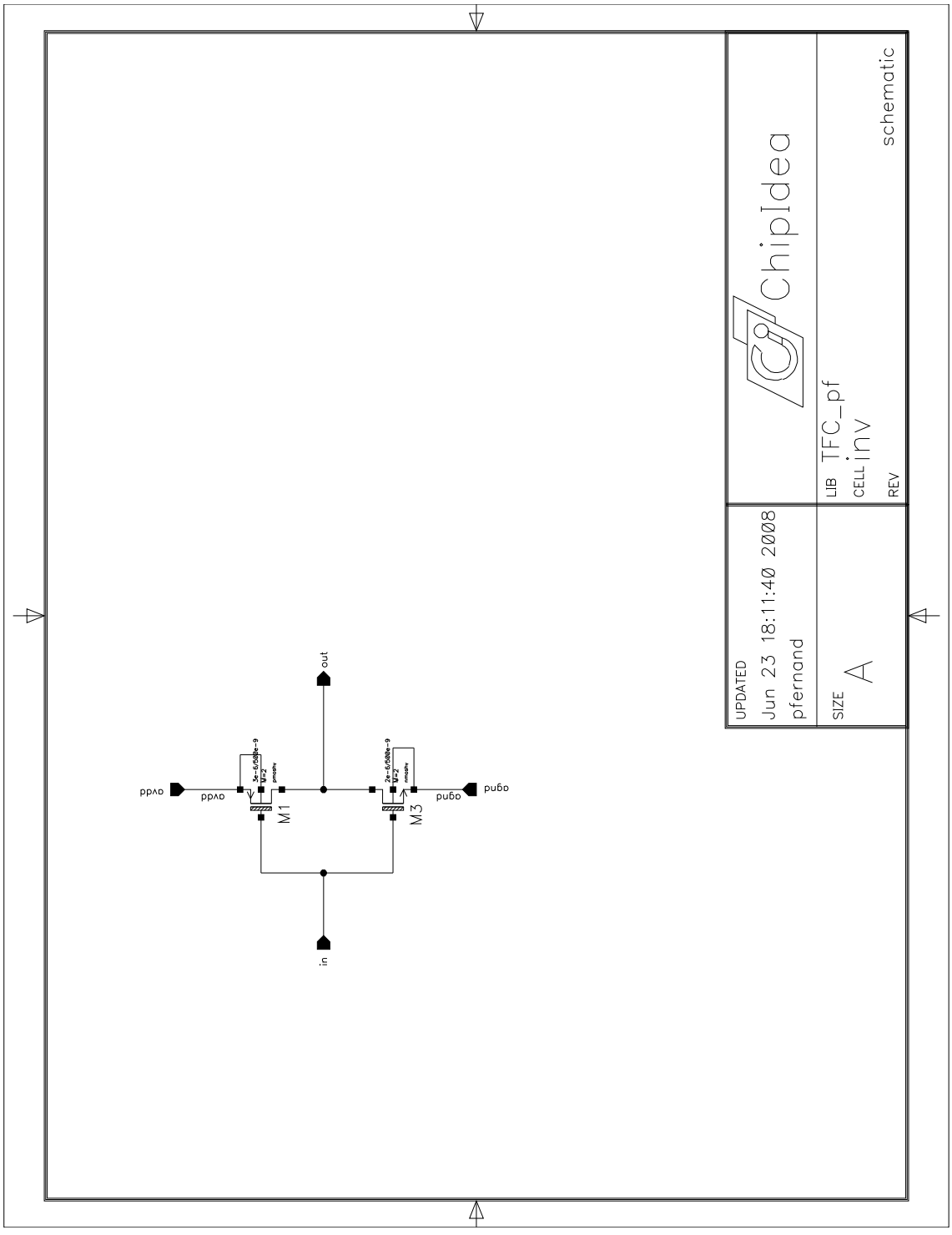

Figure B.2: Schematic of the inverter topology used in Power-Down mode.

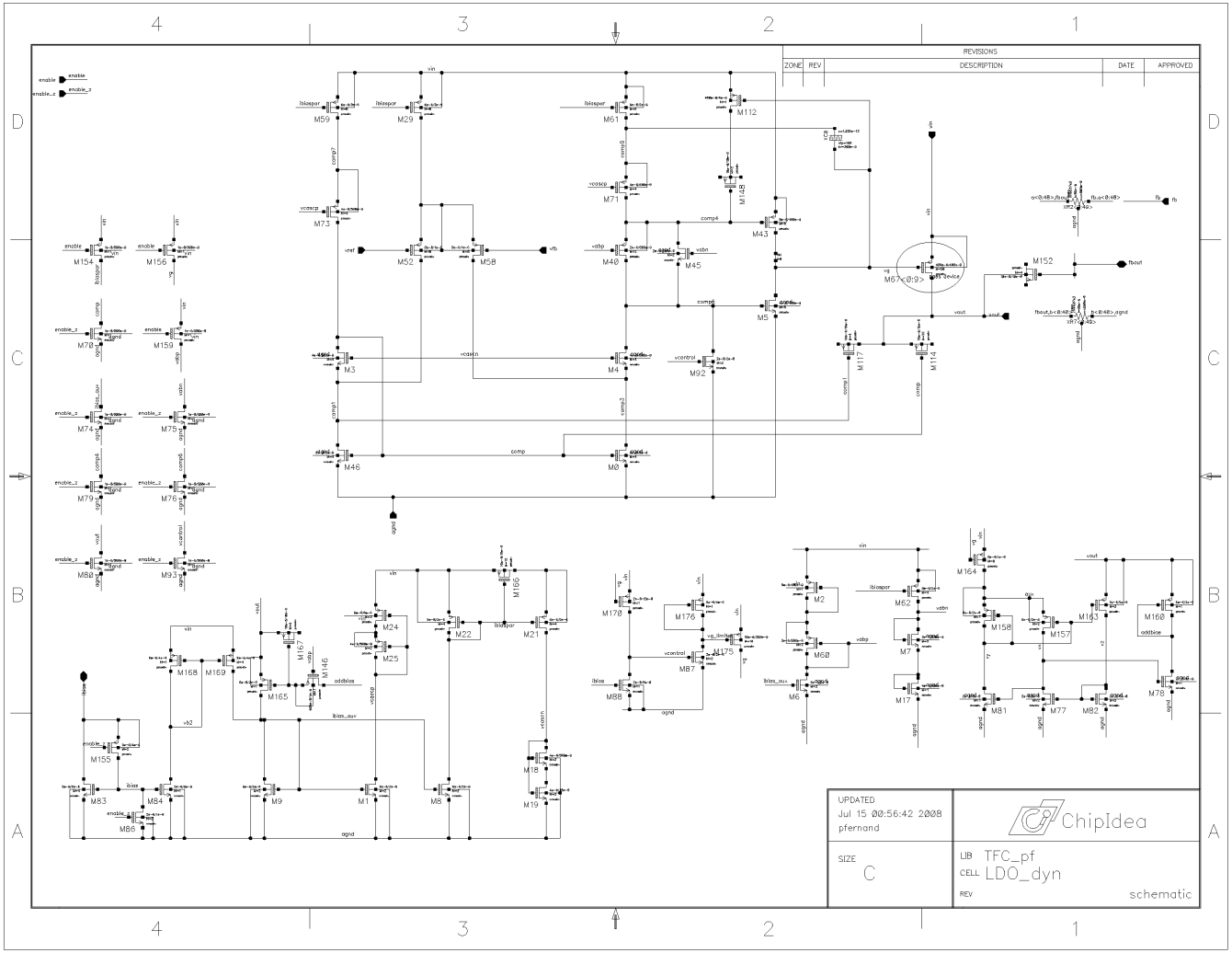

Figure B.3: Schematic of the proposed LDO topology.