Inductorless Power Management ICs for Portable Applications

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Outline

- Introduction
- Overview of Linear Regulators / Low Dropout Regulators
- Design Example
  - LDO with Buffer-Impedance Attenuation
- Conclusions

Importance of Power Management ICs

All portable battery-powered electronic devices

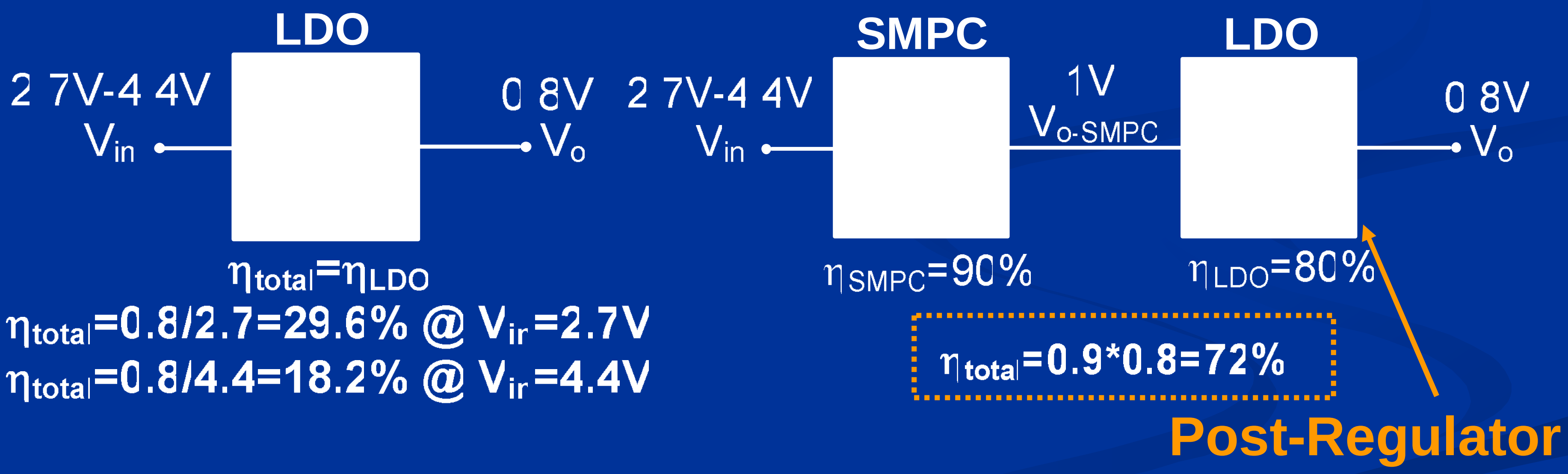
- Better quality of life
  - Continuous growth of portable market
  - Advanced features of portable equipment reduces battery lifetime
- Power management ICs are essential to provide dc-dc conversions in portable equipment.

Comparisons of DC-DC Converters

	Types	Benefits	Concerns
Inductor-based	Switched-mode power converter (SMPC)	■ High efficiency ■ Step up / down conversion	■ Large board space ■ High conducted EMI
Inductor-less	*Switched-capacitor regulator*	■ *No inductor* ■ *Step-up possible*	■ *High switch count* ■ *High loss and noise* ■ *Lack of effective control scheme*
	Linear regulator	■ ***Simplest*** ■ ***Integrable*** ■ ***Low noise***	■ ***Poor efficiency*** ■ ***No step-up operation***

Application of Linear Regulator

- Major application in portable equipment
  - To act as post-regulator for improving system power efficiency



LDO

2 7V-4 4V V_{in}

0 8V V_o

$\eta_{total}=\eta_{LDO}$

$\eta_{total}=0.8/2.7=29.6\%$ @ $V_{ir}=2.7V$

$\eta_{total}=0.8/4.4=18.2\%$ @ $V_{ir}=4.4V$

SMPC

LDO

2 7V-4 4V V_{in}

1V $V_{o\text{-}SMPC}$

0 8V V_o

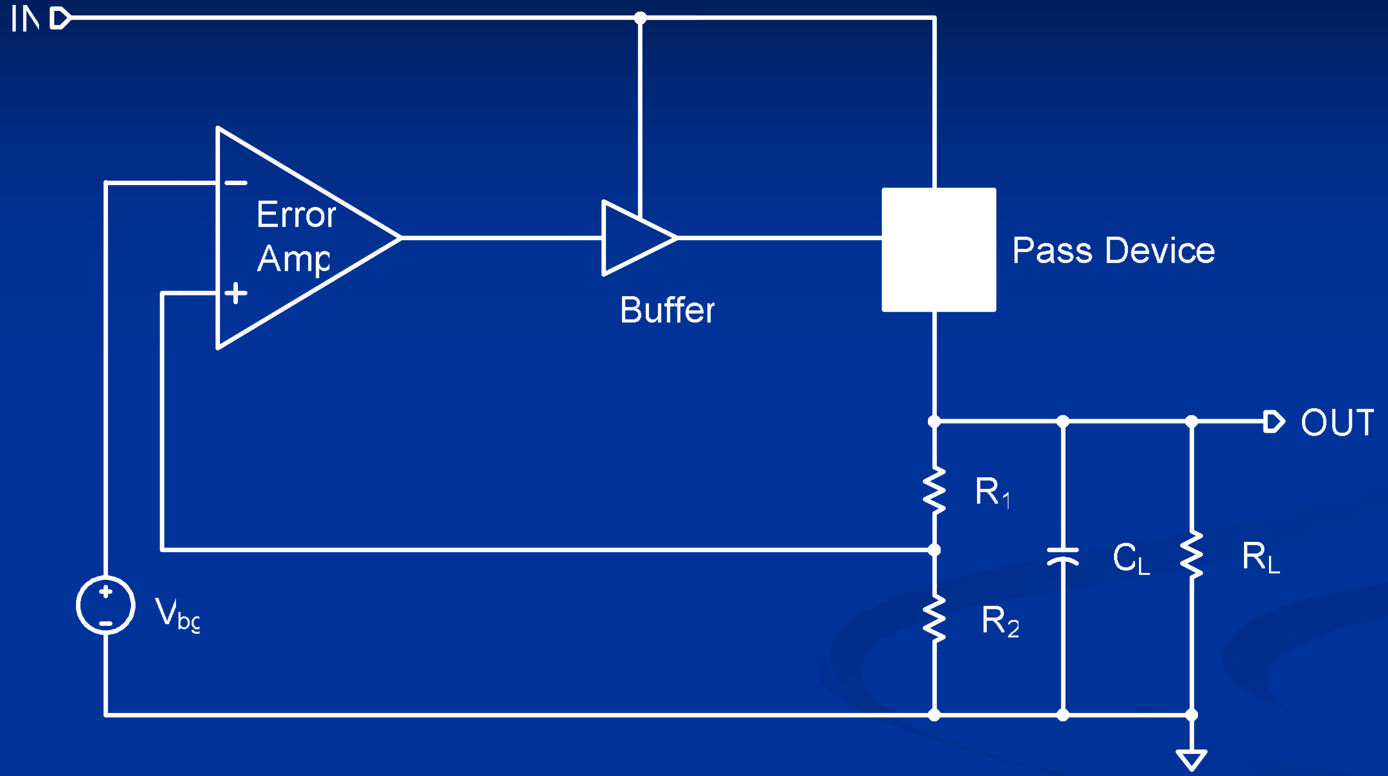
$\eta_{SMPC}=90\%$

$\eta_{LDO}=80\%$

$\eta_{total}=0.9*0.8=72\%$

Post-Regulator

Structure of Linear Regulator

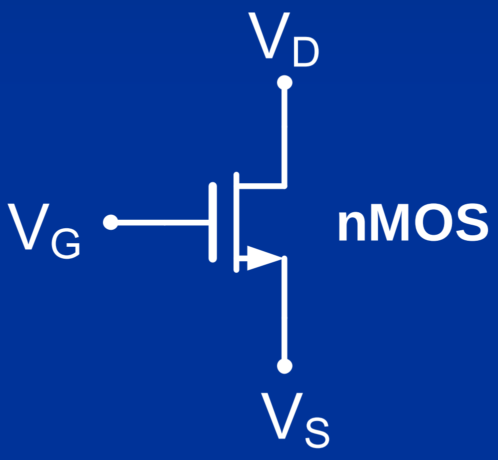


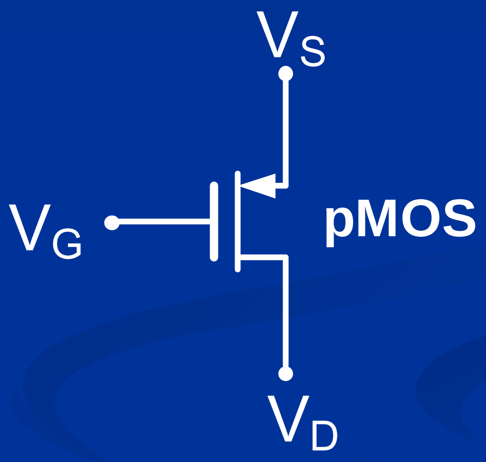
- Pass device delivers load current up to hundred mAs.
- Buffer drives the pass device.
- Error amplifier and bandgap maintain output voltage accuracy through regulation.

Linear Regulator: Power Efficiency

$$\eta = \frac{V_{out}}{V_{in}} \times \frac{I_{out}}{I_{in}} = \frac{V_{out}}{V_{in}} \times \frac{I_{out}}{(I_{out} + I_q)} \approx \frac{V_{out}}{V_{in}}$$

Options of Pass Device



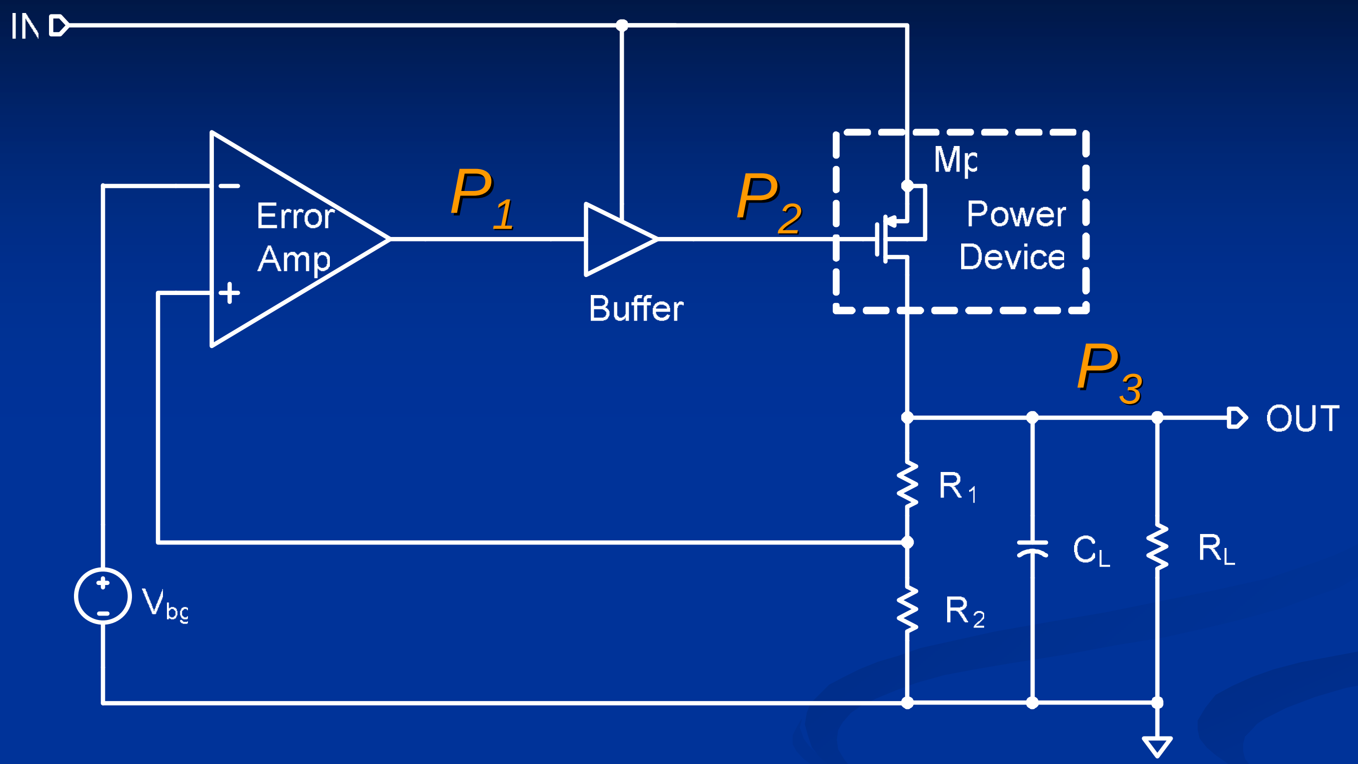


$$\eta_{nMOS} = \frac{V_{out}}{V_{in}} \approx \frac{V_{in} - V_{th} - 2V_{dsat}}{V_{in}}$$

$$\boxed{\eta_{pMOS} = \frac{V_{out}}{V_{in}} \approx \frac{V_{in} - V_{dsat}}{V_{in}}}$$

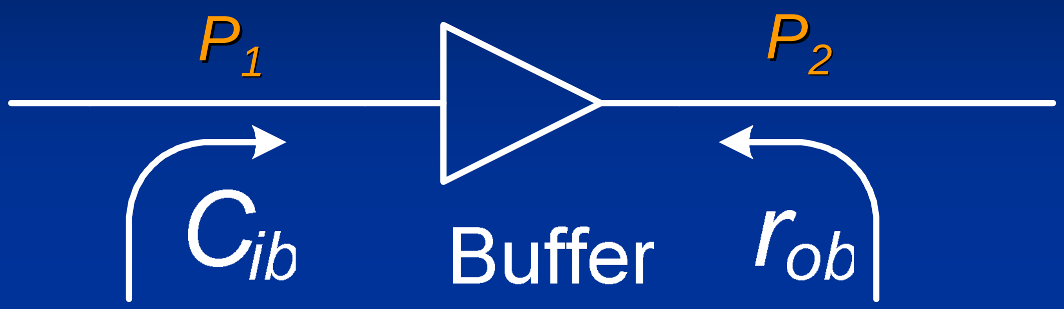
pMOS pass device provides much better power efficiency due to much smaller dropout voltage (V_{in}-V_{out}=V_{dsat})!

Design Requirements of LDO



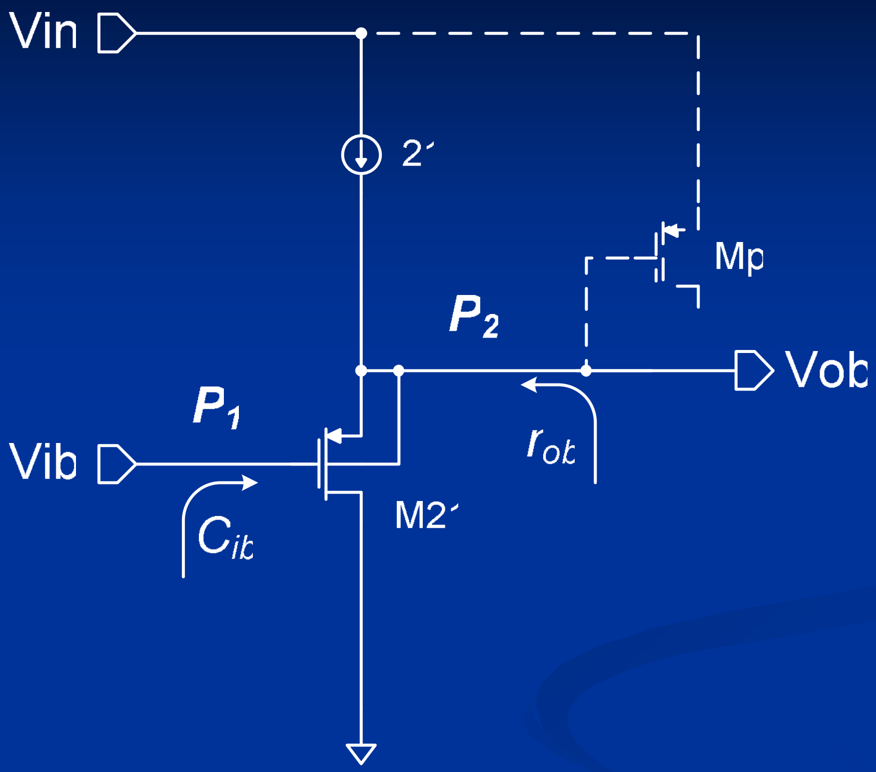
- ***"Stability"*** **under different load currents.**
- ***"Small quiescent current and output capacitor"*** **for better battery lifetime and lower cost considerations.**
- ***"Good load transient responses"*** **under small current consumption and output capacitor.**

Stability Considerations



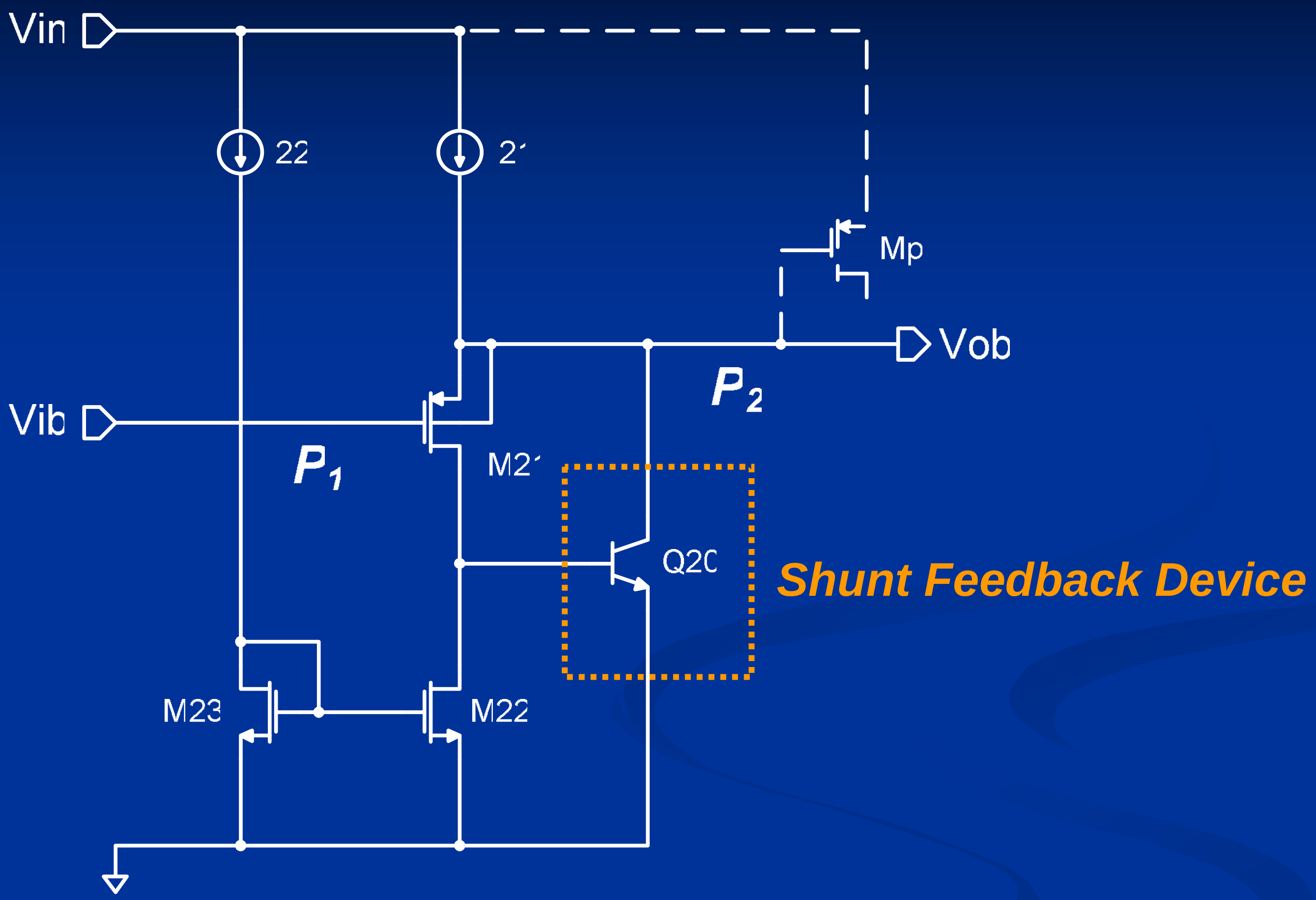
- **Pushing P_2 and P_1 to high frequency**
  - **Small buffer output resistance r_{ob}**
  - **Small buffer input capacitance C_{ib}**
- **Will we suffer from any tradeoff(s) by achieving stability?**

Conventional Source Follower



- Option 1: Moving P_2 to higher frequency by increasing g_{m21}
  - ***Increases LDO quiescent current*** or
  - ***Increases*** $(W/L)_{M21}$ ***&*** P_1 ***moves to lower frequency***
- Option 2: If using ESR zero for pole-zero cancellation
  - ***Degrades transient undershoot/overshoot performances***

Buffer-Impedance Attenuation



Shunt Feedback Device

- Add local feedback to the source follower
  - Q20 creates shunt feedback to decrease r_{ob}
  - Q20 can be replaced by nMOS

Impact of Shunt Feedback

- The effective output resistance of the buffer:

$$r_{ob} = \frac{1}{g_{m21} \cdot (1 + \beta_{Q20})}$$

where

g_{m21} : the transconductance of source follower M21

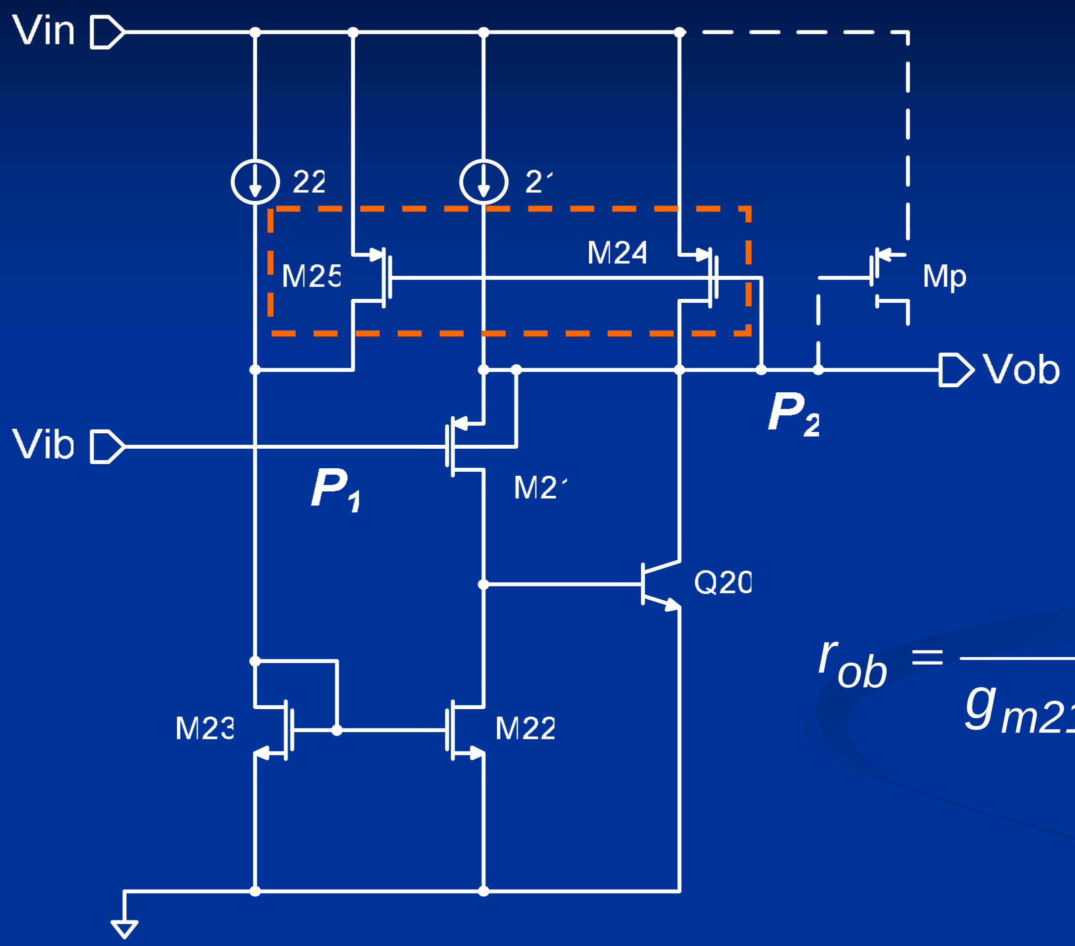
β_{Q21} : current gain of the npn device >>1

- $P_2 = 1/(r_{ob} \cdot C_g)$ moves to higher frequency by the current gain of the npn device

where

C_g is total capacitance at the buffer output

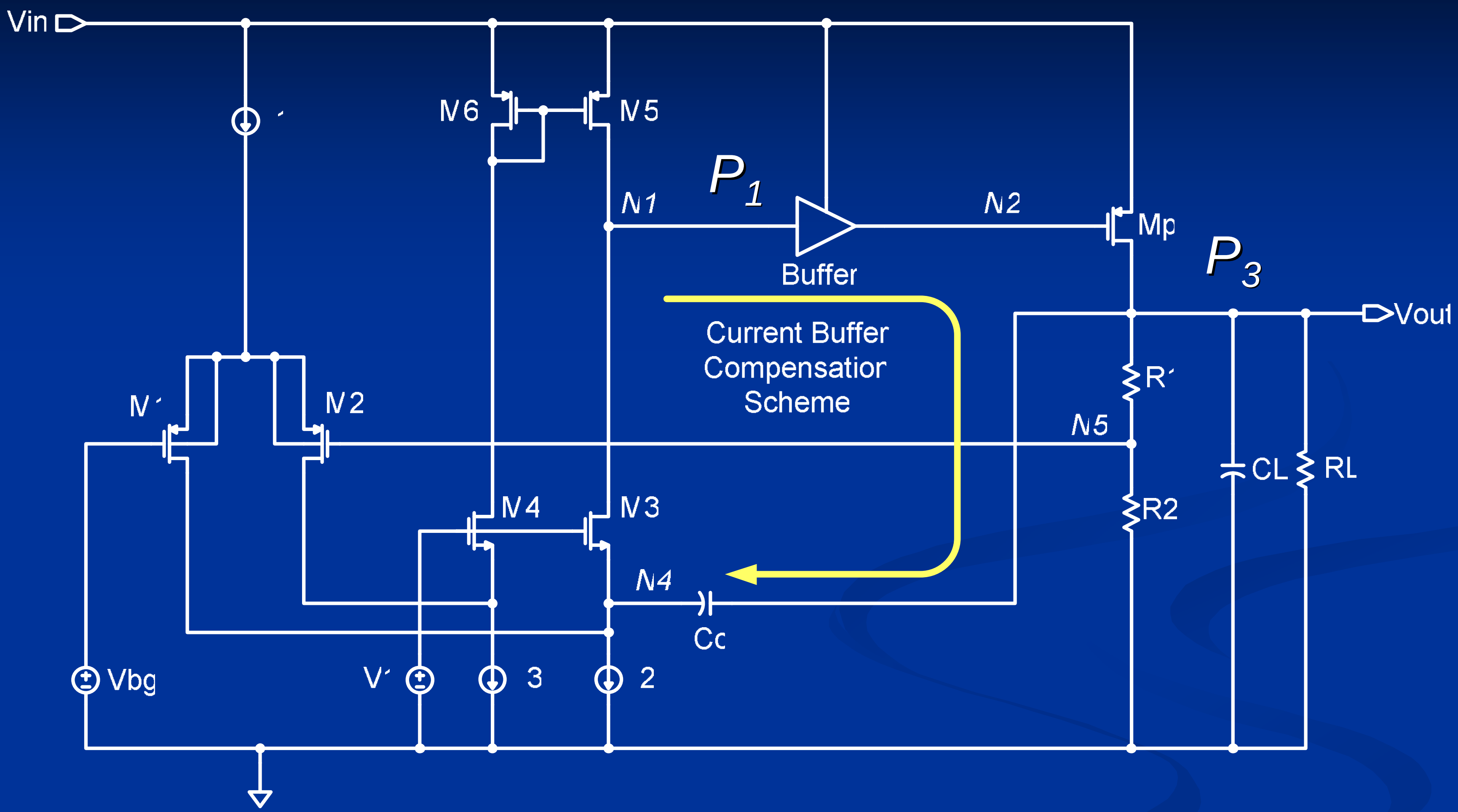
Dynamically-Biased Shunt Feedback



$$r_{ob} = \frac{1}{g_{m21} \cdot \left(1 + \beta_{Q20}\right) + g_{m24}}$$

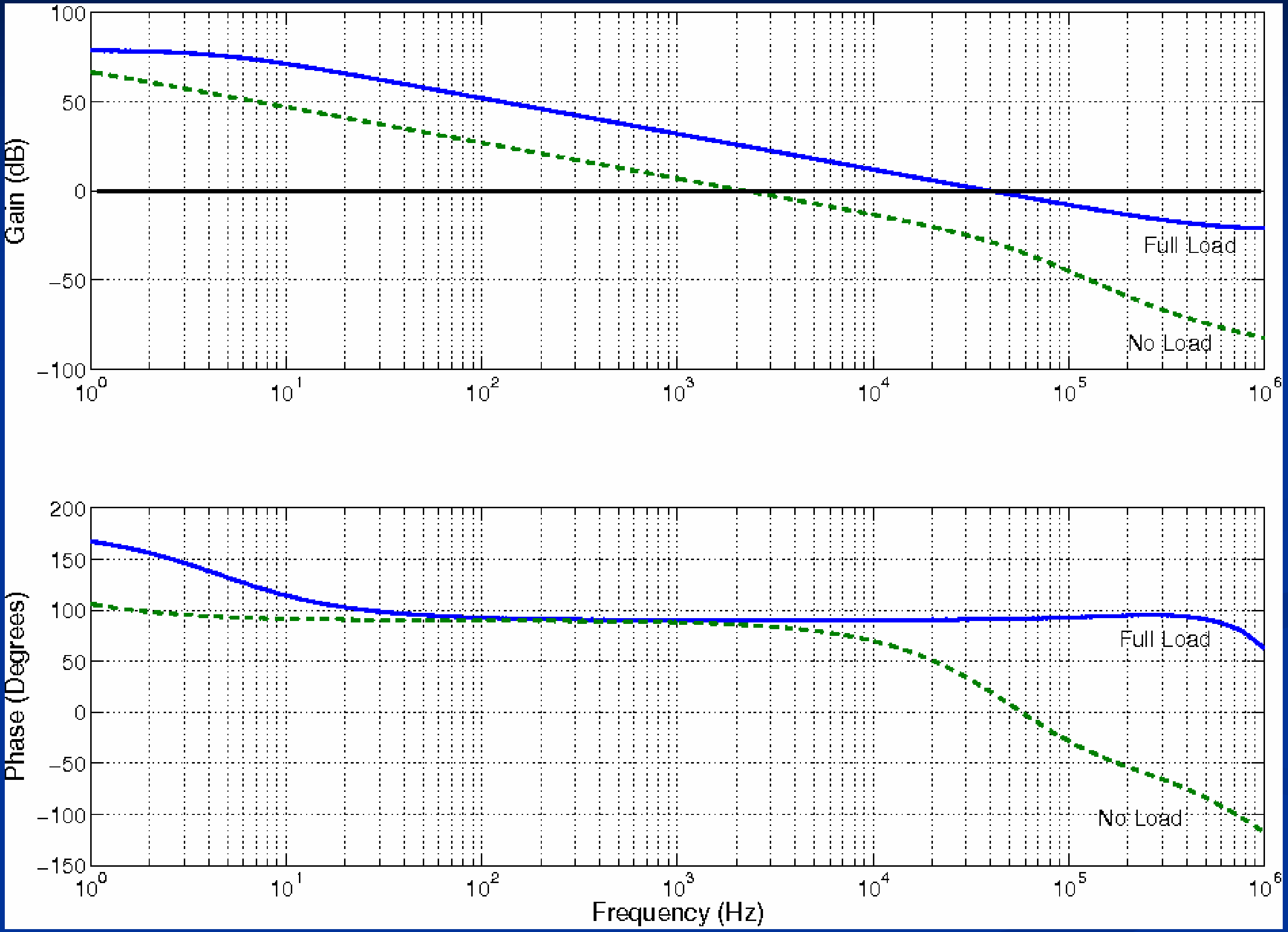
- Transistors M23 - M25 allow that r_{ob} decreases as load current increases ⇒ P_2 increases with the load current.

LDO Frequency Compensation



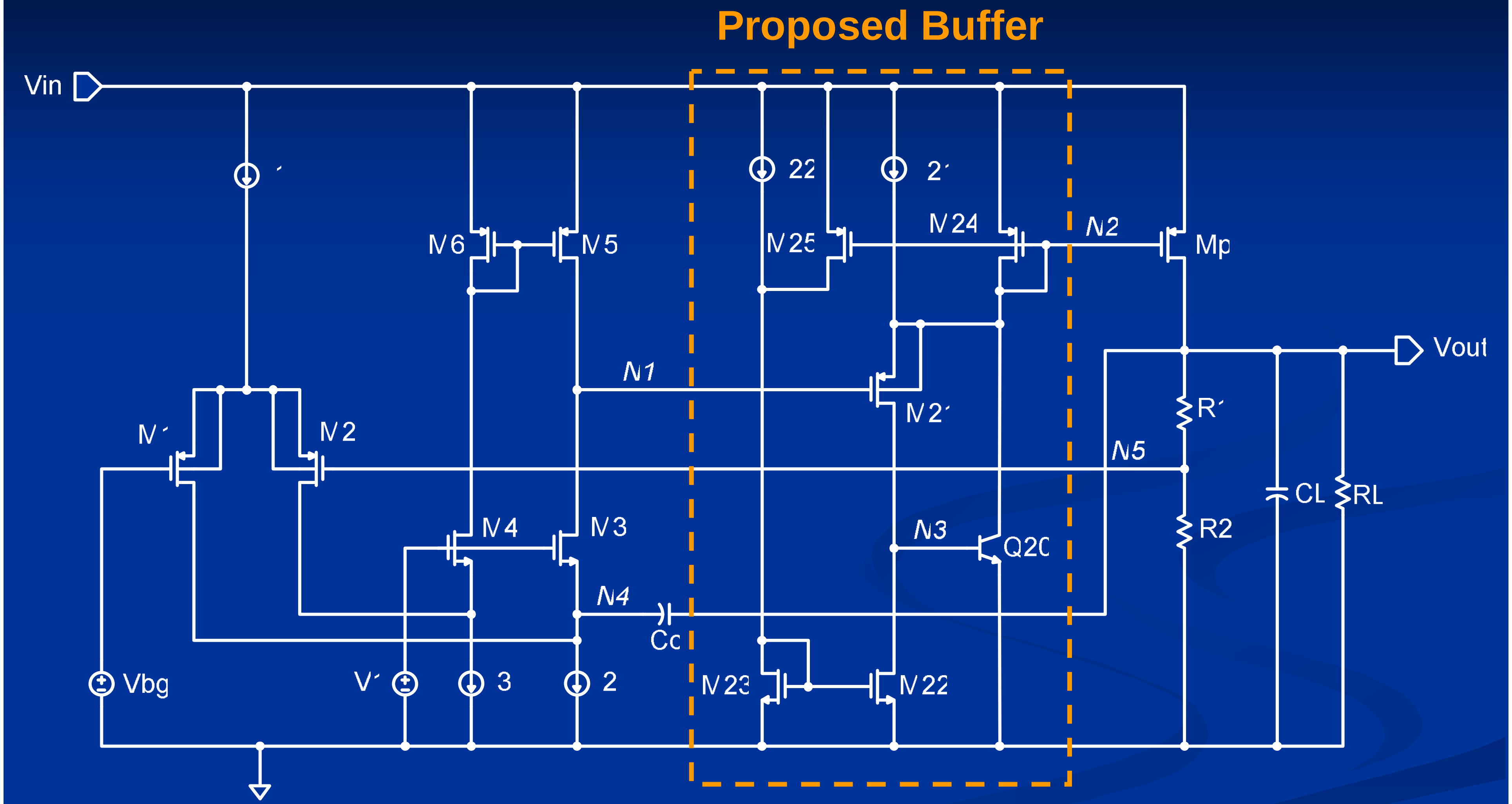
- The proposed LDO has two gain stages.
- Current-buffer compensation scheme for splitting P_1 and P_3 through C_c and M3.

LDO Bode Plots



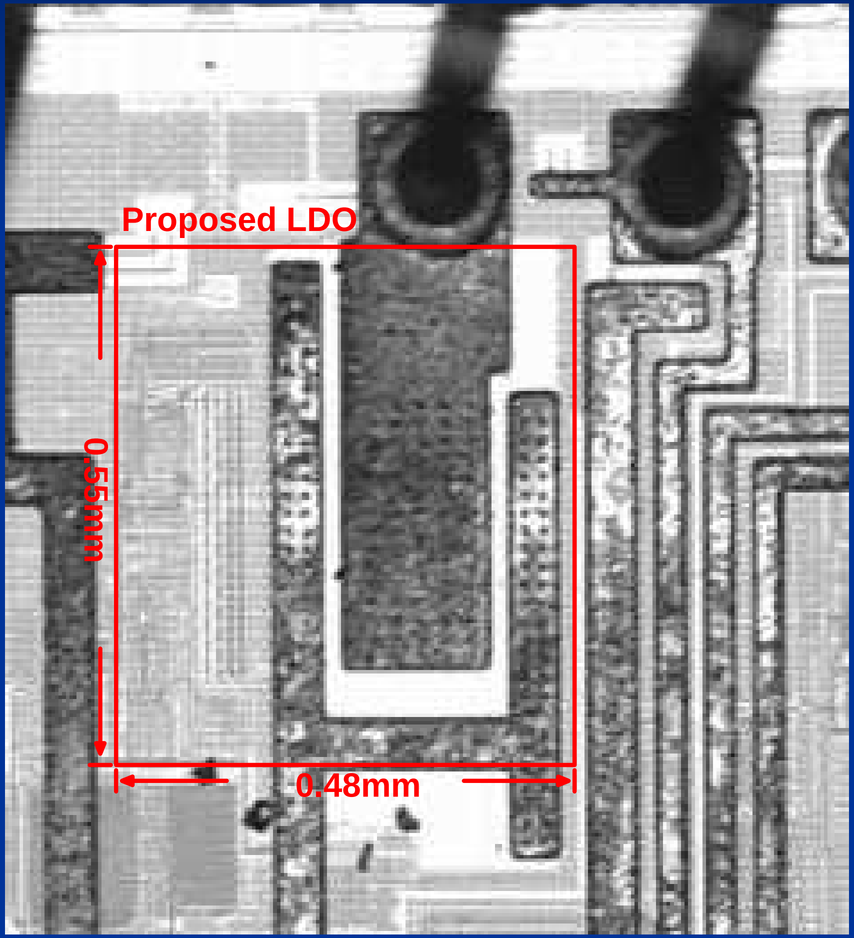
- First-order rolloff behavior under different load currents.
- Stability of the LDO is achieved.

LDO Schematic



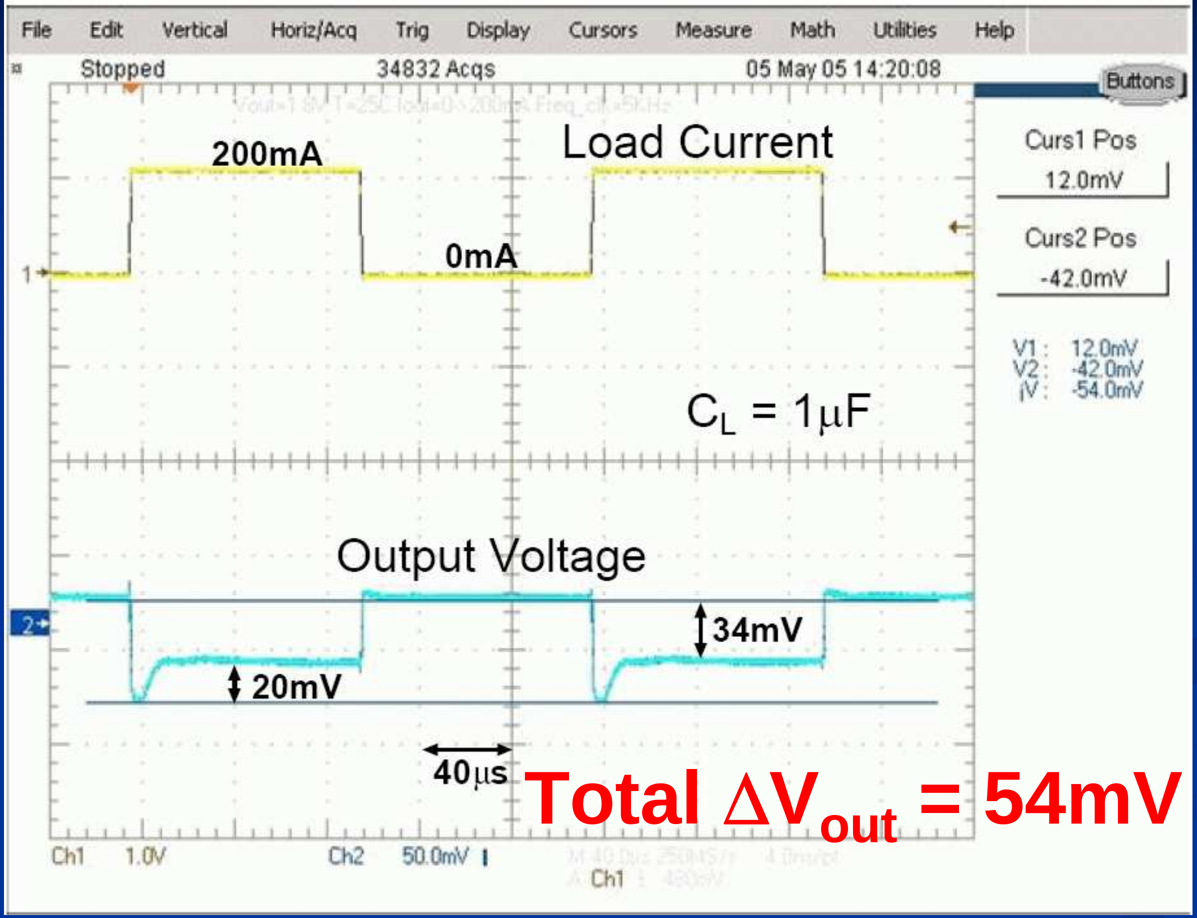
M. Al-Shyoukh, H. Lee, and R. Perez, “A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation,” *IEEE J. Solid-State Circuits*, to appear in Aug. 2007.

Micrograph of LDO



- LDO implemented in a 0.35µm CMOS process
- LDO area = 0.264 mm^2

Measured Load Transient Response



Curs1 Pos 12.0mV

Curs2 Pos -42.0mV

V1: 12.0mV

V2: -42.0mV

ΔV: -54.0mV

Total ΔV_{out} = 54mV

- **20mV undershoot under load step changes of 200mA/100ns.**

Performance Summary

Full Load Current	200 mA
I_q (no load)	20 µA
Output Capacitor	1 µF
Transient Response 0 – 200mA Step	Undershoot < 1% C_L = 1µF
DC Line Regulation ΔV_{in} = 3.5V	2 mV/V
DC Load Regulation 0 – 200mA	170 µV/mA (single bondwire)
Dropout Voltage (V_{do})	0.2 V
Die Area	0.264 mm^2
Technology	0.35 µm CMOS

Performance Comparisons of LDOs

	JSSC 1998 [1]	JSSC 2000 [2]	JSSC 2003 [3]	JSSC 2005 [4]	***This work***
Technology (μm)	2.0	1.0	0.6	0.09	***0.35***
V_{do} (V_{in}-V_{out}) (V)	0.3	N. A.	0.2	0.3	***0.2***
I_{omax} (mA)	50	200	100	100	***200***
I_q (mA)	0.023	0.030	0.038	6	***0.020***
Current Efficiency (%)	99.5	N.A.	99.96	94.3	***99.8***
ΔV_{out} (mV)	19	220	130	90	***54***
T_R (μs) $(C_L \cdot \Delta V_{out})/I_{omax}$	1.8	1.1	2	0.00054	***0.27***
C_L (μF)	4.7	1	10	0.00060	***1***
ESR Zero Required	No	Yes	Yes	No	***No***
FOM (ns) $T_R \cdot (I_q/I_{omax})$	8.2	0.165	4.9	0.032	***0.027***

Conclusions

- LDOs are widely-used inductorless dc-dc converters in portable equipment.
- Dynamically-biased shunt feedback is developed in the LDO to achieve stability and good load transient response while consuming small quiescent current and output capacitor under a wide range of load currents.