

A ROBUST FREQUENCY COMPENSATION SCHEME FOR LDO REGULATORS

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ABSTRACT

In the frequency compensation scheme of Low Drop Out (LDO) voltage regulators, a Zero generated by the series combination of load capacitor and its Electro Static Resistance (ESR) plays an important role. This frequency compensation tends to be inefficient, as we have to take into consideration a range of specified values for load capacitor and R_{ESR} , along with their variation with process and temperature. This paper presents a robust frequency compensation scheme that generates a Zero internally without relying on R_{ESR} of load capacitor. The proposed frequency compensation has better RF noise rejection, low power consumption and improved transient response. The LDO regulator is designed in 0.35 μ m TSMC technology.

1. INTRODUCTION

Low dropout voltage regulators have gained importance due to demand for power efficient circuits in mobile communications applications, which require increased battery life. While other classes of linear regulators (like NPN regulator) provide better transient response and more load current, low dropout regulators have the unique advantage of operating with very low ground currents and low input voltages.

When analyzing stability of an LDO regulator, the important difference to be noted (from other classes of linear regulators) is the fact that LDO regulator is not unconditionally stable for all loading conditions. A Zero created by the Electro Static Resistance (ESR) of the load capacitor is needed for the stability of the circuit. Therefore, the user is forced to use capacitors that have ESR in the range specified by the manufacturer.

Electrolytic, Tantalum or ceramic capacitors can be used as the load of LDO regulators. Electrolytic capacitors are not preferred because of their polarity and large variation of ESR with temperature. Tantalum capacitors are less desirable compared to ceramics because they are more expensive in the capacitance range

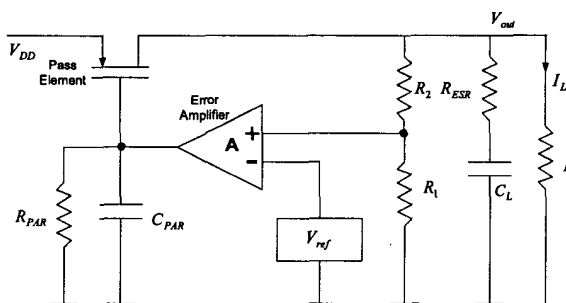


Figure 1: Typical LDO regulator structure.

of 1 μ F-10 μ F [2]. Ceramic capacitors are the best but have very low ESR values and hence cannot generate the Zero required for proper frequency compensation.

Though tantalum capacitors are typically used thus creating a Zero required for frequency compensation the problem of variation of this Zero with variation in load capacitor and R_{ESR} remains. A solution to this problem is to design an LDO regulator that doesn't need an output capacitor for stability [3]. However, that solution requires a charge pump circuit thereby greatly increasing the complexity.

In this paper we propose an LDO regulator topology that overcomes the mentioned drawbacks. The proposed regulator uses low-ESR multi layer ceramic load capacitors and is more robust compared to the existing schemes [5].

2. FREQUENCY RESPONSE OF A TYPICAL LDO VOLTAGE REGULATOR

The structure of a typical LDO regulator is shown in figure.1. The pole at the output node plays an important role when analyzing loop-gain transfer function for stability. Output impedance of PMOS transistor (called as pass element) varies a great deal since the current through it varies from a few microamperes (at no-load) to a maximum of few hundreds of milli amperes (at maximum load). The frequency of the pole at the output thus varies considerably. In most applications this pole is made dominant for all loads by using a very high capacitor whose value varies in the range of 1 μ F-20 μ F.

The next important pole to be considered is at the gate of the pass element. The size of the pass element needs to be large in order to drive large currents thus making the pole at its input significant. This pole could be pushed to higher frequencies by using a good buffer stage at the output of the error amplifier. In most cases we cannot push this pole to frequencies higher than unity gain frequency (UGF) of the loop-gain transfer function. It should also be noted that buffer stages take high currents for providing low output impedance.

Any other poles and/or zeros apart from the two mentioned above have to be kept at very high frequencies by proper design.

From the above discussion, we notice that we have a system with two poles occurring below UGF. The phase margin can become negative if phase contribution due to other parasitic poles is also taken into consideration. The system is therefore potentially unstable. The existing technique to overcome this problem is to generate a Zero utilizing ESR of the output capacitor. The product of output capacitance and R_{ESR} defines the frequency of the Zero. For a typical LDO regulator [6], the user can choose output capacitor from a wide range (1 μ F-20 μ F) and the ESR of this capacitor can also vary within a specified range (typically 50m Ω to 3 Ω). The variations can also occur with temperature and process variations. These variations vary the frequency of the Zero by as much as two decades (10Khz-1Mhz). Therefore, though manufactures ensure the stability of LDO regulators by specifying a range of values for output capacitor and its ESR, this is not a robust stabilization scheme. Another disadvantage is that the user is a part of the design process and requires knowledge of internal structure of LDO regulator to use it optimally.

3. PROPOSED TECHNIQUE

The requirement for the proposed improvement is the need to generate a Zero internally and get rid of the Zero due to output capacitor. Using multi layer ceramic load capacitor can eliminate the Zero at the output. The topology in figure.2 adds a zero in the loop gain function. An analysis of the modified transfer function gives us an idea of requirements to be met by the modified circuit. The voltage controlled current source shown in figure.2 has a transconductance that is ideally represented by $G_m(s) = sC_1$. However, for implementation sake, let us assume that this zero occurs at very low frequencies (not at the origin) and all parasitic poles are at very high frequencies.

$$G_m(s) = G_0 \left(1 + \frac{s}{\omega_{z1}} \right) \quad \omega_{z1} = \frac{G_{m0}}{C_1} \quad (1)$$

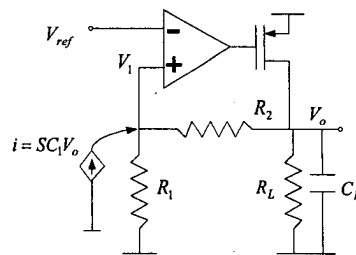


Figure2: An implementation that generates a zero in the loop gain function

G_0 is the DC conductance that should be extremely small (few hundreds of nA/V) such that DC output voltage of LDO regulator is not affected.

The loopgain transfer function of the modified system is given by

$$H(s) = \frac{A_0 \left(1 + \frac{s}{Z_1} \right)}{\left(1 + \frac{s}{P_1} \right) \left(1 + \frac{s}{P_2} \right)} \quad (2)$$

$$Z_1 = \frac{1}{R_2 C_1}, P_1 = \frac{1}{R_{out} \left(C_L - \frac{C_1}{\beta} \right)}, P_2 = \frac{1}{R_{par} C_{par}} \quad (3)$$

$$\beta = 1 + \frac{R_2}{R_1} \quad \text{and} \quad \frac{1}{R_{out}} = g_{dsp} + \frac{1}{R_L} + \frac{1}{R_1 + R_2}$$

- A_0 DC value of loopgain
- g_{dsp} Output conductance of PMOS pass element
- R_{out} Effective output impedance
- R_2, R_1, R_{par}, R_L and C_{par} are referred to figure.1.

The effect of the voltage controlled current source is to add a Zero and, to slightly change the dominant pole (P_1) frequency. This change in the frequency of P_1 is negligible since $C_L=2\mu$ F and $C_1=5$ pF. The Zero location has to be designed such that LDO regulator has a reasonable phase margin ($>45^\circ$) even with process variations.

4. IMPLEMENTATION IN CMOS TECHNOLOGY

The LDO regulator is designed in TSMC 0.35 μ m technology. It has a maximum output current capability of 50mA. The error amplifier used is a two-stage amplifier without any buffer stage. The accurate control over the compensating Zero location achieved through the new compensation scheme permits us to cancel the pole at the output of error amplifier with reasonable error. Therefore, the buffer stage, which was required in the previous schemes to push this pole to high frequencies (such that it is cancelled even in worst case value of compensating Zero), is no more required. This improves power efficiency significantly.

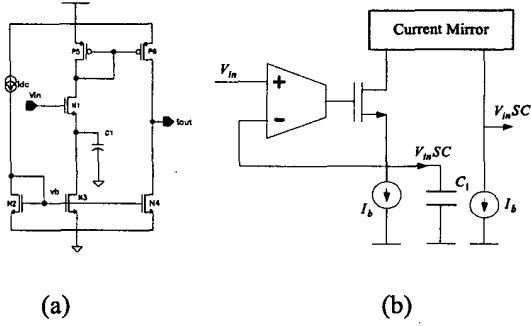


Figure3: (a) Simplest possible implementation of $G_m(s)$
 (b) Block diagram of improved implementation

4.1. Implementation of $G_m(s)$

Simplest possible transistor level implementation of $G_m(s)$ is shown in figure.3a. The transfer function of the transconductance is

$$G_m(s) = \frac{i_{out}}{v_{in}} = \frac{g_{ds3} \left(1 + \frac{sC_1}{g_{ds3}} \right)}{1 + \frac{sC_1}{g_{m1}}} \quad (4)$$

An important design consideration in the design of $G_m(s)$ is to have low bias currents in each branch such that overall power consumption is not affected. Therefore, each of the branches have $0.5\mu A$ DC current flowing through them. This means that value of g_m of the transistors will be very less. Therefore, the pole in equation.4 does not occur at very high frequencies as required. This pole occurs at around 100KHz. We should modify the topology to remove this disadvantage without increasing the bias currents. The modified topology is shown in Figure.3b wherein g_m is boosted by the auxiliary amplifier. The transistor level implementation is shown in figure.4. Use of cascode current mirror ensures that DC offset current is extremely low. The modified transconductance is given by

$$\frac{i_{out}}{v_{in}} = \frac{\frac{g_{ds7} g_{ds9}}{g_{m9}} \left(1 + \frac{sC_1}{\frac{g_{ds7} g_{ds9}}{g_{m9}}} \right)}{1 + \frac{sC_1}{\frac{g_{m3} g_{m2}}{g_{ds13}}}} \quad (5)$$

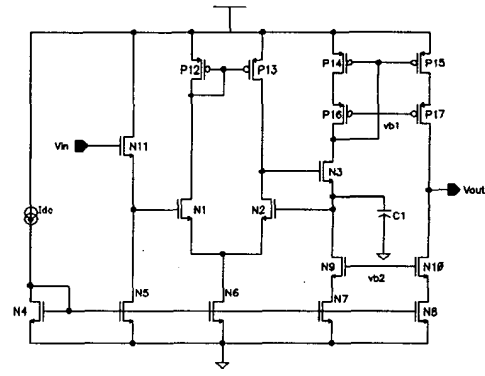


Figure4: Improved implementation of $G_m(s)$

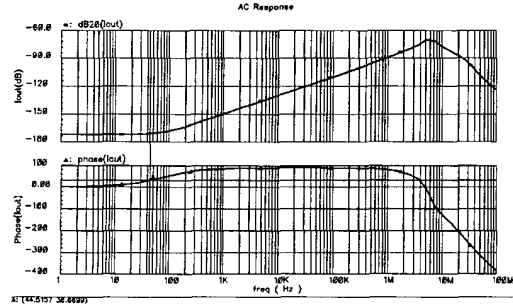


Figure5: Frequency characteristics of circuit in figure.4

We can see from equation.5 that the pole is moved to higher frequencies and Zero is moved to lower frequencies as desired. We observe from the frequency response (figure.5) that $G_{m0}=2.50nA/V$. The capacitor $C_1=5pF$. Assuming that the feedback resistor $R_2=160k\Omega$, the Zero in loopgain function, given by equation.3, appears at 200kHz. Since this Zero is well below UGF (typically few MHz) it serves the purpose. The upper limit of functionality of this circuit can be derived from the point where the effects of parasitic poles appear (around 2MHz in this case). We can move parasitic poles to higher frequencies by using proper design strategies. The total ground current taken by this circuit is below $5\mu A$. Since ground current of LDO is few hundreds of μA in typical commercial circuits [3], this ground current doesn't add much to the overall power consumption.

4.2. Basic functionality

To test the functionality of the proposed approach, loop gain of the system is plotted in figure.6 with and without $G_m(s)$ connected. This plot is taken for a load of 20mA. The simulation results included in this paper are from a prototype designed in the TSMC 0.35um process. The load capacitor is 2uF with zero ESR and the feedback resistors R_1 and R_2 are 120K and 160K, respectively. We can observe from the position of marker A and marker B that phase margin has increased to 52° from an original value of -6.6° .

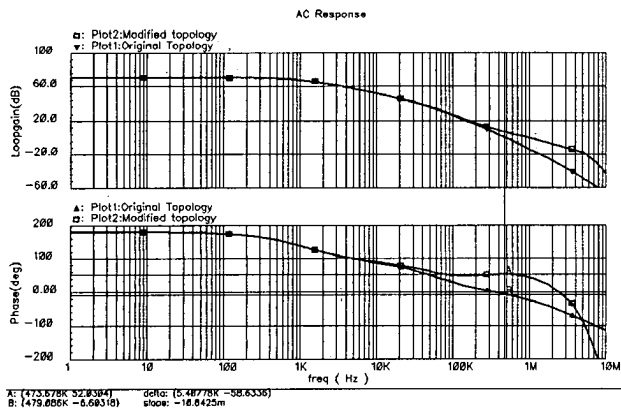


Figure6: Loopgain plot of LDO regulator with and without the suggested improvement.

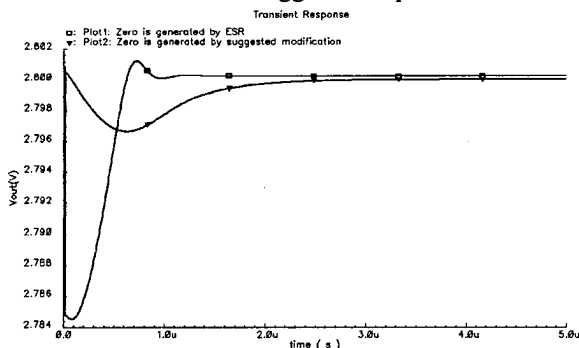


Figure7: Comparison of transient responses for original and improved cases.

4.3. Transient Analysis

A detailed description of transient analysis of LDO circuits can be found in [4]. For the purpose of this analysis, it is enough to know that the presence of ESR of capacitor would create a series voltage drop in the load transient conditions. This drop would remain till the transient current through capacitor becomes zero. Therefore, transient overshoot/undershoot is increased due to the presence of ESR of load capacitor. Figure.7 illustrates typical output voltages when load is switched from 0mA to 20mA with a rise time of 10nS. Plot.1 represents the case when the ESR of load capacitor generates Zero and plot.2 represents the case when Zero is generated by proposed scheme. R_{ESR} is adjusted to make the location of Zero in both cases equal. We observe that former case produces much higher undershoot voltage. The difference in the steady state DC values is because of the offset created by the addition of $G_m(s)$, but this error is well below 0.1%.

4.4. Noise Analysis

The general frequency range of interest for output noise of LDO regulators is from 10Hz-100KHz. Let V_{nl} represent

input referred noise of the compensating scheme. This noise referred to the output of the LDO is

$$V_{on} = \frac{s}{s + Z_1} V_{nl} \quad (6)$$

As we have seen from previous calculations, Z_1 is at 200KHz. Therefore most of the noise from $G_m(s)$ is rejected by the high pass behavior of the compensating scheme.

The high frequency noise generated by the regulator doesn't produce significant effects at the output of the regulator since low-ESR load capacitor acts as a short circuit from output node to ground at high frequencies. This is an improvement over the case when we have load capacitor with significant R_{ESR} .

4.5. Limitations

A possible disadvantage of the technique discussed is the extra area occupied by the capacitor used to implement the proposed scheme. Area occupied by the extra transistors needed to implement this technique is negligible. Another limitation is that we cannot use the regulator for low input voltages as we are using cascode current mirror stages in implementing $G_m(s)$. The cascode current mirrors can be replaced by simple current mirrors at the cost of increased DC errors that results from increased DC conductance of $G_m(s)$.

5. CONCLUSIONS

A robust frequency compensation technique for LDO regulators that also has lesser power consumption, better RF noise rejection and improved transient response, is proposed in this paper. This on-chip solution uses cheaper and compact multi layer ceramic capacitors as the load of the regulator and doesn't require the user to have knowledge of internal structure for achieving optimal performance.

6. REFERENCES

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