Low-Voltage CMOS Comparators With Programmable Hysteresis

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10th October, 2005 at 2:30 PM, Thomas & Brown, Room 108

ABSTRACT

This report describes the design and tradeoffs of the low-voltage CMOS comparators with and without hysteresis. Different types of comparators are discussed, mainly the three-stage comparator and folded-cascode comparator. It also discusses the advantages of comparators with programmable hysteresis. Optimizations are done in order to obtain minimum DC offsets. The input pulse frequency is 100 kHz. After Optimization, the comparator achieves reasonable gain with minimum delay. A method of adding programmable hysteresis is introduced and not found in the literature. The circuit is implemented in 0.5-micron technology with a ±1.25V power supply and 3-6µA of bias current. Simulation results using Cadence environment verify the functionality of the circuits. A chip prototype has been fabricated and experimentally verified. The circuit finds application in analog computation, detection of zero crossings, analog to digital and power management circuits.

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1. INTRODUCTION

Comparators, as the name suggests compares an analog signal with another analog signal and outputs a binary signal based on the comparison. The comparator can be thought of as a decision-making circuit. The comparator is widely used in the process of converting analog signals to digital signals. Since comparators are generally used in open loop mode, they can have very high open-loop gain. Comparators are generally classified as open-loop comparators and regenerative comparators. Open-loop comparators are basically operational amplifiers without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals.

Hysteresis is the quality of the comparator in which the input threshold changes depending on whether the input is rising or falling. In other words, hysteresis is the difference between the input signal levels at which a comparator turns off and turns on. A small amount of hysteresis can be useful in a comparator circuit because it reduces the circuit's sensitivity to noise, and helps reduce multiple transitions at the output when changing state. There are many ways to introduce hysteresis in a comparator. All of them use some type of positive feedback. The methods can be categorized into external methods and internal methods. External hysteresis uses external positive feedback and internal hysteresis is implemented inside the comparator. Several comparators with and without hysteresis were discussed and compared with respect to delay, offset, gain and power dissipation. The complete transfer curve of the circuit is shown in the figure 1.1 below.

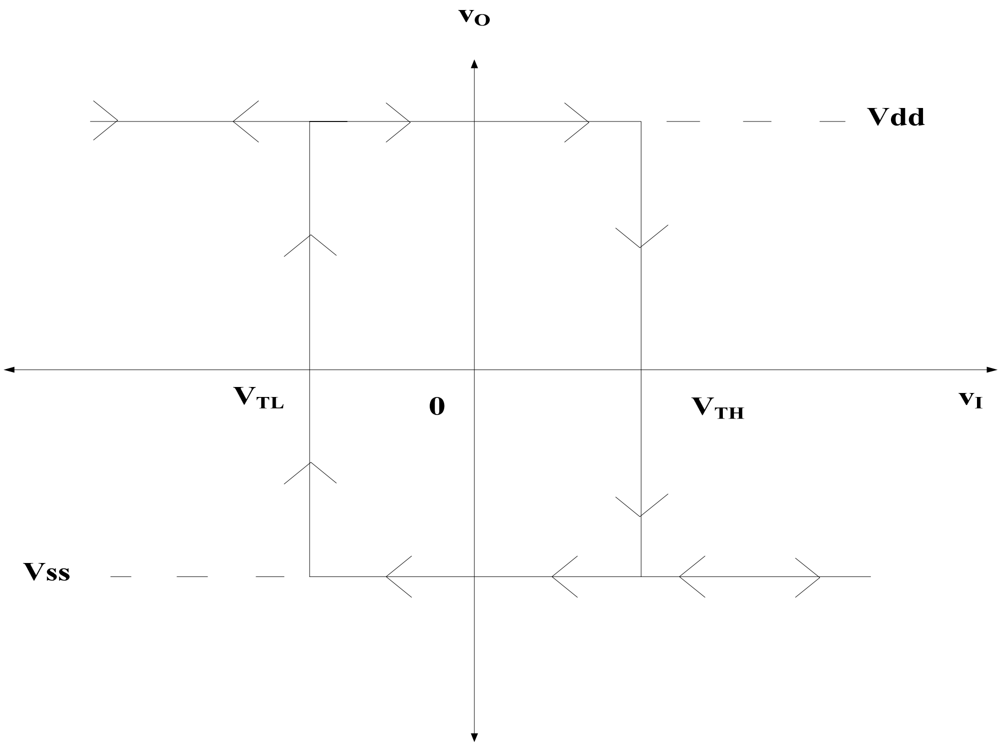


Figure 1.1 Transfer curve of the comparator with hysteresis

Original contributions in this report are:

- One method of adding programmable hysteresis is new and not found in the literature.
- Greatly increased offsets observed in folded-cascode comparator, as compared to three-stage comparator.

In chapter 2, we will discuss the background of comparators, hysteresis and its implementation, two-stage comparators and high performance comparators.

In chapter 3, the design and simulation of comparators with and without hysteresis in the AMI 0.5 μm technology is discussed. Low offset, low delay, high gain and low power dissipation were the main objectives in this design. The circuits are optimized to achieve these goals. The results of simulations are also provided.

Chapter 4 discusses the comparison of simulation results and test results. It also discusses the layout aspects of the comparators and test setups for finding delay, offset and the amount of hysteresis. In addition, we present a model to attempt to explain the large offsets observed in the folded-cascode comparator.

In chapter 5, a summary of the results obtained in measurements and simulatons are provided, along with some applications of comparators. Further extension of this work is also discussed in this chapter.

2. COMPARATORS AND HYSTERESIS

2. Comparators

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on comparison. A simple comparator is an op-amp without compensation. Comparators are generally used in open-loop mode and so it is not necessary to compensate the comparator. Since no compensation is needed, it has the largest bandwidth possible which gives a faster response. In this chapter, we will discuss the background of comparators, hysteresis, two-stage comparators and high performance comparators.

2.1 Introduction

The comparator can be thought of as a decision-making circuit. If the positive input of the comparator is at a greater potential than the negative input, the output of the comparator is at logic 1, whereas if the positive input is at a potential less than the negative input, the output of the comparator is at logic 0. The circuit symbol of the comparator is shown below in figure1.

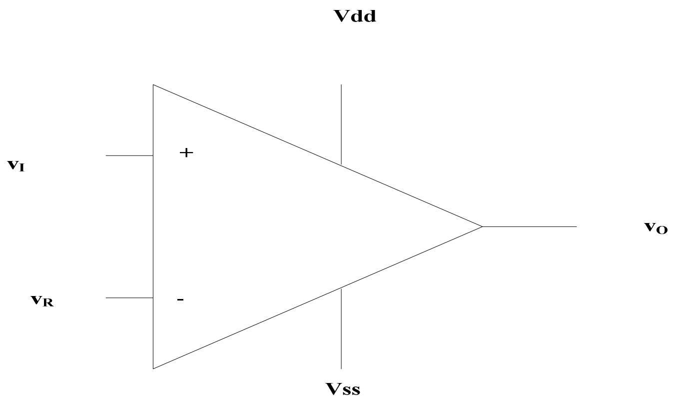


Figure 2.1: circuit symbol of the comparator

Comparators generally are designed to operate more optimally than op-amps in digital applications, in that comparator output voltages will go very close to the power supply voltage rails and their outputs will swing between these rails very fast , that is they have a very high slew rate.

2.2 Characterization of the comparator

<u>Gain</u>: The gain of the comparator is the derivative of the dc transfer curve at $v_I \sim v_R$. The transfer curve of an ideal comparator with infinite gain is shown below.[2]

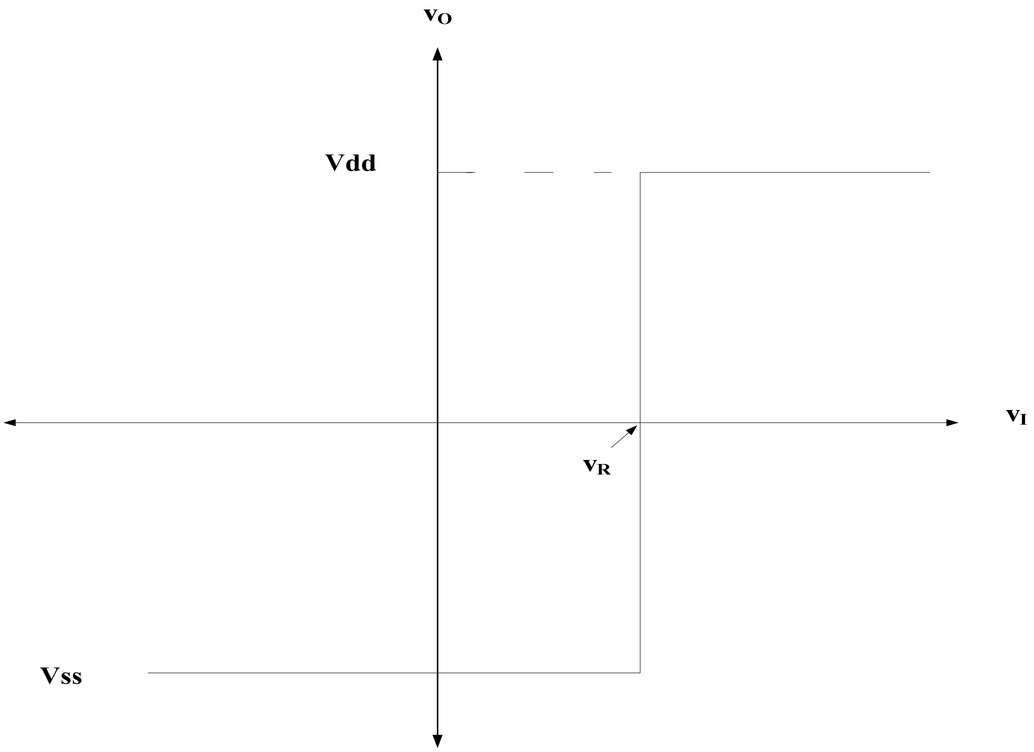


Figure 2.2: Transfer curve of an ideal comparator with infinite gain

The output equations for an ideal comparator can be defined as follows.

$$v_O = Vdd \text{ if } v_I > v_R \qquad \textbf{(2.1)}$$

$$= Vss \text{ if } v_I < v_R$$

A comparator with infinite gain is not realizable. Figure 3 shows a more realistic piecewise linear transfer curve of a comparator.

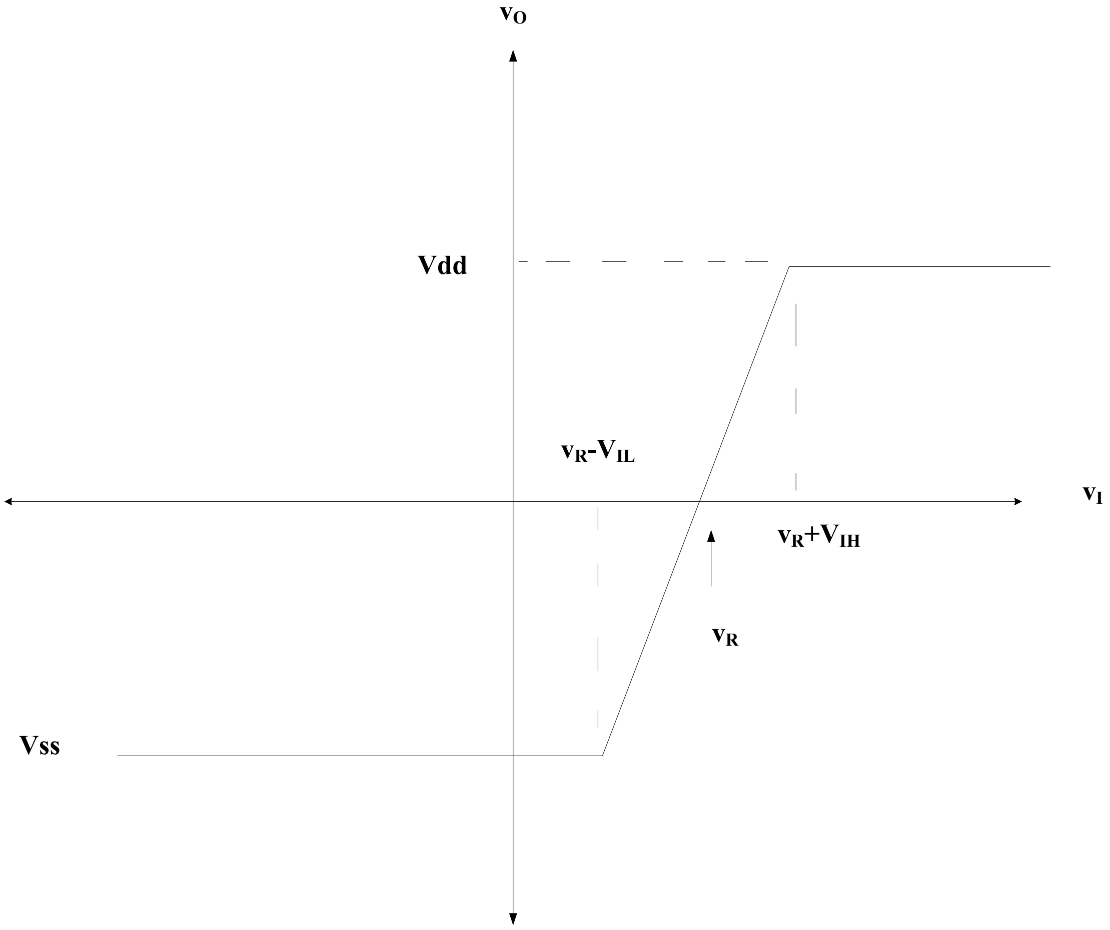


Figure 2.3: Transfer curve of the comparator with finite gain

The output equations can be defined as follows

$v_O = Vdd$ if $v_I > v_R + V_{IH}$

$= Vss$ if $v_I < v_R - V_{IL}$ **(2.2)**

$= A_V\ v_I$ if $V_{IL} < v_I < V_{IH}$ Where A_V is the non-infinite gain.

Propagation delay: The time difference between the input crossing the reference voltage and the output changing the logic state is defined as the propagation delay.[2]

t_{LH} = The delay time between the input crossing v_R i.e.,0V and the output switching the levels i.e., 0V when the output is changing from low to high.

t_{HL} = The delay time between the input crossing zero volts and the output switching the levels i.e., 0V when the output is changing from high to low..

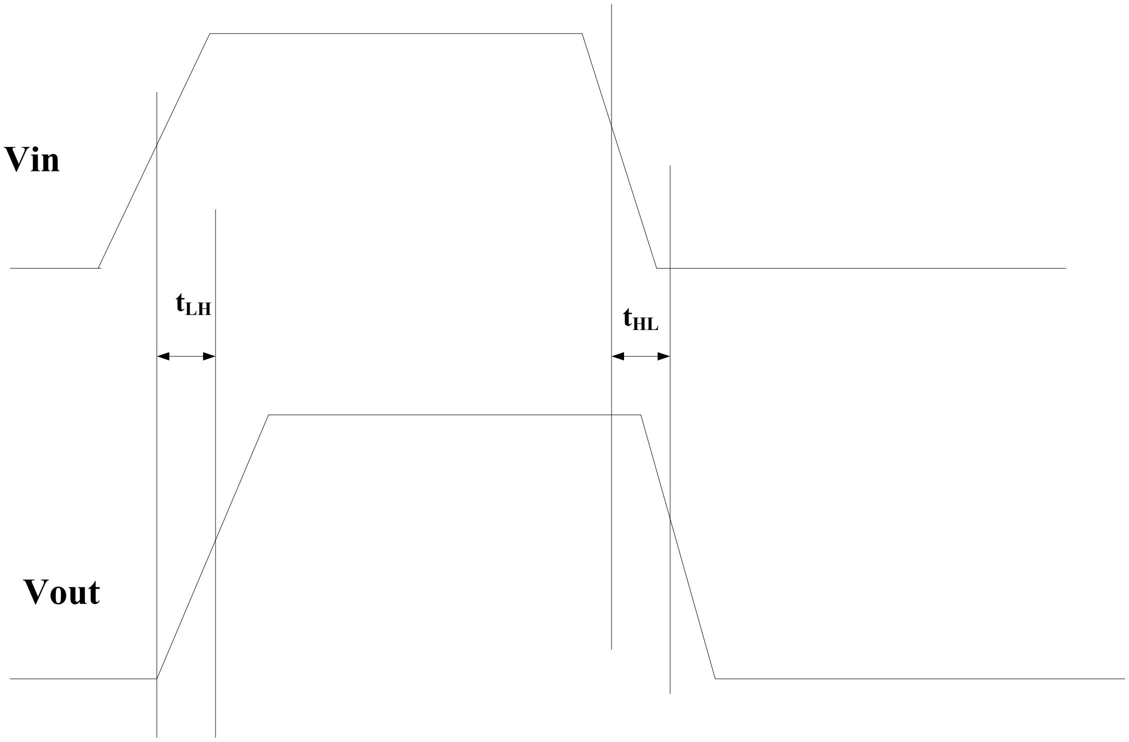


Figure2.4: propagation delay definition for a comparator

The propagation delay time of the comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. Generally, the delay of a comparator is less than that of an op-amp. The delay of the comparator is reduced by cascading several low-gain stages. In other words, the delay of a single high-gain stage is in general longer than the delay of several low-gain stages.

Input offset: Another important characteristic of the practical comparator is the presence of an input offset. The difference between the input voltages v_I - v_R, at the instance where output voltage v_O equals zero volts is defined as the input offset voltage. Offset varies from comparator circuit to comparator circuit. [2]

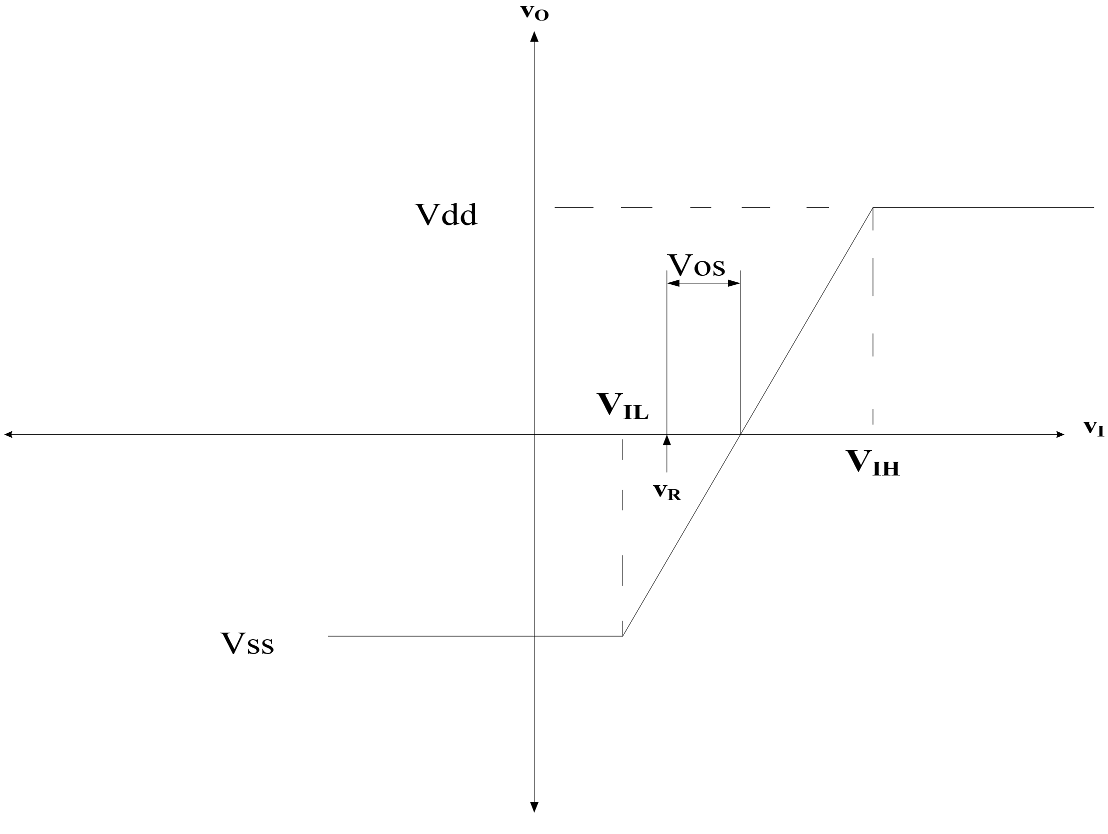


Figure 2.5: Transfer curve of the comparator including input offset voltage

The equation can be defined as follows:

For particular v_R , $Vos = v_I - v_R$ such that $v_O = 0$ V. **(2.3)**

2.3 Hysteresis

One problem with comparators is that the input signal is often corrupted with noise and/or may be very slowly changing. When the input voltage is close to the reference voltage, a little bit of noise can make the input voltage vary to values just above or below the reference voltage. This noise can cause output glitches that consume a lot of power. In such applications, it is useful to add hysteresis to the comparator's dc transfer curve. To demonstrate the need for hysteresis, consider the common application of comparators as a zero-crossing detector. Assume the signal to be processed has high frequency interference (noise) superimposed on it. When detecting the zero-crossing points of a signal, we will get errors since the signal may cross the zero axes several times for signals near zero due to the noise signal. The response of the comparator to a noisy input signal without hysteresis is shown in the figure 6 below.

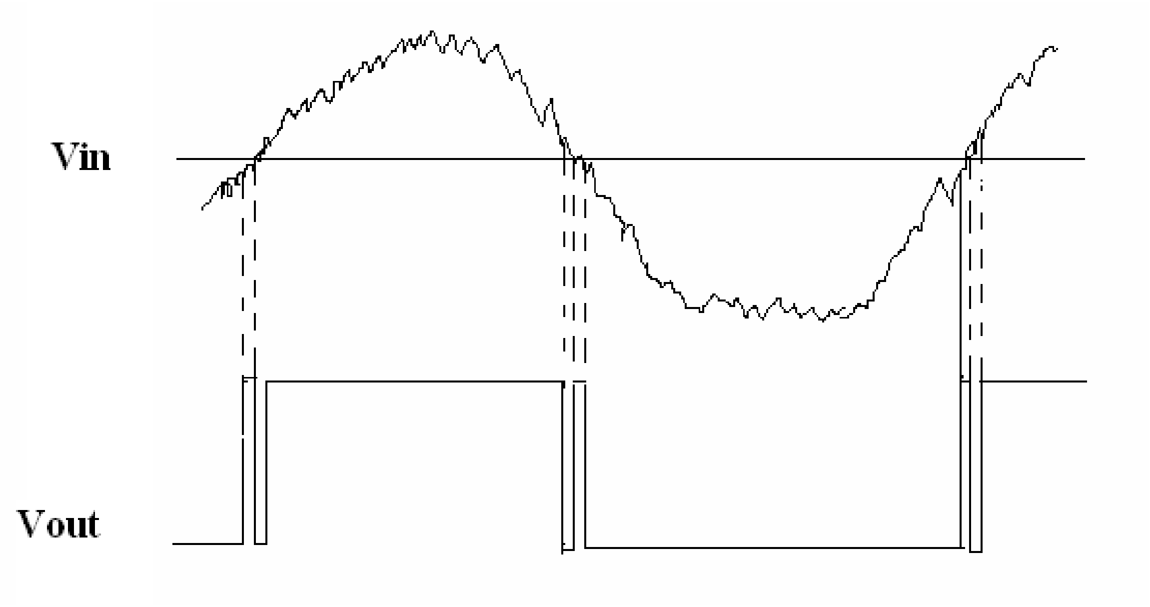


Figure 2.6: Comparator response to a noisy signal without hysteresis

The response of the comparator to a noisy input when hysteresis is added is shown in the figure 7 below.

Vth = upper threshold voltage

Vtl = lower threshold voltage

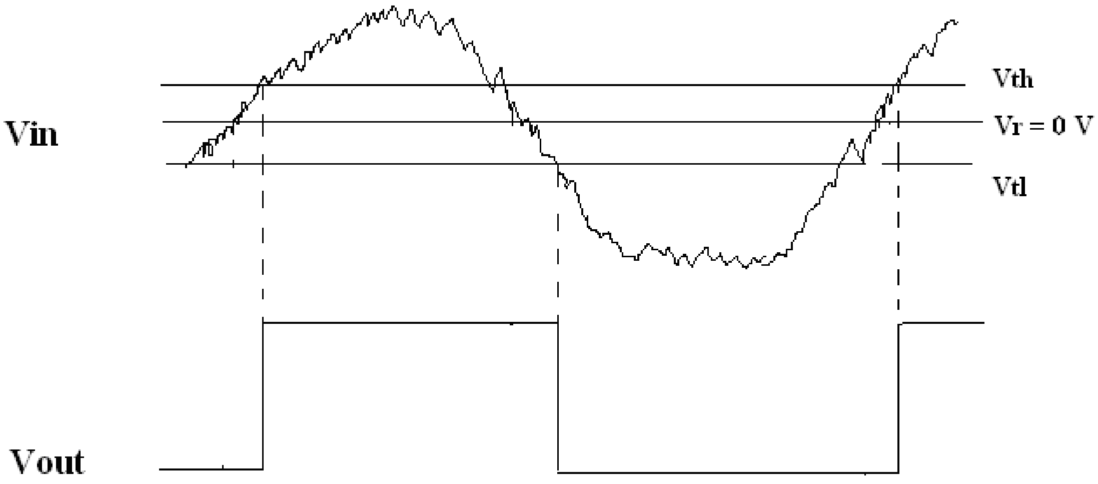


Figure2. 7: Comparator response to a noisy signal after adding hysteresis

If the peak-to-peak amplitude of the noise is known, the problem can be eliminated by placing two thresholds of the comparator on either side of the zero crossings, separated by the magnitude of the noise. Hysteresis is the quality of the comparator in which the input threshold changes depending on whether the input is rising or falling.

2.4 Implementation of hysteresis

Hysteresis can be implemented by the circuit shown below.[1]

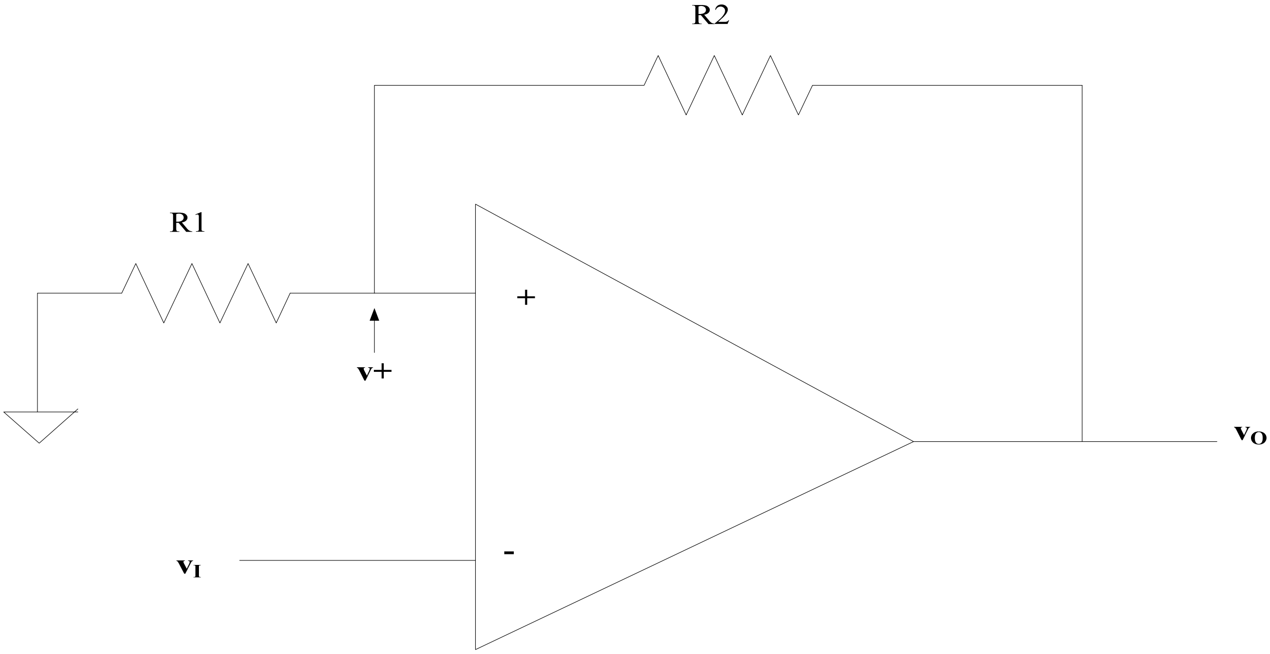


Figure 2.8: circuit for implementing hysteresis using a positive feedback resistive network

Input v_I is applied to the inverting input terminal of the comparator. Assuming that v_O is at one of the two possible levels, say Vdd, then

v+ = βVdd where $\beta = \dfrac{R1}{R1 + R2}$

As v_I increased from zero volts, nothing happens until v_I reaches a value equal to v+. As v_I exceeds this value, a net negative voltage develops between the input terminals of the comparator. This voltage is amplified by the open loop gain of the comparator and thus v_O goes negative. The voltage divider in turn causes v+ to go negative, thus increasing the net negative input to the comparator and keeping the regenerative process going. This process ends in the comparator saturating in the negative direction; that is v_O = Vss and, correspondingly, v+ = βVss. Increasing v_I further has no effect on the acquired state of the circuit. This circuit is sometimes called bi-stable circuit because it has two stable states. It can be observed that the characteristic is that of a comparator with a threshold voltage V_{TH}

Where V_{TH}= βvdd where $\beta = \frac{R1}{R1+R2}$ **(2.4)**

Now v+ = βVss. As v_I is decreased, circuit remains in a negative-saturation state until v_I goes negative to the point that it equals βVss. As v_I goes below this value, a net positive voltage appears between the comparator's input terminals. This voltage is amplified by the comparator gain and thus gives rise to a positive voltage at the comparator's output. The regenerative action of the positive feedback loop then sets in and causes the circuit eventually to go to its positive-saturation state, in which v_O = Vdd and v+ = βVdd. The transfer characteristic of the decreasing v_I is shown in the *figure 10* below. It can be observed that the characteristic is that of a comparator with threshold voltage V_{TL}

Where V_{TL} = βVss where $\beta = \frac{R1}{R1+R2}$ **(2.5)**

The complete transfer curve of the circuit is shown in the figure 9 below.

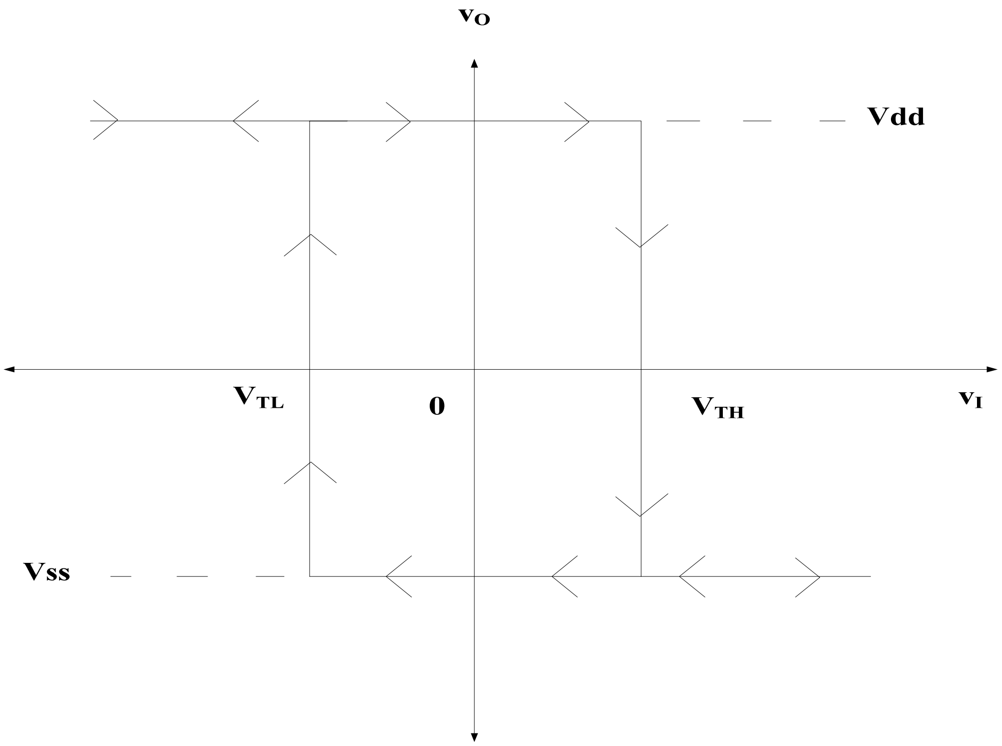


Figure2. 9: Complete transfer curve of the comparator circuit with hysteresis for increasing and deceasing v_I

The circuit changes state at different values of v_I depending on whether v_I is increasing or decreasing. Thus the circuit is said to exhibit hysteresis. The amount of hysteresis is the difference between the high threshold V_{TH} and low threshold $V_{TL.}$ This bi-stable circuit is in effect a comparator with hysteresis. As the bi-stable circuit switches from a positive state to a negative state as v_I in increased past the positive threshold voltage $V_{TH,}$ the circuit is said to be inverting. The input v_I can also be referred to as trigger signal. Schmitt triggers can be thought of as a comparator with hysteresis.

2.5 Comparator with hysteresis with non-inverting transfer curve

The input signal is applied to the positive terminal. The circuit is shown in the figure 11 below.

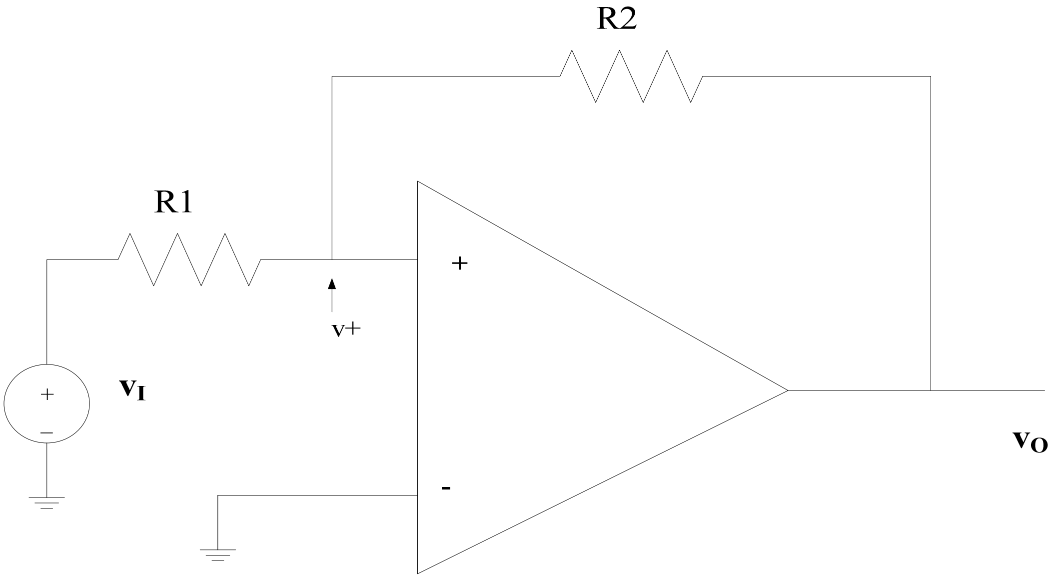


Figure 2.10: circuit (non-inverting) for implementing hysteresis

Applying superposition to the linear circuit formed by R1 and R2, v+ can expressed in term of v_I and v_O as

$$v+ = v_I \frac{R2}{R1+R2} + v_O \frac{R1}{R1+R2} \qquad \textbf{(2.6)}$$

If the circuit is in positive stable state, positive values of v_I will have no effect. To trigger the circuit into the negative stable state, v_I should be made negative. The low threshold can be found by substituting v_O = Vdd, v+ = 0 and v_I = $V_{TL.}$

$$V_{TL} = -\text{Vdd} * \frac{R1}{R2 + R1} \qquad \textbf{(2.7)}$$

Similarly the high threshold voltage can be found as

$$V_{TH} = -\text{Vss} * \frac{R1}{R2} \qquad \textbf{(2.8)}$$

The complete transfer characteristic is shown in the figure 12 below. These characteristics can also be referred as non-inverting characteristics because positive triggering signal v_I of value greater than V_{TH} causes the circuit to switch to the positive stable state.

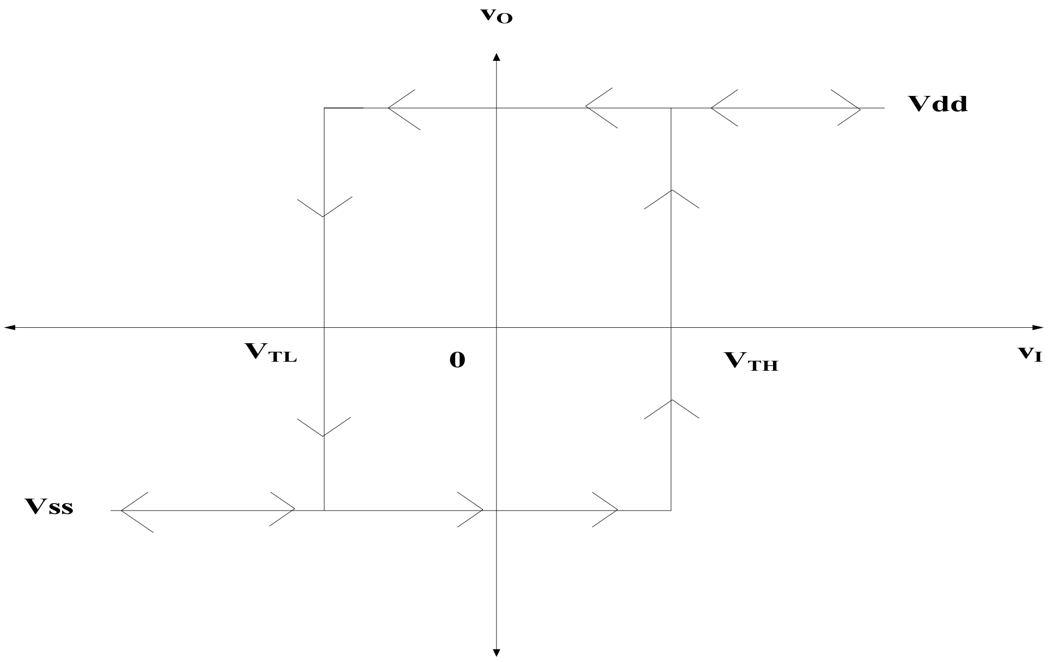


Figure 2.11: complete transfer curve of a non-inverting comparator circuit with hysteresis

2.6 Two-stage comparator

A two stage CMOSop-amp acts as a comparator if there is no compensation. Comparators are generally used in open-loop mode and so it is not necessary to compensate the comparator. Since no compensation is needed, it has the largest bandwidth possible which gives a faster response. A simple two stage comparator is an op-amp without compensation. Because speed is so important relative to the gain, typically l is not as large for comparators as for op-amps. The schematic of the two-stage comparator is shown in the figure 12 below. [5]

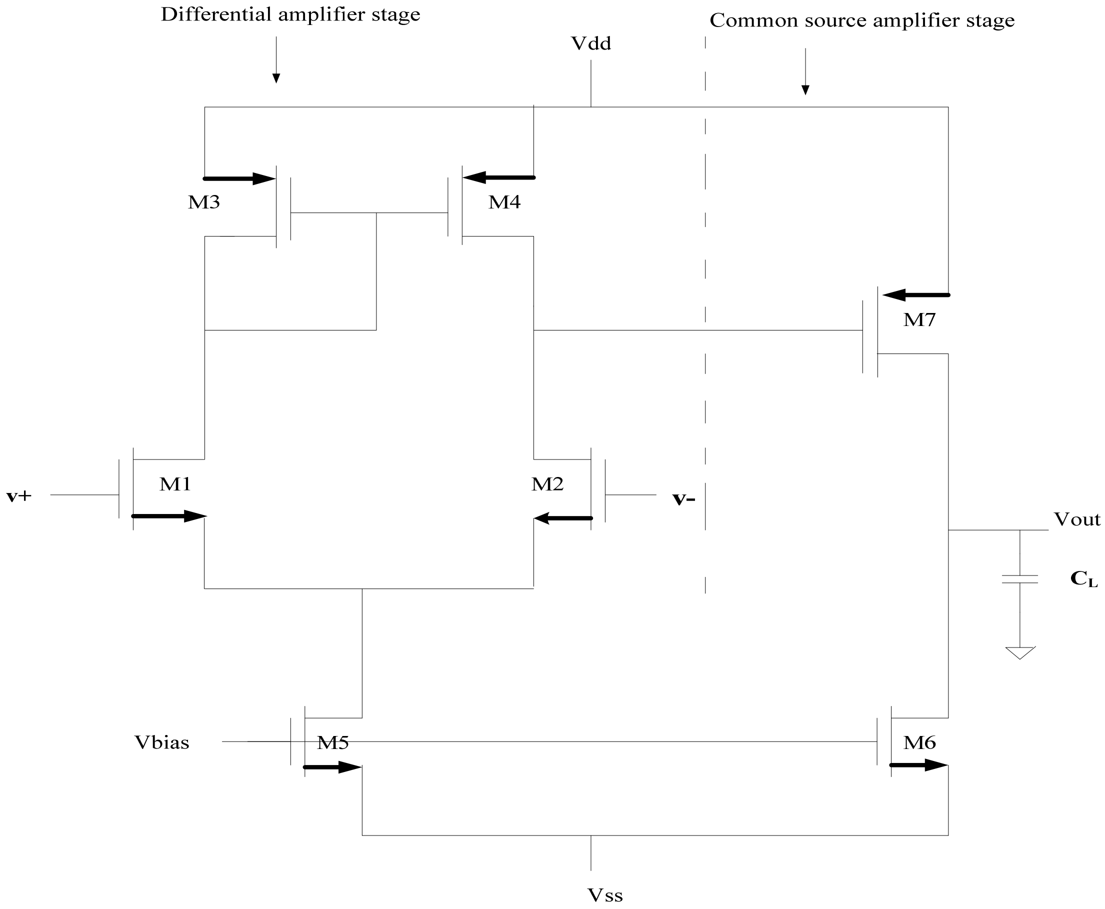


Figure2. 12: schematic of a two-stage comparator

It consists of two stages, a differential amplifier stage and common source amplifier stage. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current mirror load resulting in a single-ended output voltage. M1 and M2 form the differential pair with M3 and M4 transistors form the active load. The second stage consists of a common-source amplifier converting the second stage input voltage to a current. This transistor is loaded by a current-sink load, which converts the current to a voltage at the output node. The transistor M5 provides the bias current for the differential pair. Assuming a strictly capacitive load, the overall dc gain of the two-stage comparator is given by the equation

$$A_v = (g_{m1} * r_{02} \parallel r_{04}) (g_{m6} * r_{06} \parallel r_{07}) \qquad \textbf{(2.9)}$$

Where g_{m1} = transconductance of the M1 transistor.

g_{m6} = transconductance of the M6 transistor.

$r_{02} \parallel r_{04}$ = output resistance of the first stage.

$r_{06} \parallel r_{07}$ = output resistance of the second stage.

Slew rate (SR) is defined as the maximum rate at which the load capacitance can be charged. The slew rate of this circuit is given by the equation

$$SR = \frac{I_{BIAS}}{C_L} \qquad \textbf{(2.10)}$$

Where I_{BIAS} is the bias current of the circuit and C_L is the load capacitance.

2.7 High performance comparator

A block diagram of a high-performance comparator is shown in the figure 13 below. The comparator consists of three stages.[2]

1. Input preamplifier stage
2. Positive feedback or decision stage
3. An output buffer stage

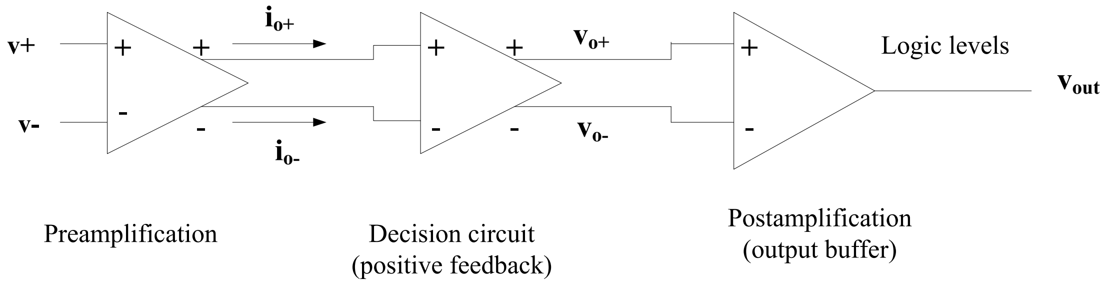


Figure 2.13: Block diagram of high-performance voltage comparator

<u>*Preamplification stage*</u>: The preamp stage amplifies the input signal to improve the comparator sensitivity. i.e., increases the minimum input signal with which the comparator can make a decision and isolates the input of the comparator from switching noise coming from the positive feedback stage. The schematic of the preamplification stage of the comparator is shown in the figure 14 below. It consists of the differential amplifier with active loads.

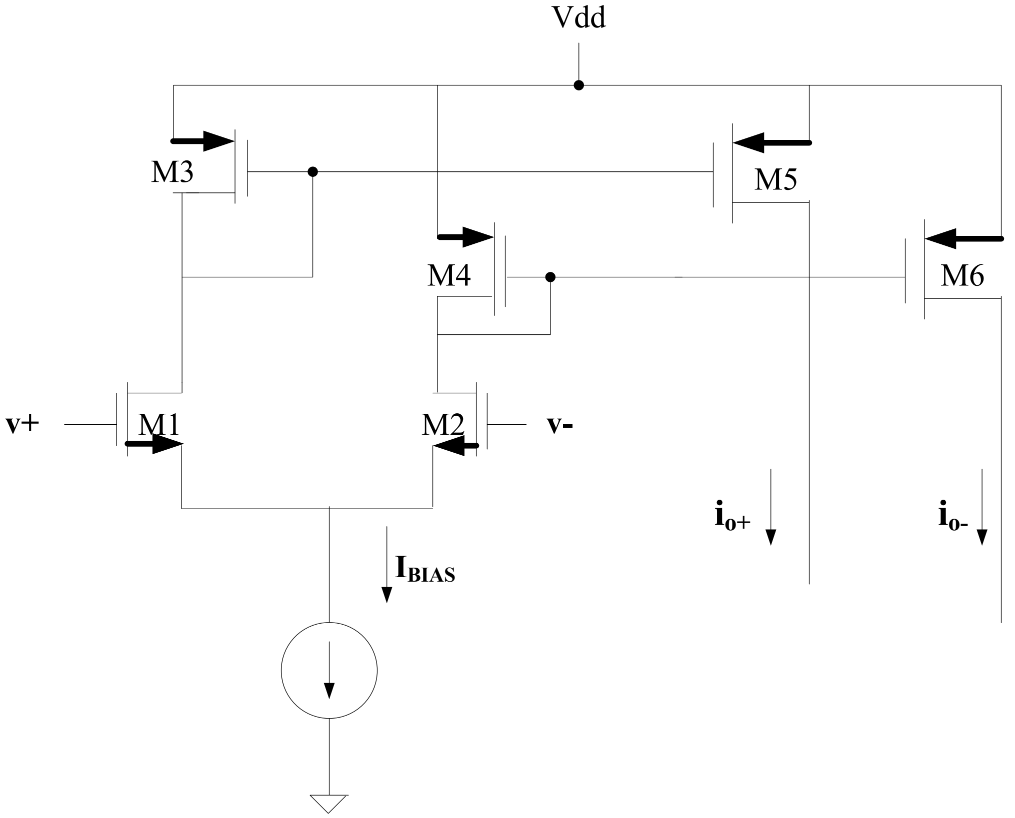


Figure 2.14: preamplification stage of the comparator

<u>Decision stage</u>: The decision stage is the heart of this comparator and is used to determine which of the input signals is larger. The schematic of the decision stage of the comparator is shown in the figure 14 below. This circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element. Hysteresis can be part of the design in the decision circuit.

Assuming that $i_{o+} > i_{o-}$, M5 and M7 are on and M6 and M8 are off. Also assume that $\beta_5 = \beta_8 = \beta_A$ and $\beta_6 = \beta_7 = \beta_B$ where β_5, β_6, β_7, β_8 are the transconductance parameters of the transistors M5, M6, M7 and M8 respectively. Under these assumptions, v_{o-} is approximately 0 V and v_{o+} is

$$v_{o+} = \sqrt{\frac{2i_{0+}}{\beta_A}} + V_{THN} \qquad \textbf{(2.11)}$$

If i_{o-} is increased and i_{o+} is decreased, switching takes place when the drain-source voltage of M7 is equal to V_{THN} of M6. So M6 turns on and M7 shuts off.

At this point, i_{o-} is given by

$$i_{o-} = \frac{\beta_B}{\beta_A} * i_{0+} \qquad \textbf{(2.12)}$$

A similar analysis for increasing i_{o+} and decreasing i_{o-} yields a switching point of

$$i_{o+} = \frac{\beta_B}{\beta_A} * i_{0-} \qquad \textbf{(2.13)}$$

The circuit can be designed to add hysteresis to it. But the major disadvantage of this comparator is the hysteresis cannot be made programmable.

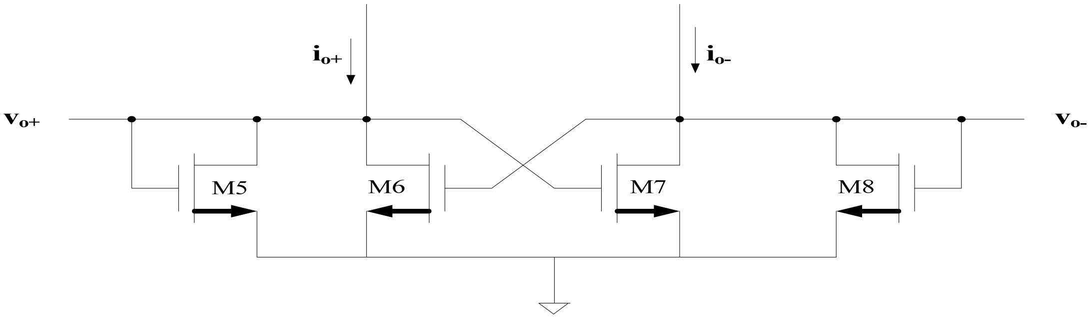


Figure 2.14: positive feedback decision circuit

Output buffer stage: This stage is also called postamplifier stage. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal.

3. DESIGN AND SIMULATIONS

This project describes the issues and tradeoffs in the design of voltage comparators with and without hysteresis. Different types of comparators were discussed. The main objective is to design a comparator with low delay, low offset, high gain and low power dissipation. The circuit is implemented in 0.5 -μm technology. Six different types of comparators were designed: two were designed without hysteresis and four were designed with hysteresis. These are:

1. Three-stage comparator.
2. Three-stage comparator with internal hysteresis.
3. Three-stage comparator with external hysteresis.
4. Folded-cascode comparator.
5. Folded-cascode comparator with internal hysteresis.
6. Folded-cascode comparator with external hysteresis.

3.1 Three-stage comparator

The three-stage comparator consists of three stages. The first stage is a differential amplifier stage, the second stage is a common source amplifier stage and the third stage is an inverter (buffer) stage. In this circuit, the bias current is set at 1µA. The circuit utilizes two power supplies, ± 1.25V. There are two input voltages, V_{iplus} and V_{iminus}. The reference voltage in this circuit is V_{iminus}. The block diagram is shown in figure 3.1.

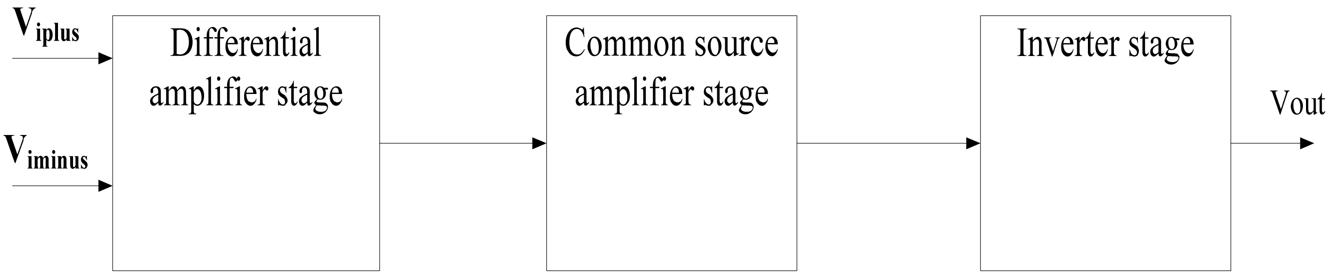


Figure 3.1: Block diagram of the three-stage comparator

The schematic of the three-stage comparator is shown in figure 3.2.

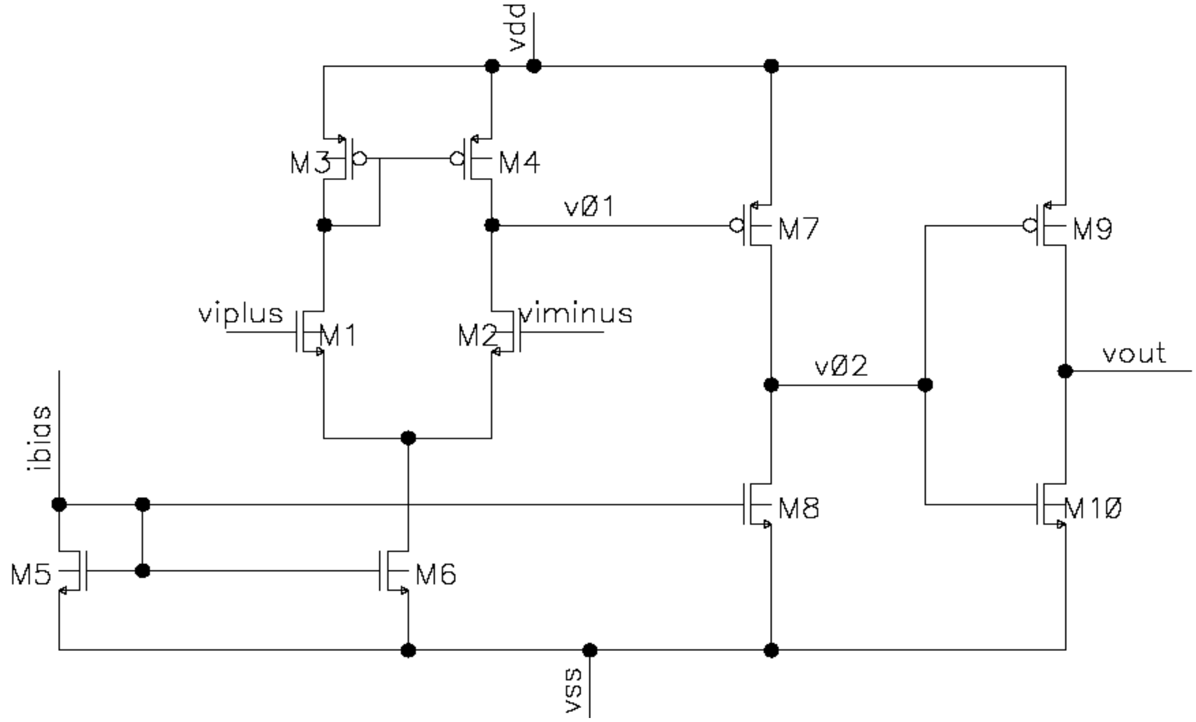


Figure 3.2: Schematic of three-stage comparator without hysteresis

The current mirror formed by transistors M5 and M6 supplies the differential pair M1-M2 with bias current. The input differential pair is actively loaded with the current mirror formed by the transistors M3 and M4. The second stage which is a common source amplifier is actively loaded with the current source transistor M7. The common-source amplifier is commonly used to increase the gain. The third stage which consists of the inverter is used to increase the gain and to improve the slew-rate at the output node

3.1.1 Sizes of the transistors

Speed is given more importance than gain in the comparator design. So the length of the transistors is chosen as 1.2µm. The bias current I_{bias} is set at 1µA.The sizes of the transistors M5 and M6 which form the current mirror are found by the equation

$$I_{bias} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_T)^2 \qquad \textbf{(3.1)}$$

The following assumptions are made in this comparator design:

$V_{GS}-V_T = V_{DSsat} = 0.2\text{V}$

$\mu_n C_{OX} = 110\frac{\mu A}{V^2}$

After substituting the values in equation 1, we get W=0.54µm and L= 1.2µm.

Since good matching is needed, the sizes of the transistor M5 and M6 are chosen as :

W = 5.4µm and L = 1.2µm with multiplier m=2. 0.5µA current flows through transistors M1 and M2 which form the differential pair. Following the equation 1, the sizes of W and L are obtained. Since more area is needed for the differential pair transistors to get better matching and higher g_m which would result in higher gain, the sizes are chosen as W =

5.4µM and L = 1.2µm with multiplier m = 4. The sizes of the transistors, M3 and M4, which act as active load for the differential pair, should be made twice that of the differential pair transistors. The size of the current source transistor M7 should be made twice that of the transistor M4. But since large gate-to-source capacitance of M7 causes a delay from the input of the differential pair to the gate of transistor M7, the area of the transistor M7 is reduced. In particular L is chosen as 0.9µm and W is chosen as 5.4µm with m=4. By adjusting the size of the transistor M7, the delay was reduced by as much as 40%. Transistors M9 and M10, which form the inverter, are made small since no matching is needed. Since the size of the PMOS transistor should me made twice that of the NMOS transistor, the sizes of the M9 and M10 are chosen as W = 5.4µm, L = 0.6µm,m = 2 and W = 5.4µm, L = 0.6µm, m = 1, respectively. DC analysis and transient analysis are performed on this circuit.

3.1.2 DC analysis

V_{iminus}, the reference voltage is connected to ground. V_{iplus}, the other input voltage is varied from -500µV to 500µV. The circuit utilizes two power supplies ± 1.25V. An external capacitance of 33fF is connected at the output. Then the transfer characteristic of *vout* versus the input V_{iplus} is observed. The plots are shown in figure 3.3.

The gain and offset are measured from the plot as 34kV/V and 140µV respectively. Gain is measured by determining the slope of the curve. Offset is measured by determining the input voltage at which output goes to zero Volts.

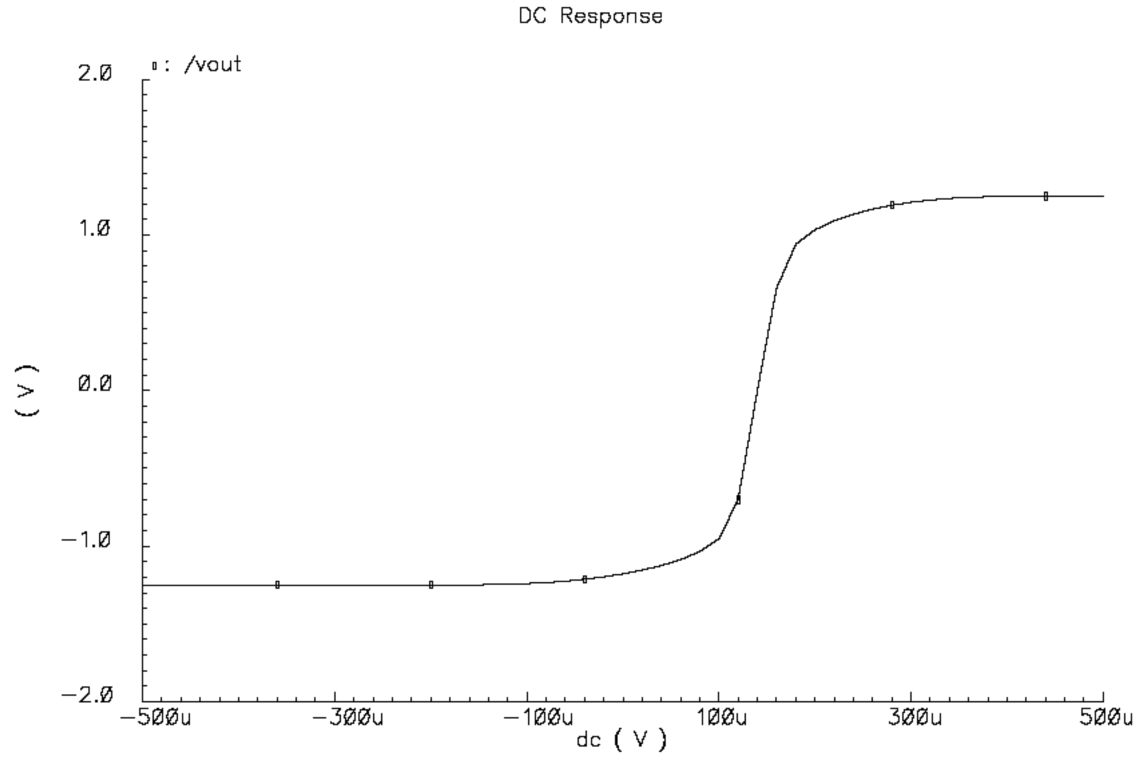


Figure 3.3: DC sweep of the comparator from -500μV to 500μ*V*, *Vdd = 1.25V, Vss = -1.25V,* I_{bias} *= 1μA*

3.1.3 Transient analysis

The reference voltage is connected to ground. A square wave is applied to V_{iplus}. The square wave is varied from *Vss* to (10mV+offset) and from *Vdd* to -10mV+offset. The output plots are observed and shown in figure 3.4.

Since the circuit is operated at a frequency of 100 kHz, the time period is set at 10μsec. The high-to-low and low-to-high propagation delays are determined from the plot as t_{hl} = 0.663μs and t_{lh} = 0.865μs.

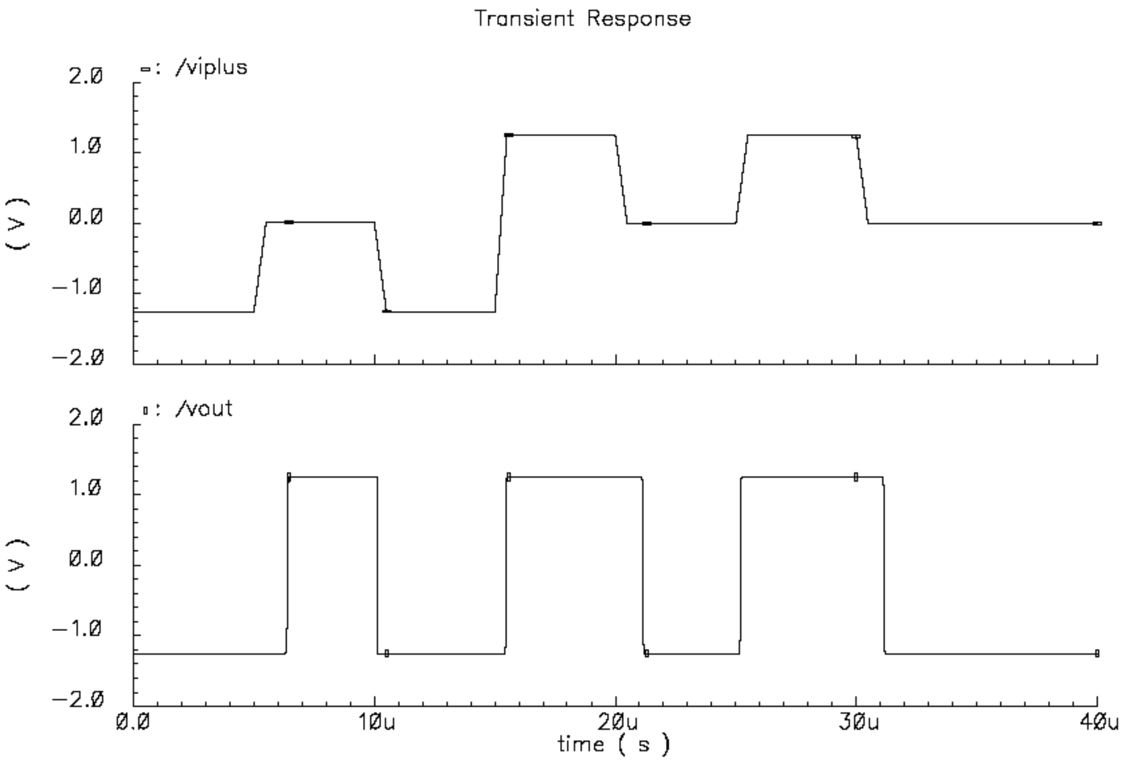


Figure 3.4: Transient simulation of the comparator, Vdd = 1.25V, Vss = -1.25V, I_{bias}*= 1*µA

3.2 Folded-cascode comparator

Folded-cascode comparator also has two stages

1. Differential stage with folded-cascode load stage
2. Output buffer stage

The differential input stage is responsible for accepting differential inputs and converts them to differential currents. It then passes them the cascode load stage. It is a NMOS differential pair whose tail current is supplied through a current mirror. An NMOS differential pair is used because NMOS transistors have higher mobility than PMOS and provide better current switching speed and thereby higher slew rates and better gain. Folded-cascode load stage provides low-input impedance for the differential currents and a high output resistance. High output resistance of this stage would yield high gain from this stage. Inverter stage is used to increase the gain and improve the slew-rate at the output node.

3.2.1 Current mirrors

The current mirror is an important component in MOS amplifiers. The current mirror uses the principle that if the gate-source potential of two identical MOS transistors are equal, the channel currents should be equal. The figure 3.5 is a simple current mirror.

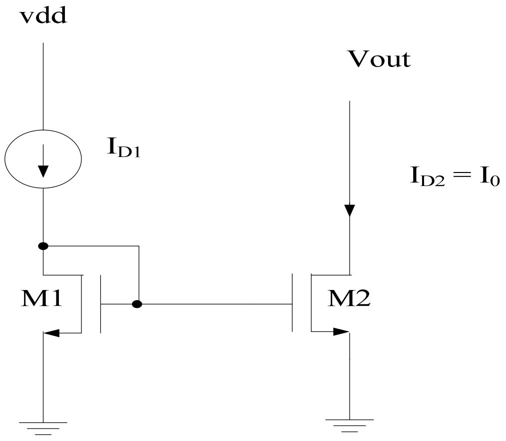


Figure 3.5: Schematic of the simple current mirror

A current I_{D1} flows through M1 corresponding to $V_{GS1.}$ Since $V_{GS1} = V_{GS2}$, ideally the same current flows through M2. If the MOSFET's are of the same size, the same drain current flows in each MOSFET provided M2 stays in the saturation region. The current I_{D1} is given by

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1}-V_{THN})^2 \qquad \textbf{(3.2)}$$

While the output current, assuming M2 in saturation flowing in M2 is given by

$$I_{D2} = \mathrm{I}_0 = \frac{\beta_1}{2}(\mathrm{V}_{\mathrm{GS2}}\text{-}\mathrm{V}_{\mathrm{THN}})^2 \quad \mathbf{(3.3)}$$

Since $V_{GS1} = V_{GS2},$ the ratio of the drain currents is given by

$$\frac{I_{D1}}{I_{D2}} = \frac{\beta_1}{\beta_2} \quad \mathbf{(3.4)}$$

By adjusting the *W/L* ratio of the two devices, a desired output current can be achieved. The main drawback of this current mirror is its low output impedance, which results in inaccurate matching due to the variation of the drain voltage of M2 with the output voltage.

3.2.2 High-swing cascode current source

Figure 3.6 is the high-swing cascode current source.[3]

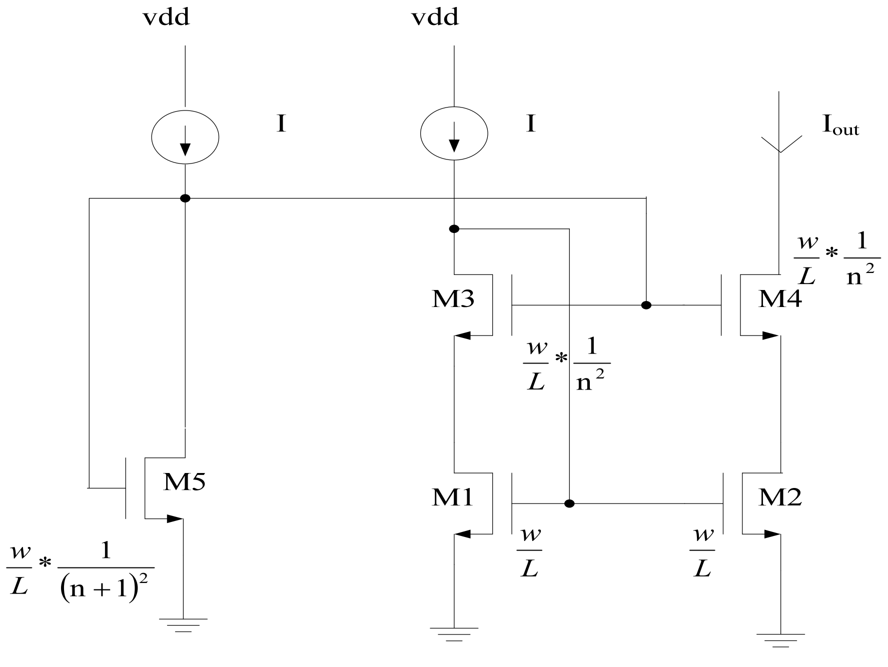


Figure 3.6: Schematic of the high-swing cascode current source

Here n is a positive integer. Using the simplified MOS I-V equation,

$$V_{GS1} = V_{GS3} = V_T + \sqrt{\frac{1}{k^{`}(W/L)}} = V_T + V_{DSsat} \text{ where } k^{`} = \frac{1}{2}\mu_n C_{ox} \qquad \textbf{(3.5)}$$

Where V_{DSsat} is the minimum drain-to-source voltage required to keep devices M1 and M3 in saturation.

For devices M3 and M5, we have

$$V_{GS3} = V_{GS4} = V_T + n * \sqrt{\frac{1}{k^{`}(W/L)}} = V_T + n * V_{DSsat} \qquad \textbf{(3.6)}$$

$$V_{GS5} = V_T + (n+1) * \sqrt{\frac{1}{k^{`}(W/L)}} = V_T + (n+1) * V_{DSsat} \qquad \textbf{(3.7)}$$

The minimum output voltage required to keep the M2 and M4 in saturation region is $2V_{DSsat.}$ Also this current source has high output impedance. It has good current matching capability since M1 and M2 have equal V_{GS} and equal V_{DS} values.

3.2.3 Operation of the folded-cascode comparator

To understand the operation of the folded cascode comparator, consider figure 3.7 initially assume the differential pair in the circuit is missing. Without the differential pair

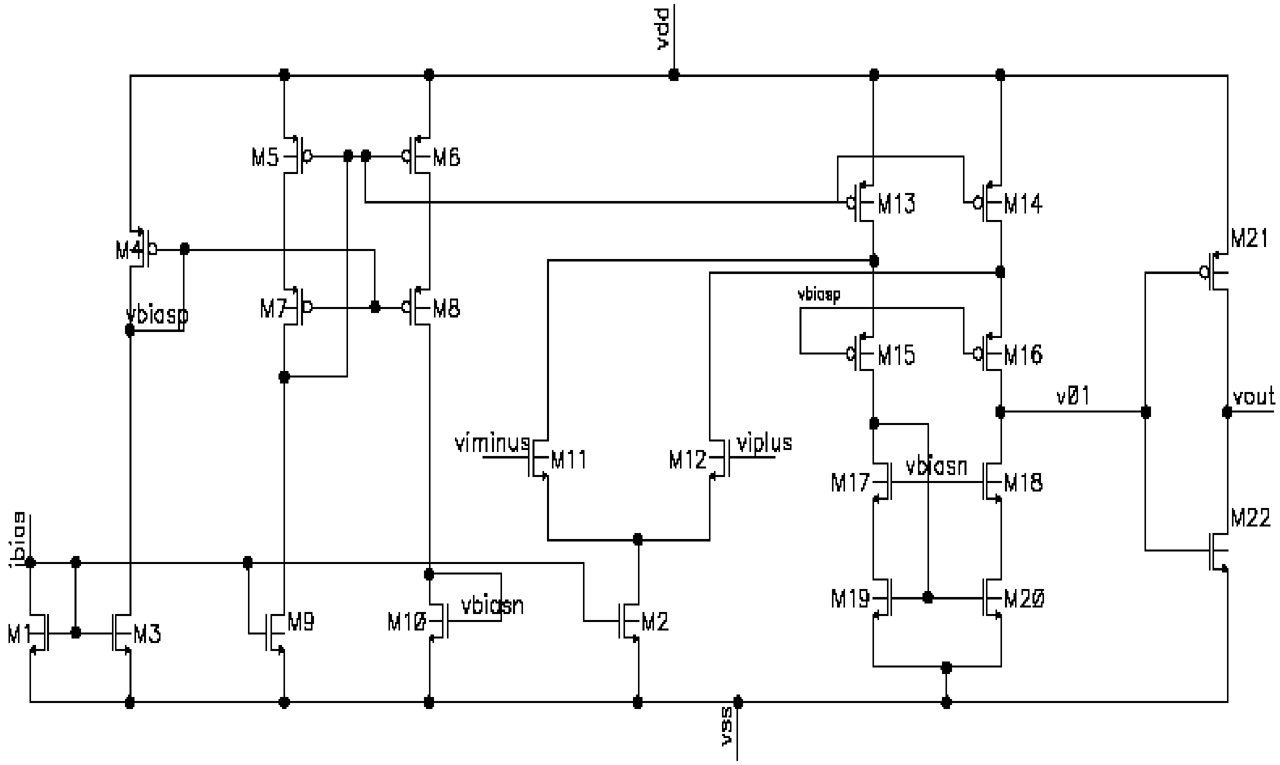


Figure 3.7: Schematic of the folded-cascode comparator without hysteresis

in the circuit, I_{bias} flows in all MOSFET's. MOSFET's M5 and M6 provide the DC bias voltages to M13 and M14. When the differential pair is added back to the circuit, it steals $I_{bias}/2$ from M15-M20, reducing their drain currents to $I_{bias}/2$. Appying differential input voltage $V_d = V_{iplus} - V_{iminus}$ causes the differential drain current to become $g_m V_{in}$, where g_m is the transconductance of the M11 and M12 transistors. This differential drain current is mirrored in the cascoded MOSFET's M15-M20.

3.2.4 Sizes of transistors

Since speed is extremely important in comparator design, L is chosen as 1.2µm. I_{bias} is set at 1µA. Transistors M1 and M2 form the current mirror and provide the bias current for the differential pair. The sizes of these transistors are found by the equation (3.1).
After substituting the same values for $\mu_n C_{OX}$ and V_{GS}-V_T , we get
W=0.54uM and L=1.2uM.

Since good matching is needed, the transistor sizes are chosen as W=5.4µm, L=1.2µm with multiplier m=2. Transistors M11 and M12 form the differential pair and 0.5uA current flows through these transistors. Following equation 1, the sizes of $W$and L are obtained. Since more area is required in differential pair transistors, the sizes of W and L are chosen as W=5.4µm, L=1.2µm with m=4.

Transistors M4, M5, M6, M7 and M8 form the low voltage PMOS wide swing current mirror which provides bias voltages for the cascoding transistors of the load stage. Transistor M9 acts as a current source for this current mirror. The sizes of the cascoding transistors M7 and M8 are adjusted to reduce the output delay. So the W and L of these transistors are chosen as W=5.4µm, L=0.9µm with m=2. The effects of reducing the areas of M7 and M8 are to increase the offset and reduce the delay. This is a trade-off between delay and offset. The same analysis holds for the transistors M10, M17, M18, M19 and M20 which form the NMOS wide swing current mirror. Transistors M21 and M22 form the inverter. Since no matching is needed and the size of the PMOS transistor should be twice that of the NMOS transistor, the sizes of the transistors M21 and M22 are chosen as W=5.4μm,L=0.6um with m=2 and W=5.4μm,L=0.6μm with m=1 respectively.

3.2.5 DC analysis

The reference voltage V_{iminus} is connected to ground. The other input voltage V_{iplus} is varied from -2mV to 2mV. The circuit utilizes two power supplies ± 1.25V. An external capacitance of 33fF is connected at the output. Then the transfer characteristic of *vout* versus the input V_{iplus} is observed. The plot is shown in the figure 3.8. DC plot between the output *vout* and the input *viplus* is observed.
The gain and offset are measured from the plots as 19K and 360μV respectively.

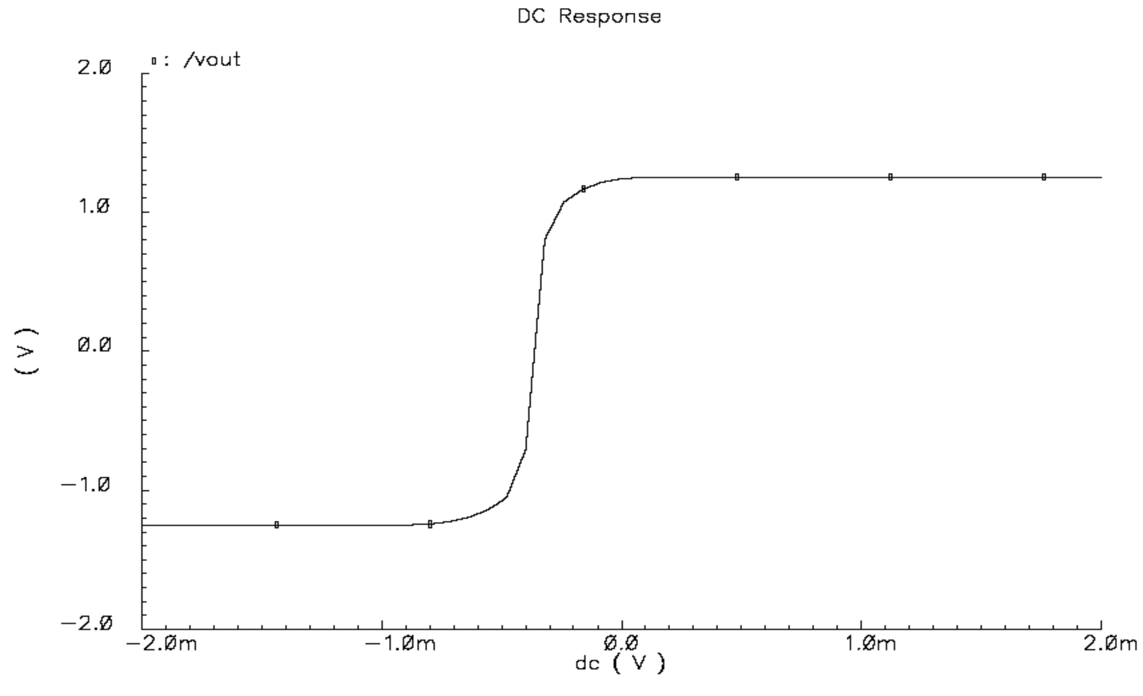


Figure 3.8: DC sweep of the comparator from -2mV to 2m*V, Vdd = 1.25V, Vss = -1.25V,* *I_{bias} = 1 μA*

3.2.6 Transient analysis

The reference voltage V_{minus} is connected to ground. A Square wave is applied to $V_{iplus.}$ The square wave is varied from *Vss* to (10mV+offset) and *Vdd* to –(10mV+offset). The output plots are observed and shown in the figure 3.9.

Since the circuit is operated at a frequency of 100 kHz, the time period is set at 10usec.The low-to-high and high-to-low propagation delays are determined from the plots as 0.880μs and 0.798μs respectively.

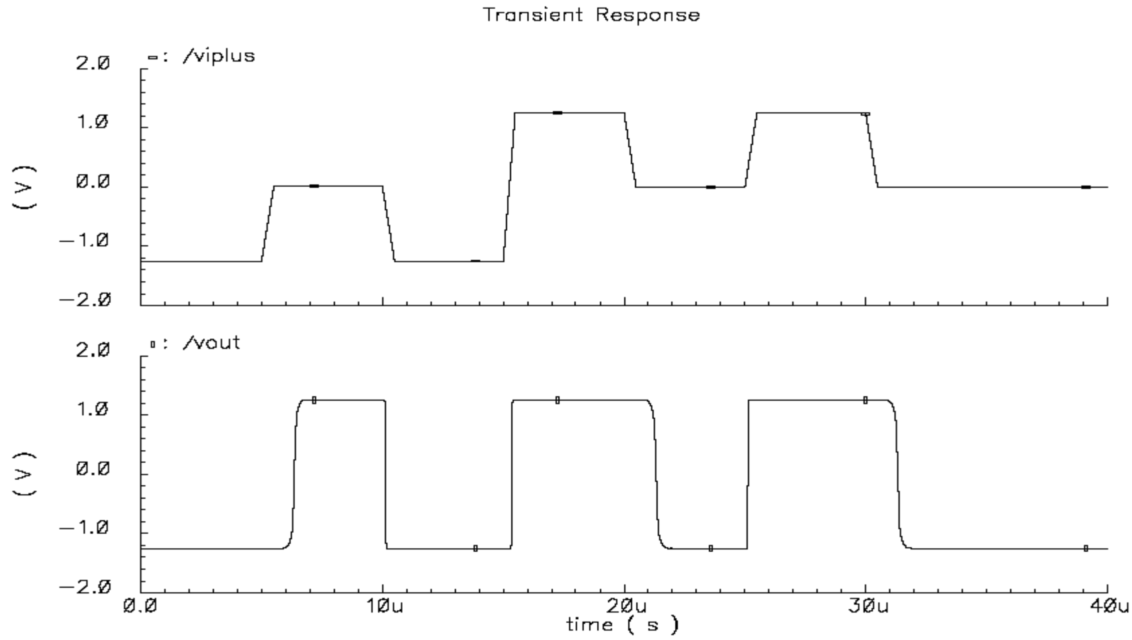


Figure 3.9: Transient simulation of the comparator, Vdd = 1.25V, Vss = -1.25V, I_{bias}*=* *1*μA

3.3 Three-stage comparator with internal hysteresis:

Hysteresis can be obtained by adding positive feedback to the comparator. Hysteresis is added to the three stage comparator which is implemented in section 3.1. The circuit is shown in figure 3.10.

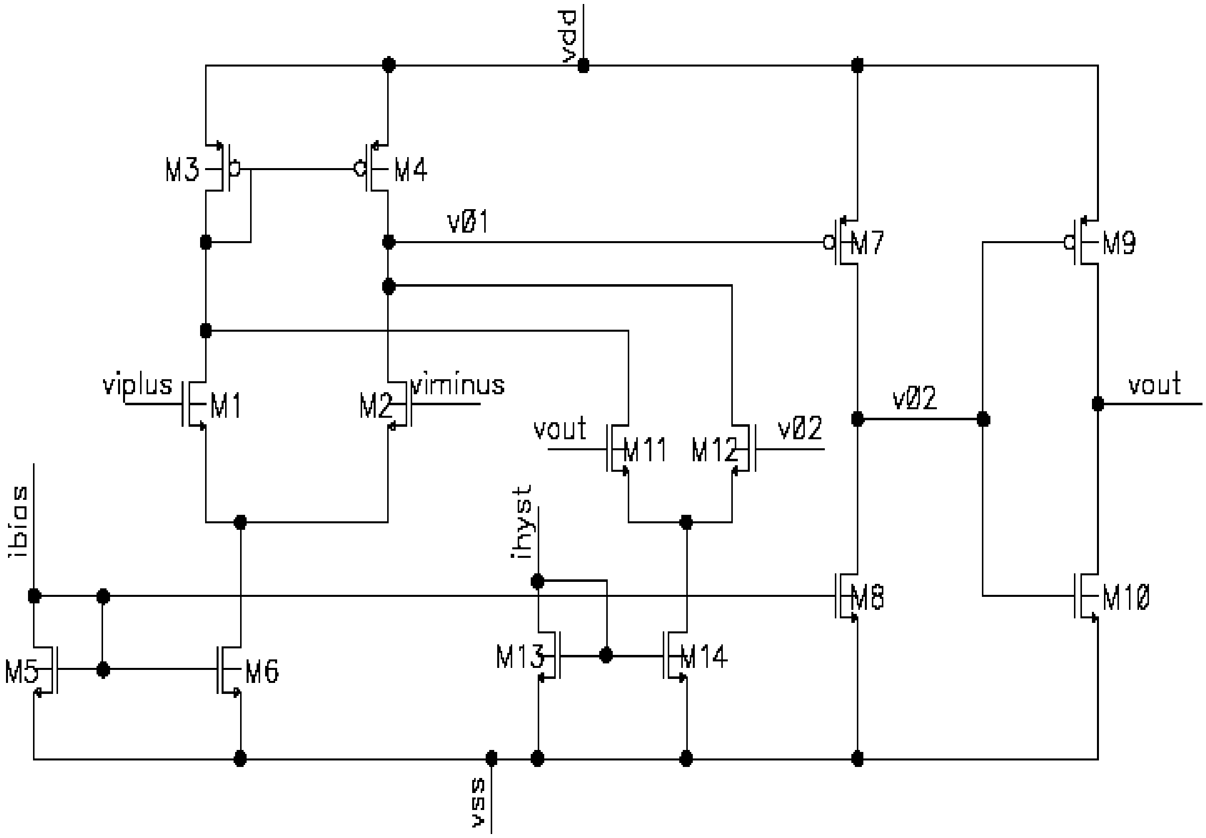


Figure 3.10: Schematic of the three-stage comparator with internal hysteresis

The transistors M11-M12 which form a second differential pair are used with positive feedback to add some amount of hysteresis. The transistors M13 and M14 form the current mirror which provides the hysteresis current for the differential pair. The amount of hysteresis can be varied by adjusting the hysteresis current. When the input voltage *viplus* is increased, the voltage at node *v01* increases, the output voltage *vout* increases and *v02* begin to decrease. As *vout* becomes high, transistor M11 is more on than transistor M12, more current flows through node *v01* which results in increase in voltage at node *v01*. As the voltage at *v01* increases, the voltage at node *v02* still decreases and *vout* increases. This regenerative process goes on till the output *vout* saturates in the positive direction i.e. at *vdd*. The same analysis holds true when *viplus* starts to decrease. The output voltage *vout* saturates in negative direction i.e., *vss.* Since the second differential pair transistors do not need good matching, the sizes of these transistors are selected as *W*=3.6µm, *L*=0.9µm with *m*=2.The sizes of the transistors M15 and M16 are chosen as *W*=5.4µm, *L*=1.2µm with *m*=2.

3.3.1 DC analysis and transient analysis are performed on this circuit. The plots are shown in the figure 3.11 below.

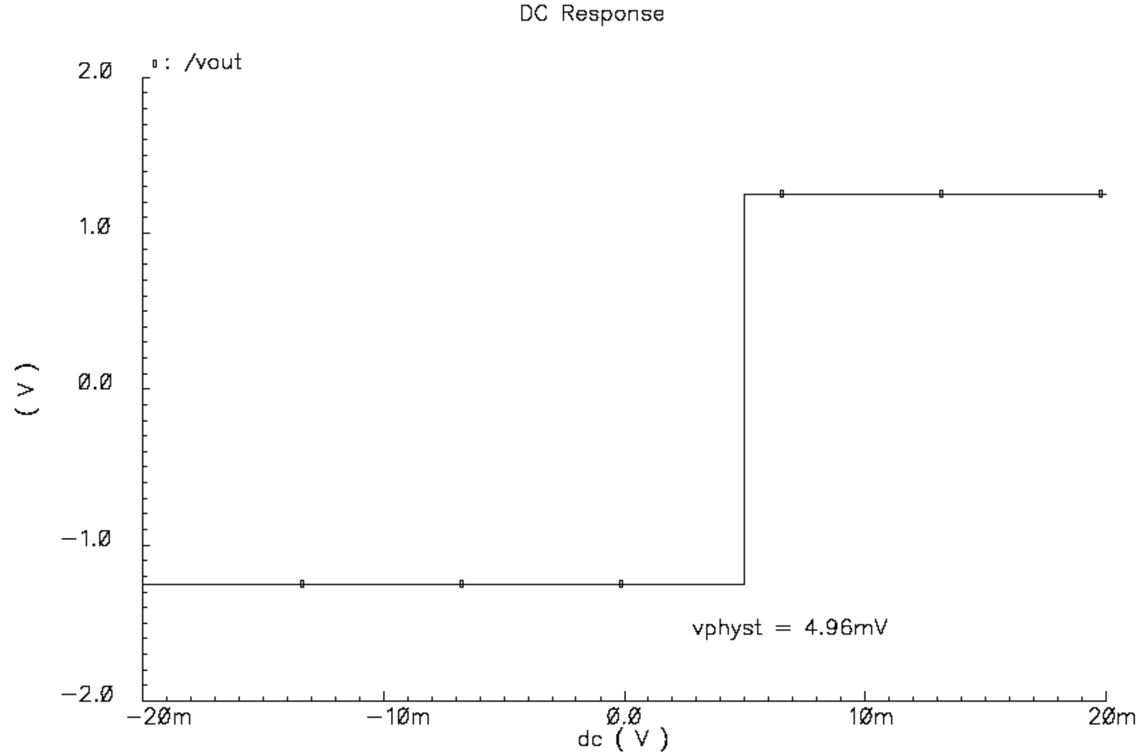


Figure 3.11: DC sweep of the comparator from -20mV to 20*mV*, *Vdd = 1.25V, Vss = -1.25V,* $I_{bias} = 1\ \mu A$, $I_{hyst} = 47nA$

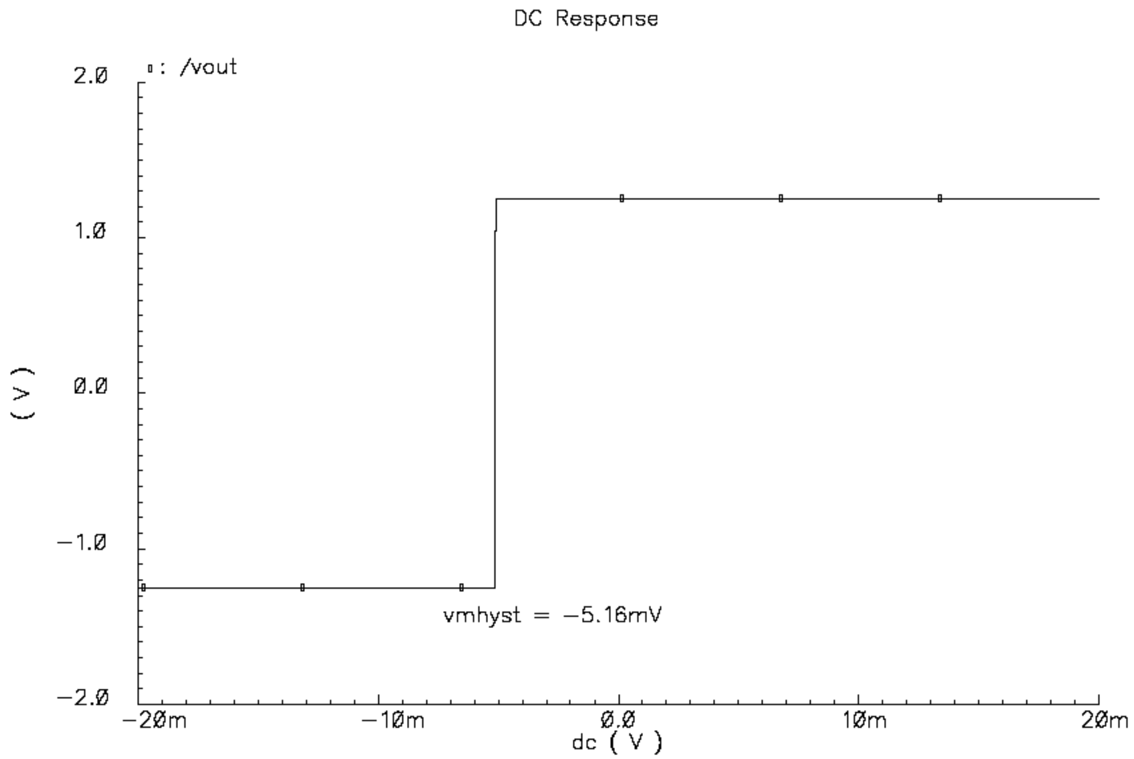


Figure 3.12: DC sweep of the comparator from 20mV to -20*mV*, *Vdd = 1.25V, Vss = -1.25V,* $I_{bias} = 1\ \mu A$, $I_{hyst} = 47nA$

From the DC plots, it can be observed that when V_{iplus} is varied from 20mV to -20mV, the lower threshold (V_{TL}) is obtained at -5.16mV. When V_{iplus} is varied from -20mV to 20mV, the upper threshold (V_{TH}) is obtained at 4.96mV. The amount of hysteresis is difference between upper threshold and the lower threshold which is approximately 10mV.

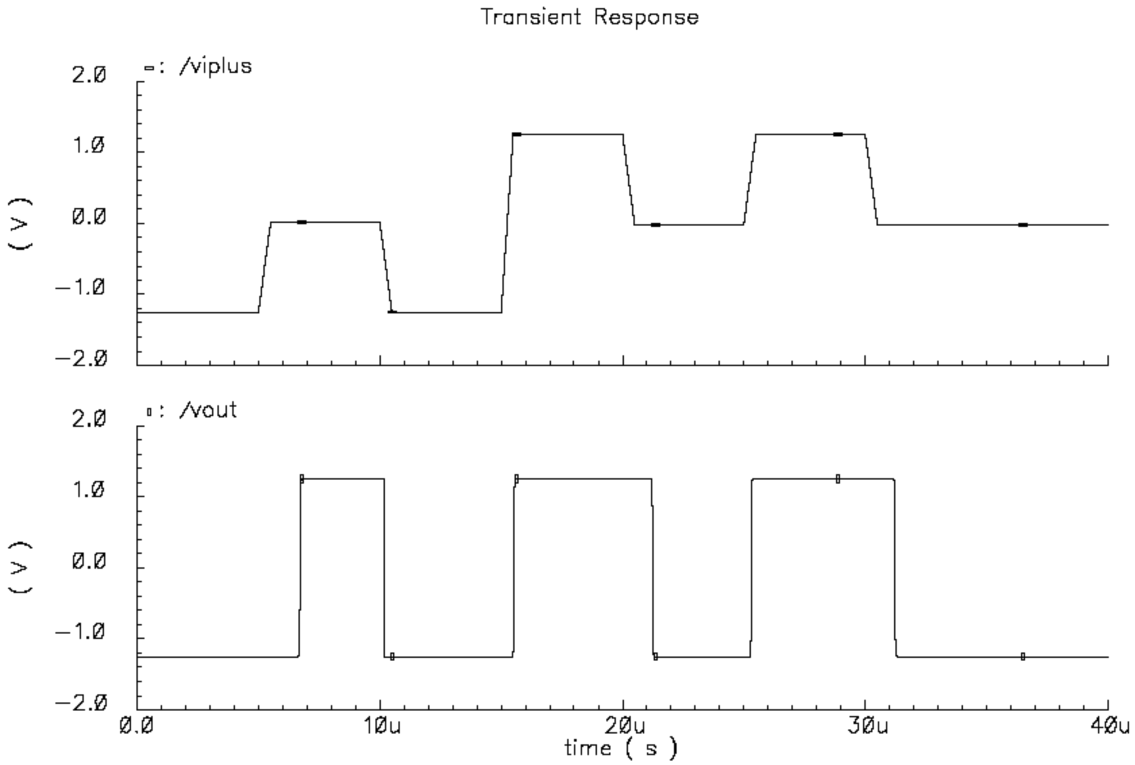


Figure 3.13: Transient simulation of the comparator, Vdd = 1.25V, Vss = -1.25V,

$I_{bias} = 1\mu A$, $I_{hyst} = 47nA$

From the transient plots, the low-high and high-to-low propagation delays are measured as 1.203µs and 0.729µs respectively.

3.4 Folded-cascode comparator with internal hysteresis

Hysteresis can be added to the folded cascode comparator internally in the same way as tit was added to the three stage comparator. The schematic of the folded cascode comparator with internal hysteresis is shown in the figure 3.14.

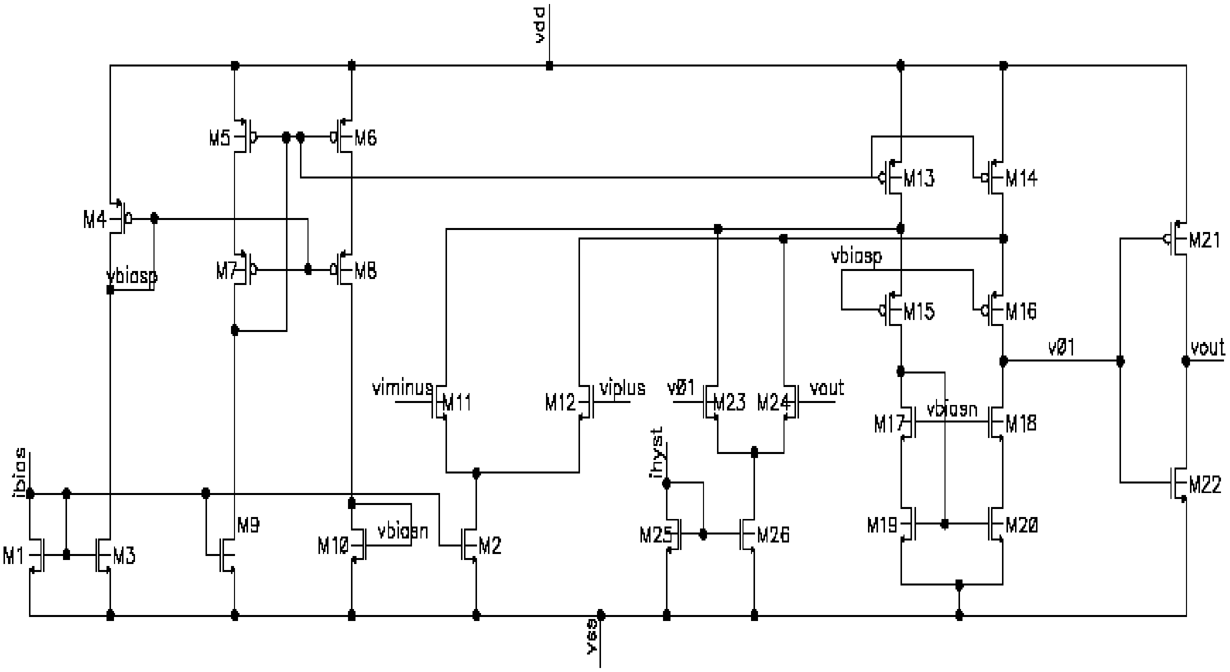


Figure 3.14: Schematic of the folded- cascode comparator with internal hysteresis

DC analysis and transient analysis are performed on this circuit. The plots are shown in the figure below.

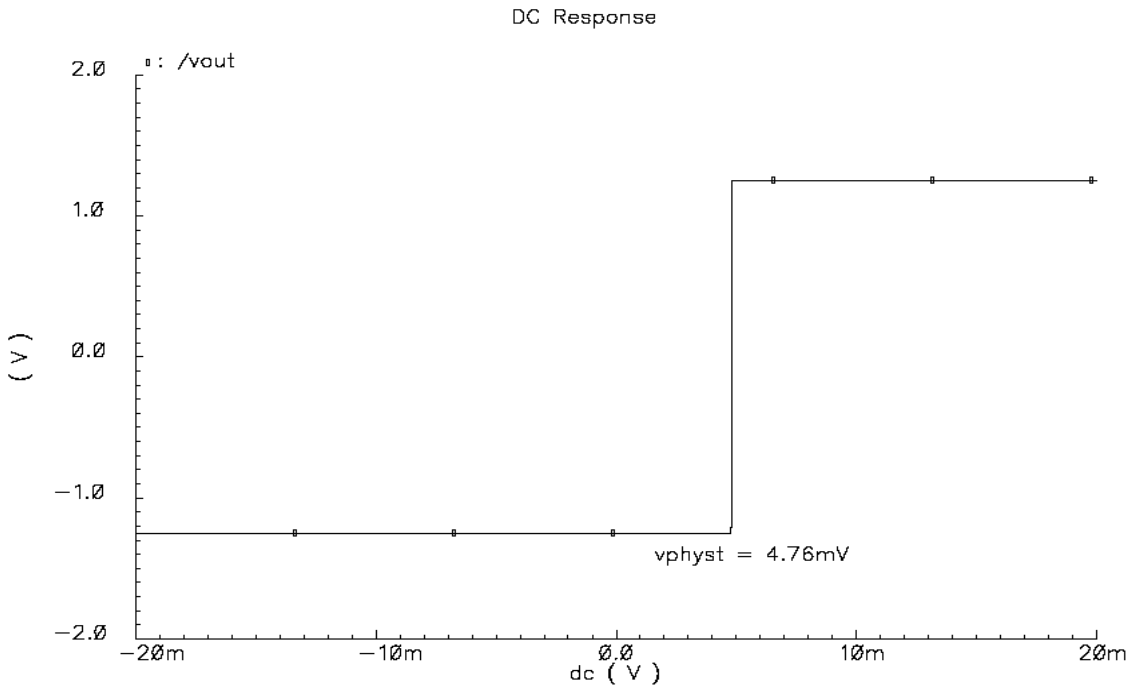


Figure 3.15: DC sweep of the comparator from -20mV to 20*mV*, *Vdd = 1.25V,*

Vss = -1.25V, I_{bias} *= 1 µA,* I_{hyst} *= 55nA*

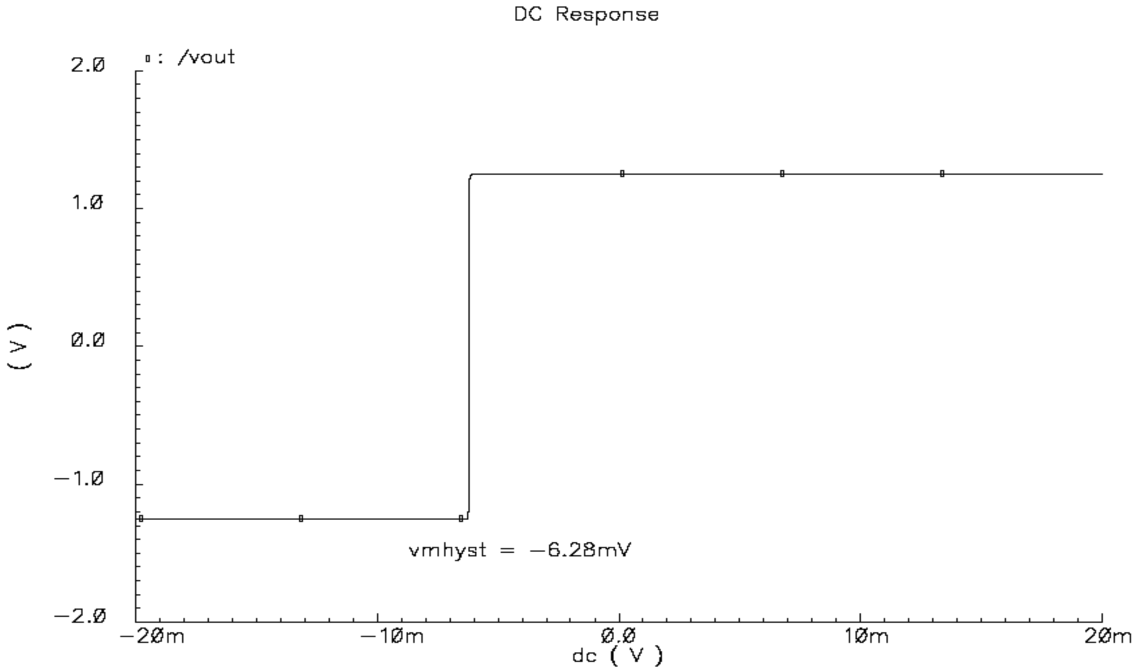


Figure 3.16: DC sweep of the comparator from 20mV to -20*mV*, *Vdd = 1.25V,*

Vss = -1.25V, I_{bias} *= 1 µA,* I_{hyst} *= 55nA*

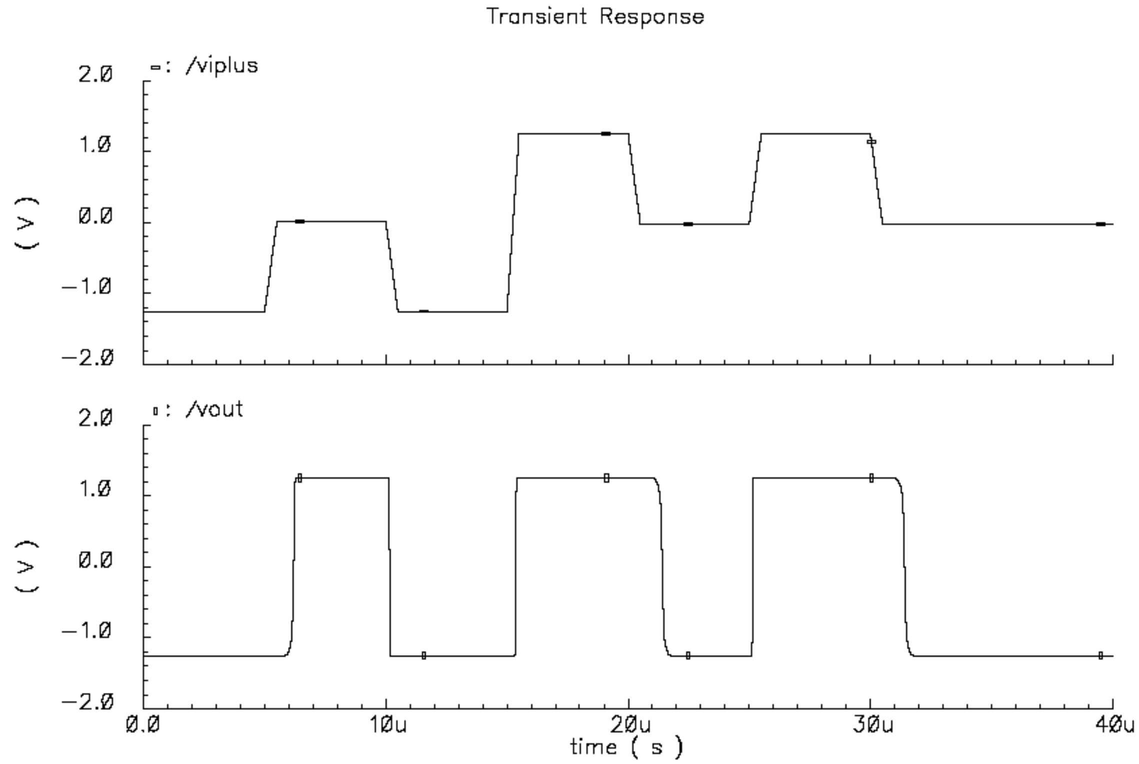


*Figure 3.17: Transient simulation of the comparator, Vdd = 1.25V, Vss = -1.25V, I_{bias} = 1*μA, *I_{hyst} = 55nA*

From the DC plots, it can be observed that when V_{iplus} varied from 20mV to -20mV, the lower threshold (V_{TL}) is obtained at -6.28mV. When V_{iplus} is varied from -20mv to 20mV, the upper threshold (V_{TH}) is obtained at 4.76mV. The amount of hysteresis is difference between upper threshold and the lower threshold which is approximately 10mV.

From the transient plots, the low-high and high-to-low propagation delays are measured as 0.606μs and 0.913 μs respectively.

3.5 Three-stage comparator with external hysteresis

In this circuit, hysteresis is added to the three stage comparator externally. The schematic of the three stage comparator with external hysteresis is shown in the figure below.

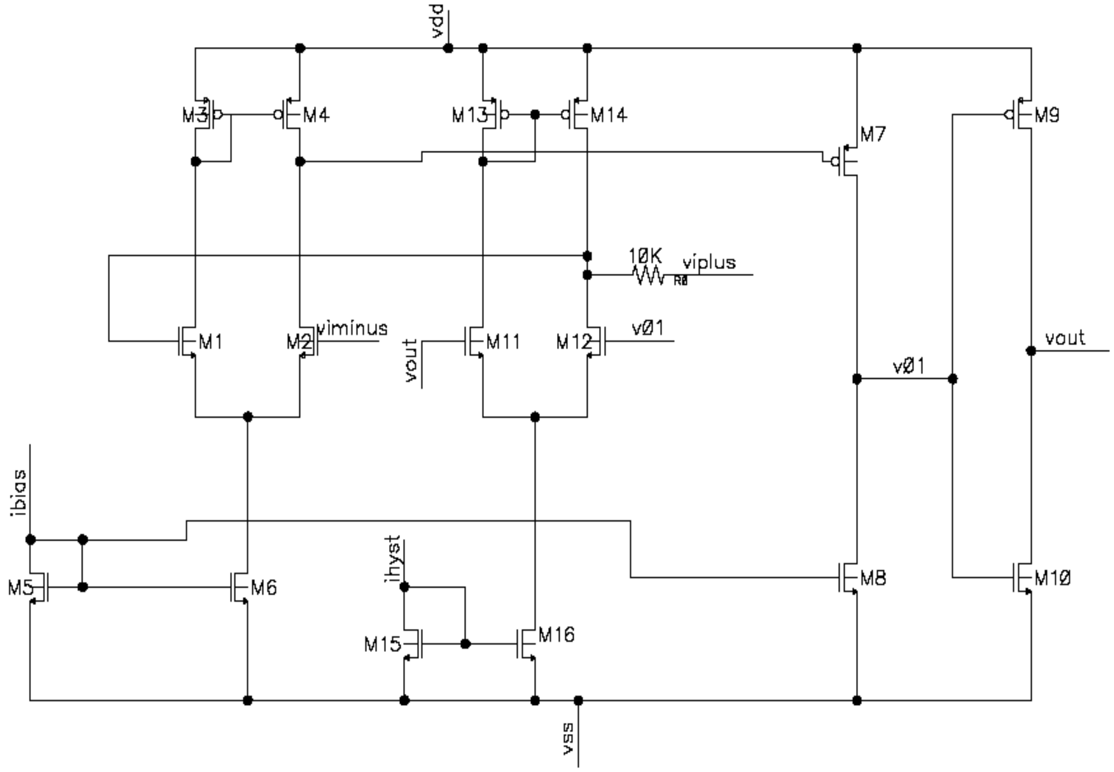


Figure3.18: Schematic of the three-stage comparator with external hysteresis

The circuit uses bi-directional current source ± I_{hyst} and a 10kΩ resistor to obtain hysteresis. The transistors M11-M12 which form a second differential pair is used with the positive feedback to add some amount of hysteresis. The transistors M16 and M17 form the current mirror which provides the hysteresis current for the differential pair. The current mirror M13 and M14 is used as an active load. The polarity of the bi-directional current source is controlled by the rail to rail output voltage *vout*. The amount of hysteresis can be adjusted by varying the hysteresis current I_{hyst}. If *vout* is *Vdd*, then the output current is I_{hyst} which gives an upper threshold voltage (V_{TH}) of $I_{hyst.}\, R$.

$$V_{TH} = I_{hyst.}\, R. \tag{3.9}$$

If *vout* is *Vss*, then the output current is $-I_{hyst}$ which gives a lower threshold voltage (V_{TL}) of

$$V_{TL} = -\, I_{hyst.}\, R. \tag{3.10}$$

The amount of hysteresis which is the difference between the upper threshold voltage and the lower threshold voltage can be adjusted by varying the hysteresis current.

DC analysis and transient analysis are performed on this circuit. The plots are shown in the figures 3.19 and 3.20.

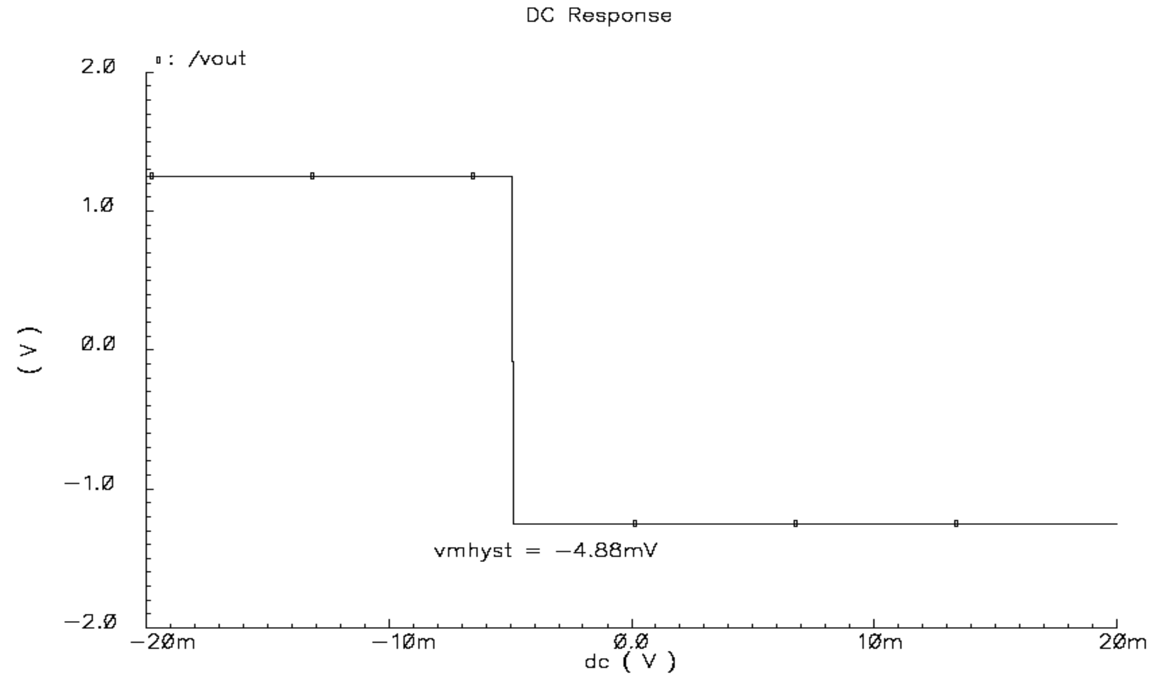


Figure 3.19: DC sweep of the comparator from- 20mV to 20*mV*, *Vdd = 1.25V, Vss = -1.25V,* $I_{bias} = 1\ \mu A$, $I_{hyst} = 500nA$

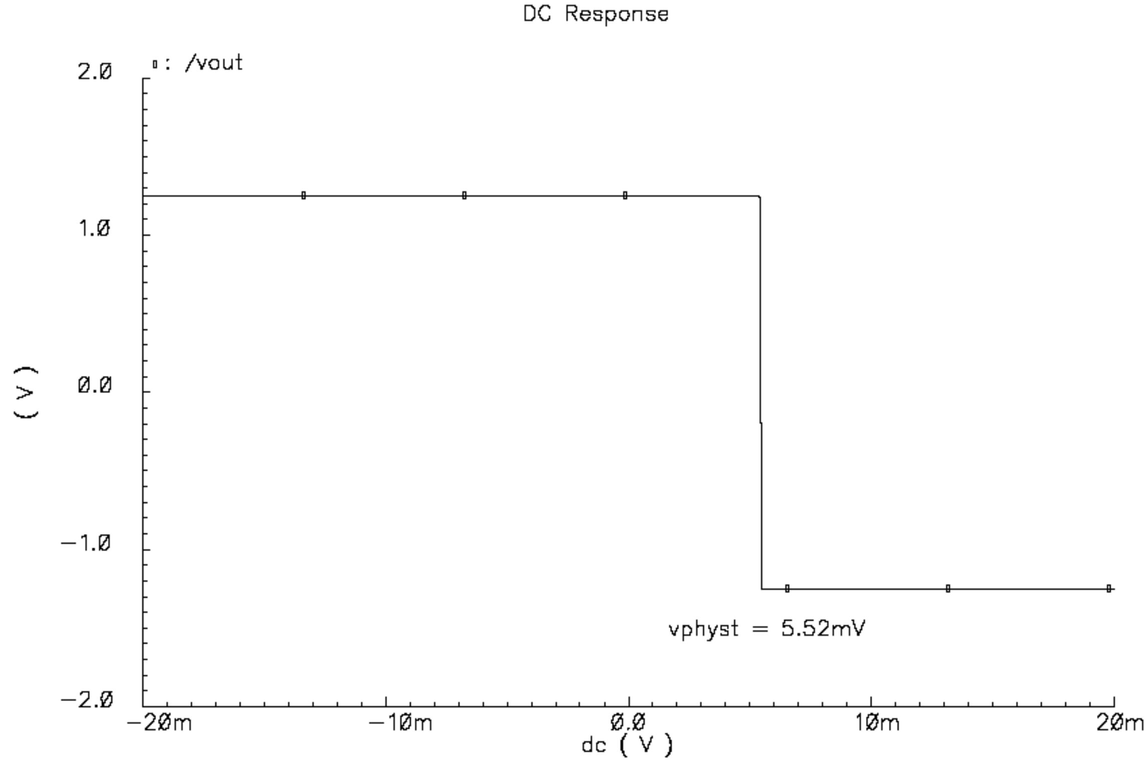


Figure 3.20: DC sweep of the comparator from -20mV to 20*mV*, *Vdd = 1.25V, Vss = -1.25V,* $I_{bias} = 1\mu A$, $I_{hyst} = 500nA$

From the DC plots, it can be observed that when V_{iplus} is varied from 20mV to -20mV, the lower threshold (V_{TL}) is obtained at -4.88mV. When V_{iplus} is varied from -20mV to 20mV, the upper threshold (V_{TH}) is obtained at 5.52mV. The amount of hysteresis is difference between upper threshold and the lower threshold which is approximately 10mV.

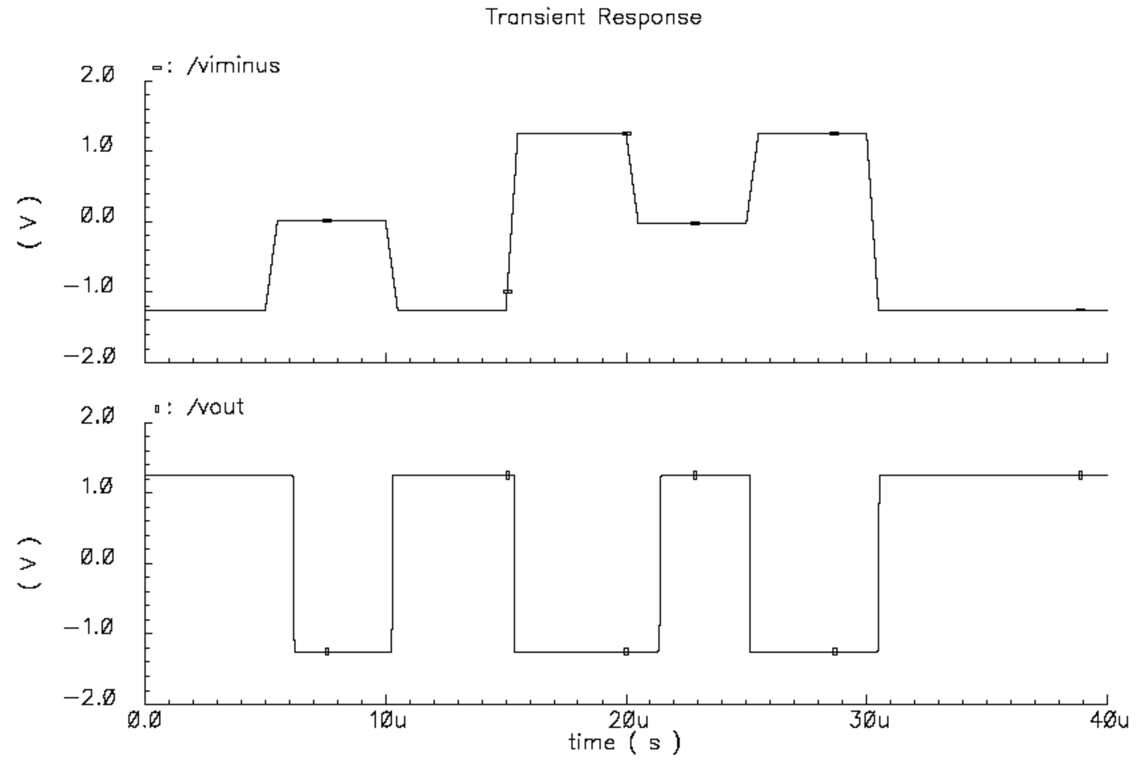


Figure 3.21: Transient simulation of the comparator, Vdd = 1.25V, Vss = -1.25V,

I_{bias}= *1*µA, I_{hyst} *= 500nA*

From the transient plots, the low-high and high-to-low propagation delays are measured as0.910µs and 0.684µs respectively.

3.6 Folded-cascode comparator with external hysteresis

Hysteresis can be added to the folded cascode comparator externally through a 10K resistor in the same way as it was added to the three stage comparator. The schematic of the folded cascode comparator with internal hysteresis is shown in the figure below.

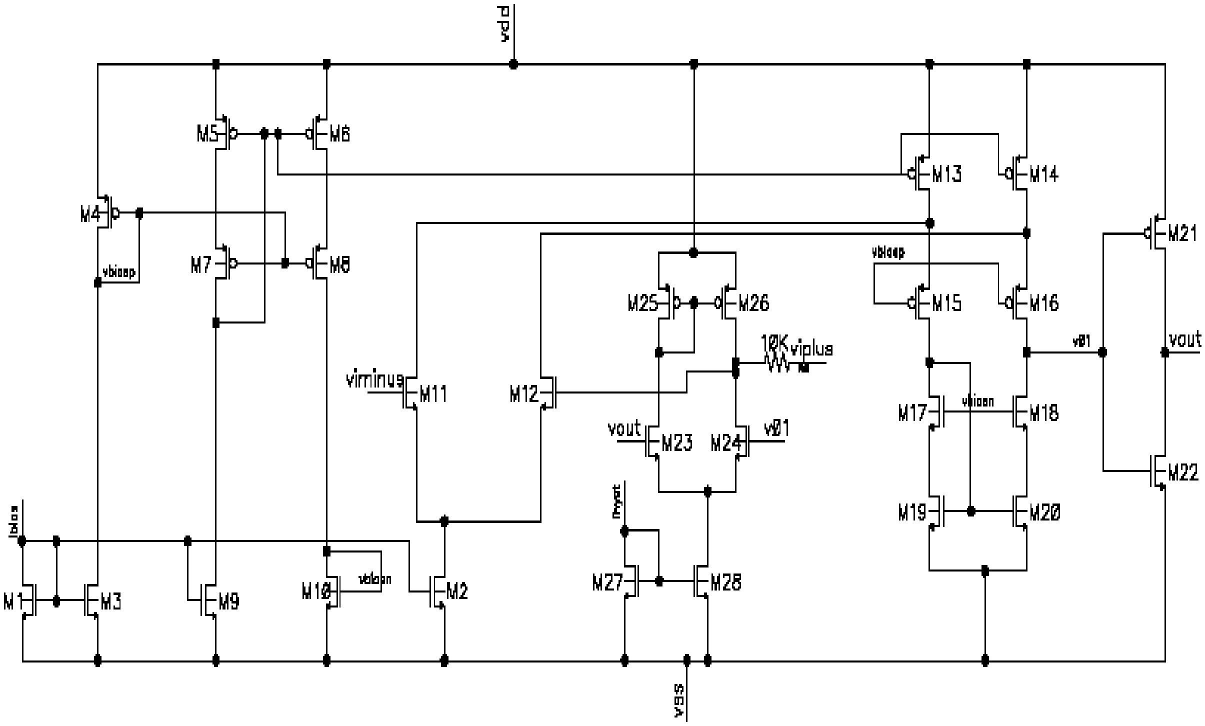


Figure 3.22: Schematic of the folded- cascode comparator with external hysteresis

DC analysis and transient analysis are performed on this circuit. The plots are shown in the figure below.

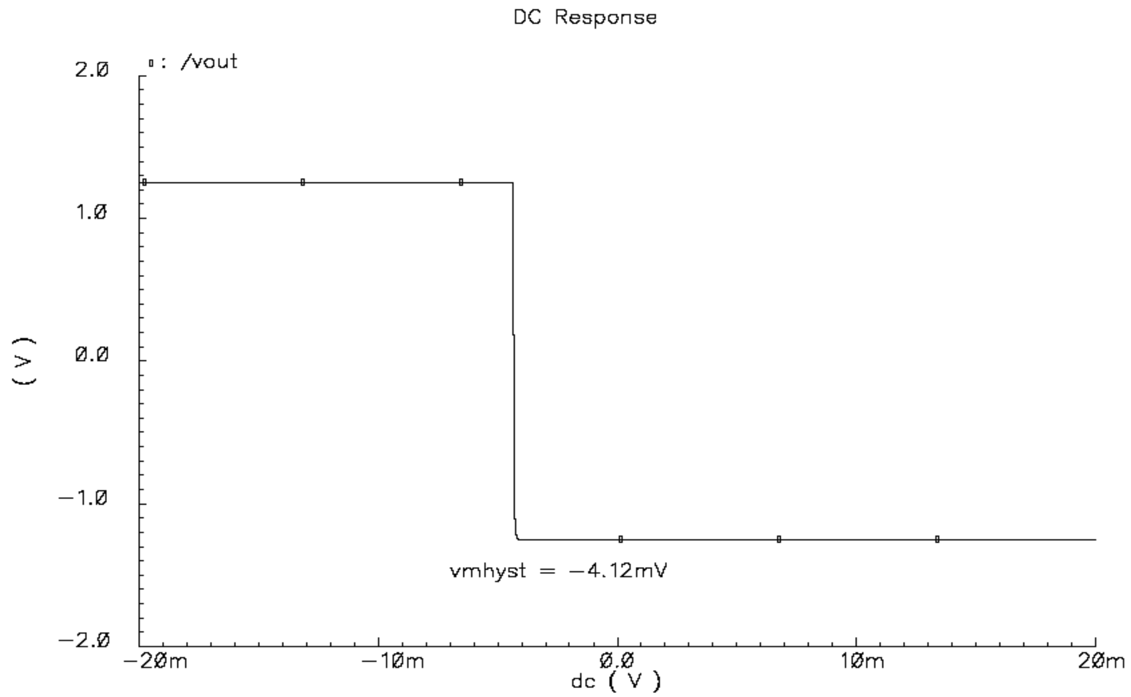


Figure 3.23: DC sweep of the comparator from - 20mV to 20*mV*, *Vdd = 1.25V,*

Vss = -1.25V, I_{bias} *= 1 µA,* I_{hyst} *= 500nA*

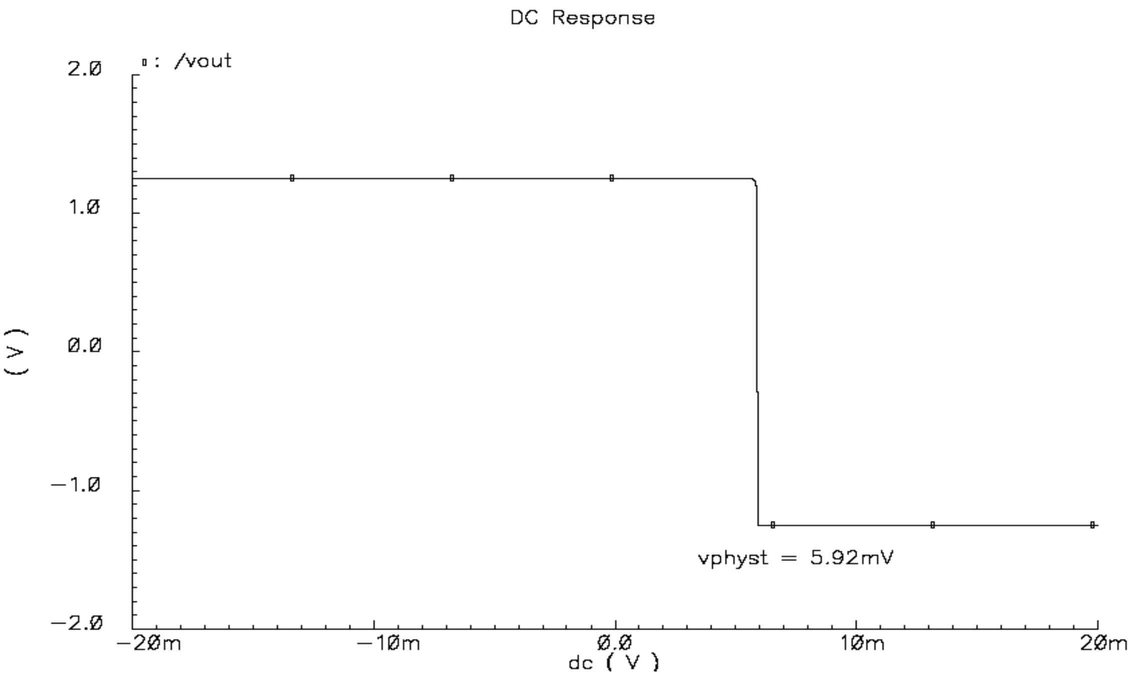


Figure 3.24: DC sweep of the comparator from 20*mV* to -20*mV*, *Vdd = 1.25V,*

Vss = -1.25V, I_{xias} *= 1µA,* I_{hyst} *= 500nA*

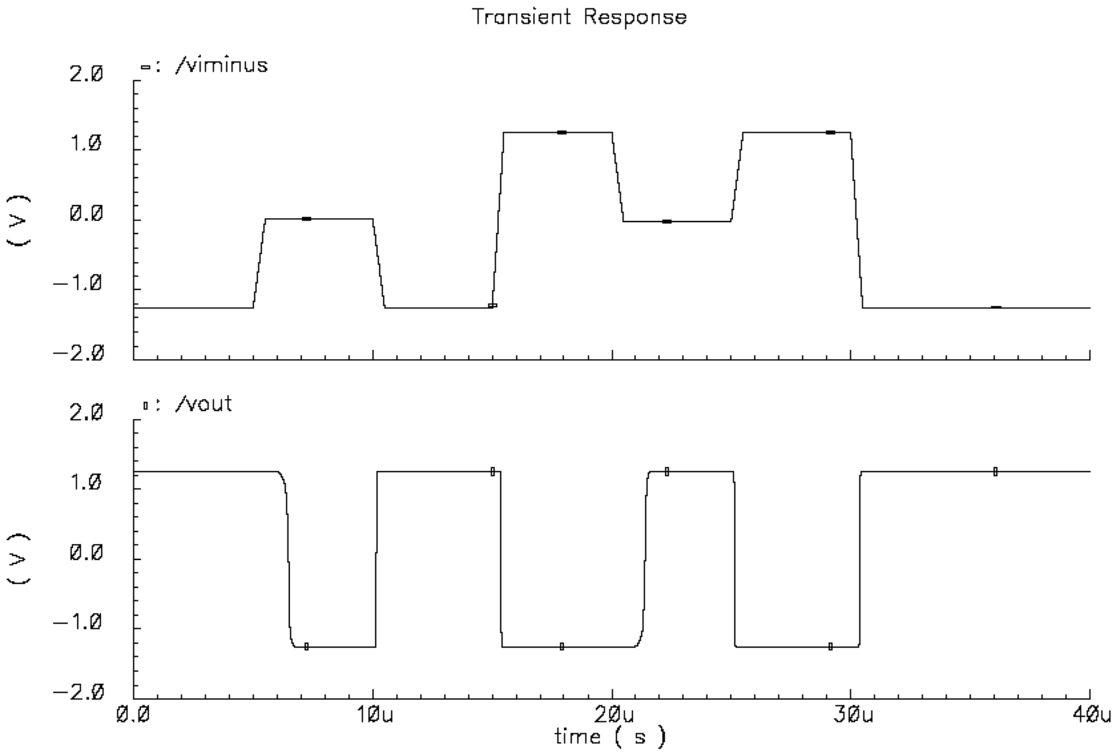


Figure 3.25: Transient simulation of the comparator, Vdd = 1.25V, Vss = -1.25V,

I_{bias}= *1*µA, I_{hyst} = *500nA*

From the DC plots, it can be observed that when V_{iplus} is varied from 20mV to -20mV, the lower threshold (V_{TL}) is obtained at -4.12mV. When V_{iplus} is varied from -20mV to 20mV, the upper threshold (V_{TH}) is obtained at 5.92mV. The amount of hysteresis is difference between upper threshold and the lower threshold which is approximately 10mV.

From the transient plots, the low-high and high-to-low propagation delays are measured as 0.899 µs and .937µs respectively.

The following table shows the summary of all comparators.

Type of comparator	**Gain kV/V**	**Offset (mV)**	**hysteresis (mV)**	**Delay(T_{LH}) (µs)**	**Delay(T_{HL}) (µs)**	**Total bias current (µA)**
Three-stage compaartor	34	0.140	0	0.866	0.664	3
Three-stage comparator with internal hysteresis	62.5	-0.1	10.12	1.203	0.729	3+0.047 +0.047
Three-stage comparator with internal hysteresis	61.8	0.52	10	0.910	0.684	3+0.5+0.5
folded-cascode comparator	20	0.360	0	0.880	0.799	6
folded-cascode comparator with internal hysteresis	61.05	-0.76	10.02	0.606	0.913	6+0.052+0.052
folded-cascode comparator with external hysteresis	60	0.9	10.04	0.899	0.937	6+0.5+0.5

Table 3.1 Summary of comparators

The following table 4.2 shows the programmability of hysteresis.

Type of comparator	**I_{hyst} in nA**	**Amount of hysteresis in mV**
Three-stage comparator with internal hysteresis	47	10.12
	91	20.02
	132	30.08
	175	40.12
folded-cascode compaartor with internal hysteresis	52	10.04
	92	20.06
	137	29.96
	180	40.12
Three-stage comparator with external hysteresis	500	10
	1000	20.02
	1500	30.06
	2000	40.04
Folded-cascode comparator with external hysteresis	500	10.04
	1000	20
	1500	30.06
	2000	40.02

Table 3.2: Programmability of hysteresis

4. LAYOUT, TEST SETUP AND MEASUREMENT RESULTS

As described in chapter 3, six comparators, three without hysteresis and three with hysteresis were designed in AMI $0.5\mu m$ technology. All six comparators were laid out. The chip has been fabricated and tested. The chip includes six digital buffers to drive external load capacitances. In the layout, the metal3 layer is not used; only the metal1, metal2 and poly layers were used. The poly layer was not used for long interconnects as it has high sheet resistance.

In the layout of each comparator, current mirrors, differential pair transistors, mirroring transistors and cascoding transistors were carefully laid out using the Common-centroid technique, as matching of individual devices is of paramount concern in analog circuit design. It is one of the commonly used analog layout techniques for improving the matching between devices on a chip.

In three-stage comparator, differential pair transistors, active load and current source transistors, current mirrors were grouped together and were laid out using common-centroid technique. In folded-cascode comparator, differential pair transistors, PMOS current sources and cascoding transistors, nmos mirroring and cascoding transistors, biasing circuit, current mirrors were grouped together and were laid out using common-centroid technique. The area occupied by the three stage comparator, folded-cascode comparator, three-stage comparator with internal hysteresis, folded-cascode comparator with external hysteresis, three-stage comparator with external hysteresis and folded-cascode comparator with external hysteresis are 1540 μm^2, 3762 μm^2, 2153 μm^2, 4224 μm^2, 2453 μm^2 and 4623 μm^2 respectively. The layouts of the six individual comparators are shown in Appendix B. The chip layout is shown in figure 4.1.

A design rule check (DRC) and layout versus schematic (LVS) were performed on the layout of each comparator and the final chips before being submitted for fabrication. The fabricated chips were packaged in a DIP (Dual Inline Package) with 40 pins each. The following sections explain the test setup and measurement results.

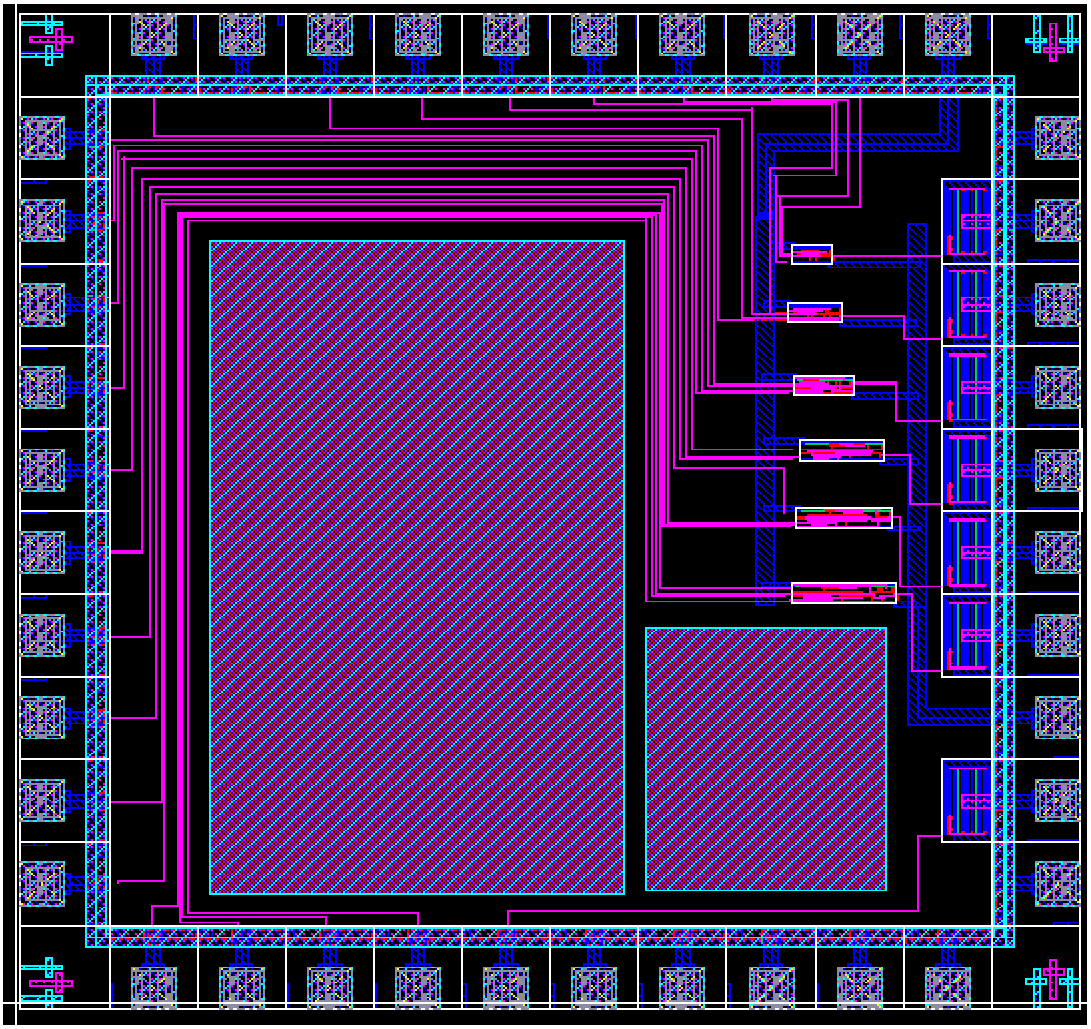


Figure 4.1: Layout of the chip

4.1 Test Set up

All the comparators were operated at a frequency of 100 kHz. A positive supply of *Vdd* = 1.25V and a negative supply of *Vss* = -1.25V were used. An input bias current I_{bias} of 1μA is used during the testing of all comparators. A bypass capacitor is connected between *Vdd* and ground, between *Vss* and ground and also a capacitor between *Vdd* and *Vss* in order to reduce power supply noise. All wires going to ground are hooked up to a single point. *Pad-Vdd* is connected to *Vdd* and *pad-Vss* is connected to *Vss*.

The setup for the generation of the bias current is shown in the figure 4.1 below. It uses a 1.75MΩ resistor, LMC 6482 op-amp and multimeter.

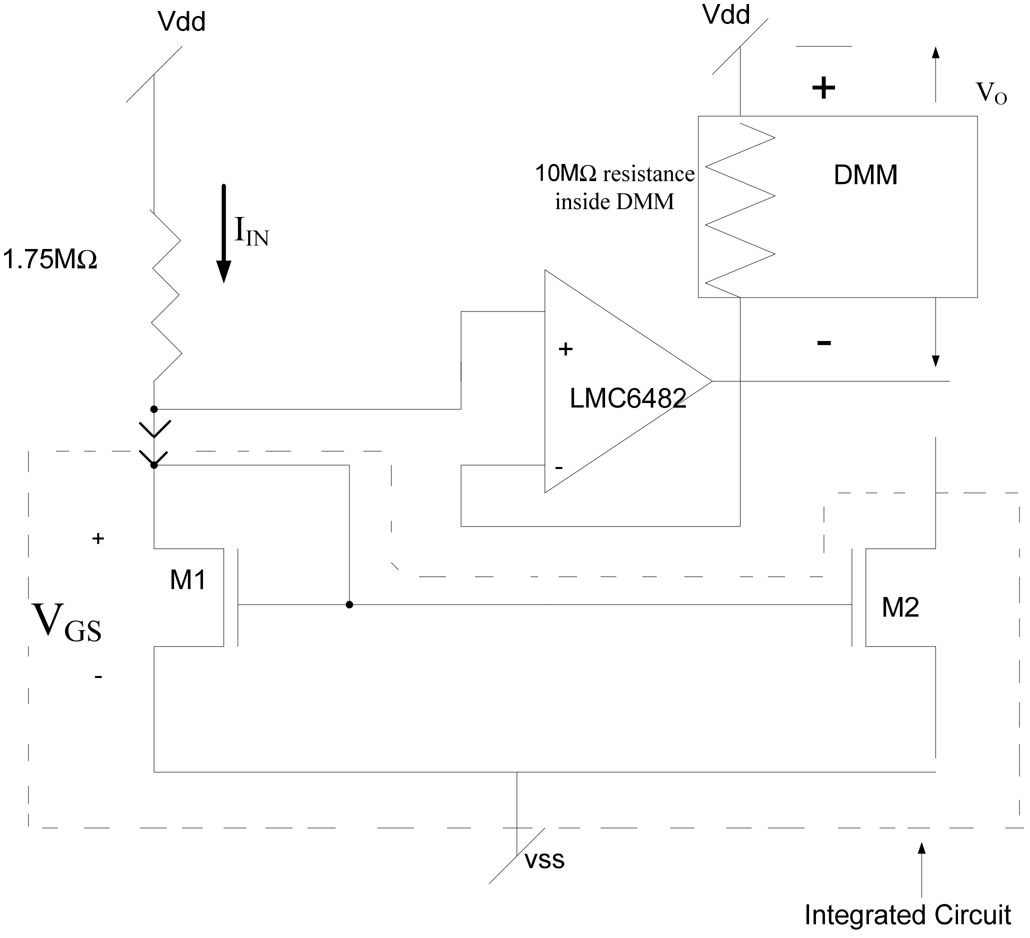


Figure 4.2 Set up for the generation of the bias current

It can be observed that $V_O = V_{GS}$ of transistor M1.

From the figure it can be found that

$$I_{IN} = \frac{Vdd - Vss - V_{GS}}{R}$$

Since the bias current is 1uA and $Vdd = 1.25\text{V}$, $Vss = -1.25\text{ V}$

$$R = \frac{2.5 - V_{GS}}{1\mu A}$$

An approximate value of V_{GS} can be found from simulations as 755mV. As such, R is found to be 1.75MΩ. Pictures of the complete test setup are shown in Appendix C. Since the DMM has internal resistance of 10MΩ, if it is connected directly across the the resistor, the output may give erroneous value. So LMC 6482 op-amp is used which acts as voltage follower.

4.2 Set up for Testing Offset

The set up for testing the DC offset is shown in the figure 4.2 below.

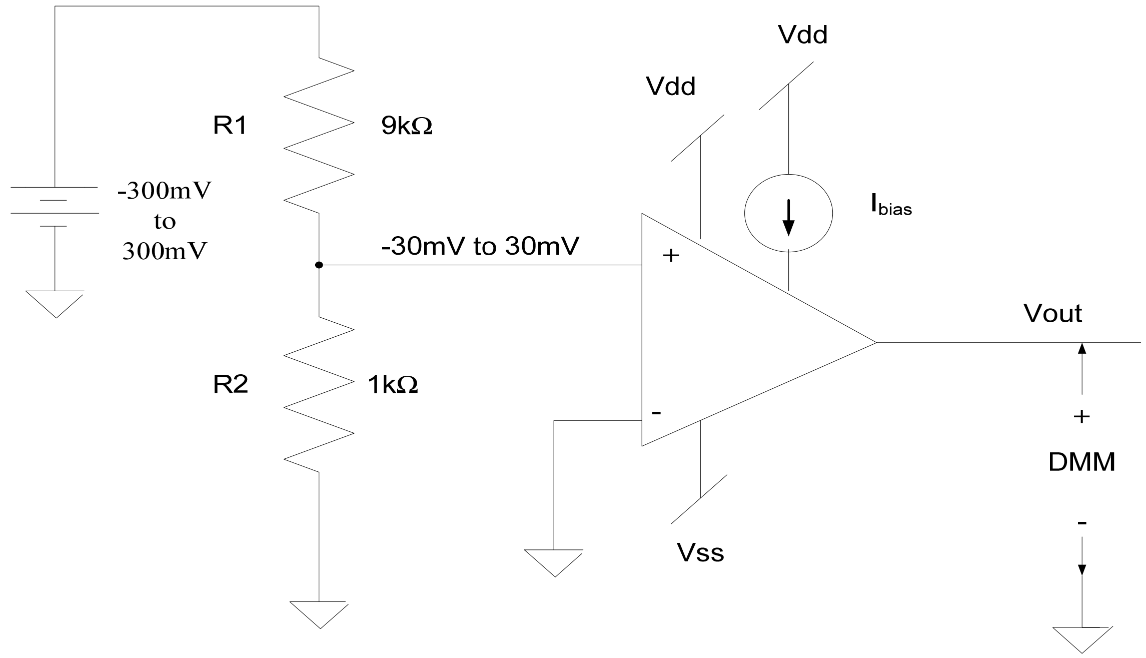


Figure 4.3 Test set up for testing offset

The set up consists of a programmable power supply, a voltage divider and a digital multimeter. The input of the voltage divider is connected to the DC supply. The output of the voltage divider is connected to the positive input of the comparator. The values of resistances *R1* and *R2* in the voltage divider are chosen such that the positive input of the comparator is 10 times the input of the voltage divider. So *R1* and *R2* are chosen as 9kΩ and 1kΩ respectively. Varying the DC supply from -50mV to 50mV is equivalent to varying the positive input of the comparator from -5mV to 5mV. The output of the comparator is measured using the multimeter. The input voltage at which output voltage switches state from *Vss* to *Vdd* is noted and the programmed input voltage is the offset voltage.

The measured DC offset voltage of each comparator is shown in table 4.1.

4.2.1 Setup for Testing the Amount of Hysteresis

The set up in figure 4.2 can be followed for testing the amount of hysteresis. Instead the DC supply is varied from -150mV to 150mV. This is equivalent to varying the positive input of the comparator from -15mV to 15mV. The output of the comparator suddenly goes high at certain input voltage and the voltage is noted down as *vphyst*. Again the DC supply is varied from 150mV to -150mV. The output of the comparator suddenly goes low at a certain input voltage and the voltage is noted down as *vmhyst*. The amount of hysteresis is the difference between the *vphyst* and *vmhyst*. The offsets of the comparators with hysteresis can be calculated as the average of *vphyst* and *vmhyst*. The offset voltages of the three-stage comparator with internal hysteresis, three-stage comparator with external hysteresis, folded-cascode comparator with internal hysteresis and folded-cascode comparator with external hysteresis are shown in table 4.3. The reason for the disparity of offsets in folded-cascode comparators will be explained in section 4.4.

For the three-stage comparator with internal hysteresis and three-stage comparator with external hysteresis, the hysteresis currents were 47nA and 500nA respectively. These currents were generated using 40.5MΩ and 3.6MΩ respectively. The set up in figure 4.1 is used for generating these currents. For the folded-cascode comparator with internal hysteresis and folded-cascode comparator with external hysteresis, the hysteresis currents were 55nA and 500nA respectively. These currents were generated using 34.2MΩ and 3.6MΩ respectively.

4.3 Test setup for delays

The input signal, a square wave is applied through a waveform generator. The output waveform is observed on an oscilloscope. The high-to-low and low-to-high propagation delays are determined from the input and output waveforms. DMM checked the switching levels of the output at 200mHz.

In the three-stage comparator, to determine low-to-high propagation delay, an input signal, square wave of frequency 100 kHz and an amplitude 1.259V(-1.25 to 10mV,went beyond 10mV above offset which is -1mV) and an offset of –0.6205V is applied to the positive input through a waveform generator. A source resistance of 1KΩ is connected to the positive input. The input and output waveforms were observed on an oscilloscope. From the waveforms, the low-to-high propagation delay is observed as 720ns. The peak-to-peak amplitude of the output is observed to be 2.5V. The plots are shown in the figure below.

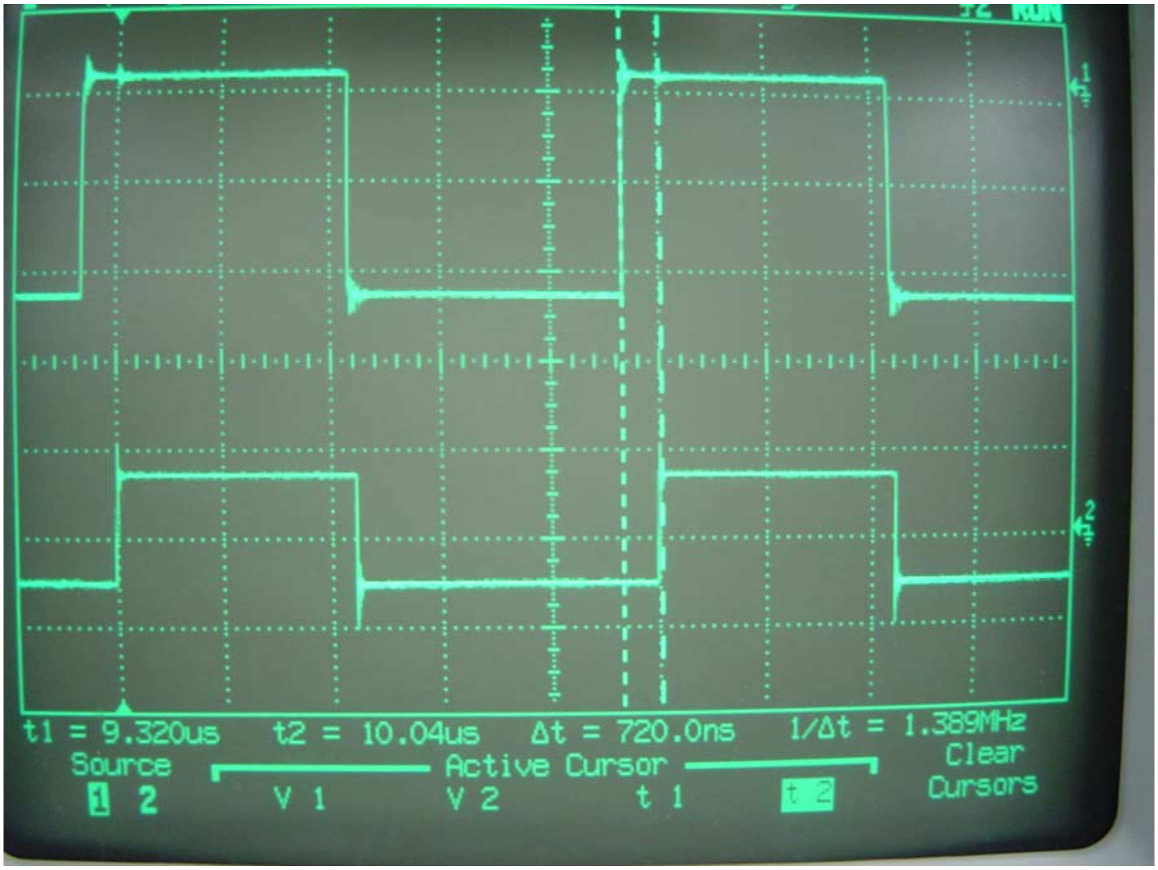


Figure 4.4 input and output waveforms of three stage comparator when the input is varied from -1.25V to 10mV, I_{bias} *= 1µA, Vdd = 1.25V, Vss = -1.25V*

To determine high-to-low propagation delay, , an input signal, square wave of frequency 100 kHz with an amplitude 1.261V(1.25 to -10mV,went beyond -10mV above offset which is -1mV) and an offset of 0.6195V is applied to the positive input through a waveform generator. The input and output waveforms were observed on an oscilloscope. From the waveforms, the low-to-high propagation delay is observed as 560ns. The peak-to-peak amplitude of the output is found to be 2.5V. The plots are shown in the figure below.

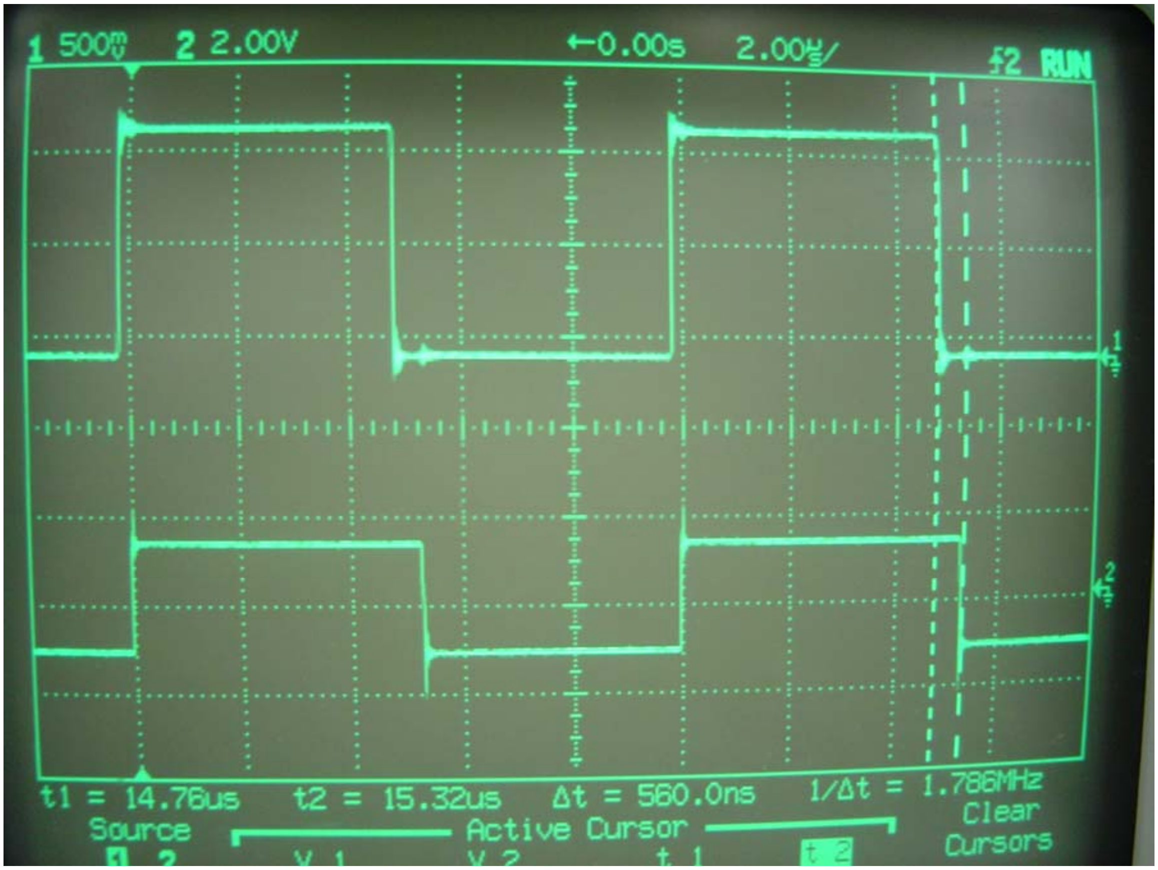


Figure 4.5 input and output waveforms of three stage comparator when the input is varied from 1.25V to -10mV, I_{bias} = 1µA, Vdd = 1.25V, Vss = -1.25V

The input and output waveforms of the folded cascode comparator are shown in the figure below. The low-to-high and high-to-low propagation delays are measured as 680ns and 640ns respectively.

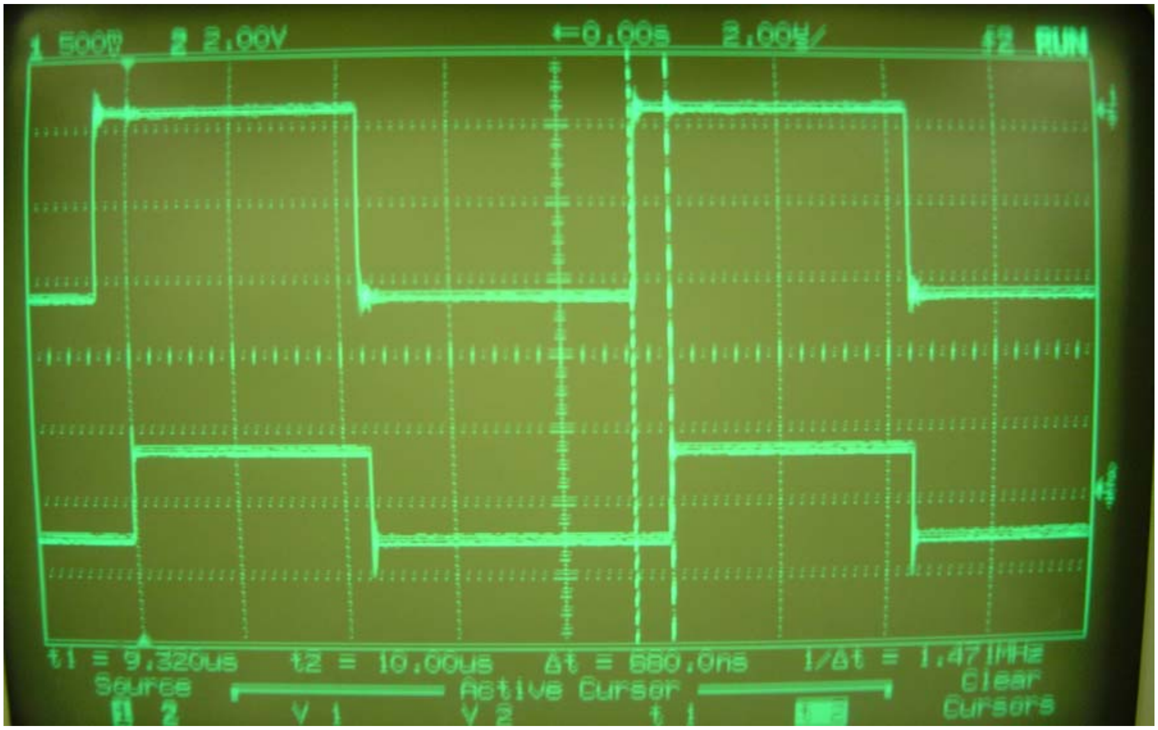


Figure 4.6 input and output waveforms of folded-cascode comparator when input signal is varied from -1.25 to 10mV, I_{bias} = 1μA, Vdd = 1.25V, Vss = -1.25V

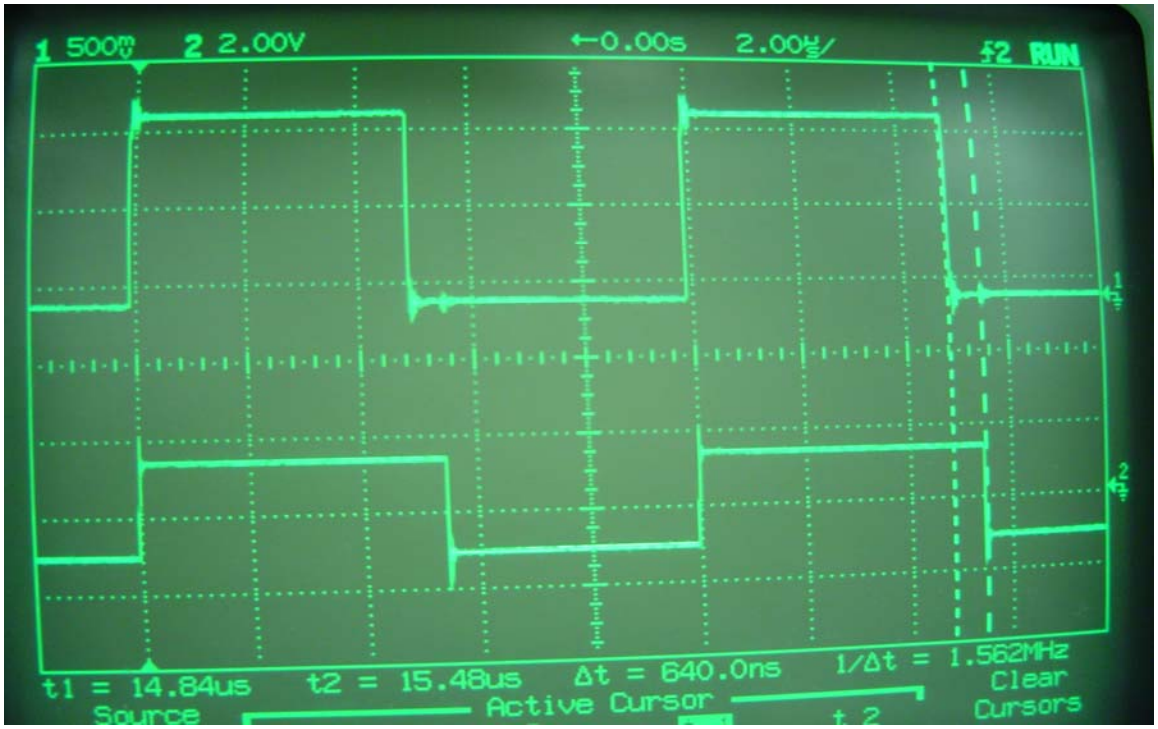


Figure 4.7 input and output waveforms of folded-cascode comparator when input signal is varied from 1.25 to -10mV, I_{bias} = 1μA, Vdd = 1.25V, Vss = -1.25V

The input and output waveforms of the three-stage comparator with internal hysteresis are shown in the figure below. The low-to-high and high-to-low propagation delays are measured as 1240ns and 640ns respectively.

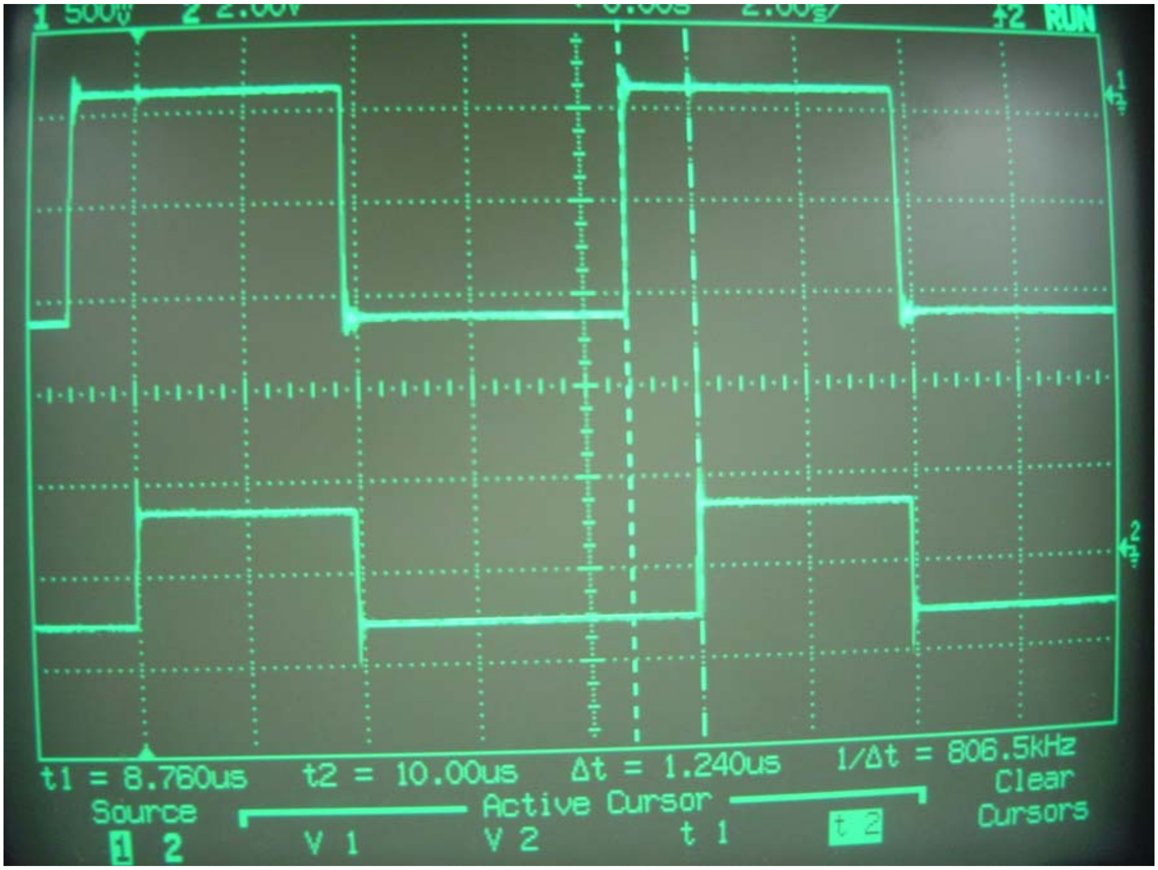


Figure 4.8 input and output waveforms of three-stage comparator with internal hysteresis when input signal is varied from -1.25 to 15mV, $I_{bias} = 1\mu A$, $I_{hyst} = 47nA$, Vdd = 1.25V, Vss = -1.25V

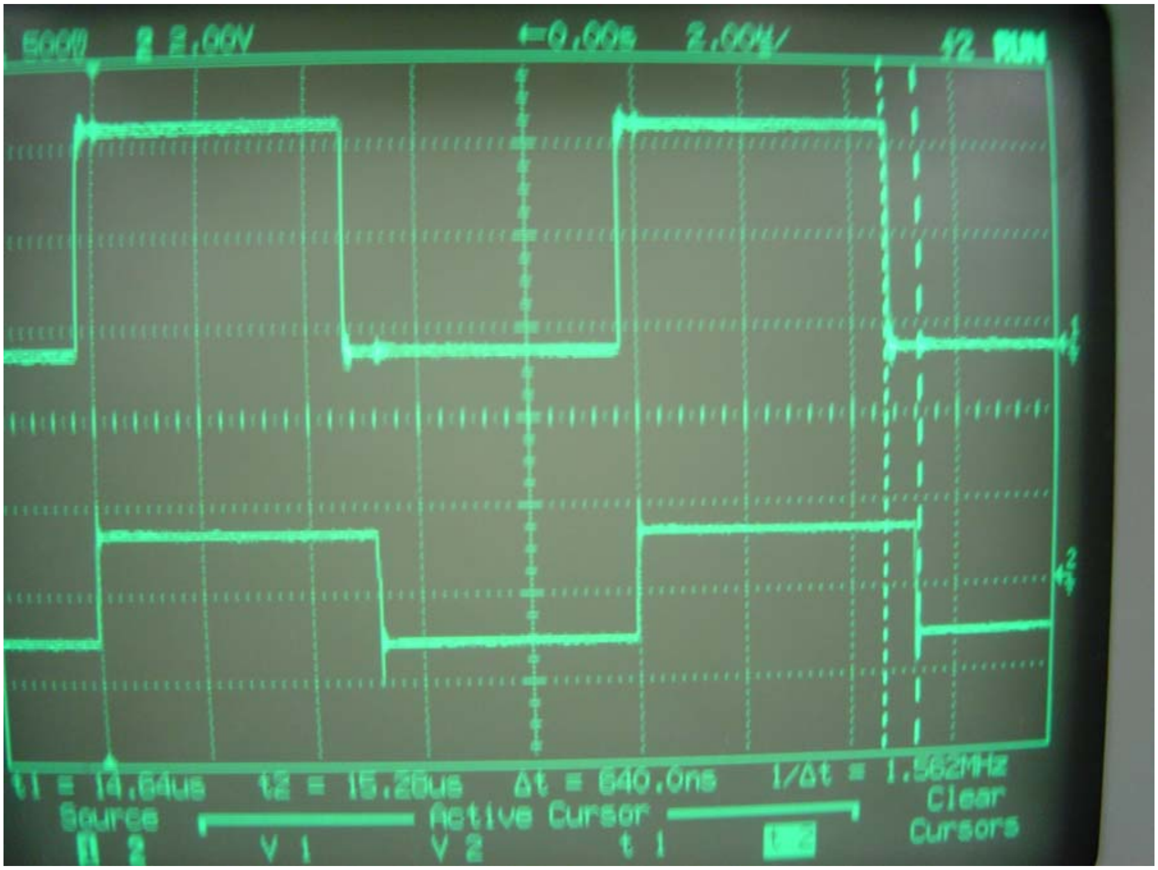


Figure 4.9 input and output waveforms of three-stage comparator with internal hysteresis when input signal is varied from 1.25 to -15mV, I_{bias} = 1µA, I_{hyst} = 47nA, Vdd = 1.25V, Vss = -1.25V

The input and output waveforms of the folded-cascode comparator with internal hysteresis are shown in the figure below. The low-to-high and high-to-low propagation delays are measured as 840ns and 880ns respectively.

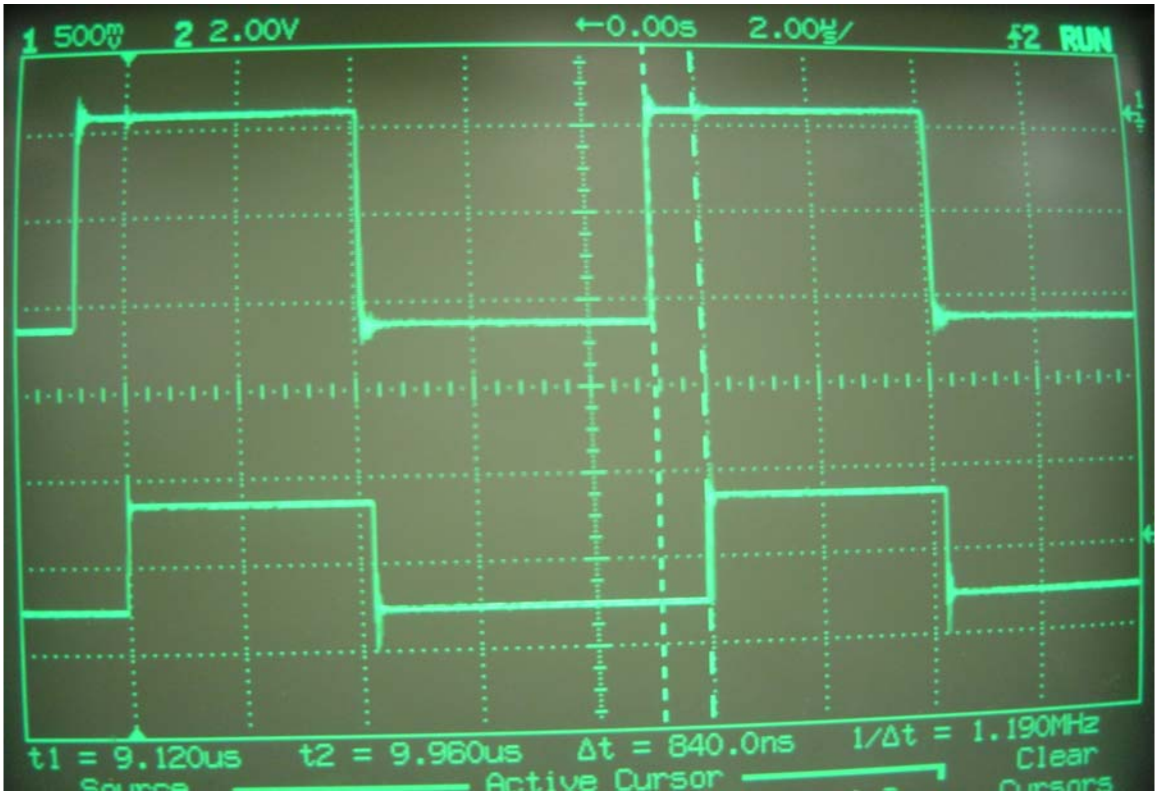


Figure 4.10 input and output waveforms of folded-cascode comparator with internal hysteresis when input signal is varied from -1.25 to 15mV, $I_{bias} = 1\mu A$*,* $I_{hyst} = 55nA$*, Vdd = 1.25V, Vss = -1.25V*

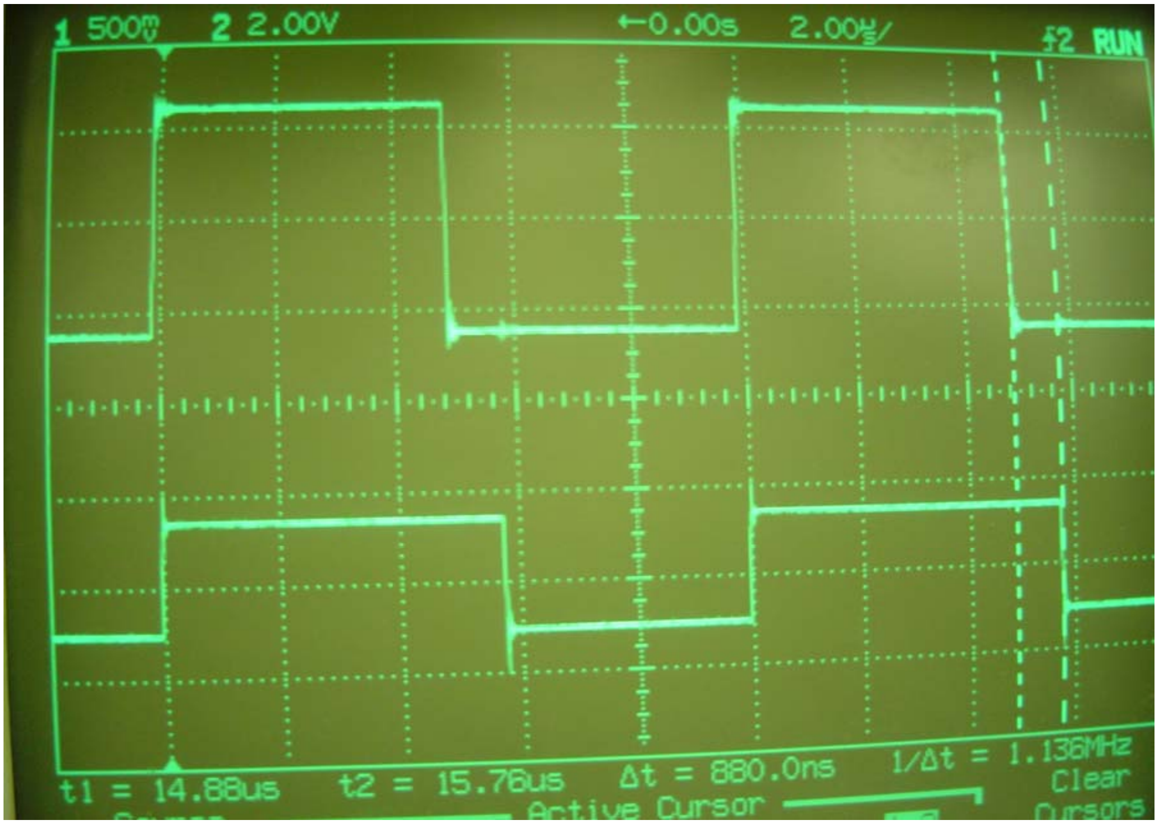


Figure 4.11 input and output waveforms of folded-cascode comparator with internal hysteresis when input signal is varied from 1.25 to -15mV, $I_{bias} = 1\mu A$, $I_{hyst} = 55nA$, *Vdd = 1.25V, Vss = -1.25V*

The input and output waveforms of the three-stage comparator with external hysteresis are shown in the figure below. The low-to-high and high-to-low propagation delays are measured as 760ns and 600ns respectively.

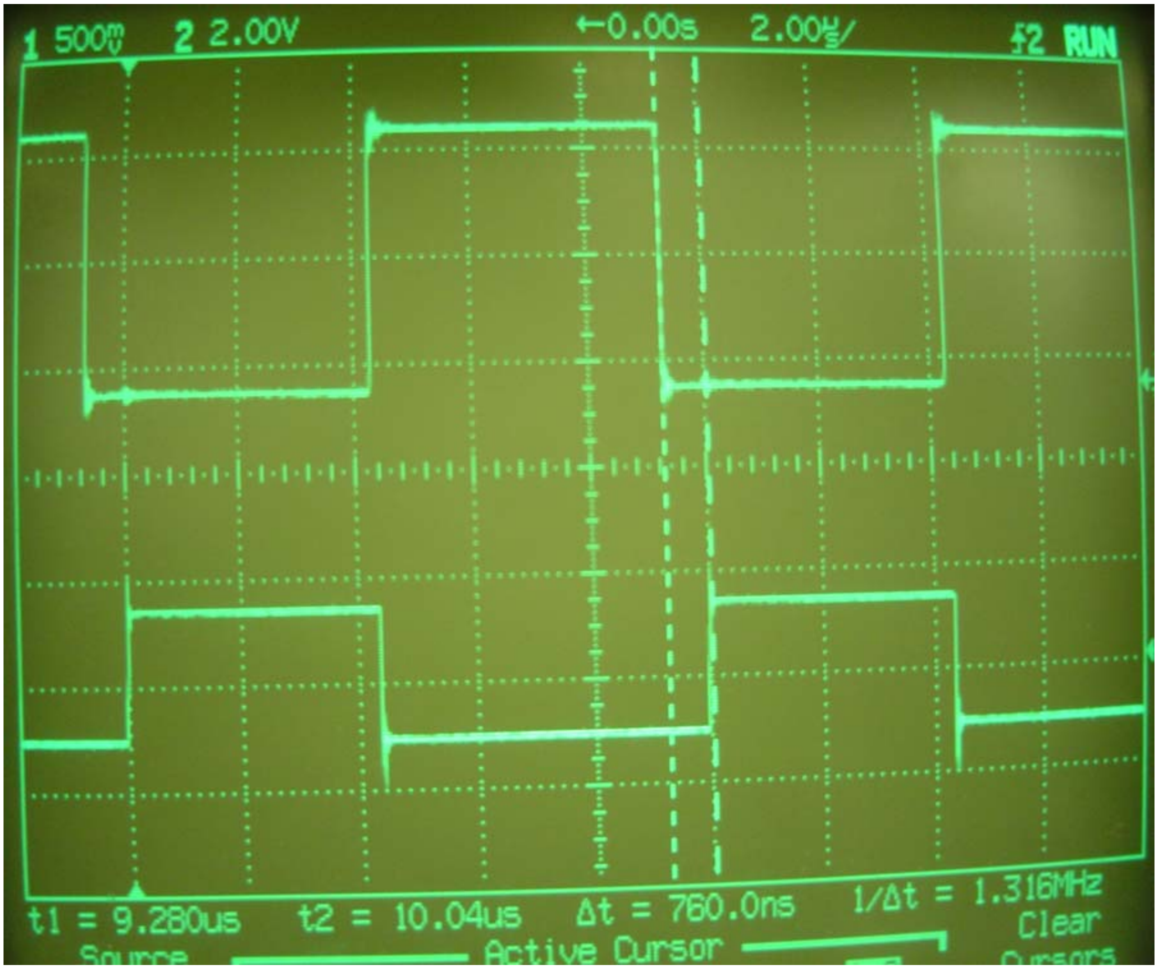


Figure 4.12 input and output waveforms of three-stage comparator with external hysteresis when input signal is varied from 1.25 to -15mV, $I_{bias} = 1\mu A$, $I_{hyst} = 500nA$, Vdd = 1.25V, Vss = -1.25V

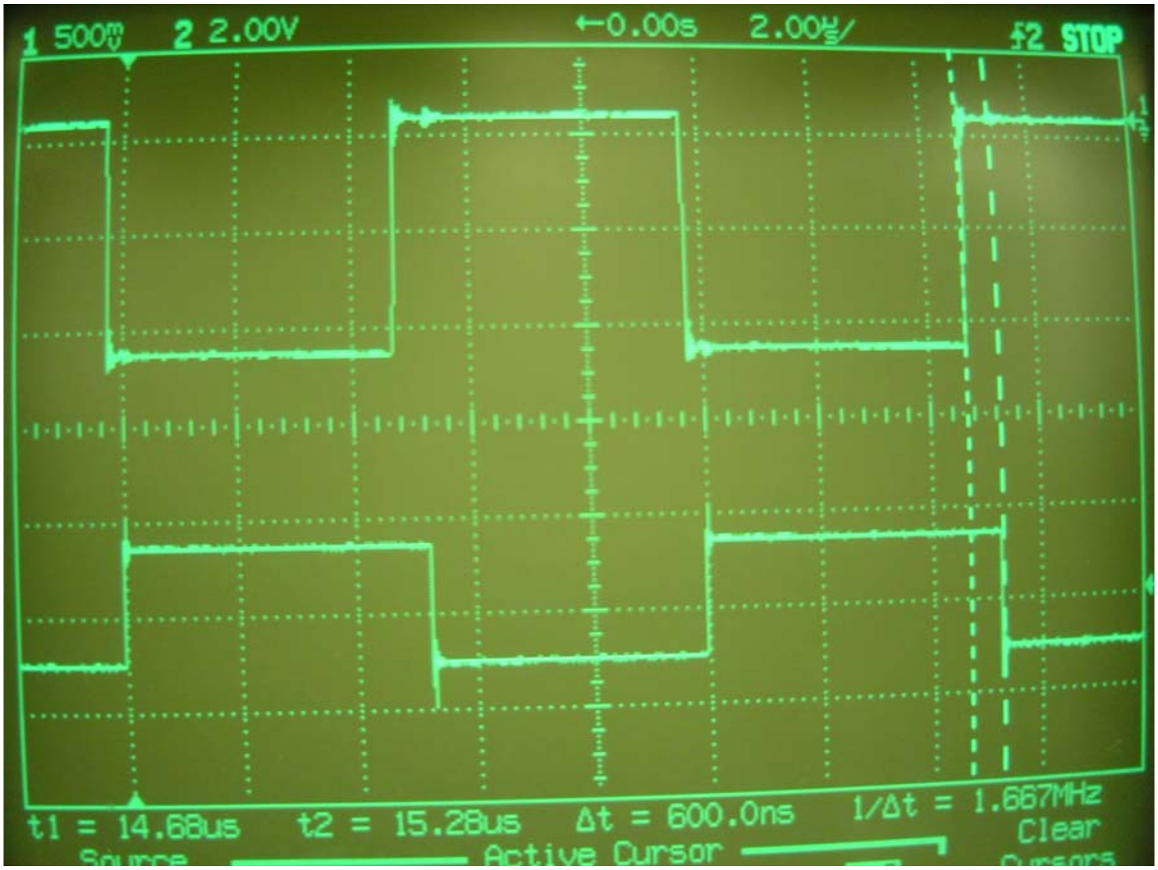


Figure 4.13 input and output waveforms of three-stage comparator with external hysteresis when input signal is varied from -1.25 to 15mV, $I_{bias} = 1\mu A$, $I_{hyst} = 500nA$, $Vdd = 1.25V$, $Vss = -1.25V$

The input and output waveforms of the folded-cascode comparator with external hysteresis are shown in the figure below. The low-to-high and high-to-low propagation delays are measured as 760ns and 1120ns respectively.

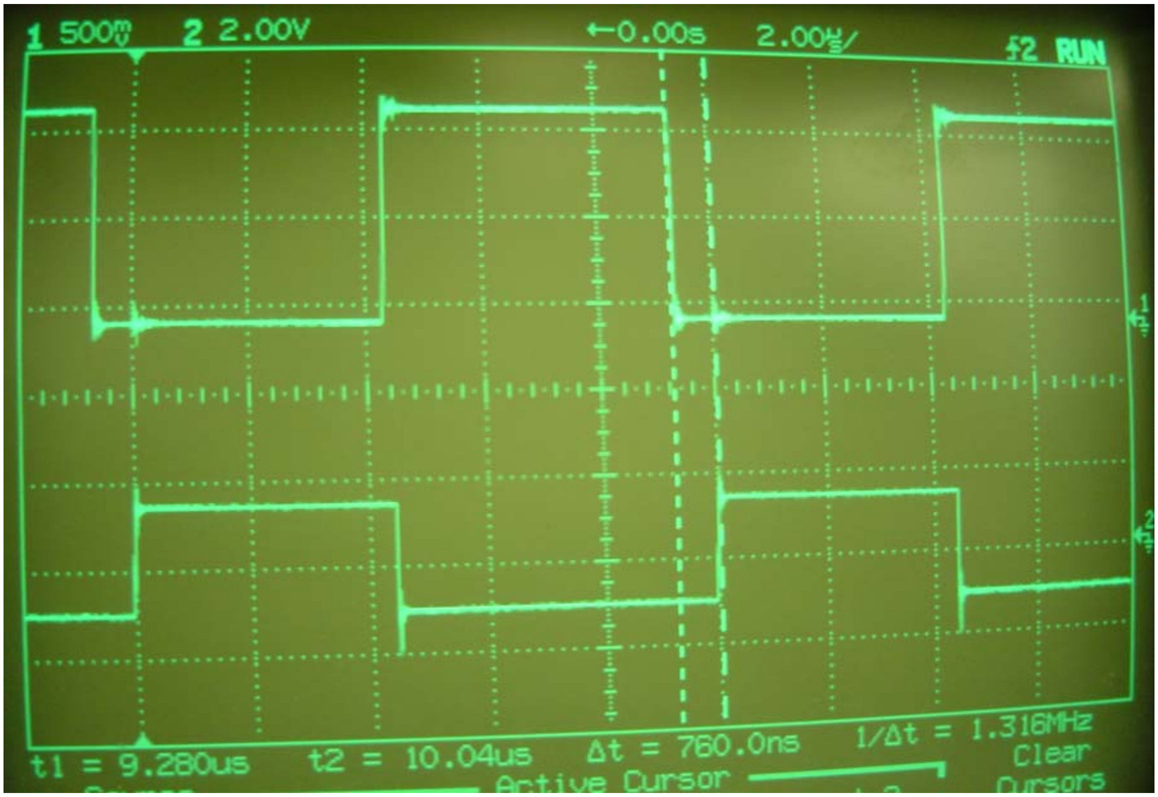


Figure 4.14 input and output waveforms of folded-cascode comparator with external hysteresis when input signal is varied from 1.25 to -15mV, $I_{bias} = 1\mu A$*,* $I_{hyst} = 500nA$*, Vdd = 1.25V, Vss = -1.25V*

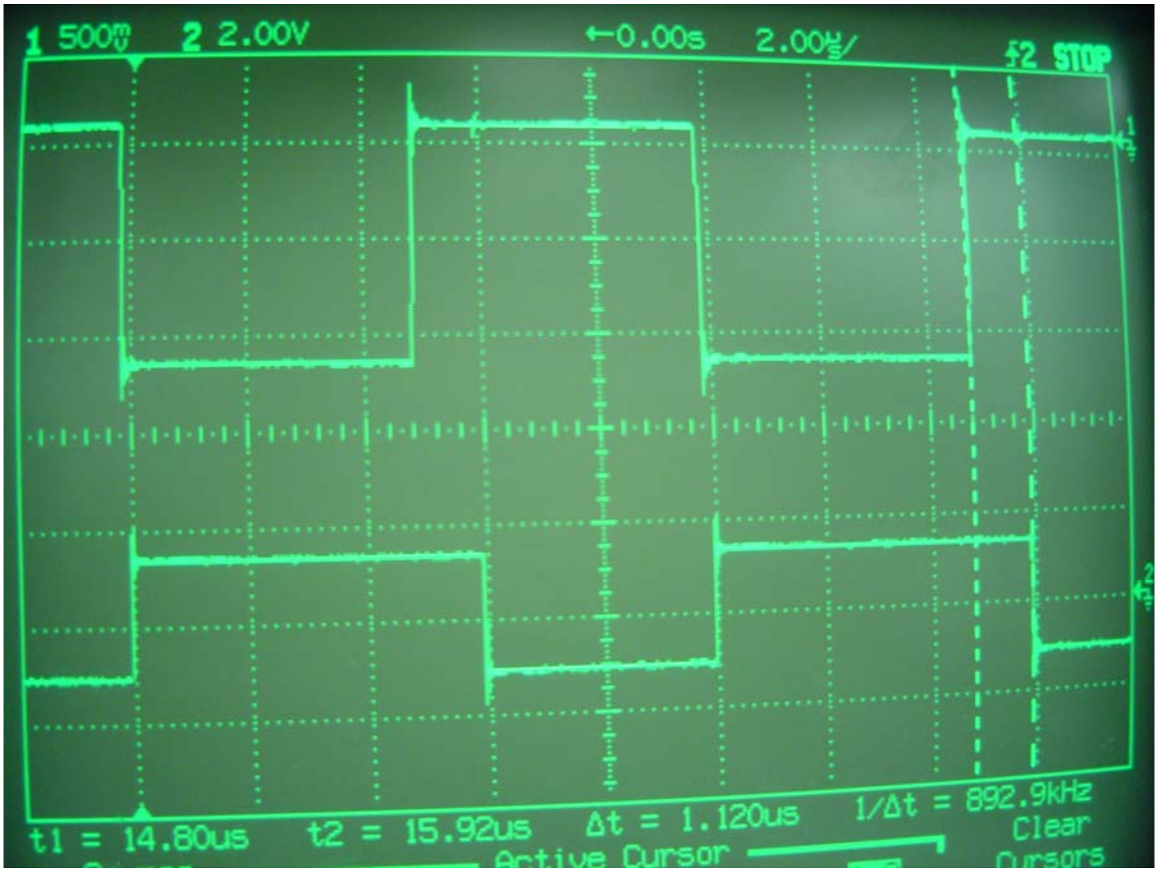


Figure 4.15 input and output waveforms of folded-cascode comparator with external hysteresis when input signal is varied from -1.25 to 15mV, I_{bias} = 1µA, I_{hyst} = 500nA, Vdd = 1.25V, Vss = -1.25V

4.4 comparisons of simulation results and test results

The following table in figure 4.15 shows the comparison of simulation results and test results of offsets and propagation delays.

Type of comparator	**Simulation results**			**Test results**			**% change in T_{LH}**	**% change in T_{HL}**
	Offset (mV)	*T_{LH} (ns)*	*T_{HL} (ns)*	*Offset (mV)*	*T_{LH} (ns)*	*T_{HL} (ns)*		
Three-stage comparator	0.140	866	664	-1	712	552	-17.7	-16.8
Folded-cascode comparator	0.360	880	799	-4	672	632	-23.6	-20.9
Three-stage comparator with internal hysteresis	-0.1	1203	729	-1	1232	632	2.4	-13.3
Folded-cascode comparator with internal hysteresis	-0.76	606	913	-10	792	872	23.4	-4.5
Three-stage comparator with external hysteresis	0.52	910	684	-1.5	752	592	-17.36	-13.4
Folded-cascode comparator with external hysteresis	0.9	899	937	-19	752	1112	-16.3	15.7

Table 4.1 comparisons of simulation and test results of offsets and propagation delays

The following tables 4.4 and 4.5 shows the comparisons of simulation results and test results of the amount of hysteresis and power dissipation. Bias currents, hysteresis currents and power supply voltages are held constant.

.

Type of comparator	**Simulation results**	**Test results**	**% difference**
	Amount of hysteresis	**Amount of hysteresis**	
Three-stage comparator with internal hysteresis	10.12	10	12
Folded-cascode comparator with internal hysteresis	10.3	8	22.5
Three-stage comparator with external hysteresis	10	9	10
Folded-cascode comparator with internal hysteresis	10.04	10	4

Table 4.2: comparisons of simulation and test results of amount of hysteresis

Type of comparator	**Simulation results**	**Test results**	**% difference in power dissipation**
	Power dissipation (μW)	*Power dissipation (μW)*	
Three-stage comparator	7.95	7.25	8.8
Folded-cascode comparator	15.875	14.75	7
Three-stage comparator with internal hysteresis	8.025	7.75	3.4
Folded-cascode comparator with internal hysteresis	16.34	15.25	6.6
Three-stage comparator with external hysteresis	8.5025	8.125	4.4
Folded-cascode comparator with internal hysteresis	20.25	19.75	2.4

Table 4.3: comparisons of simulation and test results of power dissipation

The following table 4.6 shows the randomness of offsets of different chips.

Type of comparator	**Chip2**	**Chip3**	**Chip4**	**Mean**	**Standard deviation**	**Range** **(mV)**
	Offset (mV)	Offset (mV)	Offset (mV)			
Three-stage comparator	-1	-2	-3	-2	0.816	-3 to -1
Folded-cascode comparator	-4	7	-10	-2.33	7.04	-10 to 7
Three-stage comparator with internal hysteresis	-1	2	3.5	1.5	1.87	-1 to 3.5
Folded-cascode comparator with internal hysteresis	-10	-19	15.5	-4.5	14.61	-19 to 15.5
Three-stage comparator with external hysteresis	-1.5	-3	5	0.167	3.50	-3 to 5
Folded-cascode comparator with external hysteresis	13	14.5	10	12.5	1.87	10 to 13.5

Table 4.4 Effect of randomness of offsets

4.5 Offset modeling

The following tables 4.5 and 4.6 attempts to explain the offsets in three-stage comparator and folded-cascode comparator. It is assumed that the area of the transistors is inversely proportional to the mismatch of the transistors. The reason for the offsets in three-stage comparator can be mainly attributed due to the mismatch in the mirroring transistors and differential pair transistors.

Transistors	**Area in μm^2**	**ΔW in µm**	**%change**	**Cumulative**	
				Max offset in mV	**Min offset in mV**
Differential pair	25.92	0.45	1.4%	1.75	-1.457
Mirroring transistors	25.92	0.45	1.4%	2.959	-2.642
Differential bias	12.96	0.45	2.8%	2.974	-2.689
Common source bias	12.96	0.45	2.8%	3.108	-2.797
Common source transistor	19.44	0.45	1.87%	3.138	-2.801

Table 4.5 Effect of mismatch on offsets in Three-stage comparator

Here ΔW is the difference between the widths of the transistors. Area of the transistor can be calculated by multiplying the width and the length of the transistor. If the variations in differential pair transistors are such that ΔW is 0.45µm, then the maximum and minimum offsets are found to be 1.75mV and -1.457mV. Keeping these variations in tact, if the variations in mirroring transistors are such that ΔW is 0.45µm, then the maximum and minimum cumulative offsets are found to be 5.297 and -6.227mV. In the same way, if the mismatches are introduced in differential bias transistors, common source bias transistors and common source transistor, then the maximum and minimum cumulative offsets are found to be 3.138mV and -2.801mV respectively. From table 4.4, it can be observed that the range of offsets in three-stage comparator during testing is from -2mV to 3mV.

The following table 4.3 shows the effect of mismatches on offsets in folded-cascode comparator. The reason for large offsets in folded-cascode comparators can be largely attributed to the mismatch in differential pair transistors, cascoding transistors, mirroring transistors and differential bias transistors. It can be observed from table 4.3 that the effect of mismatch in mirroring transistors is larger than that of the differential pair transistors and cascoding transistors.

Transistors	**Area in μm^2**	**ΔW in μm**	**%change**	**Cumulative**	
				Max offset in mV	**Min offset in mV**
Differential pair	25.92	0.45	1.4%	1.241	-1.983
Current source (p-type)	25.92	0.45	1.4%	3.956	-4.689
cascoding (p-type)	9.72	0.45	3.72%	4.054	-4.811
Cascoding (n-type)	25.92	0.45	1.4%	4.061	-4.893
Mirroring (n-type)	9.72	0.45	1.4%	6.119	-6.98
Differential bias	12.96	0.45	2.8%	6.559	-7.404

Table 4.6 Effect of mismatches on offsets in folded-cascode comparator

The analysis of offset modeling of folded-cascode comparator can be done in the same way as that of the three-stage comparator. It can be observed from the table that if the mismatches are introduced in differential pair transistors, P-type current sources, p-type cacoding transistors, n-type cascoding transistors, n-type mirroring transistors and differential bias transistors, then the maximum and minimum cumulative offsets are found to be 6.559mV and -7.404mV respectively. From table 4.4, it can be observed that the range of offsets in folded-cascode comparator during testing is found to be -10mV to 7mV.

4.5.1 Offset model for comparators with hysteresis

The following table attempts to explain the offsets in three-stage comparator with hysteresis. During simulations, it can be observed from table 4.6 that the range of offsets in three-stage comparator with hysteresis is from -3.97mV to 3.92mV. During testing, it can be observed from table 4.4 that the range of offsets is from -1 to 3.5mV.

Transistors	**Area in μm^2**	**ΔW in µm**	**%change**	**Cumulative**	
				Max offset in mV	**Min offset in mV**
Differential pair	25.92	0.6	2.8%	2.02	-2.24
Mirroring transistors	25.92	0.6	2.8%	3.66	-3.84
Differential bias	12.96	0.6	5.6%	3.78	-3.88
Common source bias	12.96	0.6	5.6%	3.86	-3.90
Common source transistor	19.44	0.6	3.73%	3.90	-3.94
2nd differential pair	6.48	0.6	11.2%	3.91	-3.96
2nd differential bias	12.96	0.6	5.6%	3.92	-3.97

Table 4.7 Effect of mismatches on offsets in three-stage comparator with hysteresis

The following table attempts to explain the large offsets in folded-cascode comparator with hysteresis.

Transistors	**Area in µm^2**	**ΔW in µm**	**%change**	**Cummulative**	
				Max offset in mV	**Min offset in mV**
Differential pair	25.92	0.6	2.8%	1.34	-2.94
current source transistors (p-type)	25.92	0.6	2.8%	5	-6.58
cascoding transistors (p-type)	9.72	0.6	7.28%	5.12	-6.7
cascoding transistors (n-type)	25.92	0.6	2.8%	5.14	-6.74
Mirroring transistors (n-type)	9.72	0.6	7.28%	7.74	-9.33
Differential bias	12.96	0.6	5.6%	8.55	-10.37
2nd differential pair	6.48	0.6	11.2%	8.56	-10.38
2nd differential bias	12.96	0.6	5.6%	8.58	-10.40

Table 4.8 Effect of mismatches on offsets in folded-cascode comparator with hysteresis

5. CONCLUSIONS AND RECOMMENDATIONS

This report has dealt with the optimization of low voltage comparators with and with out programmable hysteresis. The comparators were fabricated and measurement results were compared with simulations. The circuits were operated at a frequency of 100 kHz and the input bias current of1µA.

The comparators were designed with low delay, low offset, high gain and low power dissipation. This project mainly deals with three-stage comparator and folded-cascode comparator. It can be observed that comparator output voltages are very close to the power supply voltage rails and their outputs would swing between these rails very fast, that is they have a very high slew rate. It can also be observed from chapter 4 that the folded-cascode comparator dissipates more power than three-stage comparator. The power consumption of three-stage comparator is approximately 7.5µW whereas for the three-stage comparator, it is 15µW. The offset of three stage comparator is lower than that of the folded cascode comparator because of the mismatches in the cascoding transistors in folded-cascode comparator. The gain of the three-stage comparator is higher than that of the folded-cascode comparator. It is also observed that the folded-cascode comparator consumes more area than the three-stage comparator.

For the comparators with hysteresis, it can be observed that by adjusting the hysteresis current, the amount of hysteresis can be varied. The method of adding programmable hysteresis is new and is not found in any literature.

Among the comparators without hysteresis, three-stage comparator is the best because it has high gain, low offset, low power consumption and it occupies less area.

Among the comparators without hysteresis, comparator with external hysteresis is the best because the variation of hysteresis current with the amount of hysteresis is linear.

APPLICATIONS

Comparators are generally used in analog computation and signal generation. They are also used in the detection of zero crossings. Comparators are used in such devices as switched capacitor filters, analog to digital converters and power management circuits.

FUTURE WORK

The future work could be to design a comparator with low offsets.

APPENDIX A

The figures shown below are the layouts of three-stage comparator three-stage comparator with internal hysteresis, three-stage comparator with external hysteresis, folded-cascode comparator, folded-cascode comparator with internal hysteresis, folded-cascode comparator with external hysteresis and the the layout of the chip.

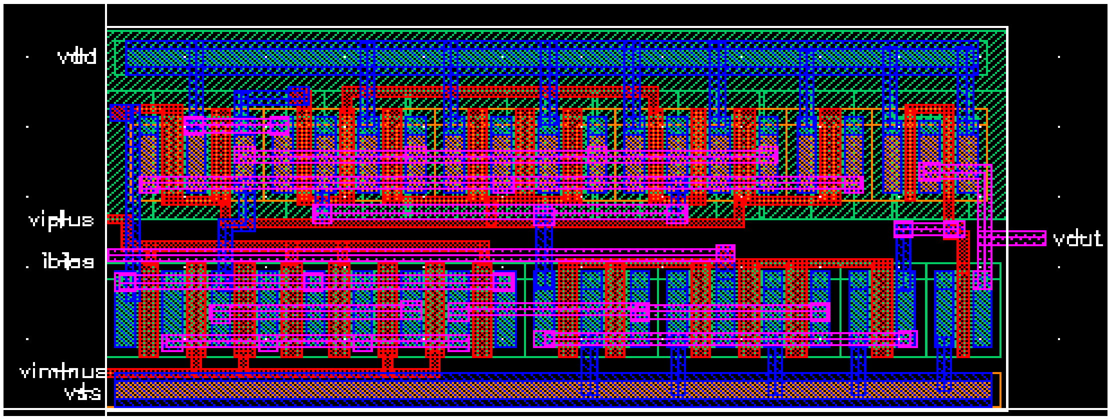


Figure A.1 Layout of the three-stage comparator

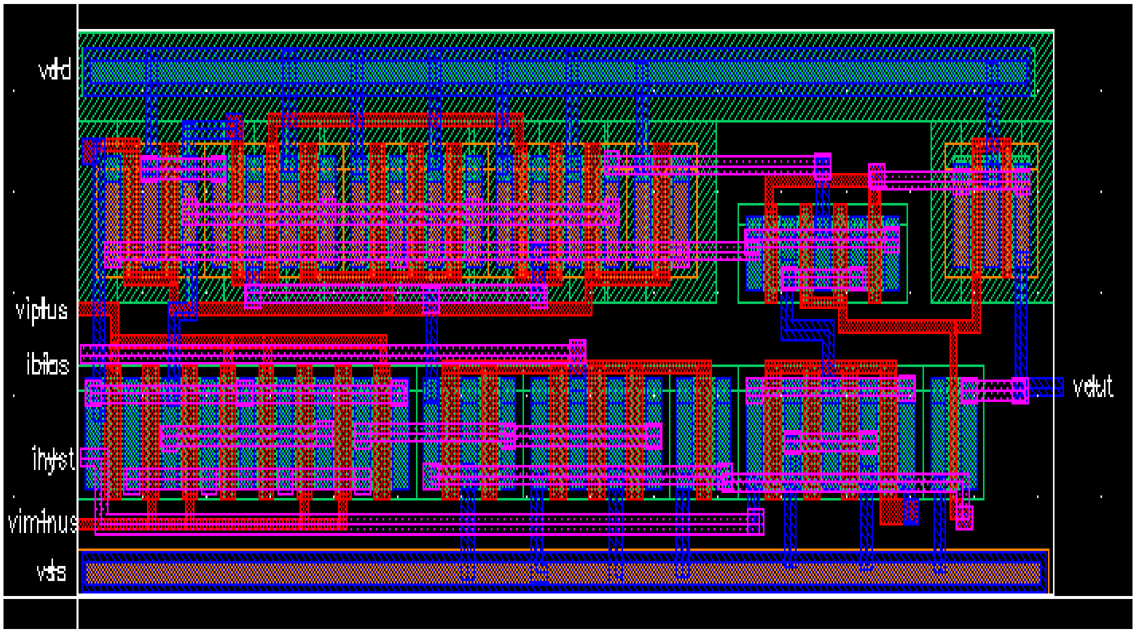


Figure A.2 Layout of the three-stage comparator with internal hysteresis

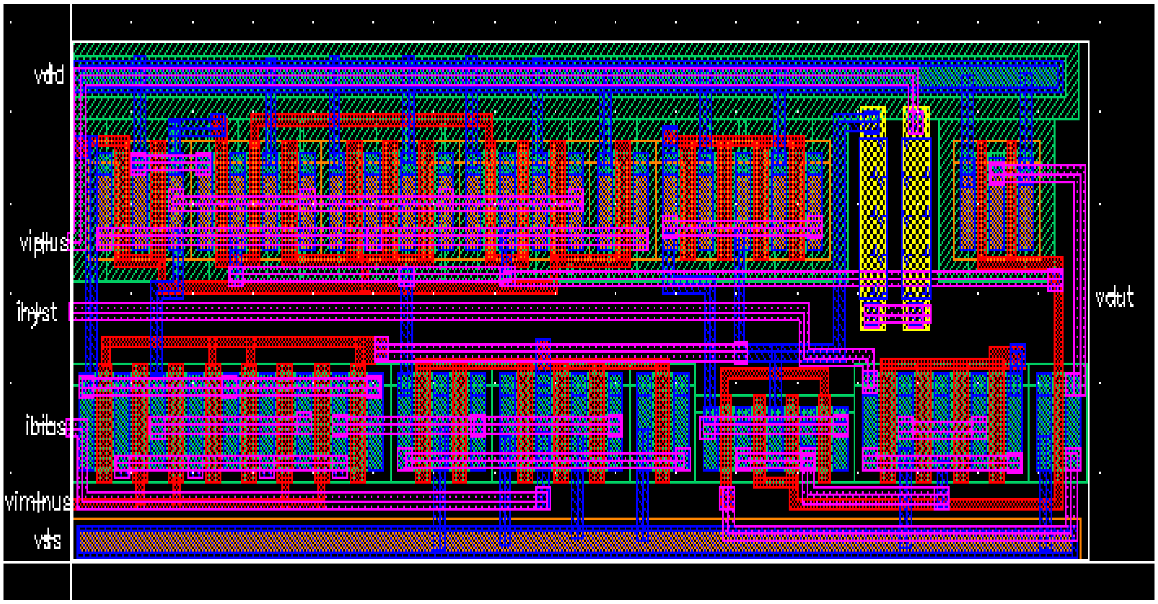


Figure A.3 Layout of the three-stage comparator with external hysteresis

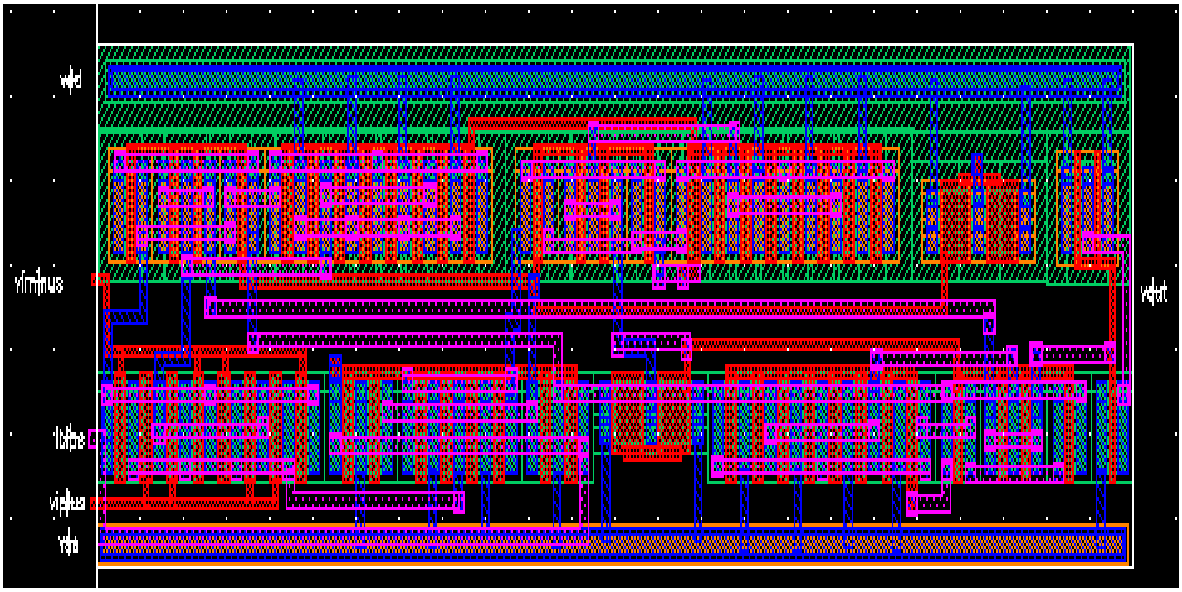


Figure A.4 Layout of the folded-cascode comparator

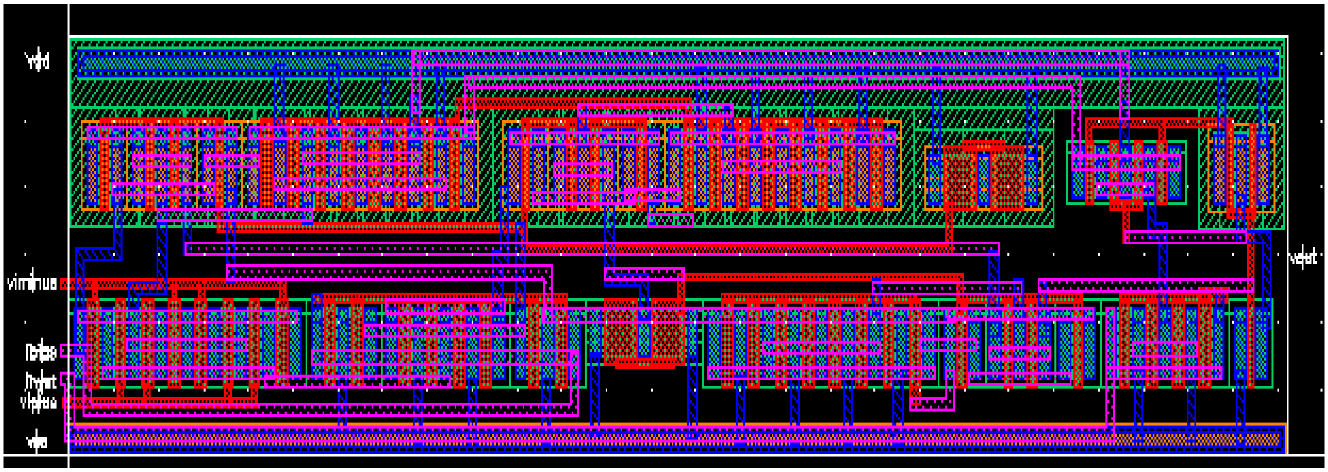


Figure A.5 Layout of the folded-cascode comparator with internal hysteresis

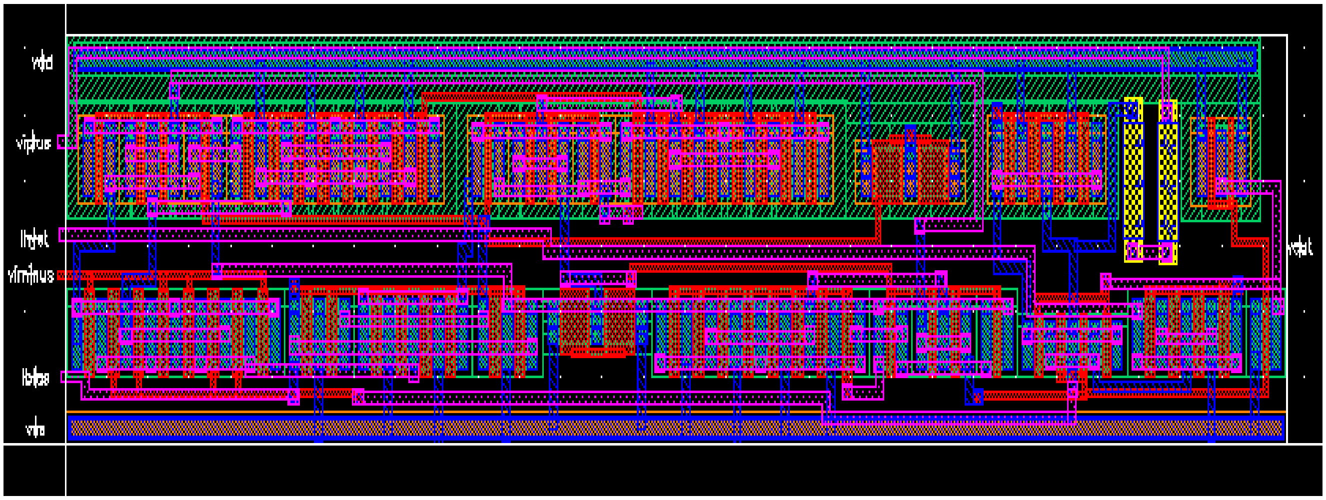


Figure A.6 Layout of the folded-cascode comparator with external hysteresis

APPENDIX B

The following figures B1. and B.2 shows the pictures of test setup and lab apparatus respectively.

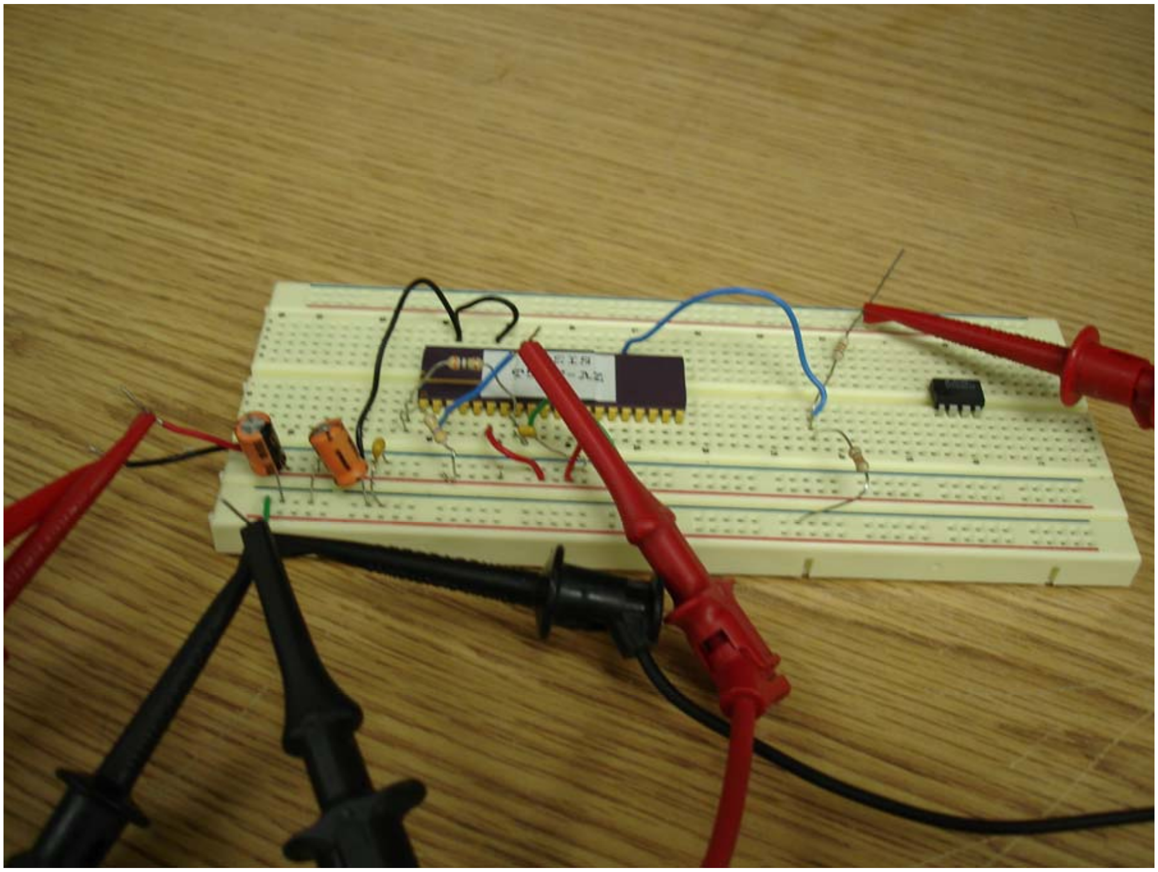


Figure B.1 Test setup

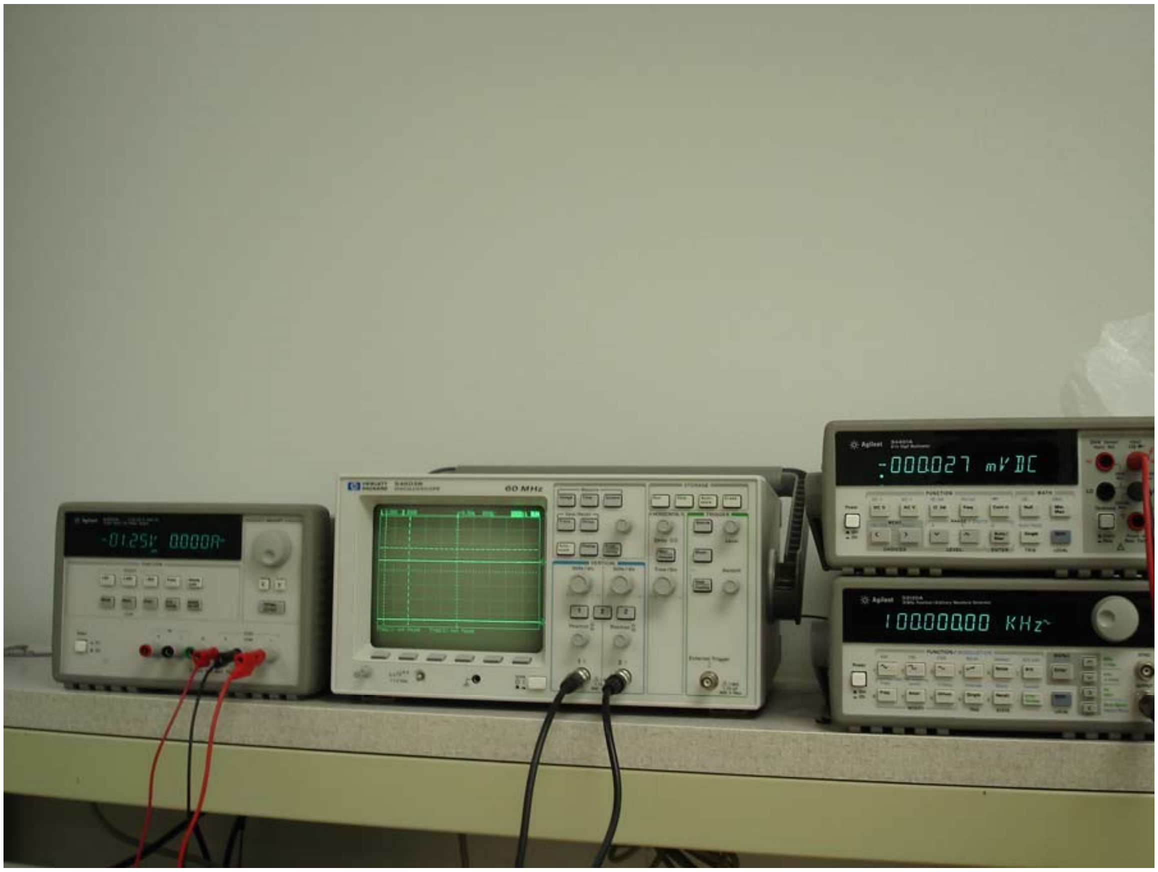


Figure B.2 Lab apparatus

APPENDIX C: MOSIS FILE, PIN CONFIGURATION AND TEST PROCEDURE

Project Name: Low voltage CMOS comparator with programmable hysteresis
Project Author: Vishnu b kulkarni
Submitted : May 23rd 2005.
Fabrication : 0.5 µm AMI double-poly n-well with 3 metal layers.
Apparatus : Signal Generator, Oscilloscope, DMM and a breadboard.
Description : Comparators with and without hysteresis.

Your "NEW-PROJECT" request was executed.

Project Status

- * Design 73228 status: WAITING FOR LAYOUT
- * Design name: comparator_vbk
- * E-mail address: vishnu2981@yahoo.com,pfurth@nmsu.edu
- * Phone number: 505-646-4008
- * Technology: SCN3ME_SUBM, lambda = 0.3
- * Fabrication restricted to AMI only.
- * Fill to be added: by MOSIS
- * This project can be fabricated on a AMI_C5F run.
- * Layout file: not present
- * Intended disposition: RESEARCH
- * Requested packaging: DIP40 [MOSIS to generate bonding diagram] (5 parts)

* Maximum die size: 7366 x 7366

To request fabrication for your project, use the Fabricate Form
MOSIS Reply Id 00202065-001-002 / 23-MAY-2005 13:52:17

myIPaddress.com

Your computer's IP address is:*

128.123.131.138

crcchecksum 73748656 274432 comparator_vbk.gds

Your "FABRICATE" request was executed.

Request Notes

- For help with the Design File FTP Server, see http://www.mosis.org/Faqs/faq-ftp_server.html

* Waiting for ftp transfer of your design file. Please ftp to ftp.design.mosis.org from host "128.123.131.138", login as user "73228" and put your file under name "comparator_vbk.gds". Transfer authorization will expire in 8 h 0 min 0 s.

Project Status

- Design 73228 status: IN TRANSIT
- Design name: comparator_vbk
- E-mail address: vishnu2981@yahoo.com,pfurth@nmsu.edu
- Phone number: 505-646-4008
- Technology: SCN3ME_SUBM, lambda = 0.3
- Fabrication restricted to AMI only.
- Fill to be added: by MOSIS
- This project can be fabricated on a AMI_C5F run.
- Layout format: GDS
- Top or root structure is "chip".
- Layout file: waiting for your ftp
- Waiting for ftp transfer of design file from host "128.123.131.138" into file "comparator_vbk.gds" within 7 h 59 min 59 s
- Intended disposition: RESEARCH
- Requested packaging: DIP40 [MOSIS to generate bonding diagram] (5 parts)

* Maximum die size: 7366 x 7366

MOSIS Reply Id 00202070-001-002 / 23-MAY-2005 14:04:14

Your "FABRICATE" request was executed.

Request Notes:

For help with the Design File FTP Server, see
http://www.mosis.org/Faqs/faq-ftp_server.html

Waiting for ftp transfer of your design file. Please ftp to
ftp.design.mosis.org from host "128.123.131.138", login as
user "73228" and put your file under name
"comparator_vbk.gds". Transfer authorization will expire
in 8 h 0 min 0 s.

Project Status:

Design 73228 status: IN TRANSIT

Design name: comparator_vbk
E-mail address: vishnu2981@yahoo.com,pfurth@nmsu.edu
Phone number: 505-646-4008
Technology: SCN3ME_SUBM, lambda = 0.3
Fabrication restricted to AMI only.
Fill to be added: by MOSIS
This project can be fabricated on a AMI_C5F run.
Layout format: GDS
Top or root structure is "chip".
Layout file: waiting for your ftp
Waiting for ftp transfer of design file from host
"128.123.131.138" into file "comparator_vbk.gds" within 7 h
59 min 59 s
Intended disposition: RESEARCH
Requested packaging: DIP40 [MOSIS to generate bonding diagram]
(5 parts)
Maximum die size: 7366 x 7366

Mosis-Reply-Id: 00202070-001-001

The MOSIS Service Support support@mosis.org
Information Sciences Institute Web http://www.mosis.org
University of Southern California Phone 310.448.9400
4676 Admiralty Way, Suite 700 Fax 310.823.5624
Marina del Rey, CA 90292

TABLE 1:

Three stage comparator - tsc
Folded cascode comparator - fcc

Pin no	Name	Pad type	Description
1	voutfc1	Dig buffer	Output of the folded cascade comparator
2	vout3st3	Dig buffer	Output of the tsc with external hysteresis
3	vout3st2	Dig buffer	Output of the tsc with internal hysteresis
4	vout3st1	Dig buffer	Output of the tsc without hysteresis
5	NC	pad protect	no connection
6	vdd	pad protect	+1.25V to power all the comparators
7	vip3st1	pad protect	Positive input for the tsc without hysteresis
8	ibias3st1	pad protect	Bias current for the tsc without hysteresis
9	vim3st1	pad protect	Negative input for the tsc without hysteresis
10	Vip3st2	pad protect	Positive input for the tsc with internal hysteresis
11	ibias3st2	pad protect	Bias current for the tsc with internal hysteresis
12	ihyst3st2	pad bare	input hysteresis current for the tsc with internal hysteresis
13	vim3st2	pad protect	negative input for the tsc with internal hysteresis
14	vdd_pad	pad vdd	+1.25V to pad frame for output buffers and protection
15	vip3st3	pad protect	positive input of the tsc with external hystersis
16	ihyst3st3	pad bare	input hysteresis current for the tsc with external hysteresis
17	ibias3st3	pad protect	input bias current for the tsc with external hysteresis
18	vim3st3	pad protect	negative input for the tsc with external hysteresis
19	vimfc1	pad protect	negative input for the fcc without hysteresis
20	ibiasfc1	pad protect	input bias current for the fcc without hysteresis
21	vipfc1	pad protect	positive input for the fcc without hysteresis
22	vimfc2	pad protect	negative input for the fcc with internal hystersis
23	ibiasfc2	pad protect	input bias current for the fcc with internal hysteresis
24	ihystfc2	pad bare	input hysteresis current for fcc with internal hysteresis
25	vipfc2	pad protect	positive input for fcc with internal hysteresis
26	vipfc3	pad protect	positive input for fcc with external hysteresis
27	ihystfc3	pad bare	input hysteresis current for fcc with external hysteresis
28	vimfc3	pad protect	negative input for fcc with external hysteresis
29	ibiasfc3	pad protect	input bias current for the fcc with external hysteresis
30	inp		input signal for testing digital buffer
31	NC	pad protect	no connection
32	NC	pad protect	no connection
33	NC	pad protect	no connection
34	NC	pad protect	no connection
35	vss	pad vss	-1.25 V to power all the pads
36	NC	pad protect	no connection
37	outp	Dig buffer	output signal for testing digital buffer
38	vss	pad protect	-1.25V to power all the comparators

39	voutfc3	Dig buffer	output of the fcc with external hysteresis
40	voutfc2	Dig buffer	output of the fcc with internal hysteresis

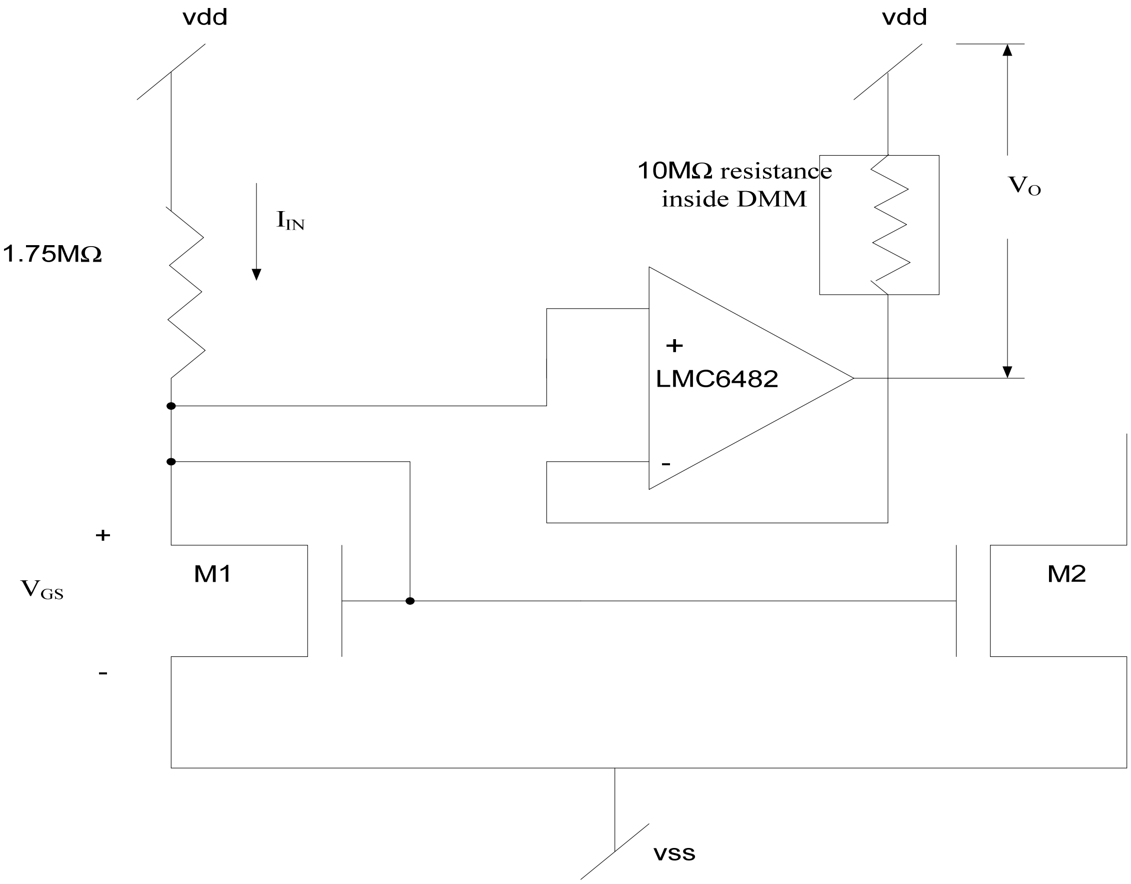
Suggested Test procedure

Split supplies: vdd = +1.25 V (logic 1) AGnd = 0 V, vss = -1.25 V (logic 0)

1. Only hook up vdd (pin 14) and vss (pin 35) to the PADS. Smell and touch chip to see if on fire.

2. Attach a function generator to the inp (pin30). Attach x10 scope probe to outp (pin 37). Apply a test input signal, sinusoidal wave 10 MHz, +/- 2.5V (pin 30) and observe the same signal at the output of the digital buffer (pin 37). Increase the frequency gradually and observe the output.

3. For the three stage comparator (without hysteresis), supply ibias3st1 (pin 8), a current of 1uA (1.74Mohm resistor from vdd)



It can be observed that V0 = Vgs of transistor M1.
From the figure it can be found that

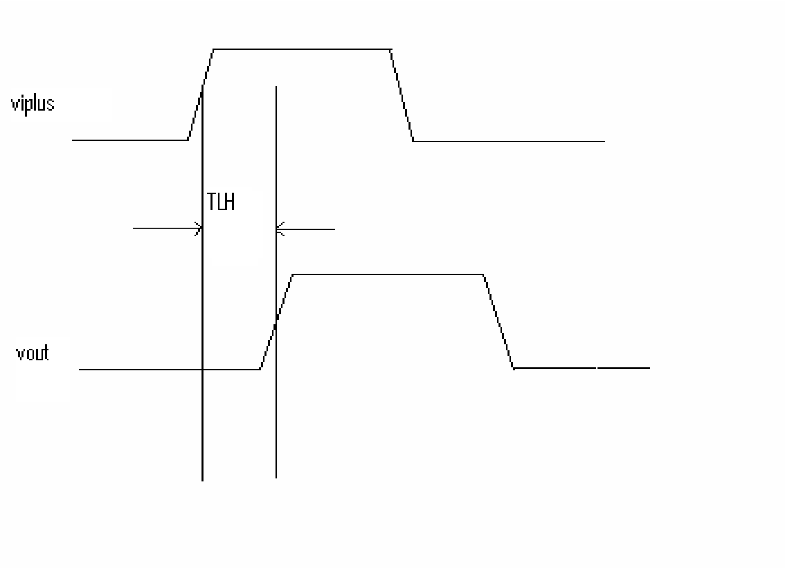
$$Iin = (vdd - Vgs)/ R$$

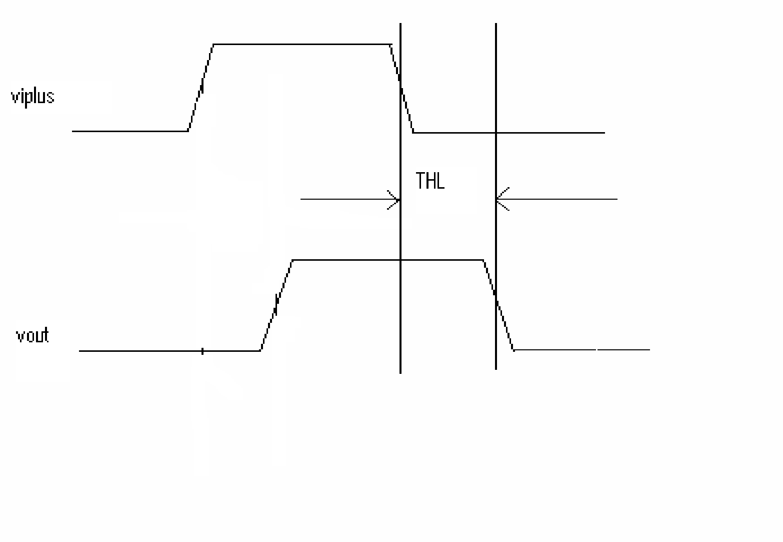
Since the bias current is 1uA and vdd = 1.25V, R = (2.5 – Vgs) / 1uA
Vgs is found to be 755mV (from the simulations).
R = (2.5-0.755) / 1uA = 1.745Mohms.

4. Short vim3st1 (pin 9) to AGnd (0V). Vary the DC supply from -50mV to 50mV. A voltage divider circuit is shown below. Attach the DC supply to the input of the voltage divider circuit. Connect the output of the voltage divider circuit to the positive input (vip3st1, pin7) of the three stage comparator, vout3st1 (pin 4). Measure the output voltage of the tsc (without hysteresis) using DMM (Digital multimeter). Measure the input voltage at which output voltage of the comparator goes to 0V. The measured voltage is the **offset voltage**.

5. Test the digital pad (pin 4). Apply an input signal, square wave of frequency 100 KHz and amplitude 1.26V (-1.25 to 10mV, Go beyond 10mV above offset) and offset = -0.62V to positive input (vip3st1, pin 7). Attach pin 9 to the signal ground. Test the comparator output through the digital buffer at pin 4. The peak to peak amplitude of the output should be 2.5V. Observe the output signal (square wave) and input signal (square wave) on the oscilloscope. Measure the low to high **(T_{LH})** propagation delays.

Apply an input signal, square wave of frequency 100 KHz and amplitude 1.26V (1.25 to -10mV) and offset = 0.62V to positive input. (vip3st1, pin 7). Attach pin 9 to signal ground. Test the comparator output through the digital buffer at pin 4. The peak to peak amplitude of the output should be 2.5V. Measure the low to high **(T_{HL})** propagation delays.





5. Now gradually increase the frequency and find the max frequency where the comparator works.

Testing for offset:

6. Short vim3st1 (pin 9) to AGnd (0V). Vary the DC supply from -50mV to 50mV. A voltage divider circuit is shown below. Attach the DC supply to the input of the voltage divider circuit. Connect the output of the voltage divider circuit to the positive input (vip3st1, pin7) of the three stage comparator, vout3st1 (pin 4). Measure the output voltage of the tsc (without hysteresis) using DMM (Digital multimeter). Measure the input voltage at which output voltage of the comparator goes to 0V. The measured voltage is the **offset voltage**.

7. For the three stage comparator with internal hysteresis, follow the same procedure (steps1 to 6) except that also supply ihyst3st2 (pin 12) a current of 45nA. For generating this current, follow the procedure shown in **step 3.**

Calculating the amount of hysteresis :

8. Follow the set up shown in step 6.Instead vary the DC supply from -1000mV to 1000mV. At certain input voltage, the output suddenly goes high. Let it be **vphyst**. Note down the voltage. Now vary the DC supply from 1000mV to -1000mV. Note down the voltage at which the output suddenly goes low. Let it be **vmhyst. The amount of hysteresis** is the difference between vphyst and vmhyst.

9. For the folded cascode comparator with internal hysteresis, follow the same procedure (steps1 to 6) except that also supply ihystfc2 (pin 24) a current of 55nA. For generating this current, follow the procedure shown in **step 3.** For finding the delay; follow the procedure shown in **step 4**.

10. For the three stage comparator with external hysteresis, follow the same procedure except that supply ihyst3st3 (pin 16) a current of 500nA. For generating this current, follow the procedure shown in **step 3.** For finding the delay; follow the procedure shown in **step 4**.

11. For the three stage comparator with external hysteresis, follow the same procedure except that supply ihystfc3 (pin 27) a current of 500nA. For generating this current, follow the procedure shown in **step 3.** For finding the delay; follow the procedure shown in **step 4**.

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