UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Science

R.W. Brodersen	**Homework #7**	**EECS 140**
Mike Chen	**(Due 4/27/04)**	**Spring 2004**

1) Do problem 9.21 in G&M textbook with our device model and following changes.
   a) Vdd=1.2V, and Vss=0V.
   b) (W/L) of M3 and M4 are 5um/0.13um, and the rest of device are 10um/0.13um. (Note: you should derive your own (W/L) for M9)
   c) Vic=0.6V. Vsb of M9 = 0.

Device model:

```
.model nch nmos LEVEL=1 tox=2.6n vt0=0.3 gamma=0.2 phi=0.6 u0=250 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+ lambda=0.2
.model pch pmos LEVEL=1 tox=2.6n vt0=-0.3 gamma=0.2 phi=0.6 u0=100 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+ lambda=0.15
```

2) Given the circuits in Figure 1 and 2, answer the following questions in terms of gm, ro of transistors, capacitors and resistors denoted in the figures.
   a) Identify the feedback loop and type.
   b) Find out forward gain A, feedback gain f, and loop gain T.
   c) Find out closed loop gain, input and output impedance.

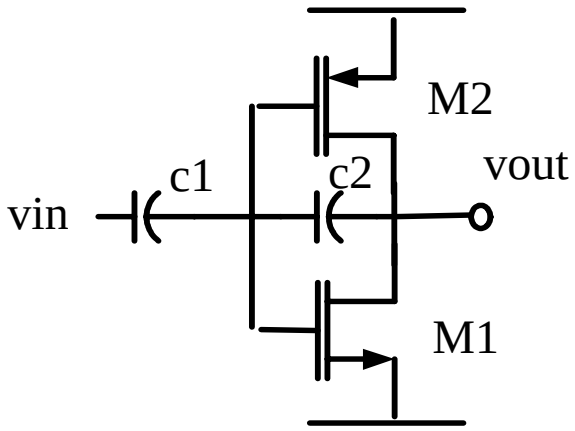

Figure 1

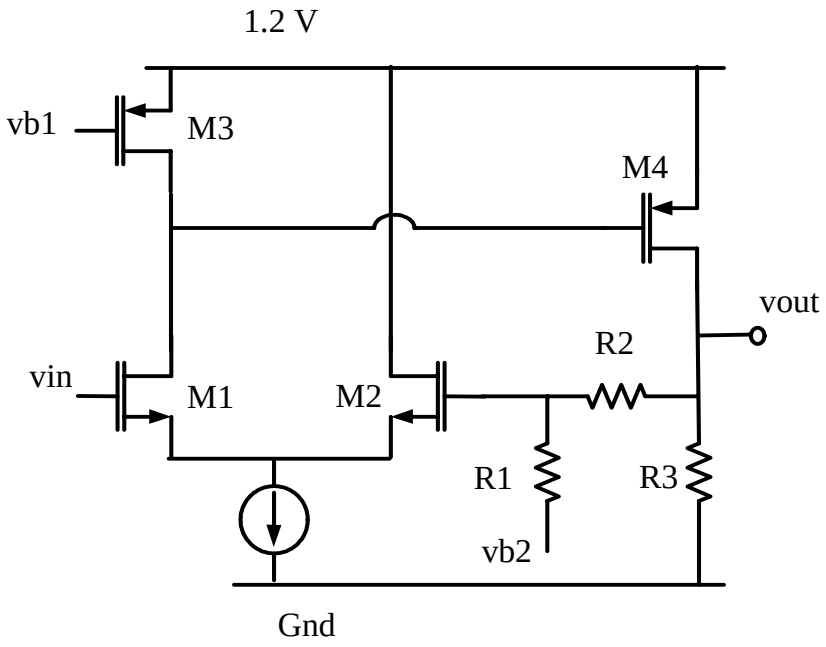

Figure 2

3) Using feedback analysis, identify the type of feedback, and calculate the closed loop gain, input and output impedance. How does this compare to a traditional common drain stage? At what frequency range the circuit lost its advantage compared to common drain? Assume $A(S) = \dfrac{K}{1 + S/\omega p}$