HOMEWORK # 6 SOLUTION

1) (a) $V_{GS_1} = V_{GS_2} + R I_{OUT}$

$\Rightarrow V_T + V_{DSat_1} = V_T + V_{DSat_2} + R I_{OUT}$

$\Rightarrow \sqrt{\frac{2 I_{IN}}{k'(W/L)_1}} = \sqrt{\frac{2 I_{OUT}}{k'(W/L)_2}} + R I_{OUT}$

Since $I_{IN} = I_{OUT}$ (Current mirror):

$\Rightarrow \sqrt{\frac{2 I_{OUT}}{k'(W/L)_1}} = \sqrt{\frac{2 I_{OUT}}{k'(W/L)_2}} + R I_{OUT}$

One (trivial) solution is $I_{OUT} = 0$. The more interesting solution can be found by dividing out $\sqrt{\frac{2 I_{OUT}}{k'}}$:

$$\frac{1}{\sqrt{(W/L)_1}} = \frac{1}{\sqrt{(W/L)_2}} + \sqrt{\frac{k'}{2}} R \sqrt{I_{OUT}}$$

$$\Rightarrow I_{OUT} = \frac{2}{k' R^2} \left[\frac{1}{\sqrt{(W/L)_1}} - \frac{1}{\sqrt{(W/L)_2}} \right]^2$$

(b) $$g_{m5} = \sqrt{2k'\left(\frac{W}{L}\right)_5 I_{DS5}}$$

$$\frac{I_{DS5}}{(W/L)_5} = \frac{I_{DS1}}{(W/L)_1}$$

$$\Rightarrow g_{m5} = \sqrt{2k' \frac{(W/L)_5^2}{(W/L)_1} I_{DS1}}$$

$$\Rightarrow \boxed{g_{m5} = \frac{2}{R} \frac{(W/L)_5}{(W/L)_1} \left[1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\right]}$$

This bias circuit is called a 'constant-g_m' reference, since g_m does not depend on electrical transistor parameters, such as V_T, k', ... (wich are not well controlled), but g_m only depends on W/L-ratio's (which are well controlled) and R (which can be made accurate using special techniques).

2) From the device model: $k'_{NMOS} = 332\ \mu A/V^2$

$k'_{PMOS} = 133\ \mu A/V^2$

@ $I_{DS4a} = 9.375\mu A$

$$\Rightarrow V_{Dsat4a} = \sqrt{\frac{2 I_{DS4a}}{k'(W/L_{eff})_{4a}}} = 206\,mV$$

$$= V_{Dsat4b}$$

$$V_{Dsat2a} = \sqrt{\frac{2 I_{DS2a}}{k'_{NMOS}(W/L)_{2a}}} = 25\,mV$$

$$V_{Dsat2b} = \sqrt{\frac{2 I_{DS2b}}{k'_{PMOS}(W/L)_{2b}}} = 25\,mV$$

Since $V_{GS2a} + V_{GS2b} = V_{GS1a} + V_{GS1b}$

and $I_{DS2a} = I_{DS2b}$ and $I_{DS1a} = I_{DS1b}$

we get $V_{DSat1a} = V_{Dsat2a} = 25\,mV$

$V_{Dsat1b} = V_{Dsat2b} = 25\,mV$

$I_{DS1a} = I_{DS1b} \approx I_{DS2a} = I_{DS2b}$

(The currents in M_{1a} and M_{2b} will be slightly larger because of higher V_{DS})

$$I_{DS_3} = I_{DS4b}$$

$$\Rightarrow V_{Dsat_3} = \sqrt{\frac{2 I_{DS_3}}{\mu_{NMOS} (W/L)_3}} = 206\,mV$$

The conclusion of $V_{Dsat,1a} = V_{Dsat_{2a}}$ and $V_{Dsat_{1b}} = V_{Dsat_{2b}}$ can also be derived mathematically:

$$I_{DS_{2a}} = I_{DS_{2b}} \quad \text{and} \quad I_{DS_{1a}} = I_{DS1b} \quad (\text{for } V_{OUT} = 0V)$$

$$\Rightarrow \frac{I_{DS2a}}{I_{DS1a}} = \frac{I_{DS\,2b}}{I_{DS\,1b}}$$

$$\Leftrightarrow \frac{V_{Dsat_{2a}}^2}{V_{Dsat_{1a}}^2} = \frac{V_{Dsat_2}^2}{V_{Dsat,1b}^2}$$

If we call this ratio x^{-2}, we get $\begin{cases} V_{Dsat,1a} = x \cdot V_{Dsat_{2a}} \\ V_{Dsat_{1b}} = x \cdot V_{Dsat_{2b}} \end{cases}$

so that $V_{Dsat_{2a}} + V_{Dsat_2b} = V_{Dsat,1a} + V_{Dsat_{1b}}$

$$\Leftrightarrow \quad x = 1$$

$$\Rightarrow V_{Dsat,1a} = V_{Dsat_{2a}} \quad \text{and} \quad V_{Dsat_{1b}} = V_{Dsat_2b}$$

(b) $V_{IN} = V_{GS_3} = V_T + V_{Dsat_3} \approx 500\,mV$

$$\boxed{V_{IN} \approx 500\,mV}$$

(c) Upper part of the swing:

- M_{1b} will be cut off
- All V_{GS} stay the same, except for $V_{GS_{1a}}$, which will change greatly with the output current

- We always have:

$$|V_{DS_4}| + V_{Tn} + V_{Dsat_{1a}} + \underbrace{R_{LOAD}\, I_{OUT}^{+}}_{= V_{OUT}^{+}} = V_{DD}$$

- Maximum output swing:

$$|V_{Dsat_{4b}}| + V_{Tn} + V_{Dsat_{1a,max}} + \underbrace{R_{LOAD}\, I_{out,max}^{+}}_{= V_{OUT,max}^{+}} = V_{DD}$$

$$= R_{LOAD}\, \frac{k'_{NMOS}}{2} \left(\frac{W}{L_{eff}}\right)_{1a} V_{Dsat_{1a,max}}^{2}$$

$$\Rightarrow 15V^{-1}\, V_{Dsat_{1a}}^{2} + V_{Dsat_{1a}} + (200\,mV + 300\,mV - 1.2V) = 0$$

$$\Rightarrow V_{Dsat_{1a,max}} = \frac{-1 + \sqrt{1 + 4 \cdot 15 \cdot 0.7}}{2 \cdot 15}$$

$$= 185\,mV$$

$$V_{OUT,max}^{+} = V_{DD} - |V_{Dsat_{pa}}| - V_{Tn} - V_{Dsat,a,max}$$

$$\Rightarrow \boxed{V_{OUT,max}^{+} = 515\,mV}$$

Similarly, $\boxed{|V_{OUT,max}^{-}| = +515\,mV}$

(e) $$\eta \times \frac{\pi}{4} \frac{V_{OUT}}{V_{DD}} = \frac{\pi}{4} \cdot \frac{515\,mV}{1.2V} = 33.7\%$$

Using this class B approximations means neglecting the (small) bias currents.

$$\boxed{\eta = 33.7\,\%}$$

If we would like to include the effects of bias currents:

$$P_L = V_{OUT}^2 / 2R_{LOAD}$$

$$P_{SUPPLY} = \underbrace{\frac{2}{\pi} V_{DD} \frac{V_{OUT}}{R_{LOAD}}}_{\text{average of sinusoidal currents in output transistors}} + \underbrace{V_{DD} \cdot 3 I_B}_{\text{bias currents in } M_{4b} \text{ and } M_{4b} - M_3}$$

$$\Rightarrow \eta^{-1} = \frac{P_{SUPPLY}}{P_{LOAD}}$$

$$= \left(\frac{\pi}{4} \frac{V_{OUT}}{V_{DD}}\right)^{-1} + \frac{6 V_{DD} I_B R_{LOAD}}{V_{OUT}^2}$$

$$\Rightarrow \eta = 31\%$$