UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Science

R. W. Brodersen **Homework #6** **EECS 140**
Johan Vanderhaegen **(Due 10/9/02)** **Fall 2002**

```
.model nmos
+ nmos level=1 tox=2.6n vt0=0.3 gamma=0.2 phi=0.6 u0=250 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+ lambda=0.2

.model pmos
+ pmos level=1 tox=2.6n vt0=-0.3 gamma=0.2 phi=0.6 u0=100 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+ lambda=0.15
```

When using the above models, remember to use W/L_{eff} in your calculations, where $L_{eff} = L - 2LD$ and $LD = 0.025$ µm.

1) For the circuit shown in figure 1:
   a) Calculate I_{OUT} as a function of R, k', $(W/L)_1$, $(W/L)_2$.
      Assume $\lambda = \gamma = 0$.
      Assume M2 and M3 are in saturation. Assume M3 is identical to M4.
   b) Calculate g_{m5} and explain why this circuit is called a *constant-gm bias circuit*.
      Assume M5 is in saturation.

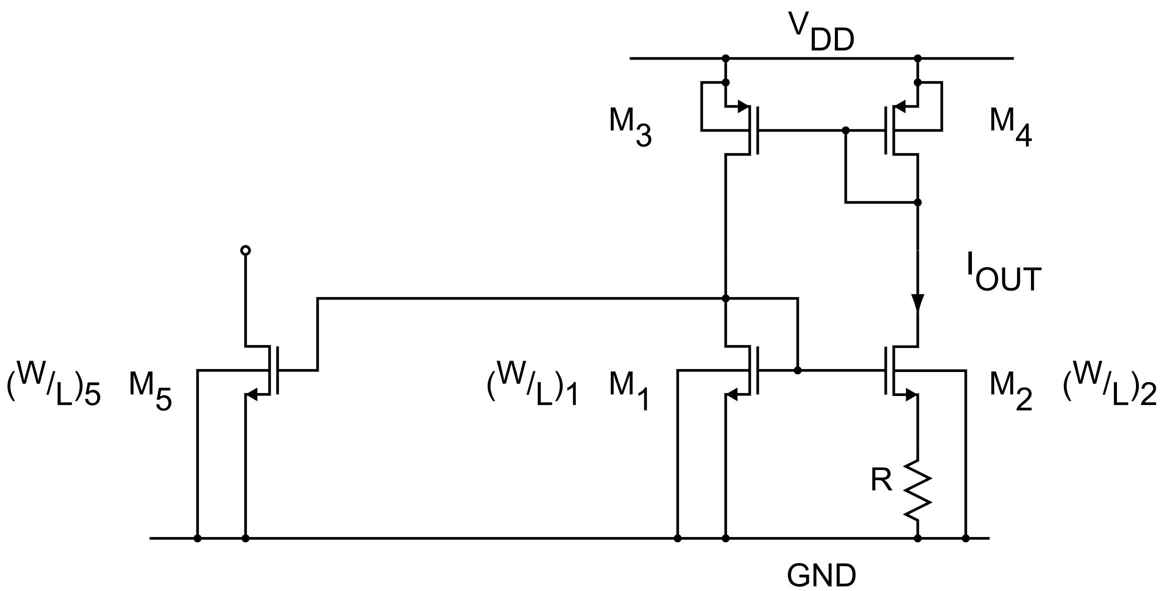

Figure 1.

2) For the circuit shown in figure 2:

V_{DD} = 1.2 V, R_{LOAD} = 1 KΩ, I_B = 9.375 µA.
$(W/L)_{1a} = (W/L)_{2a}$ = 7.2 µm / 0.13 µm $(W/L)_{1b} = (W/L)_{2b}$ = 18 µm / 0.13 µm
$(W/L)_3$ = 0.4 µm / 0.35 µm $(W/L)_{4a} = (W/L)_{4b}$ = 1 µm / 0.35 µm

V_{in} is referenced to the negative supply rail.

a) Calculate the V_{Dsat}'s for all the transistors, assuming the output is at 0 V.
b) Calculate the value of V_{IN} so that the output is at 0 V.
c) Calculate the range of output voltages so the active transistors remain in saturation. (e.g. for a negative output voltage, M1b,M2b,M3 have to remain in saturation).
d) Verify part (a)-(c) with SPICE:
   i) Do a DC sweep with a small step size around the calculated value of V_{IN} to verify the range of output voltages and to determine the real value of V_{IN} for which the output becomes 0 V.
   Use this experimentally determined voltage V_{IN}, for which the output becomes 0 V, as the input bias voltage.
   ii) Do an operating point analysis to verify the V_{Dsat}'s.
e) Calculate the sine wave efficiency (power into load / total power) for a full swing sine wave at the output ('full swing' meaning the range of output voltages calculated in part (c) and verified in part (d))
f) Verify the efficiency with SPICE:
   i) Make your input voltage source a sine wave source:|

```
vin in1 in2 sin(<dc-voltage> <amplitude> <freq>)
```

   Use the value for <dc-voltage> from part (d). Set <amplitude> to get the full output swing. Set <freq> to 1K (= 1 KHz)
   ii) Do a transient analysis (time domain analysis) for one period of the sine wave and measure the power into the load and the total supply power:

```
.meas tran p_load avg p(rload)
.meas tran p_supply_p avg p(vddp)
.meas tran p_supply_n avg p(vddn)
.meas tran p_supply param='-p_supply_p-p_supply_n'
.meas tran p_eff param='100*p_load/p_supply'
.tran 1u 1m
```

   where 'rload' is the load resistance, 'vddp' is the positive supply and 'vddn' is the negative supply. The measured values will be listed in your output file. '`p_eff`' is the efficiency.

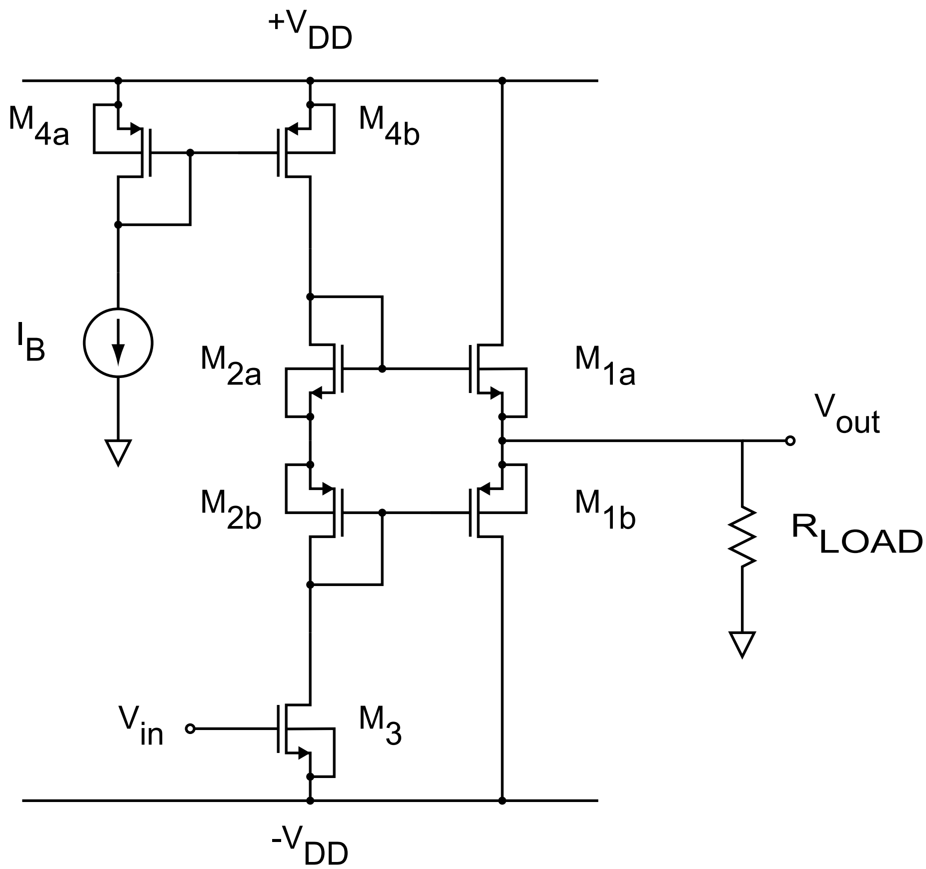

Figure 2.