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Homework #5
(Due 10/2/02)

EECS 140
Fall 2002

```
.model nmos
+ nmos level=1 tox=2.6n vt0=0.3 gamma=0.2 phi=0.6 u0=250 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+ lambda=0.2
```

```
.model pmos
+ pmos level=1 tox=2.6n vt0=-0.3 gamma=0.2 phi=0.6 u0=100 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+ lambda=0.15
```

When using the above models, remember to use W/L_{eff} in your calculations, where $L_{eff} = L - 2LD$ and $LD = 0.025 \mu\text{m}$. You can calculate k' directly from the SPICE model parameters $u0$ and tox .

- 1) For each of four the circuits, shown in figure 1, do the following steps. Assume $V_{DD} = 1.2 \text{ V}$, $W = 4 \mu\text{m}$, $L = 0.13 \mu\text{m}$, $R_S = 1 \text{ K}\Omega$. Use the models given above.
 - a) Choose R_{REF} so that the output current I_{out} is $200 \mu\text{A}$.
 - b) Calculate the output resistance R_{out} , assuming that all the transistors are in saturation.
 - c) Calculate the range of voltages at the output node over which the transistors remain in saturation.
 - d) Compare the results from part (a)-(c) with SPICE.

To compare part (a) and part (b) with SPICE, put a voltage source `vout` at the output of the circuit with a dc voltage high enough to ensure that all transistors are in saturation; next, do a `.op` and a `.tf i(m1) vout` analysis, where `m1` is the name of the output transistor.

To compare part (c) with SPICE, sweep the output voltage from 0 to V_{DD} and plot $1/(d(I_{out})/d(V_{out}))$. Label all the breakpoints.

It is not sufficient to print or plot something like $g_{m2}r_{o2}r_{o1}$, since this will only verify that you used the correct small signal parameters, not that you used the correct formula for R_{out} .

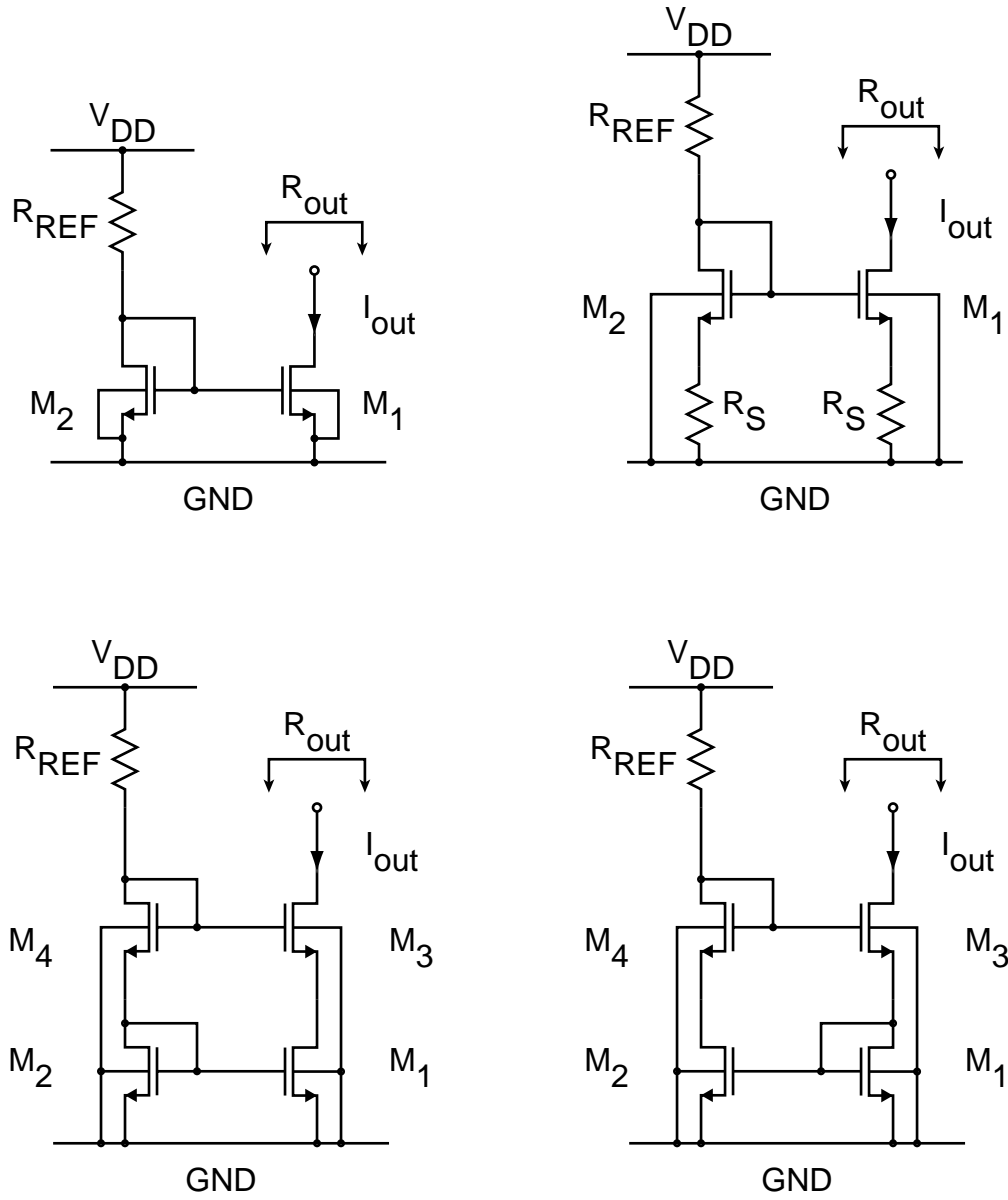


Figure 1.

- 2) For the circuit shown in figure 2, assume $V_{DD} = 1.2\text{ V}$, $W = 4\text{ }\mu\text{m}$, $L = 0.13\text{ }\mu\text{m}$, $R_D = 1\text{ K}\Omega$, $I_B = 400\text{ }\mu\text{A}$.
- Calculate $R_{out,dm}$, $R_{out,cm}$, A_{dm} and A_{cm} for $V_{id} = 0$ and $V_{ic} = 0.9\text{ V}$, assuming that all the transistors are in saturation.
 - Calculate the range of common mode input voltages V_{ic} for which all the transistors remain in saturation. Assume $V_{id} = 0\text{ V}$. For this step, do not assume that the input voltages are limited to $[0, V_{DD}]$.
 - Calculate the range of differential mode input voltages V_{id} for which both input transistors remain in saturation. Assume $V_{ic} = 0.9\text{ V}$.
 - Verify part (a) and (c) using SPICE.
 To verify part (a), use a .tf analysis.
 To verify part (b), plot V_{oc} versus V_{ic} from 0 V to 1.5 V for $V_{id} = 0\text{ V}$.
 To verify part (c), plot V_{od} versus V_{id} from -1.2 V to $+1.2\text{ V}$ for $V_{ic} = 0.9\text{ V}$.
 Label all the breakpoints.

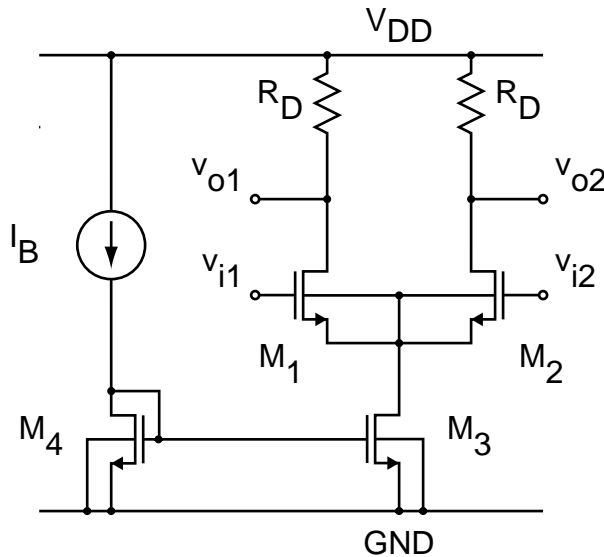


Figure 2.

SPICE hint: to apply and sweep a differential voltage, you will need an 'e'-element: a voltage-controlled voltage source (vcvs). Syntax: 'e1 out1 out2 in1 in2 gain'. This will add a vcvs between nodes out1 and out2, with voltage equal to $\text{gain} * v(\text{in1}, \text{in2})$.