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Homework #4
(Due 9/23/02)

EECS 140
Fall 2002

Indicate on your homework in which discussion section (Tuesday / Friday) you would like to get your homework back.

- 1) For the circuit shown in figure 1, calculate the small signal voltage gain v_{out}/v_{in} in terms of the circuit elements R_1 , R_2 , R_B and the small signal parameters g_m , g_{mb} and r_o of M1 and M2. Assume that all the transistors are identical and in saturation. I_B is a bias current and V_B is a bias voltage.

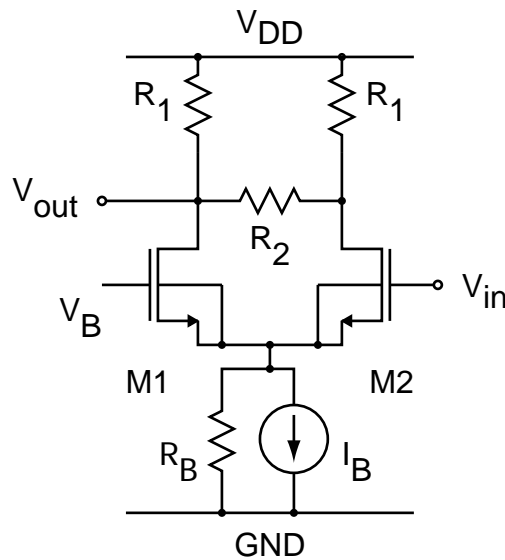


Figure 1.

2) For the circuits shown in figure 2:

Assume $W = 4 \mu\text{m}$, $L = 0.13 \mu\text{m}$ for all transistors. Use the models given below.

- Calculate the bias voltage V_{IN} needed to get a bias current I_{DS} of $150 \mu\text{A}$.
Do not neglect the effect of λ .
- Calculate R_{out} and a_0 .
- Verify with SPICE.

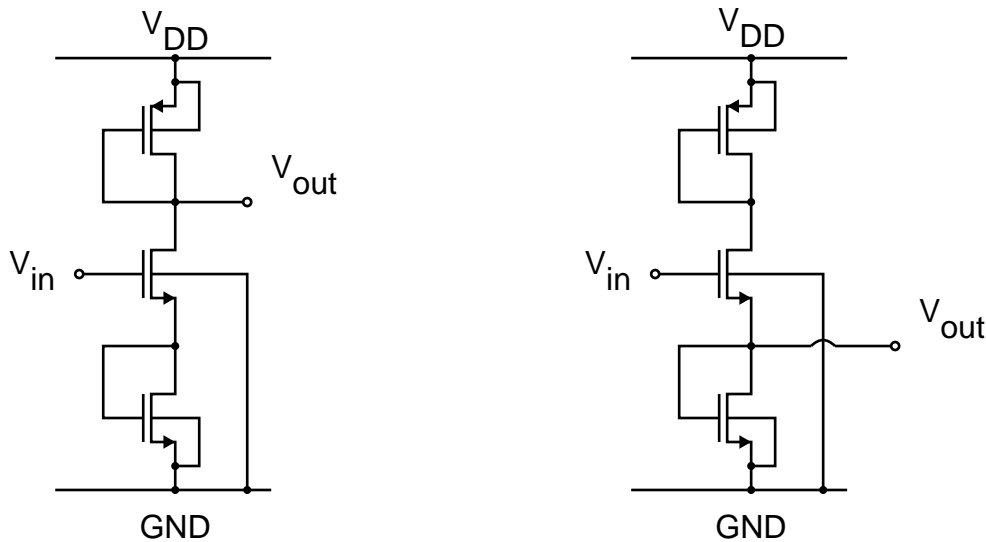


Figure 2.

SPICE hints for problem 2:

- Use a `.op` analysis to get the operating point and to verify your calculated values for V_T , V_{DSAT} , g_m , g_{mb} and g_{ds} .
- Use a `.tf` analysis to get R_{out} and a_0 .
e.g. `.tf v(out) vin` will calculate the gain from ac voltage input 'vin' to the voltage on node 'out' and will give you the input and output resistance.

Transistor models:

```
.model nmos
+ nmos level=1 tox=2.6n vt0=0.3 gamma=0.2 phi=0.6 u0=250 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+ lambda=0.2
.model pmos
+ pmos level=1 tox=2.6n vt0=-0.3 gamma=0.2 phi=0.6 u0=100 ld=0.025u
+ capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+ lambda=0.15
```