UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
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Homework #7
Due 10/15/99 before noon in 497 Cory

EECS 140
Fall 1999

Note: Use the device parameters given in the class handout "Device Parameters & SPICE Models" and also available on the EECS 140 website, **http://kowloon.eecs.berkeley.edu/~courses/140**

Grading: Problem 1: 15% Problem 2: 15% Problem 3: 30%% Problem 4: 40%

1) Consider the cascode current mirror shown in Fig.1. Assume equal W/L for all devices.
   a) Use the small signal model of the circuit to derive an analytical expression for the systematic error $\varepsilon=(I_{out}/I_{in})-1$ as a function of $\Delta V=(V_{out}-V_{in})$.
   b) Show that compared to a simple current mirror (M2 and M4 removed), the systematic error is reduced by the factor $1/g_m r_o$.
   c) Calculate the systematic error for a simple current mirror and for the shown cascode current mirror using ΔV=2V, (W/L)=10µm/2µm, and I_{out}=200µA.

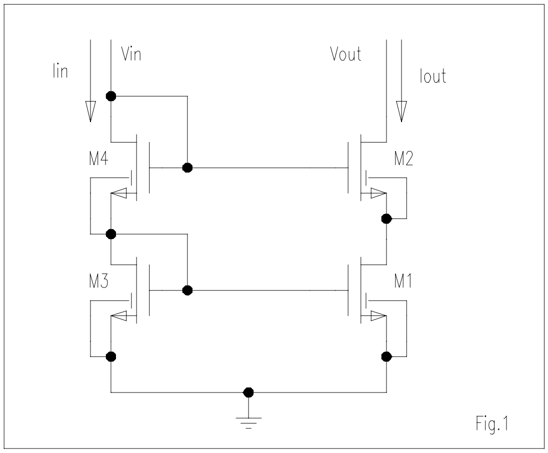
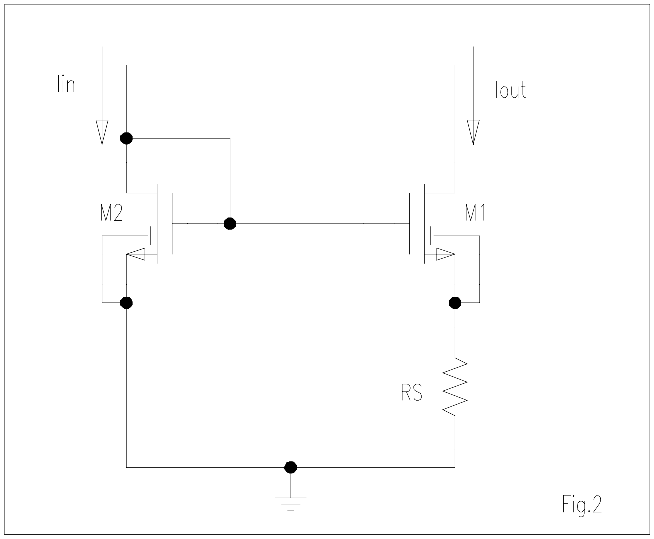
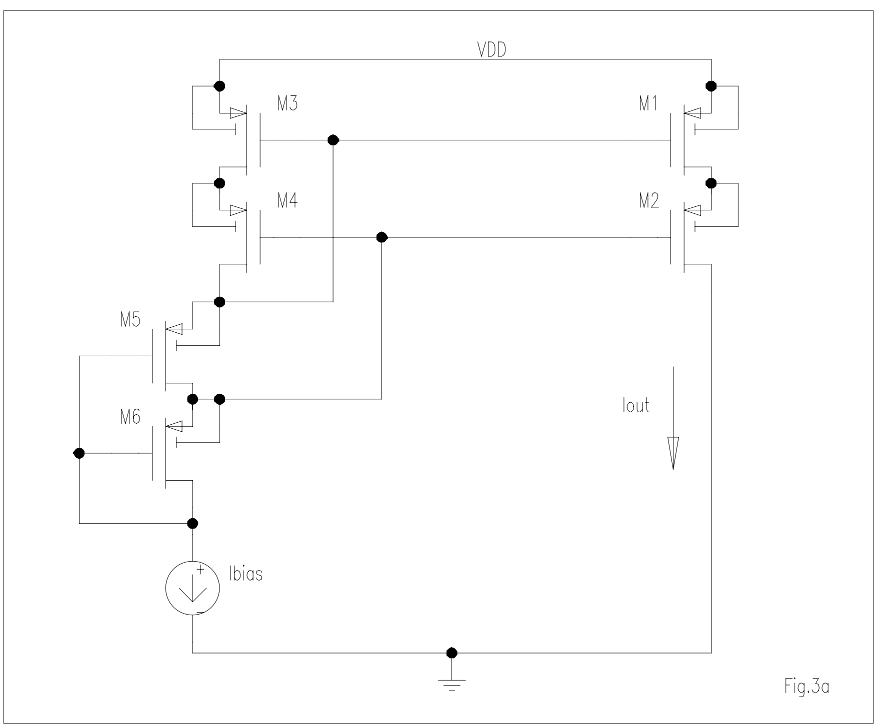


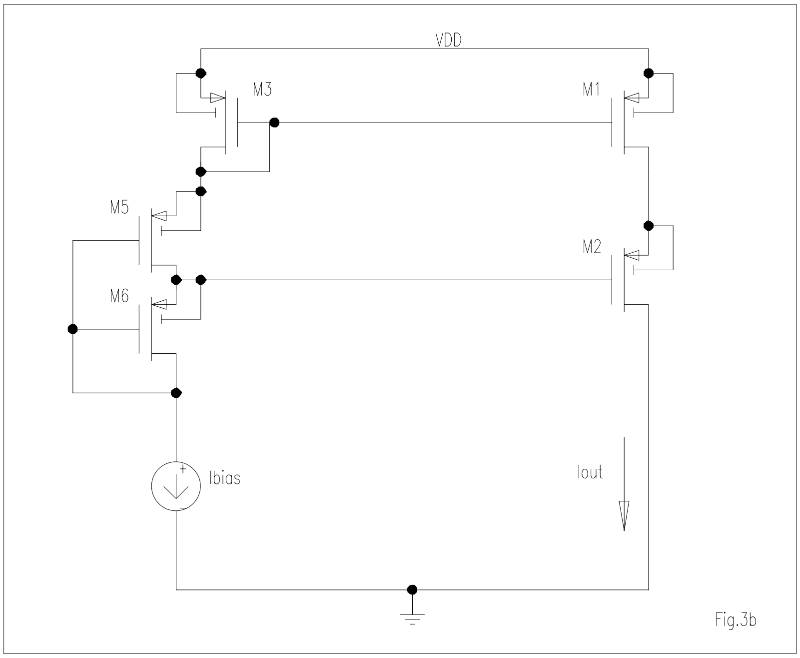
Fig.1

2) Consider the current mirror shown in Fig.2. In the layout of the circuit, the source of M2 had accidentally been connected to ground using polysilicon, resulting in a significant source resistance R_S.
   Use (W/L)=100, R_S=100Ω and I_{in}=200µA to calculate ε and $\Delta V_{GS}=V_{GS1}-V_{GS2}$.
   Assume λ=0 and $(W/L)_1=(W/L)_2$. Note how a small ΔV_{GS} can result in a fairly large mismatch in the branch currents!



3) Consider the high swing bias circuits shown in Fig. 3a.
   a) Design the circuit in Fig. 3a, i.e. find all (W/L) for V_{min}=400mV and I_{bias}=100µA. Assume λ=0 for this part of the analysis.
   b) Draw the circuit and numerically label all node voltages and branch currents. Explicitly verify the region of operation of M4. Let V_{DD}=10V.
   c) Calculate the systematical error $\varepsilon=(I_{out}/I_{bias})$ with and without the presence of M4. (After the removal of M4, the circuit reduces to the one shown in Fig. 3b)





4) Fig. 4 shows a differential pair, biased through a current source I_{SS} that has a finite output resistance R_x. Assume λ=0 for the analysis of the circuit.

a) Using the circuit's large signal model, find an analytical expression for the small signal differential gain $A_{dm0}=dV_{od}/dV_{id}$ as a function of the applied differential voltage V_{id}. Assume $Rx\rightarrow\infty$ for this part of the analysis.

b) Using your result from (a), calculate A_{dm0} for V_{id}=0 and for V_{id}=100mV using the circuit parameters (W/L)=50, R_D=30k and I_{SS}=200μA.

c) Use SPICE to generate a plot of $A_{dm0}=dV_{od}/dV_{id}$ for V_{id}=-250mV…+250mV, using the circuit parameters from part (b). Set V_{i-}=3V and DC sweep V_{i+} ±250mV with respect to Vi-. Use the "Awaves Expression Builder" to generate and display the expression for A_{dm0}. In the same diagram also show the differential output voltage V_{od}.
(i) Verify your result from part (b). Mark your calculated value from (b) in the plot. What is the corresponding output voltage for V_{id}=100mV?
(ii) What are the minimum and maximum small signal gain values as V_{od} swings from –5.5 to +5.5V ? Calculate the percent change [A_{dm0}(max) - A_{dm0}(min)] / A_{dm0}(max). In practice, which gain should be quoted in the circuit's datasheet?

d) Using the circuit's small signal model, find an analytical expression for the common mode gain $A_{cm}=V_{ocm}/V_{icm}$ as a function of the current source resistance R_x. Recall that $V_{i+}=V_{icm}+V_{id}/2$ and $V_{i-}=V_{icm}-V_{id}/2$, $V_{o+}=V_{ocm}+V_{od}/2$, $V_{o-}=V_{ocm}+V_{od}/2$

e) Calculate A_{cm} using the circuit parameters from (b) and R_x=100kΩ. Repeat for R_x=10MΩ.

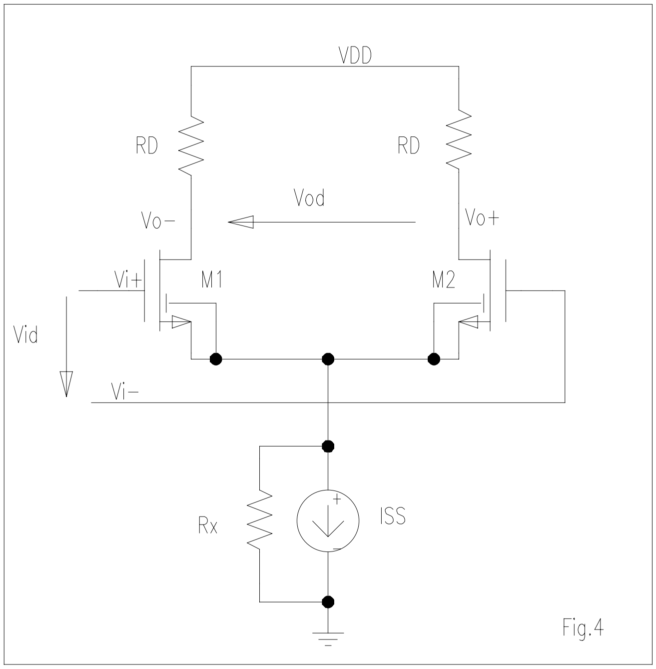


Fig.4