UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

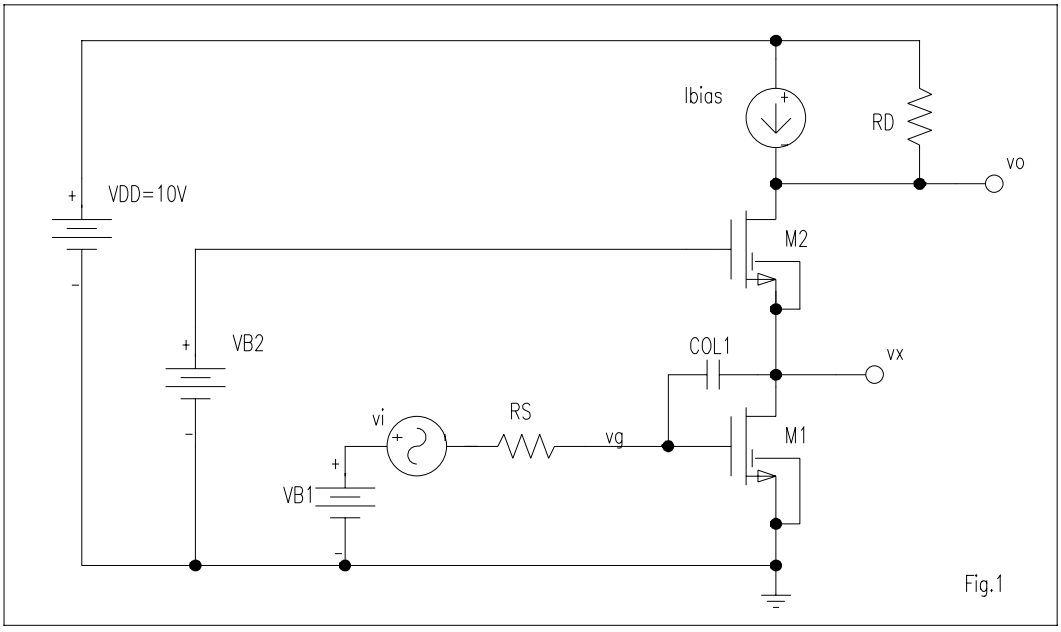
	Homework #6	**EECS 140**
B. E. Boser	Due 10/08/99 before noon in 497 Cory	**Fall 1999**

Note: Use the device parameters given in the class handout "Device Parameters & SPICE Models" and also available on the EECS 140 website, **http://kowloon.eecs.berkeley.edu/~courses/140**. Use the following parameters to calculate parasitic capacitors: C_{ox}=5fF/µm, C_{OL}=W·0.5fF/µm, C_{sb0}=C_{db0}=1fF/µm², ψ_0=0.5V, AS=AD=W·1µm.

Grading: Problem 1: 40% Problem 2: 40% Problem 3: 20%

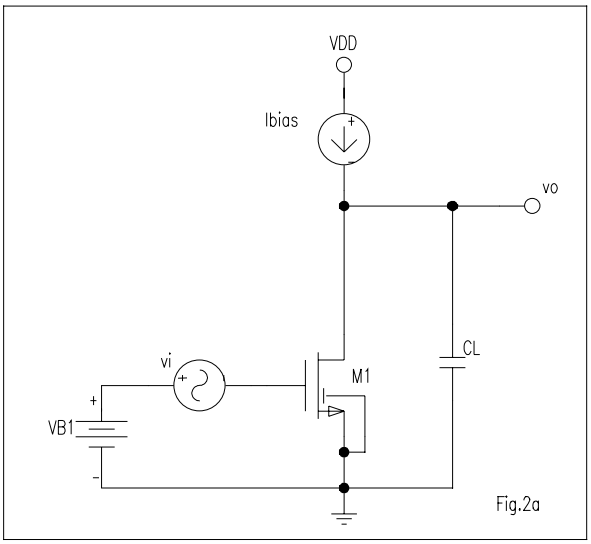
1) Cascode amplifier stages are often used to eliminate bandwidth reduction due to Miller multiplication of the parasitic gate to drain capacitance. The following problem examines a case in which a poorly designed cascode amplifier circuit still suffers from bandwidth degradation due to the Miller effect. Consider the circuit shown in Fig.1. For the analysis, neglect all parasitic junction capacitances.

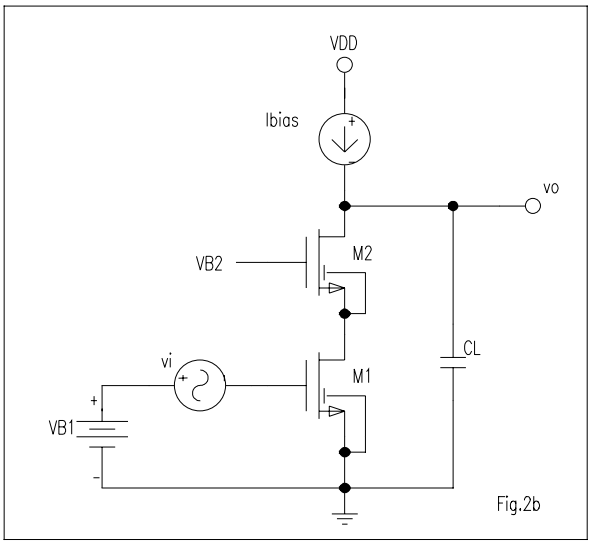
   a) Derive analytical expressions for the small signal resistance R_x at node v_x and the DC voltage gain $A_{vx} = v_x/v_i$. Assume $R_D >> r_{o2}$.
   b) Find an expression for the pole frequency f_{p1} that is present at node v_g using the Miller approximation.
   c) Using the results from (b), find A_{vx}, and f_{p1} for I_{bias}=1mA, R_D=1MΩ, R_S=500kΩ, W_2=5µm, W_1=100µm and L_1=L_2=1µm. Compare f_{p1} with the pole frequency f_{p1}'=1/ $R_S C_{gs1}$, i.e. find f_{p1}/f_{p1}'. Note that f_{p1}' approximately represents the expected pole frequency at node v_g neglecting the Miller effect.
   d) Verify your results from part (c) using SPICE. Use V_{B2}=3V and run a DC analysis to find V_{B1} such that V_O=5V at the operating point. Use 5 significant digits when extracting V_{B1}.
      Next, perform an AC analysis and printout a Bode plot for the voltage gains $a_{vx}=v_x/v_i$ and a_v=vo/vi. In the same diagram, plot a_{vx} and a_v after setting C_{OL1}=0, thus neglecting the Miller effect. Compare the observed pole frequencies fp1 and fp1' and their ratio with your hand calculations. Mark the calculated pole frequencies in your plot.
   e) The result from the above analysis suggests that the Miller effect ***can*** cause bandwidth degradation in a cascode amplifier stage. Referring to the topology of the circuit in Fig.1 and for R_S=constant, what must be done to avoid the Miller effect? What are the tradeofffs?



2) Fig. 2a and Fig. 2b show common source amplifiers before and after the insertion of a cascode device. For the analysis of these circuits, neglect all extrinsic parasitic capacitances.

   a) Find an analytical expression for the the DC voltage gains a_{voa} and a_{vob} and their ratio a_{vob}/a_{voa}, where the indices a and b correspond to the circuits in Fig. 2a and Fig. 2b, respectively.
   b) Find an expression for the pole frequencies f_{p1a} and f_{p1b} and their ratio f_{p1a}/f_{p1b} caused by a fixed load capacitor C_L.
   c) The insertion of M2 causes another pole to appear in the transfer function v_o/v_i of the circuit in Fig. 2b. Briefly explain the origin of this pole using appropriate circuit diagrams. Find an expression for its pole frequency f_{p2b}.
   d) Find an expression for the unity gain frequencies f_{ua} and f_{ub} and their ratio f_{ua}/f_{ub}. Assume that $f_{p2b} >> f_{ub}$.
   e) Calculate numerical values for all expressions found in (a) through (d) using I_{bias}=500µA, $(W/L)_1=(W/L)_2$=20µm/1µm and C_L=0.5pF.
   f) Verify your results from part (d) using SPICE. Use V_{DD}=10V and V_{B2}=3V. For both circuits, run a DC analysis to find V_{B1} such that V_O=5V at the operating point. Use 5 significant digits when extracting V_{B1}.
      Perform AC analyses to printout the frequency response of v_o/v_i for both circuits in the same diagram. Mark the calculated DC voltage gains, pole frequencies and unity gain frequencies in your plot. Comment on discrepancies.





3) Fig. 3 shows a cascode current source consisting of M1A and M1B, and a single transistor current source consisting of M2. Assume that the cascode current source is optimally biased, i.e. V_{B1B} is chosen such that $V_{DS1a}=V_{d1A}(sat)$. Assume also that both current sources supply the same current I_D.

   a) Find relationships between W_1, L_1 and W_2, L_2 such that both current sources have the same parasitic output capacitance, and the same minimum output voltage V_{min}. Assume $\lambda=0$ in this part of the analysis.

   b) Using the result from (a), show that: $$\frac{R_{O1}}{R_{O2}} \cong \frac{g_{m1} \cdot r_{o1}}{4}$$ where R_{O1} and R_{O2} are the output resistances of each current source, as indicated in Fig. 3.

   c) Calculate V_{min}, R_{o1} and R_{o2} for $I_D=100\mu A$ and $(W/L)_1=10\mu m/2\mu m$.