UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Homework #5 **EECS 140**

B. E. Boser Due on **Friday** 10/01/99 before noon in 497 Cory **Fall 1999**

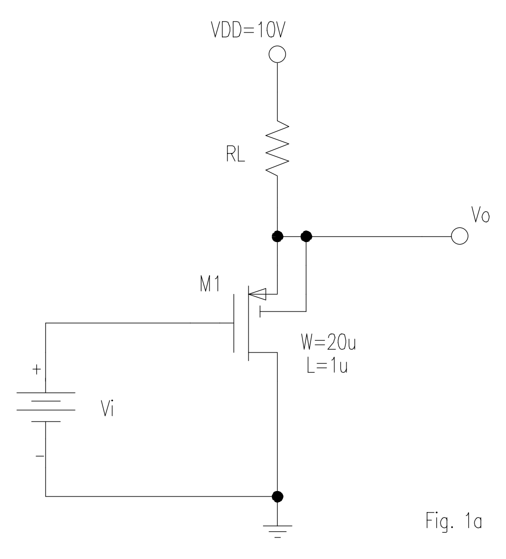
Note: Use the device parameters given in the class handout "Device Parameters & SPICE Models" and also available on the EECS 140 website, **http://kowloon.eecs.berkeley.edu/~courses/140**.

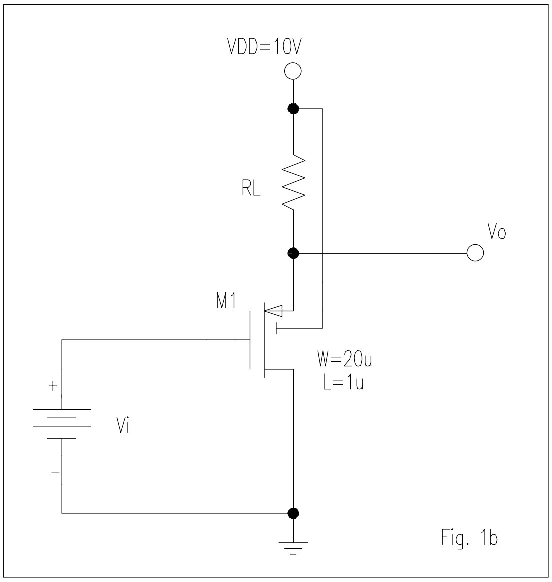
1) Consider the two source follower circuits shown in Fig. 1a and Fig. 1b.

   a) For an output voltage swing from 5V to 9V in both circuits, calculate the corresponding voltage swing at the input node V_I, for R_L=1kΩ and R_L=1MΩ.. Determine these values using the transistor's **large signal** model. For each case, also calculate $\Delta V_O/\Delta V_I$, thus estimating the voltage gain. Summarize your results in a table. Explain how different values for R_L and how the two different bulk connection schemes (Fig. 1a and 1b, respectively) affect the required input voltage swing.

   b) Draw a **small signal** equivalent for the circuit of Fig. 1a. Find an analytical expression for the low frequency small signal gain $a_{vo}= v_o/v_i$ as a function of R_L and the DC bias at V_O. Assume $\lambda=0$. Calculate the small signal gain at V_O=5V and V_O=9V using R_L=1k. Calculate the percent change in small signal gain when V_O changes from 5V to 9V.

   c) Verify your results from part (b) using SPICE. First, perform a .DC analysis to find the input voltages that correspond to the given output voltages. Next, run a .TF analysis for each bias point to find the small signal gains. Printout the portions of your SPICE listing files that show the transistor biasing information and the results of the transfer function analysis. Calculate the percent change between the small signal gain at V_O=5V and V_O=9V.





2) Consider the circuits shown in Fig.2a-d. Assume $\lambda=0$ and neglect all *extrinsic* parasitic capacitances.

   a) Draw the small signal equivalent circuit. Find an expression for the output impedance $Z_{O(s)}$, looking into the output terminal as shown in Fig. 2a.

   b) Show that for $R_S>1/g_m$, the output impedance can be modeled as an RL circuit as shown in Figure 2b. Express L, R_1 and R_2 as functions of R_S, g_m and C_{gs}.

   c) Calculate the values for L, R_1 and R_2, using I_{bias}=1mA and R_S=1MΩ. Verify that $R_S>1/g_m$.

   d) Set up a SPICE deck to verify the inductive behavior of the output impedance using the values from part (c). Run a .AC analysis using an AC current source at the output node to plot the magnitude of the circuit's output impedance $|Z_{O(s)}|$ as a function of frequency (see Fig. 2c).
   Next, include the RL circuit model with the calculated values from (c) in your SPICE deck. Printout it's impedance $|Z_{RL}|$ over frequency in the same diagram with $|Z_{O(s)}|$. Comment on discrepancies and mark the expected output impedance values for f=0 and $f\to\infty$ in your plot.
   <u>Hint</u>: Set the magnitude of the AC current source I_o to 1A, then the voltage at the output will directly represent the output impedance in Ohms.
   <u>Remark:</u> For good agreements between hand analysis and simulation in the upper GHz frequency range, you will have to force HSPICE to use the simple "level one" capacitor that we are using in the hand analyses. You can do so by specifying "CAPOP=0" in the .MODEL line for M1. Note that by default, HSPICE uses a model that smoothes out the abrupt change between linear and saturation region. Therefore, C_{gd} doesn't drop to *exactly* zero in the forward active region. This small capacitance then effects the frequency response of this circuit at very high frequencies, causing a discrepancy between hand analysis and simulation, unless you set "CAPOP=0".

   e) Since the output impedance contains an inductive component, ringing should occur in a step response with a capacitive load. Setup a SPICE deck for the circuit shown in Fig. 2d. Run a transient analysis and use a PWL source to step the input voltage from 3V to 4V within 1ns, set I_{bias}=1mA. Printout the transient response, showing the output voltage until about 300ns after the step. Extract the approximate ringing frequency that is observable at the output node. Compare with the expected resonant frequency at $fo = 1/2p\sqrt{LC_L}$, using the calculated value for L from part (c).

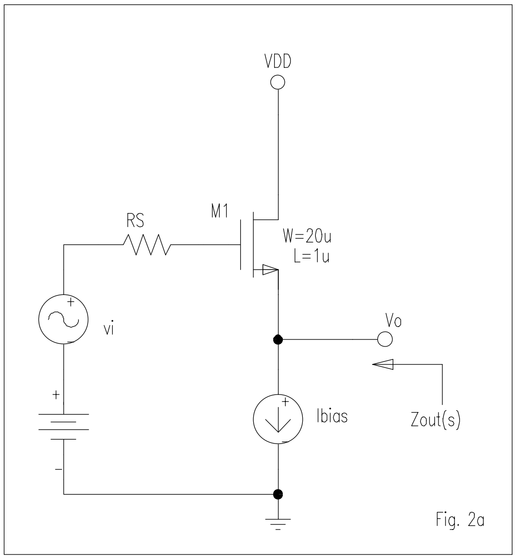


Fig. 2a

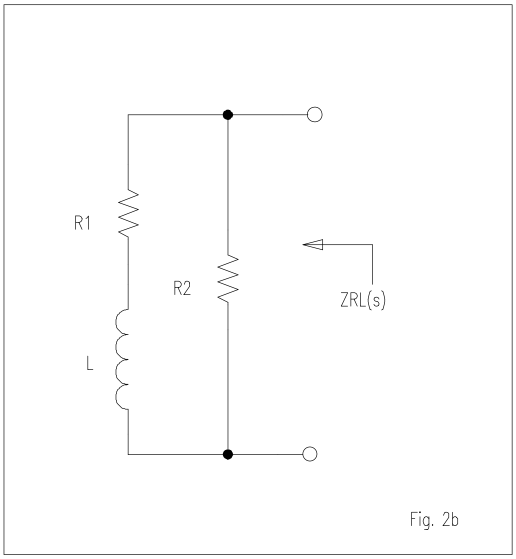


Fig. 2b

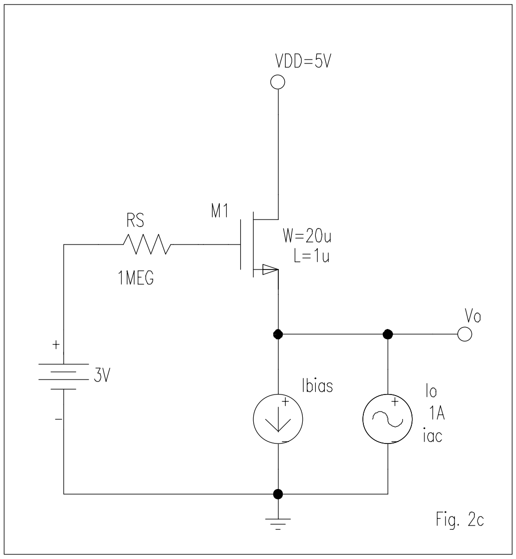


Fig. 2c

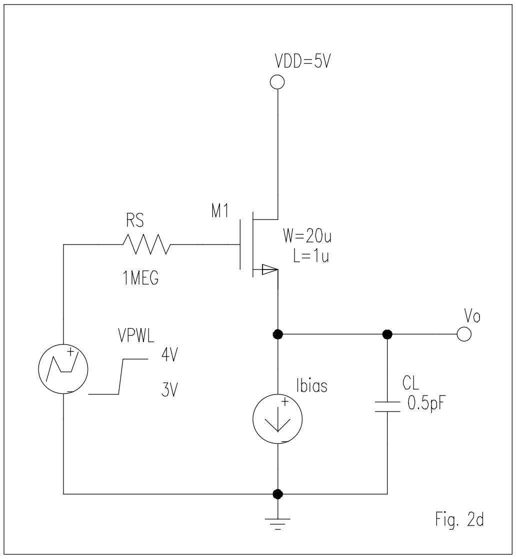


Fig. 2d