UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Homework #4	**EECS 140**
B. E. Boser	Due 09/22/99 before noon in 497 Cory	**Fall 1999**

Note: Use the device parameters given in the class handout "Device Parameters & SPICE Models" and also available on the EECS 140 website, **http://kowloon.eecs.berkeley.edu/~courses/140**. Use the following parameters to calculate parasitic capacitors: C_{OL}=W·0.5fF/µm², C_{sb0}=C_{db0}=1fF/µm², ψ_0=0.5V, AS=AD=W·1µm.

Grading: Problem 1: 40% Problem 2: 20% Problem 3: 40%

1) Consider the common source amplifier with source degeneration shown in Fig.1a. Assume that M1 is operating in the forward active region and that the device's parasitic capacitors are negligible compared to C_L.

   a) Derive analytical expressions for the small signal parameters G_m and R_o for the compound device as shown in Fig.1b. Assuming r_o>>R_S, show that:

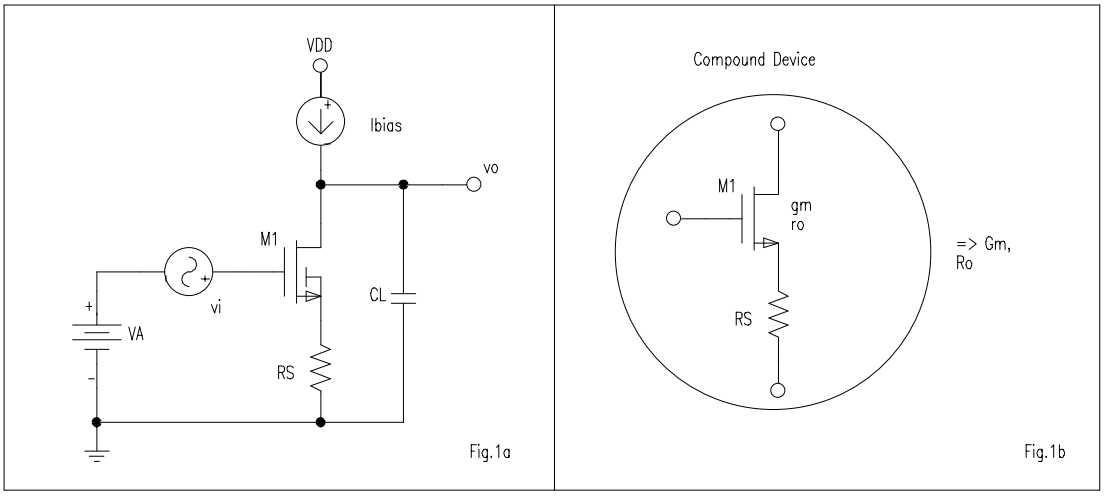
   $$G_m \cong \frac{1}{R_S + 1/g_m} \qquad \text{and} \qquad R_o \cong r_o(1 + g_m R_S)$$

   where g_m and r_o represent the small signal parameters of the active device M1.

   b) Using the results from part (a), formulate expressions for the voltage gain a_{vo}, the pole frequency f_p and the unity gain frequency f_u of the source degenerated amplifier.

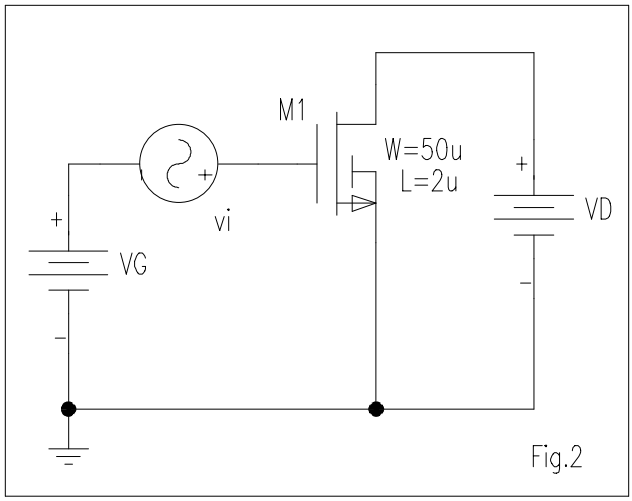
   c) Calculate a_{vo}, f_p and f_u for R_S=0 and R_S=500Ω. For both cases, sketch a Bode plot showing the frequency response of the amplifiers voltage gain. Assume g_m=500µA/V, r_o=100kΩ and C_L=1pF.

   d) In a typical CMOS process, the resistance of a Metal to Active contact window can be as high as 50Ω. Accidentally, the source terminal of a common source amplifier has been connected to ground using only one contact, resulting in R_S=50Ω. Estimate the bandwidth degradation resulting from this flaw, i.e. calculate the ratio $f_u(R_S=50\Omega)/f_u(R_S=0)$. Assume W=10µm, L=1µm and I_{bias}=500µA.



2) As discussed in class, we distinguish between device *intrinsic* and device *extrinsic* parasitic capacitances of a MOSFET. To further illustrate this notion and to show how we implement each of these capacitances in our SPICE simulations, analyze an NMOS device with W/L= 50µm/2µm as follows:

   a) Draw a circuit diagram showing the device with its **intrinsic** parasitic capacitances connected to the appropriate terminals. Calculate the values of these capacitances for the forward active and triode region of operation.
   b) Verify (a) through SPICE simulations. Enter a SPICE deck for the circuit shown in Figure 2. Run a .AC analysis for the device operating in the forward active region, use V_A=1.5V and V_D=3V. Repeat for the triode region, use V_A=3V and V_D=1V. Open your SPICE listing files and find the transistor bias point information with the computed values for CGS and CGD. Compare these values with your results from (a). Printout the portion of the SPICE listing files that show the transistor bias point information.
   c) Draw a circuit diagram showing the device with its **extrinsic** parasitic capacitances connected to the appropriate terminals. Assume that the device is connected as shown in Fig. 2. Calculate the extrinsic capacitances for V_D=1V and V_D=3V.
   d) Using the EE140 device models, SPICE does **not** automatically include the extrinsic parasitic capacitances in the simulation. We would need to use a more complicated model to have these capacitances included automatically.
   Thus, we have to add the extrinsic parasitics **manually** to our SPICE deck where specified (see e.g. problem 3 of this homework).
   Modify your SPICE deck from part (b) by including the calculated extrinsic capacitances from part (b) as separate circuit components. Use the component values obtained for V_D=3V. Printout the resulting SPICE deck.
   e) Now, for the SPICE deck obtained in (d) draw a circuit diagram showing all the parasitic capacitors that are now being modeled for simulation!



3) Consider the common source amplifier shown in Fig.3.
   a) Calculate the values for the overlap capacitors C_{OL} and for the device intrinsic capacitance C_{gs}. Determine V_A such that V_O=3V at the operating point.
   b) Calculate the low frequency voltage gain a_{V0} and find the amplifier's bandwidth f_u using the Miller approximation. Ignore the pole that is present at the output node V_O and Assume that M1 has negligible parasitic drain/source junction capacitances.
   c) Run a SPICE simulation to verify your results from (b). For the simulation, include the extrinsic parasitic capacitors C_{OL} and C_{db} manually as additional circuit elements. Hand calculate the value for C_{db} at the chosen bias point. Printout a Bode plot of the amplifier's voltage gain frequency response. Circle the two data points from your hand analysis in your plot.
   d) Compare the simulation results with your hand analysis. Note that in your hand calculations, you assumed the junction capacitances to be negligible. Was this a valid assumption? Explain. Comment on the validity of the Miller approximation for the analysis of this circuit by estimating the second pole frequency at the output node V_O.

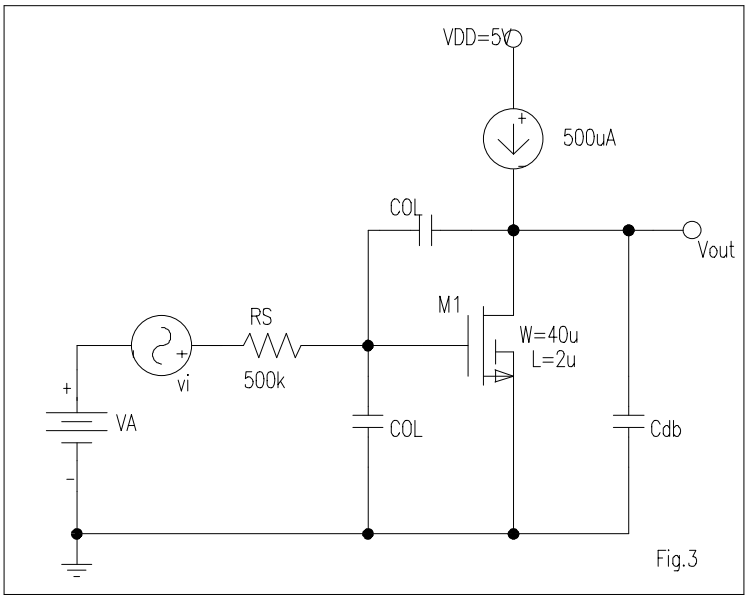


Fig.3