**UNIVERSITY OF CALIFORNIA**
**College of Engineering**
**Department of Electrical Engineering**
**and Computer Sciences**

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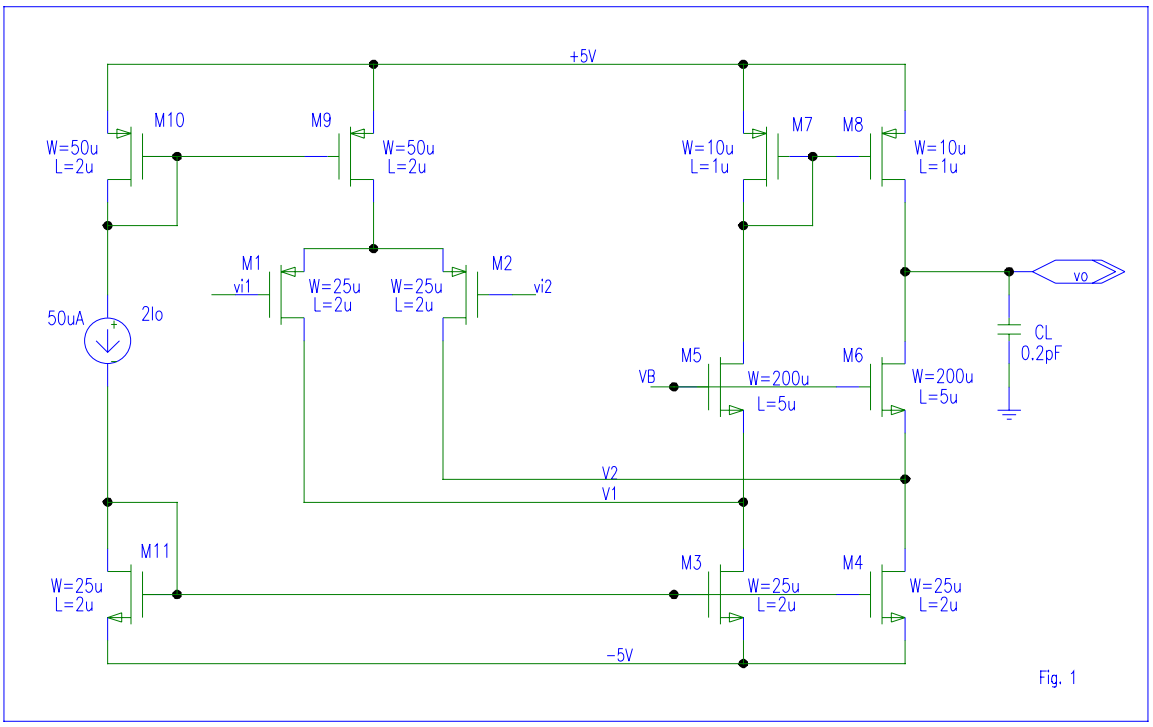
| | **Homework #12** | **EECS 140** |
| **B. E. Boser** | Due 12/03/99 before noon in 497 Cory | **Fall 1999** |

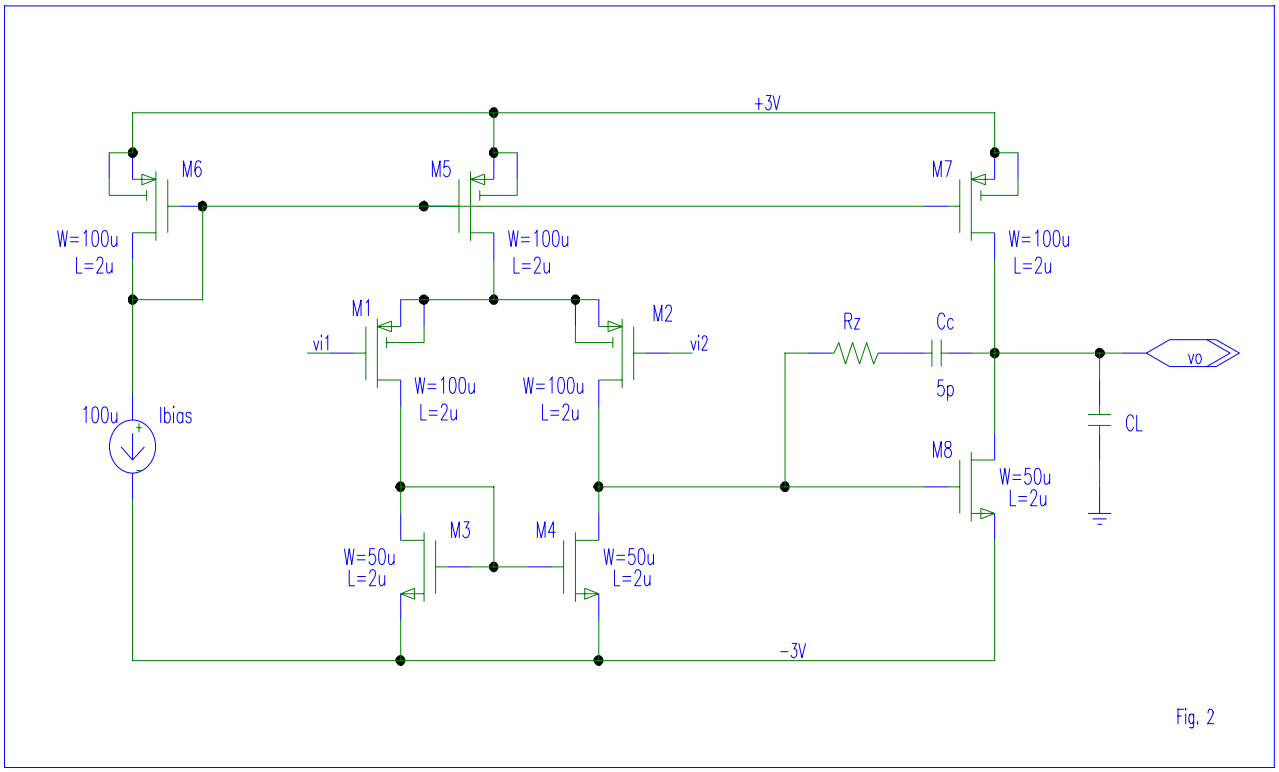
**Note:** Use the device parameters given in the class handout "Device Parameters & SPICE Models" and also available on the EECS 140 website, **http://kowloon.eecs.berkeley.edu/~courses/140**

1) Consider the circuit shown in Fig.1. Neglect extrinsic parasitic capacitances and body effect in your analysis.
   a) Estimate the unity gain frequency and lowest frequency non-dominant pole.
   b) Determine the phase margin of this circuit for unity gain feedback. Neglect the pole-zero doublet caused by M7-M8. Assume that the feedback circuit does not load the amplifier output (ideal buffer in feedback loop).
   c) Find the *minimum* value of the load capacitor $C_L$' that yields a phase margin of 60 degrees for unity gain feedback.
   d) Assume $C_L$=$C_L$', but $I_0$ is cut in half while all other parameters are left unchanged (W/L's, VDD, VSS, etc.). Will the phase margin of the amplifier increase or decrease? By how much will it change?
   e) Repeat (d) for the case where W1 and W2 are doubled ($C_L$=$C_L$' and $I_O$ as in the original circuit).
   f) Verify (b) and (c) with SPICE. Plot the magnitude and phase of the return ratio for the case with $C_L$ and $C_L$' in one diagram. Mark the results from your hand analysis.
   g) *Optional*: Verify (e) and (f) with SPICE.



2) Consider the amplifier shown in Fig. 2. Neglect both intrinsic and extrinsic parasitic capacitances in the analysis of the circuit. Neglect channel length modulation in bias point calculations.

a) Find the value of $R_z$ that moves the RHP zero to infinity.
b) Calculate the unity gain frequency and non-dominant poles contributed by the load and compensation. Calculate the *maximum* value $C_{Lmax}$ that still yields a phase margin of 60 degrees. Assume unity feedback and $R_z$ from part (a).
c) Double W1, W2 and W5 and calculate the new unity gain frequency and phase margin (Assume $C_L=C_{Lmax}$).
d) Double W7 and W8 and readjust $R_z$ to keep the zero at infinity. Calculate the new unity gain frequency and phase margin.
e) Double $I_{bias}$ and readjust $R_z$ to keep the zero at infinity. Calculate the new unity gain frequency and phase margin.
f) Assume $C_L$=2pF and calculate $R_z$ such that the resulting zero cancels the lowest frequency non-dominant pole of the circuit. What are the unity gain frequency and phase margin for the so compensated circuit?
g) Verify (b) using SPICE. Show a Bode plot of the return ratio for the calculated $C_{Lmax}$. In the same plot, show the frequency response and phase margin for $R_z$=0.
h) *Optional*: Verify (c) through (f) using SPICE.



**3)** The folded cascode amplifier of Fig.1 is used as a voltage follower as shown in Fig.3. Assume that the total load capacitance is $C_L$=10pF.

a) Calculate the systematic offset error $V_{os}$ of the amplifier.
b) Calculate the static settling error caused by the finite gain of the amplifier.
c) Calculate the slew rate and settling time constant.
d) Suggest a simple change (new W/L for selected devices) to:
(i) double the slew rate (ii) reduce the settling time constant by a factor of 2.
e) Calculate the settling time $t_s$ that it takes for the amplifier to settle within 0.1% of the final output for an input voltage step of $\Delta$Vi=50mV.
f) Repeat (e) for $\Delta$Vi=500mV.
g) Verify your results using SPICE as follows:

- Systematic offset voltage (closed loop system, .DC). Show the plot of a .DC analysis to find $V_{in}$ such that $V_{out}$=0. (Add source in series with input to cancel amp systematic offset for subsequent analyses).
- Static settling error (closed-loop, .DC): Show the static error in $V_{out}$ for Vin=-1V…1V. Plot abs[(Vout-Vin)·100 (%)]. Record the static output voltages $V_{o+}$ and $V_{o-}$ for both voltages steps of ±25mV and ±250mV.
- Dynamic settling error (.TRAN). Use the following input stimulus to test for both a positive and negative transition:
  `vin vin 0 pwl 0 -25m 100n -25m 120n 25m 2000n 25m 2020n -25m`
  Use the static settling values $V_{o+}$ and $V_{o-}$ to generate plots for the dynamic deviation. Plot [100%·($V_{out}$ - $V_{o+}$)/25mV] and [100%·($V_{out}$ - $V_{o-}$)/25mV] for the two settling values respectively. Scale properly and mark the settling time $t_s$ for each case.
- Repeat the .TRAN analysis for the voltage step of ±250mV.

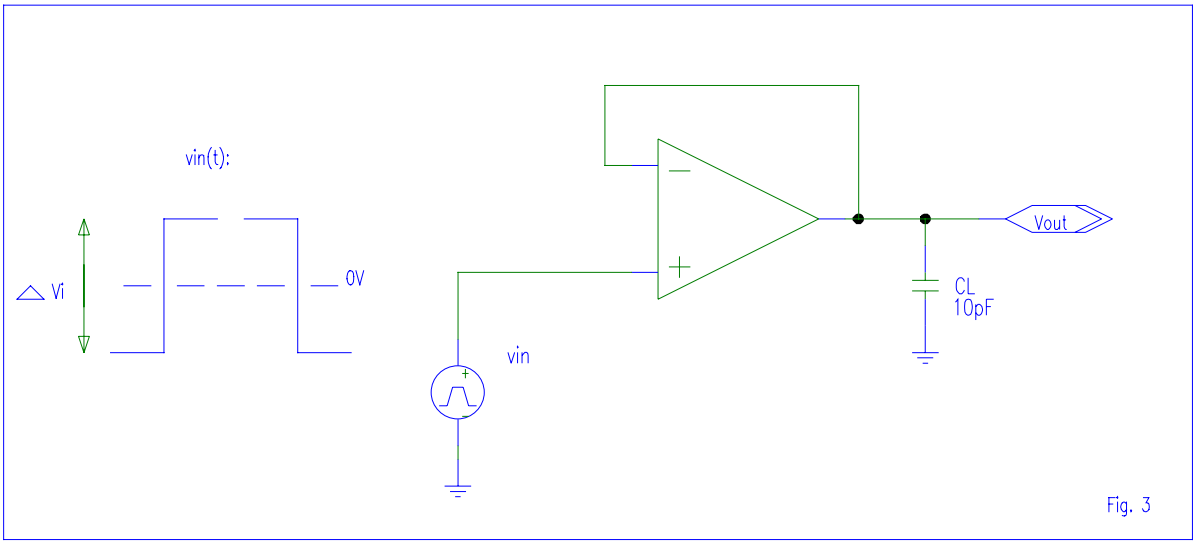


Fig. 3

**4)** Suppose that the amplifier of Fig.2 is used as a voltage follower as shown in Fig.3. Assume that the total load capacitance is $C_L$=10pF.

a) Calculate the slew rate that is determined by the drain current $I_{D5}$.
b) Calculate the slew rate that is determined by the drain current $I_{D7.}$
c) Which of the two calculated slew rates define the slew rate for
   (i) a positive slewing output ?
   (ii) a negative slewing output ?
d) Calculate the maximum load capacitor $C_L$ for which positive and negative slew rates are identical.