UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Homework #11	**EECS 140**
B. E. Boser	Due 11/19/99 before noon in 497 Cory	**Fall 1999**

Note: Use the device parameters given in the class handout "Device Parameters & SPICE Models" and also available on the EECS 140 website, **http://kowloon.eecs.berkeley.edu/~courses/140**

1) Consider the circuit shown in Fig.1. Assume that the OpAmp has infinite input impedance, zero output impedance and that its transfer function can be modeled using the following transfer function:

$$Vo(s) = Vid \frac{a_0}{1 + s/p_1}$$

   a) Find an analytical expression for the return ratio (RR) of the circuit.
   b) Calculate the unity gain frequency f_u and phase margin φ_m of the return ratio for a_0=1000 and p_1= -2π·1kHz. Is the circuit stable?
   c) Verify part (b) using SPICE. Refer to the class handout "Return Ratio Simulation with SPICE". Print a Bode plot showing the magnitude and phase of the RR. In your plot, mark up the simulated phase margin and show the results from your hand analysis.
   Hint: You can model the OpAmp using a LAPLACE expression in SPICE. Alternatively, you can use a circuit consisting of two voltage controlled voltage sources ("E") and one RC combination.

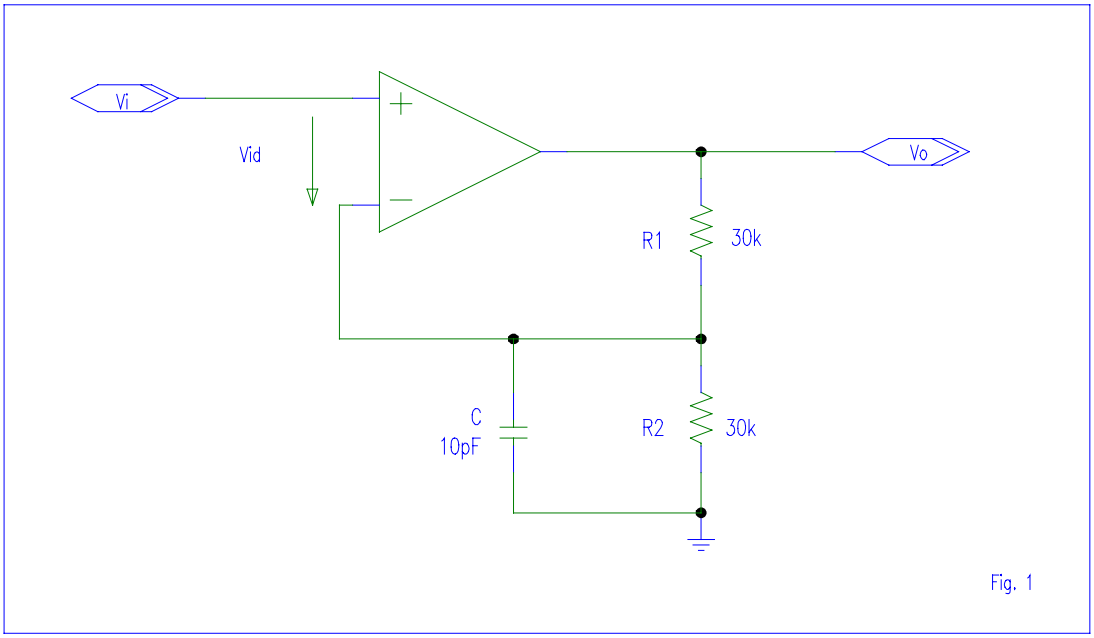
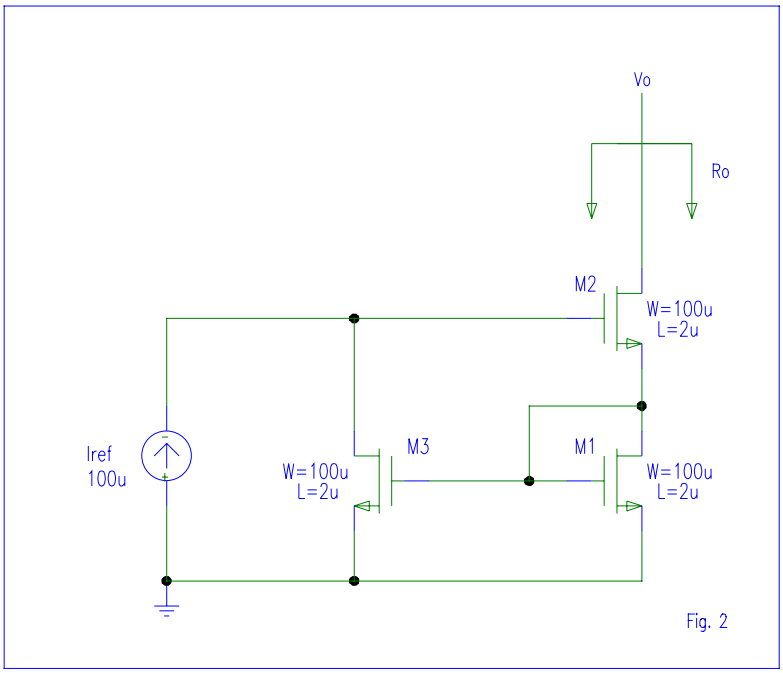


Fig. 1

2) Consider the Wilson current source circuit shown in Fig. 2. Neglect body effect and both intrinsic and extrinsic parasitic capacitances in the analysis of the circuit. Neglect channel length modulation in large signal calculations.

a) Calculate the return ratio (RR) of the circuit.
b) Calculate the output impedance R_o at node V_o using Blackman's formula.



3) Fig. 3 shows a V_{BE}-referenced self –bias circuit used in an integrated circuit (startup circuit not shown). In order to test the circuit and externally modify the bias current, the chip designer made the node V_x "off-chip" accessible by connecting it to one of the device pins. Due this connection, there are now parasitic capacitances present at node V_x. All these parasitics have been lumped into capacitor C as shown in Fig. 3.
In the analysis of the circuit, neglect channel length modulation, body effect, extrinsic *and* intrinsic parasitic devices capacitances unless otherwise stated.

Important Notes:

- The circuit examined here has a ***positive*** feedback loop.
- A circuit with positive feedback is unstable unless its return ratio is <1.

a) Find the large signal bias point, assuming the circuit is stable, i.e. a "normal" reference that started up correctly.
b) Find expression for the compound transconductance G_{m2} as function of g_{m2}, R and C_x. Note that G_{m2} is frequency dependent.
c) Draw the complete small signal model for the circuit. Use the compound device from (b) to replace M2, R and C_x. Assume that C_1=0.
d) Break the loop, either at the G_{m2} or g_{m3} transconductor. Again, assume C_1=0. Find the return ratio of the circuit. Is the circuit stable?
e) Verify (d) using SPICE. Perform a .AC analysis to plot the phase and magnitude of the return ratio. Mark your hand analysis results in the plot. (Note that now the intrinsic parasitic capacitances will be present in your circuit).

f) Perform a .TRAN analysis to show the oscillation at node V_x. . Measure the oscillation frequency and mark this value in your plot from (e). Hint: Use a 100mV voltage step on top of VDD to initialize the oscillation.

g) Calculate the minimum value for C_1 that stabilizes the circuit.

h) Repeat (e) and (f) with the calculated value from part (g). The circuit should now be stable.

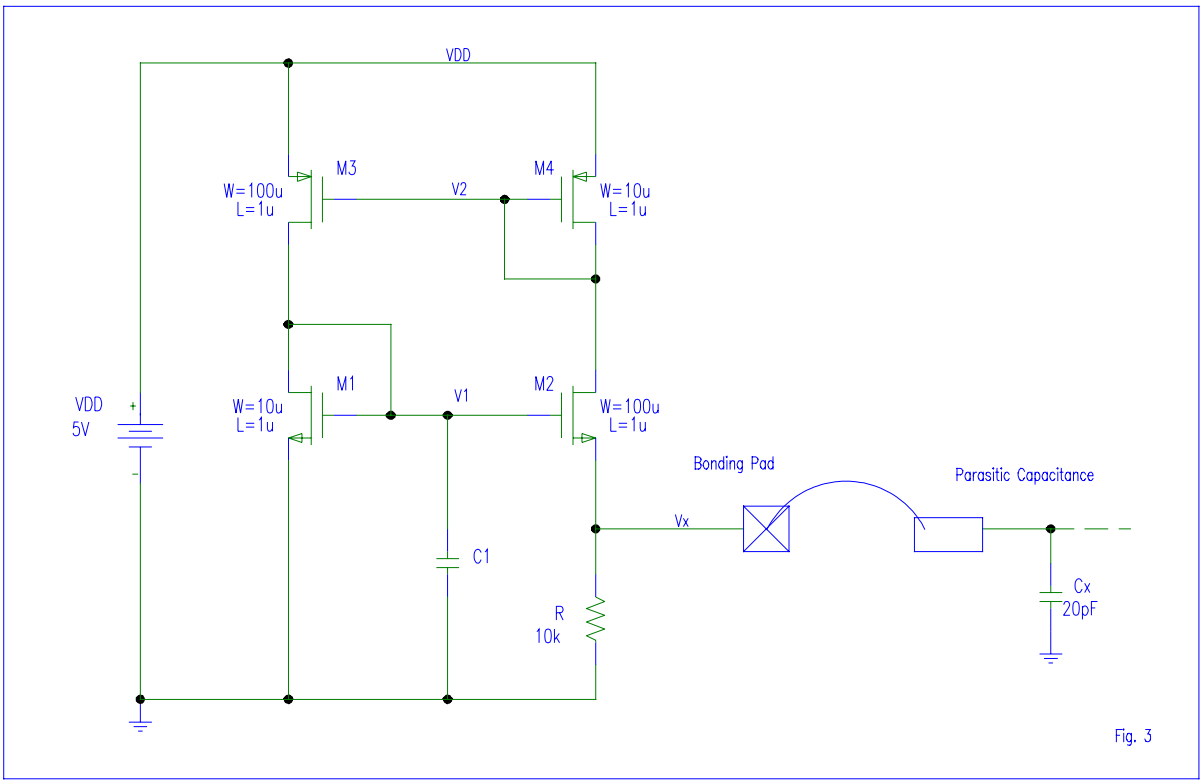


Fig. 3