UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

B. E. Boser | **Homework #10** Due 11/05/99 before noon in 497 Cory | **EECS 140** **Fall 1999**

Note: Use the device parameters given in the class handout "Device Parameters & SPICE Models" and also available on the EECS 140 website, **http://kowloon.eecs.berkeley.edu/~courses/140**

You are to design a folded cascode OTA that has a singled ended output and utilizes a PMOS differential input pair. The power supply for the circuit is a single voltage source VDD that is fixed at 3V. The following specifications should be met:

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Common Mode Voltage	V_{icm}		0		1	V
Output Voltage	V_{out}		0.6		2.4	V
Low Frequency Differential Mode Gain	A_{dm0}		60			dB
Unity Gain Frequency	f_u	C_L=10pF	20			MHz
Low Frequency Common Mode Rejection Ratio	CMRR		130			dB

Suggestions and constraints:

- You are allowed to use one ideal floating bias current source.
- For simplicity, use the same channel length and V_{dsat} for all devices.
- Maximize V_{dsat} to minimize C_{in} and layout area.

Initial Design and Hand Analysis:

a) Choose a circuit topology that is likely to meet the specification. Verify qualitatively that your topology is capable of meeting the specifications for the output range and input common mode range.
b) Calculate the minimum G_m that is required to meet the bandwidth specification.
c) Find the maximum V_{dsat} that will satisfy the output range requirement.
d) Find the required bias currents for your topology from the above. Draw the circuit showing all branch currents and node voltages at the bias point.
e) Estimate the minimum channel length that will still meet the gain requirement.
f) Calculate all W/L. Neglect the effect of lambda and body effect in your hand calculations (V_{DS} and V_{SB} are small for most devices).
g) Estimate the CMRR of your circuit. Modify your circuit if you don't meet the specification.

Verification and Refinement using SPICE:

- Include channel length modulation and body effect in your simulations.
- Include only intrinsic parasitic device capacitances.
- Modify your design until all the specifications are met.
- Mark all calculated values in your plots

a) Verify the Gain requirement by performing a .DC analysis. Printout the small signal differential gain of the circuit for V_{out}=0.6…2.6V (V_{icm}=0V). Repeat for V_{icm}=1V.
b) Perform an AC analysis to find the unity gain frequency f_u of the differential gain for C_L=10pF. Printout the resulting Bode plot.
c) Perform a .TF analysis to find the common mode gain. Calculate the CMRR.