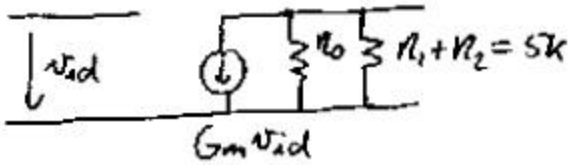
EECS 140 Solution HW8

(1) a) $G_m = g_{m1} = g_{m2} = \sqrt{I_{bias} \cdot k' \frac{W}{L}} = \sqrt{0.6m \cdot \frac{0.2m \cdot 100}{3}} = \underline{2mS}$

$R_o = r_{o3} \| r_{o1} = \frac{1}{2} \frac{1}{\lambda I_D} = \frac{1}{2} \frac{1}{0.033 \cdot 300\mu} = \underline{50k\Omega}$

$A_{dmo} = G_m R_o = 2mS \cdot 50k\Omega = \underline{100}$

b)



$\Rightarrow A_{dm} = G_m \cdot \left(R_o \| (R_1+R_2)\right) = 2mS \cdot 4.545k = \underline{9.09}$ effective open loop gain

$\Rightarrow \frac{v_o}{v_i} = \frac{A_{dm}}{1 + A_{dm} \cdot f} \qquad f = \frac{R_2}{R_1+R_2} = 0.2$

$\frac{v_o}{v_i} = \frac{9.09}{1 + 9.09 \cdot 0.2} = \underline{3.22}$

c) Adm with Buffer is 100

$\Rightarrow \frac{v_o}{v_i} = \frac{100}{1 + 100 \cdot 0.2} = \underline{4.76}$

(compare with ideal OpAmp $A_{dm} \to \infty$

$\frac{v_o}{v_i} = 1 + \frac{R_2}{R_1} = 5$

w/ Buffer	4.76	error = 4.8%
w/o Buffer	3.22	error = 35.6%!)

$\Rightarrow$ d) Resistive feedback causes a substancial decrease in the amplifiers open loop gain. Ideally want the open loop gain to be as large as possible ($\to \infty$ ideally)

(1) e) Opamp ≃ OTA + Output stage

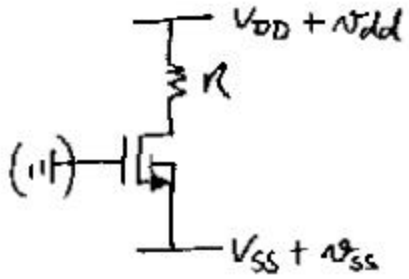
Why OTAs on chip?

- Reduced power consumption
- Reduced layout area

} since there is no O/P stage

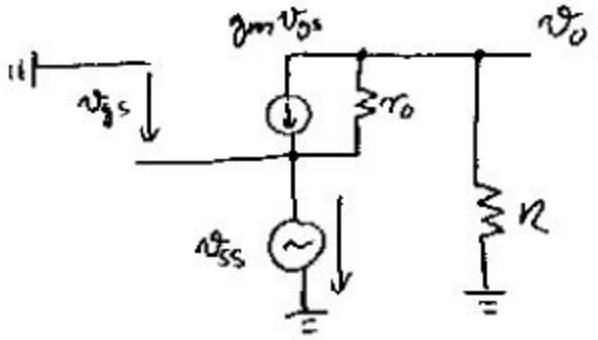
- In some cases, output stage would introduce additional unwanted nonlinearity
- design time might be shorter

(2)



$$A_V = \frac{g_m}{\frac{1}{r_o} + \frac{1}{R}}$$

a) PSRR⁻:



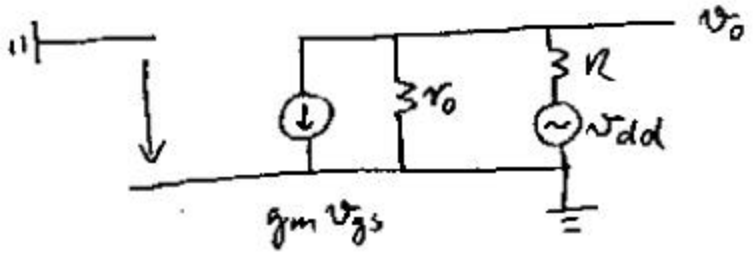
$v_{gs} = -v_{ss}$

$$0 = v_o\left(\frac{1}{R} + \frac{1}{r_o}\right) + v_{ss}\left(-g_m - \frac{1}{r_o}\right)$$

$$\Rightarrow A_{vss} = \frac{v_o}{v_{ss}} = \frac{\frac{1}{r_o} + g_m}{\frac{1}{r_o} + \frac{1}{R}} = \frac{1 + g_m r_o}{1 + \frac{r_o}{R}}$$

$$\Rightarrow PSRR^- = \frac{A_v}{A_{vss}} = \frac{g_m}{\frac{1}{r_o} + g_m} \simeq 1 \quad !$$

(2) (b) PSRR+:



$\rightarrow v_{gs} = 0$

$\Rightarrow \frac{v_o}{v_{dd}} = A_{vDD} = \frac{r_o}{r_o + R}$

$\Rightarrow PSRR^+ = \frac{A_v}{A_{vDD}} = \frac{g_m (r_o + R)}{1 + \frac{r_o}{R}}$

(→ interesting case: $r_o \rightarrow \infty$

$\Rightarrow A_v \rightarrow g_m R$

$A_{vDD} \rightarrow 1$

$PSRR^+ \rightarrow g_m R$)

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(3) a) $A_{dmo} = g_m \cdot \frac{r_o}{2} = \frac{1}{\lambda V_{dsat}}$ (see Hw 3!)

$A_{dmo} \geq 100$

$\Rightarrow V_{dsat} \geq \frac{1}{\lambda A_{dmo}} = \frac{1}{0.05 \cdot 100} = \underline{200mV}$

$\Rightarrow$ choose $V_{dsat} = 200mV$ for minimum input cap.

$C_{IN} \propto WL$; $W \propto \frac{1}{V_{dsat}^2}$

b) $f_u = \frac{1}{2\pi} \frac{G_m}{C_L} \Rightarrow G_m \geq 2\pi f_u C_L$

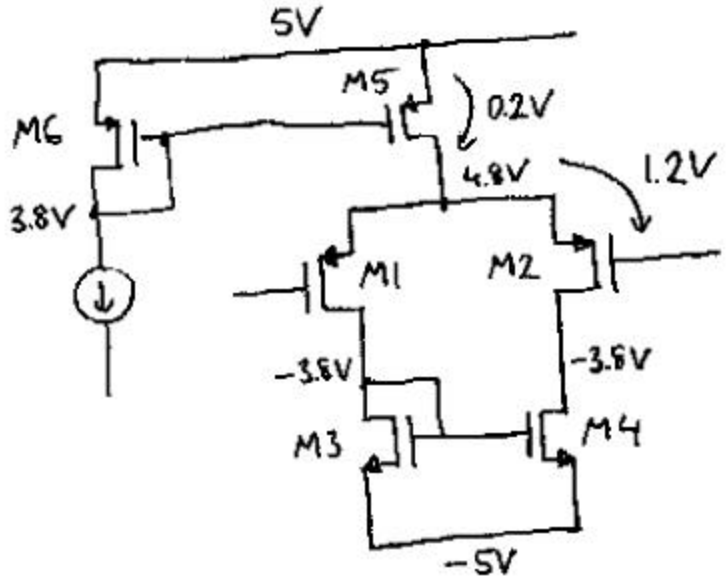
$G_m \geq 2\pi \cdot 30MHz \cdot 10pF$

$\underline{G_m \geq 1.885mS}$

$G_m = g_m = \frac{2I_D}{V_{dsat}} = \frac{I_{bias}}{V_{dsat}}$

$\Rightarrow I_{bias} = 1.885mS \cdot 0.2V = \underline{377\mu A} \rightsquigarrow 380\mu A$

c)



$\Rightarrow V_{icm} = 5V - 1.4V = \underline{3.6V}$

(3) c) ctd.

$\left(\frac{W}{L}\right)_1 \stackrel{!}{=} \left(\frac{W}{L}\right)_2$:

$I_D = \frac{1}{2} k' \frac{W}{L} V_{dsat}^2 (1 + \lambda V_{DS})$

$188.5\mu = 50\mu \left(\frac{W}{L}\right)_1 \cdot 0.2^2 (1 + 0.05 \cdot 8.6V)$

$\Rightarrow \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 65.91 \rightarrow$ choose $\frac{132}{2}$ //

$\left(\frac{W}{L}\right)_3 \stackrel{!}{=} \left(\frac{W}{L}\right)_4$:

$I_D = 188.5\mu = 100\mu \left(\frac{W}{L}\right) \cdot 0.2^2 (1 + 0.05 \cdot 1.2)$

$\Rightarrow \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 44.46 \rightarrow$ choose $\frac{89}{2}$ //

→ M5 and M6 have different VDS, but we want these devices to match so:

$\left(\frac{W}{L}\right)_5 \stackrel{!}{=} \left(\frac{W}{L}\right)_6$

$377\mu = 50\mu \left(\frac{W}{L}\right) \cdot 0.2^2 (1 + 0.05 \cdot 0.2)$

$\Rightarrow \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = 186.63$

→ choose $\frac{400}{2}$ // (leave a little headroom to avoid triode region)

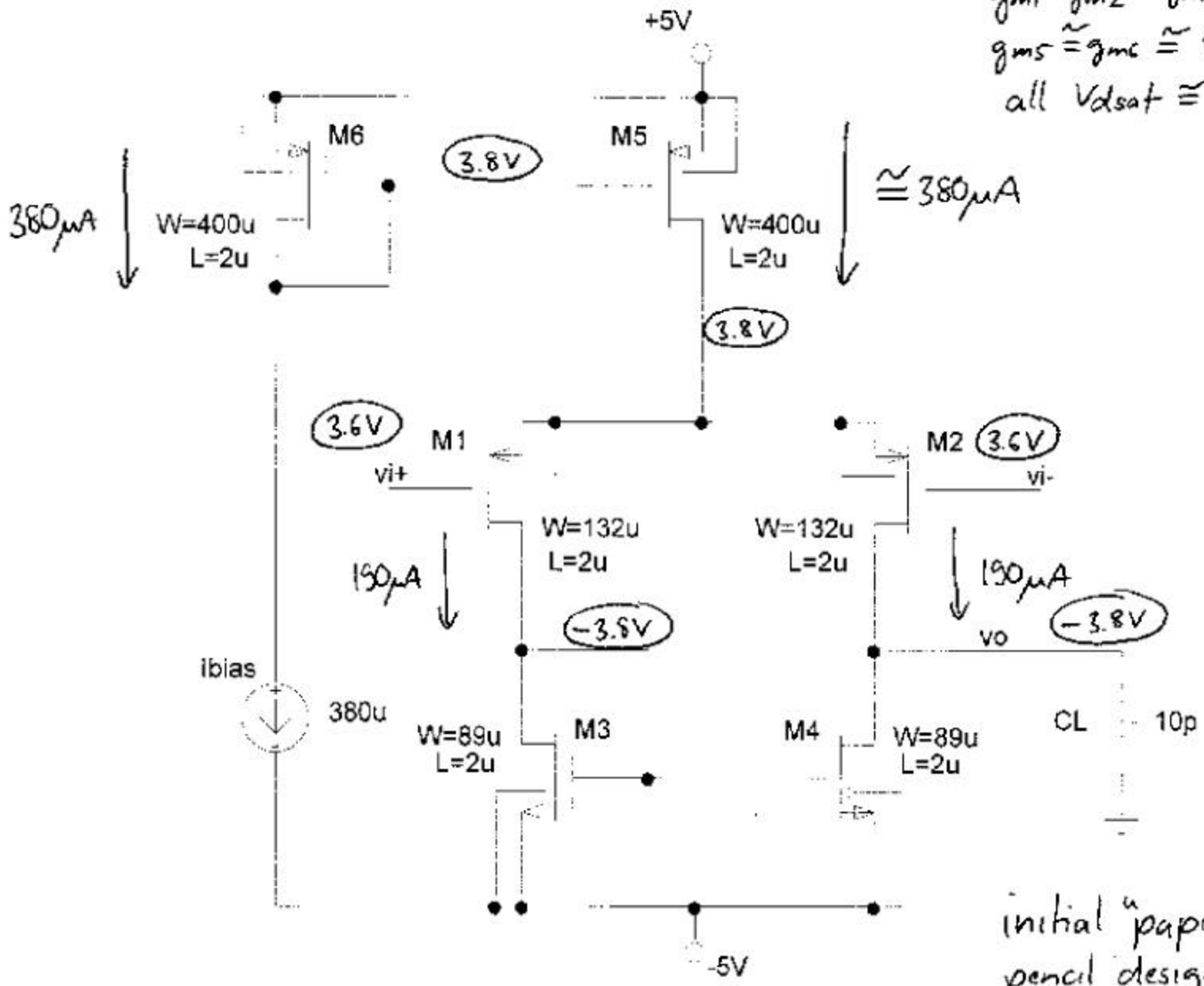
(d) annotated schematic see attached

(3) d)

$g_{m1} = g_{m2} = g_{m3} = g_{m4} = 1.885\,mS$

$g_{m5} \cong g_{m6} \cong 3.8\,mS$

all $V_{dsat} \cong 200\,mV$



initial "paper and pencil design"

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(3) e) f) initial simulation results:

$\frac{dV_o}{dV_i} > 100$ for $-4.5 \leq V_o \leq 4$ SPEC MET ✓ *

$f_u = 29.167\ MHz < 30MHz$ SPEC NOT MET **

* The gain is higher than estimated in (a). Reason:
$A_{dmf} = \frac{1}{\lambda V_{dsat}}$ is an approximate expression
(using $r_o \cong \frac{1}{\lambda I_D}$, but $r_o = \frac{1+\lambda V_{DS}}{I_D \cdot \lambda}$)

calculated: $A_{dmo} \overset{!}{=} 100$ @ $V_o = -3.8V$
simulated: $A_{dmo} = 123$ @ $V_o = -3.8V$
} ≈ 20% error

** This is due to the fact that $I_{D5} \neq I_{D6}$ due to the difference in V_{DS}. To fix this, we simply increase I_{bias}!

second run: Use $I_{bias} = 420\mu A$

$\frac{dV_o}{dV_i} > 100$ for $-4.5 \leq V_o \leq 4$ SPEC MET ✓ → see plot

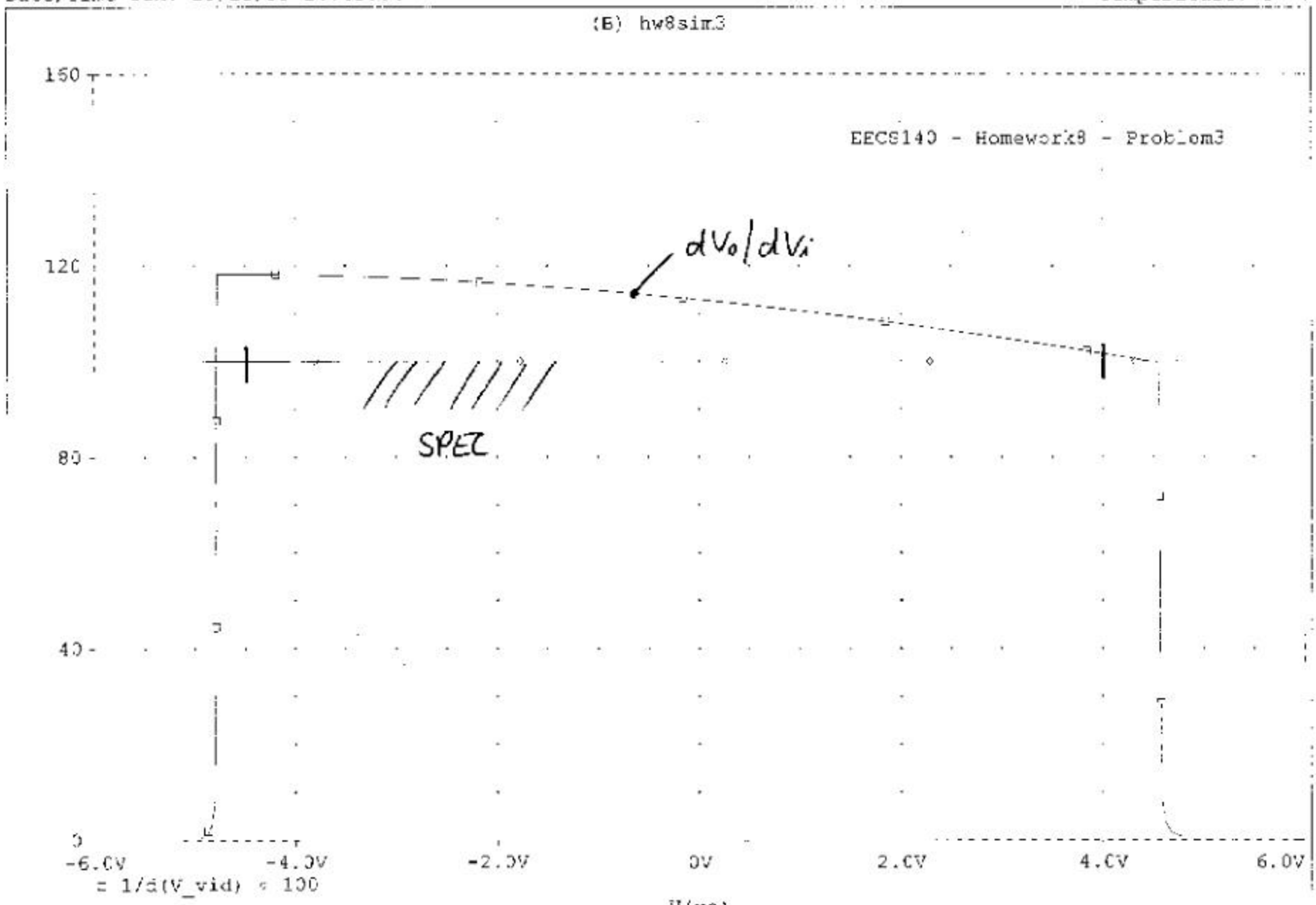
$f_u = 30.65\ MHz > 30MHz$ SPEC MET ✓ → see plot

Important note: After changing the bias current, you will always have to verify the ROP of each device! Change V_{icm} if necessary.

* D:\Ee140\spice\hw8sim3.sch

Date/Time run: 10/21/99 16:42:51 Temperature: 27.0

(B) hw8sim3



Date: October 21, 1999 Page 1 Time: 16:45:21

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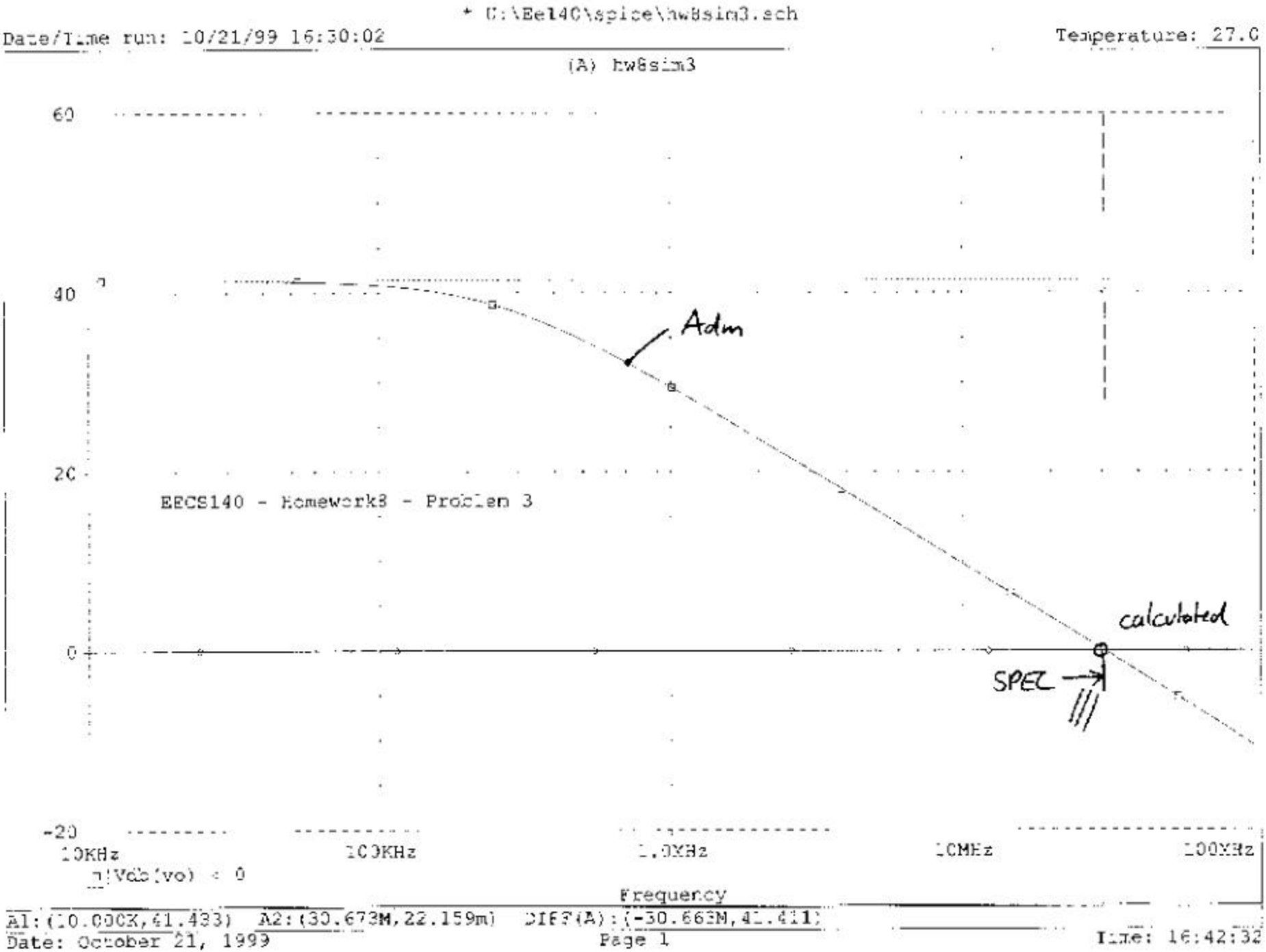
* C:\Ee140\spice\hw8sim3.sch
Date/Time run: 10/21/99 16:30:02
Temperature: 27.0
(A) hw8sim3
60
40
20
0
-20
Adm
calculated
SPEC
EECS140 - Homework8 - Problem 3
10KHz
100KHz
1.0MHz
10MHz
100MHz
n(Vdb(vo)) = 0
Frequency
A1:(10.000K,41.433)
A2:(30.673M,22.159m)
DIFF(A):(-30.663M,41.411)
Date: October 21, 1999
Page 1
Time: 16:42:32

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** eecs140 homework8 #3

** schematics netlist **

vdd         vdd 0       5
vss         0  vss      5
v_vid       vid 0       dc 0v ac 1
e_e2        vi- vicm vid 0 -0.5
e_e1        vi+ vicm vid 0 0.5
r_rdumm     0 vid  1
v_vic       vicm 0 3.6
c_cl        0 vo  10p

m_m6         vbp vbp vdd vdd pmos2 l=2u w=400u
m_m5         1 vbp vdd vdd   pmos2 l=2u w=400u
m_m1         2 vi+ 1 1       pmos2 l=2u w=132u
m_m2         vo vi- 1 1      pmos2 l=2u w=132u
m_m3         2 2 vss vss     nmos2 l=2u w=89u
m_m4         vo 2 vss vss    nmos2 l=2u w=89u
i_ibias      vbp vss dc 420u


** analysis setup **
.include ee140.mod
.ac dec 101 10k 100meg
.dc v_vid -200m 200m 0.1m
.option post brief


******  operating point information      tnom=  25.000 temp=  25.000

   node    =voltage      node    =voltage      node    =voltage

+0:1       =   4.8058  0:2       =  -3.7942  0:vbp     =   3.8009
+0:vdd     =   5.0000  0:vi+     =   3.6000  0:vi-     =   3.6000
+0:vicm    =   3.6000  0:vid     =   0.      0:vo      =  -3.7942
+0:vss     =  -5.0000

**** mosfets
element  0:m_m6     0:m_m5     0:m_m1     0:m_m2     0:m_m3     0:m_m4

model    0:pmos2    0:pmos2    0:pmos2    0:pmos2    0:nmos2    0:nmos
2
 id      -420.0000u -399.8496u -199.9248u -199.9248u  199.9248u  199.9
248u
 ibs        0.         0.         0.         0.         0.         0.

 ibd       11.9906f    1.9417f   85.9998f   85.9998f  -12.0585f  -12.0
585f
 vgs       -1.1991    -1.1991    -1.2058    -1.2058     1.2058     1.2
058
 vds       -1.1991  -194.1701m   -8.6000    -8.6000     1.2058     1.2
```

vbs	0.	0.	0.	0.	0.	0.
vth	-1.0000	-1.0000	-1.0000	-1.0000	1.0000	1.0000
vdsat	-199.0588m	-194.1701m	-205.8299m	-205.8299m	205.8451m	205.8451m
beta	21.1991m	20.1942m	9.4380m	9.4380m	9.4366m	9.4366m
gam eff	500.0000m	500.0000m	500.0000m	500.0000m	500.0000m	500.0000m
gm	4.2199m	3.9211m	1.9426m	1.9426m	1.9425m	1.9425m
gds	19.8122u	118.5232u	6.9904u	6.9904u	9.4278u	9.4278u
gmb	1.3620m	1.2655m	626.9784u	626.9784u	626.9321u	626.9321u
cdtot	6.4008f	126.4252f	15.1498f	15.1498f	1.4322f	1.4322f
cgtot	2.7647p	2.8832p	924.5061f	924.5061f	614.5575f	614.5575f
cstot	2.6691p	2.6676p	880.8063f	880.8063f	593.8770f	593.8770f
cbtot	89.1891f	89.1891f	28.5499f	28.5499f	19.2483f	19.2483f
cgs	2.6691p	2.6676p	880.8063f	880.8063f	593.8770f	593.8770f
cgd	6.4008f	126.4252f	15.1498f	15.1498f	1.4322f	1.4322f