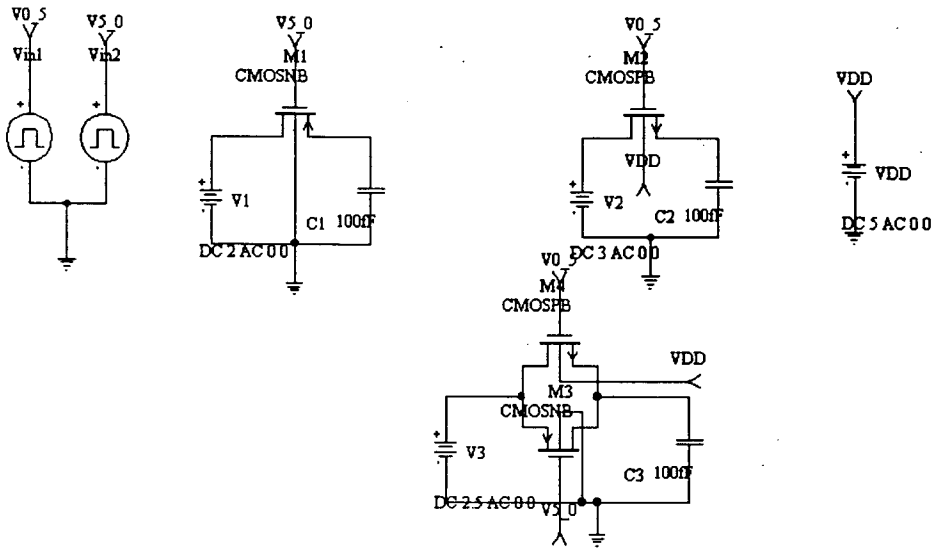
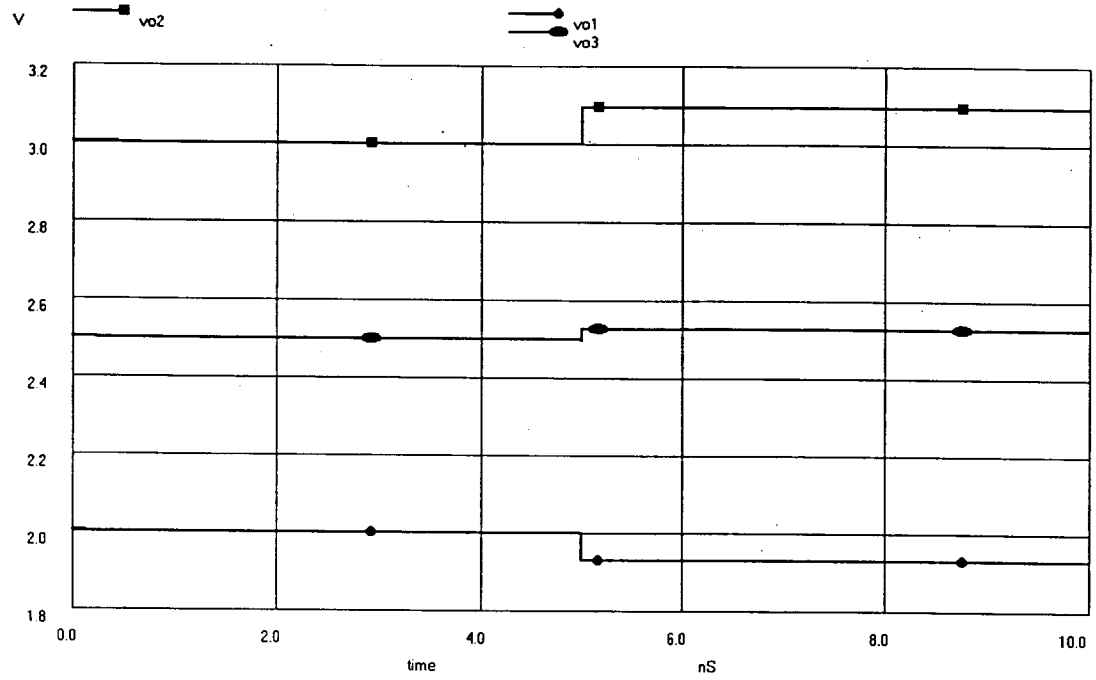
Problem 27.1

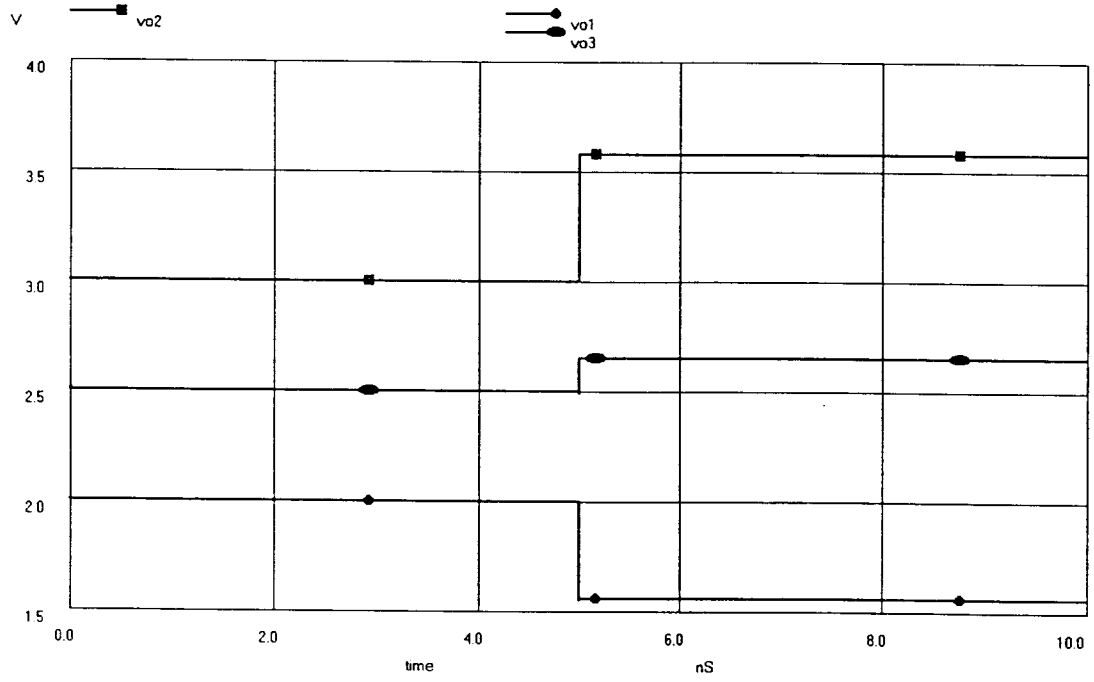



```
*** Top Level Netlist ***
C1        0 Vo1 100fF
C2        0 Vo2 100fF
C3        0 Vo3 100fF
M1        1 V5_0 Vo1 0 CMOSNB  L=2u W=3u
M2        5 V0_5 Vo2 VDD CMOSPB  L=2u W=3u
M3        Vo3 V5_0 9 0 CMOSNB  L=2u W=3u
M4        9 V0_5 Vo3 VDD CMOSPB  L=2u W=3u
V1        1 0       DC 2 AC 0 0
V2        5 0       DC 3 AC 0 0
V3        9 0       DC 2.5 AC 0 0
VDD       VDD 0  DC 5 AC 0 0
Vin1      V0_5 0 DC 0 AC 0 0 PULSE(0 5 5ns 1ps 1ps 5ns 10ns)
Vin2      V5_0 0 DC 0 AC 0 0 PULSE(5 0 5ns 1ps 1ps 5ns 10ns)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=5mv
.op
.tran .1ns 10n 0 .1n
.end
```

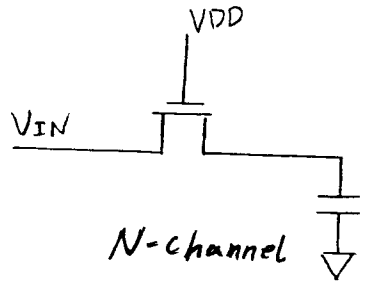
C = 100fF



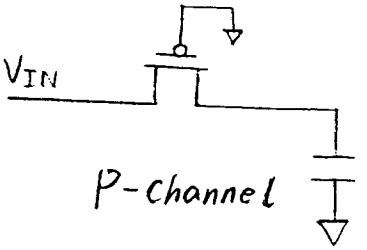
C = 15fF



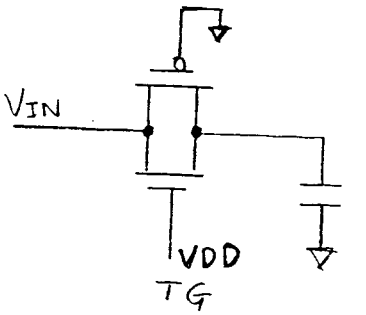
Problem 27.2



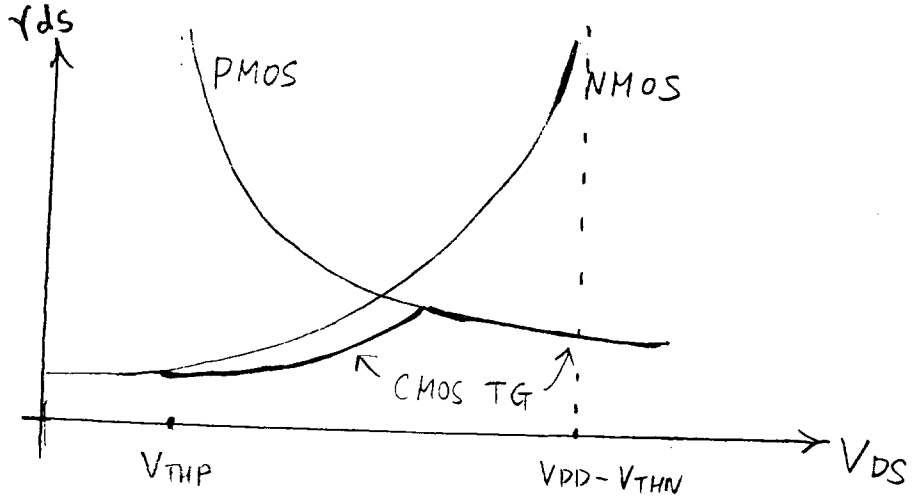
$$r_{on} = \frac{1}{\beta(V_{GS} - V_{THN})} = \frac{1}{\beta(V_{DD} - V_{IN} - V_{THN})}$$



$$r_{op} = \frac{1}{\beta(V_{GS} - V_{THN})} = \frac{1}{\beta(V_{IN} - V_{THP})}$$



$$r_o = r_{on} \,//\, r_{op}$$



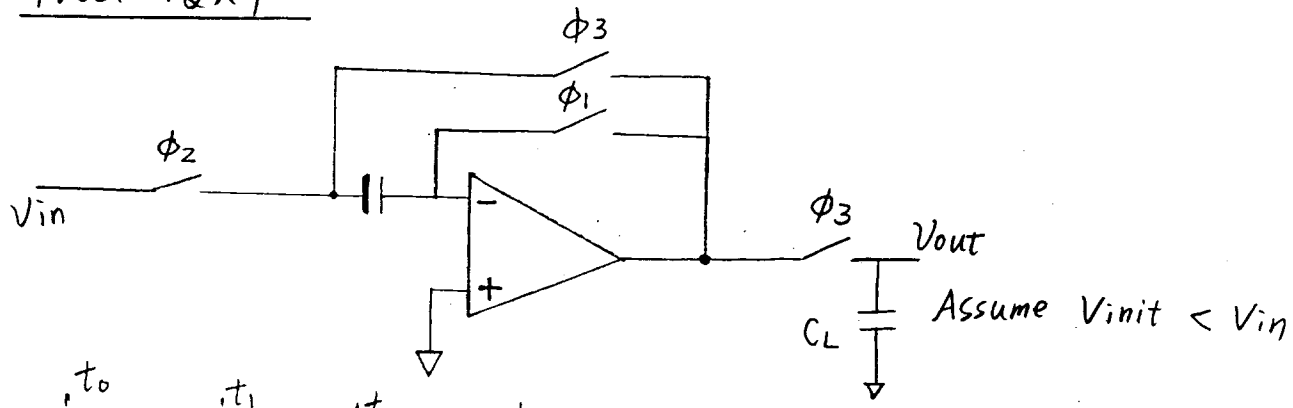
Problem 27.3

C(F)	VN (V)
1.00E-15	0.002035
1.10E-14	0.000613
2.10E-14	0.000444
3.10E-14	0.000365
4.10E-14	0.000318
5.10E-14	0.000285
6.10E-14	0.000261
7.10E-14	0.000241
8.10E-14	0.000226
9.10E-14	0.000213
1.01E-13	0.000202
1.11E-13	0.000193
1.21E-13	0.000185
1.31E-13	0.000178
1.41E-13	0.000171
1.51E-13	0.000166
1.61E-13	0.00016
1.71E-13	0.000156
1.81E-13	0.000151
1.91E-13	0.000147
2.01E-13	0.000144
2.11E-13	0.00014
2.21E-13	0.000137
2.31E-13	0.000134
2.41E-13	0.000131
2.51E-13	0.000128
2.61E-13	0.000126
2.71E-13	0.000124
2.81E-13	0.000121
2.91E-13	0.000119
3.01E-13	0.000117
3.11E-13	0.000115
3.21E-13	0.000114
3.31E-13	0.000112
3.41E-13	0.00011
3.51E-13	0.000109
3.61E-13	0.000107
3.71E-13	0.000106
3.81E-13	0.000104
3.91E-13	0.000103
4.01E-13	0.000102
4.11E-13	0.0001
4.21E-13	9.92E-05
4.31E-13	9.8E-05
4.41E-13	9.69E-05
4.51E-13	9.58E-05
4.61E-13	9.48E-05
4.71E-13	9.38E-05

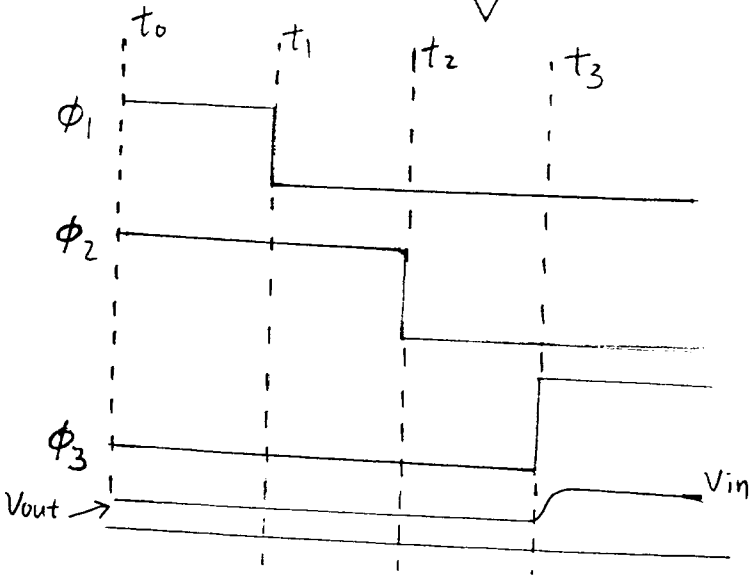
4.81E-13	9.28E-05
4.91E-13	9.18E-05
5.01E-13	9.09E-05
5.11E-13	9E-05
5.21E-13	8.91E-05
5.31E-13	8.83E-05
5.41E-13	8.75E-05
5.51E-13	8.67E-05
5.61E-13	8.59E-05
5.71E-13	8.51E-05
5.81E-13	8.44E-05
5.91E-13	8.37E-05
6.01E-13	8.3E-05
6.11E-13	8.23E-05
6.21E-13	8.16E-05
6.31E-13	8.1E-05
6.41E-13	8.04E-05
6.51E-13	7.97E-05
6.61E-13	7.91E-05
6.71E-13	7.85E-05
6.81E-13	7.8E-05
6.91E-13	7.74E-05
7.01E-13	7.68E-05
7.11E-13	7.63E-05
7.21E-13	7.58E-05
7.31E-13	7.53E-05
7.41E-13	7.47E-05
7.51E-13	7.42E-05
7.61E-13	7.38E-05
7.71E-13	7.33E-05
7.81E-13	7.28E-05
7.91E-13	7.23E-05
8.01E-13	7.19E-05
8.11E-13	7.14E-05
8.21E-13	7.1E-05
8.31E-13	7.06E-05
8.41E-13	7.02E-05
8.51E-13	6.97E-05
8.61E-13	6.93E-05
8.71E-13	6.89E-05
8.81E-13	6.86E-05
8.91E-13	6.82E-05
9.01E-13	6.78E-05
9.11E-13	6.74E-05
9.21E-13	6.7E-05
9.31E-13	6.67E-05
9.41E-13	6.63E-05
9.51E-13	6.6E-05
9.61E-13	6.56E-05
9.71E-13	6.53E-05
9.81E-13	6.5E-05

9.91E-13	6.46E-05
1.00E-12	6.43E-05

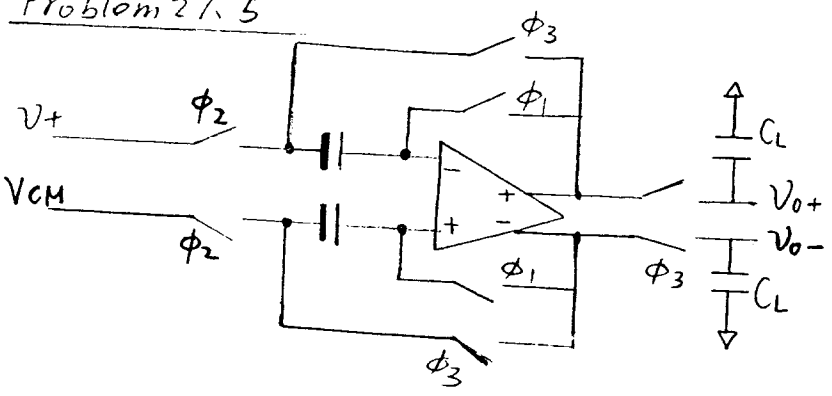
Problem 27.4



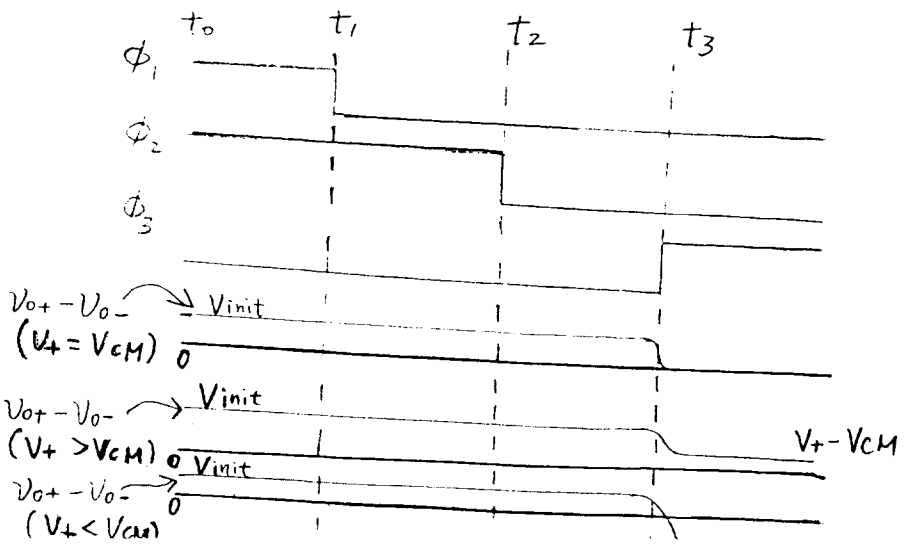
Assume $V_{init} < V_{in}$



Problem 27.5



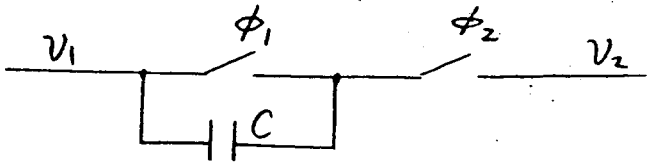
Assume $V_{init} = V_{o+} - V_{o-} > V_{CM}$



Note that the clock feedthrough and charge injection appear as a common-mode signal on input of op-amp and are ideally rejected.

Problem 27.6

(1) Series

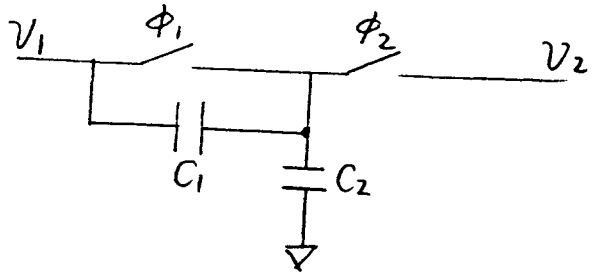


$\phi_1 = 1, \quad q_1 = 0$

$\phi_2 = 1, \quad q_2 = (v_2 - v_1)C$

$$I_{avg} = \frac{q_1 - q_2}{T} = \frac{(v_1 - v_2)C}{T} \Rightarrow R_{SC} = \frac{1}{C \cdot f_{clk}}$$

(2) Series-paralled



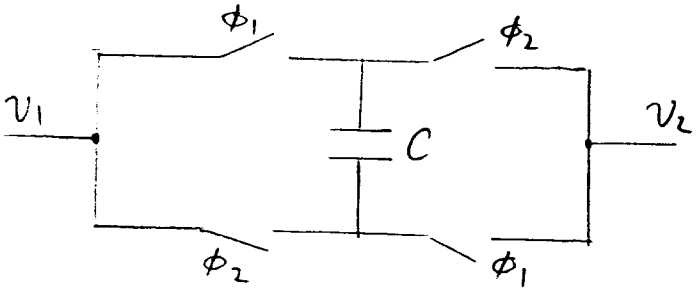
$\phi_1 = 1, \quad q_1 = v_1 C_2$

$\phi_2 = 1, \quad q_2 = C_1(v_2 - v_1) + v_2 C_2$

$q_1 - q_2 = (C_1 + C_2)(v_1 - v_2)$

$$I_{avg} = \frac{(C_1 + C_2)(v_1 - v_2)}{T} \Rightarrow R_{SC} = \frac{1}{(C_1 + C_2) f_{clk}}$$

(3) Bilinear



Problem 27.6 (cont.)

Just prior to ϕ_1 closing, C is charged to $(V_2 - V_1)$

After ϕ_1 closes, C is charged to $(V_1 - V_2)$

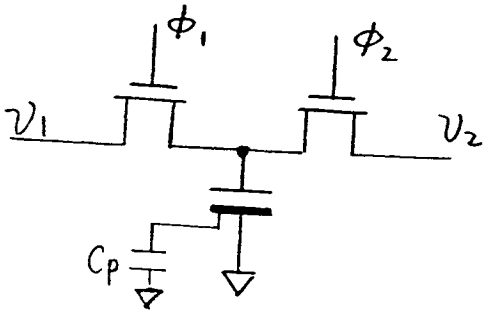
$$q_1 = C(V_1 - V_2) - C(V_2 - V_1) = 2C(V_1 - V_2)$$

Similarly,

$$q_2 = C(V_2 - V_1) - C(V_1 - V_2) = 2C(V_2 - V_1)$$

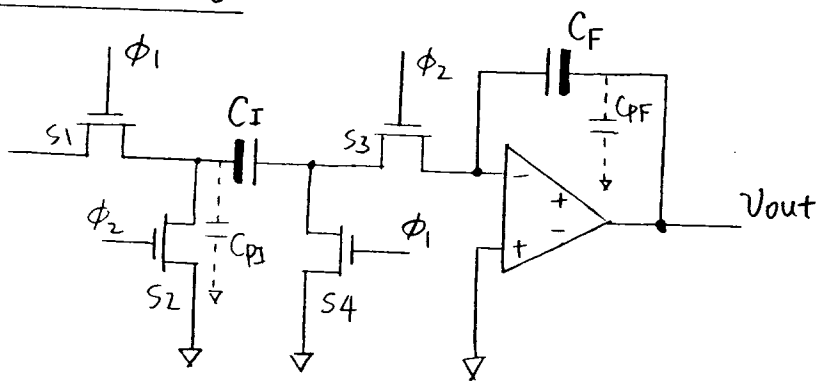
$$I_{avg} = \frac{q_1 - q_2}{T} = \frac{4C(V_1 - V_2)}{T} \Rightarrow R_{SC} = \frac{1}{4C\,C_{clk}}$$

Problem 27.7



The selection of the bottom plate of Fig 27.14(a) is shown above, where the capacitance, C_p, is the parasitic capacitance from bottom plate to the substrate. Since the bottom plate is connected to the ground, the coupled noise from the substrate to bottom plate is shorted and have no effect on the circuit.

Problem 27.8



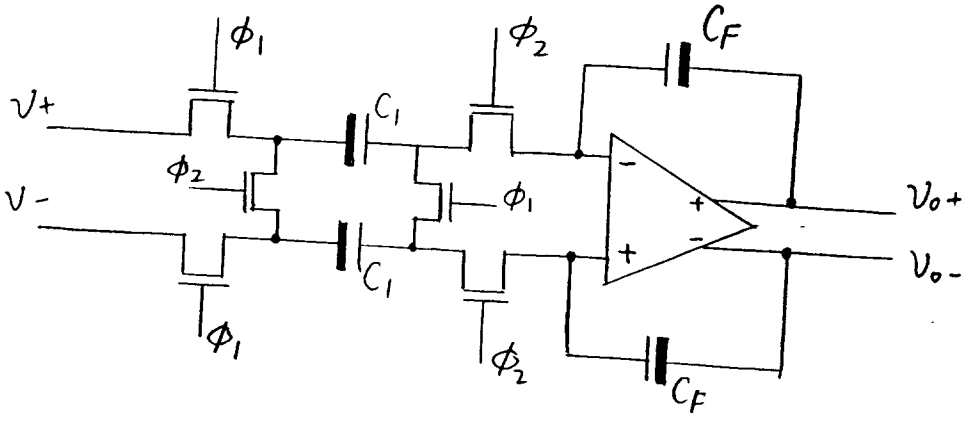
Problem 27.8 (cont.)

The selection of the bottom plate of the capacitors is shown in the figure above. C_{PI} is the parasitic capacitance from the bottom plate of C_I to substrate. It is charged to Vin when S1 is closed and discharged to ground when S2 closes, and therefore the coupled noise from the substrate to bottom plate has little effect on the input of op-amp and the intergrating operation.

For the capacitor C_F, C_{PF} is the parasitic capacitance from bottom plate of C_F to substrate. Since noise signal is set by the output of the op-amp, it has little effect on the circuit operation either.

Problem 27.9

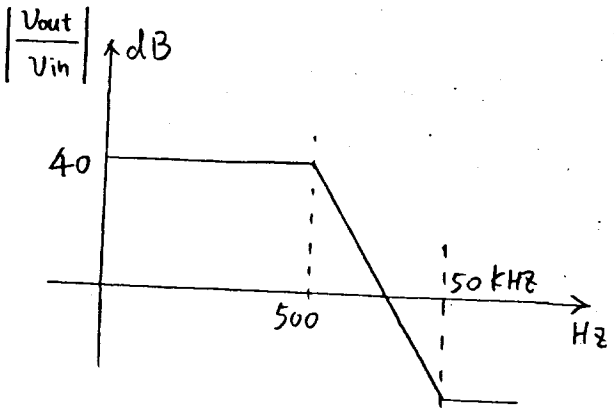
The schematic is shown below:



The transfer function is

$$\frac{V_{o+} - V_{o-}}{V_+ - V_-} = \frac{1/j\omega C_F}{R_{SC}} = \frac{1}{j\omega\left(\frac{C_F}{C_I} \cdot \frac{1}{f_{CLK}}\right)}$$

Problem 27.10



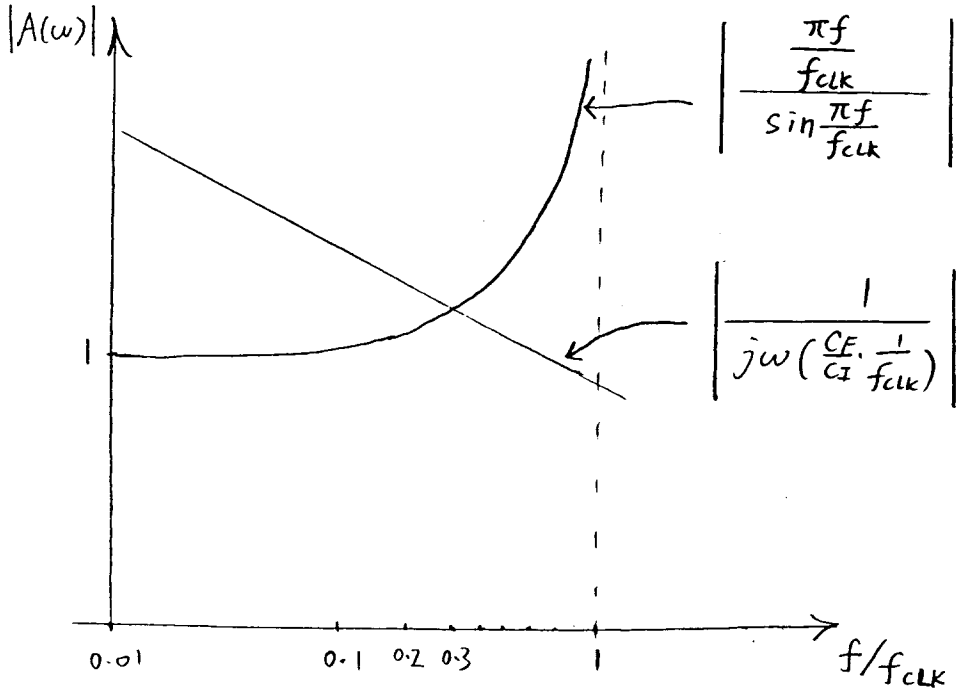
The low frequency gain is $100\ (40\ dB) = \frac{C_3}{C_4}$

$$\begin{cases} f_p = \dfrac{1}{2\pi\left(\frac{C_2}{C_4}\cdot\frac{1}{f_{clk}}\right)} = 500\,Hz \\ f_z = \dfrac{1}{2\pi\left(\frac{C_1}{C_3}\cdot\frac{1}{f_{clk}}\right)} = 50\,kHz \end{cases}$$

(Set $f_{clk} = 100\,kHz$, and $C_4 = 100fF$)

$$\Longrightarrow \quad C_3 = 10\,pF,\ C_2 \simeq 3.2\,pF \text{ and } C_1 = 0.32\,pF$$

Problem 27.11



Problem 27.12

$\because f_{CLK} = 100\,kHz, \therefore T = \frac{1}{f_{CLK}} = 10\,\mu S$

For the time of $\frac{T}{2} = 5\,\mu S$, C_1 should be charged to V_{in}.

Assume $V_{in} = VDD = 5V$, then the slew rate required for op-amp is

$SR = \frac{5V}{5\mu s} = \underline{\underline{1V/\mu S.}}$ (for 5pF load capacitance).

Problem 27.13

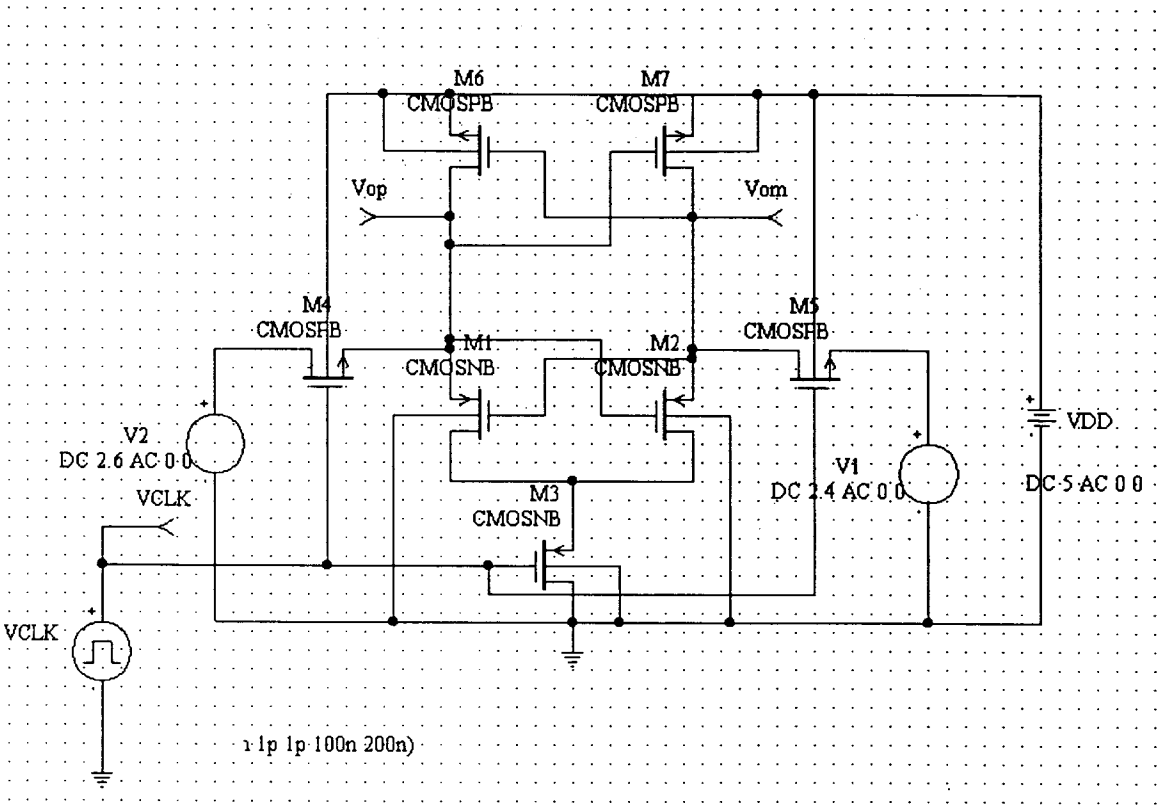
The op-amp must charge the capacitor (5pF) to its final value (less than 1%) during ϕ_1 is high ($\frac{T}{2} = 0.5\,\mu S$), therefore the circuit time constant τ is given by.

$$5\tau = 0.5\,\mu S \Rightarrow \tau = 0.1\,\mu S.$$

As $\tau = \frac{1}{2\pi f_u \cdot \beta}$, where $\beta = 0.5$, we get

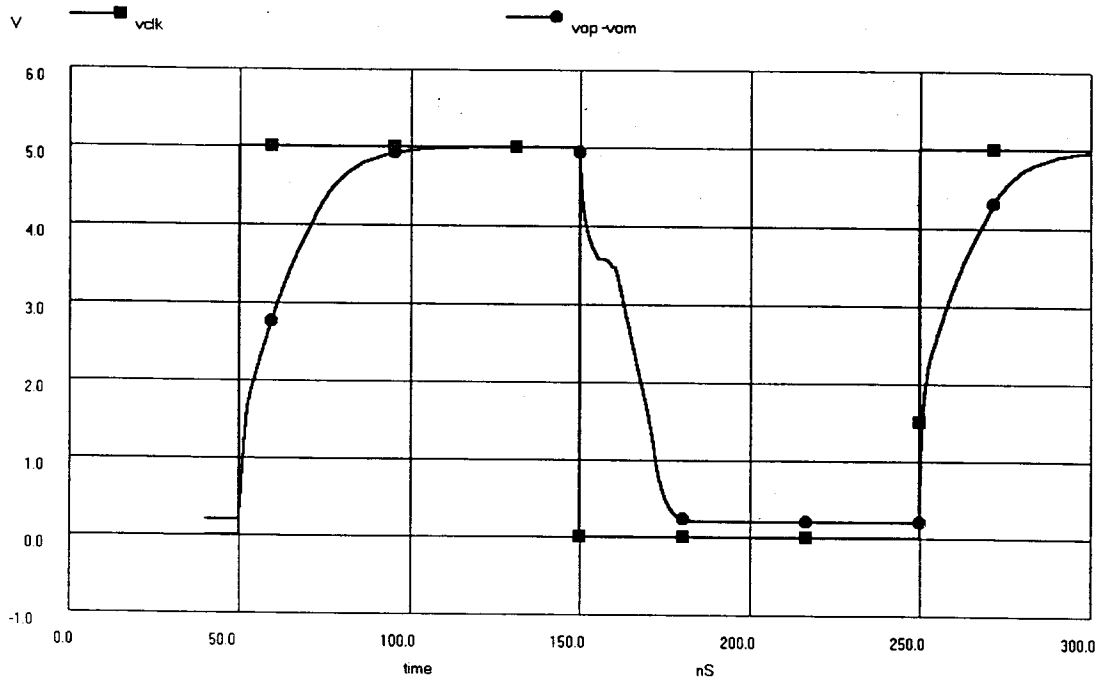
$$f_u = \frac{1}{2\pi\beta\tau} = \frac{1}{2\pi \times 0.5 \times 0.1\mu s} \simeq \underline{\underline{3.18\,MHz}}.$$

Problem 27.14

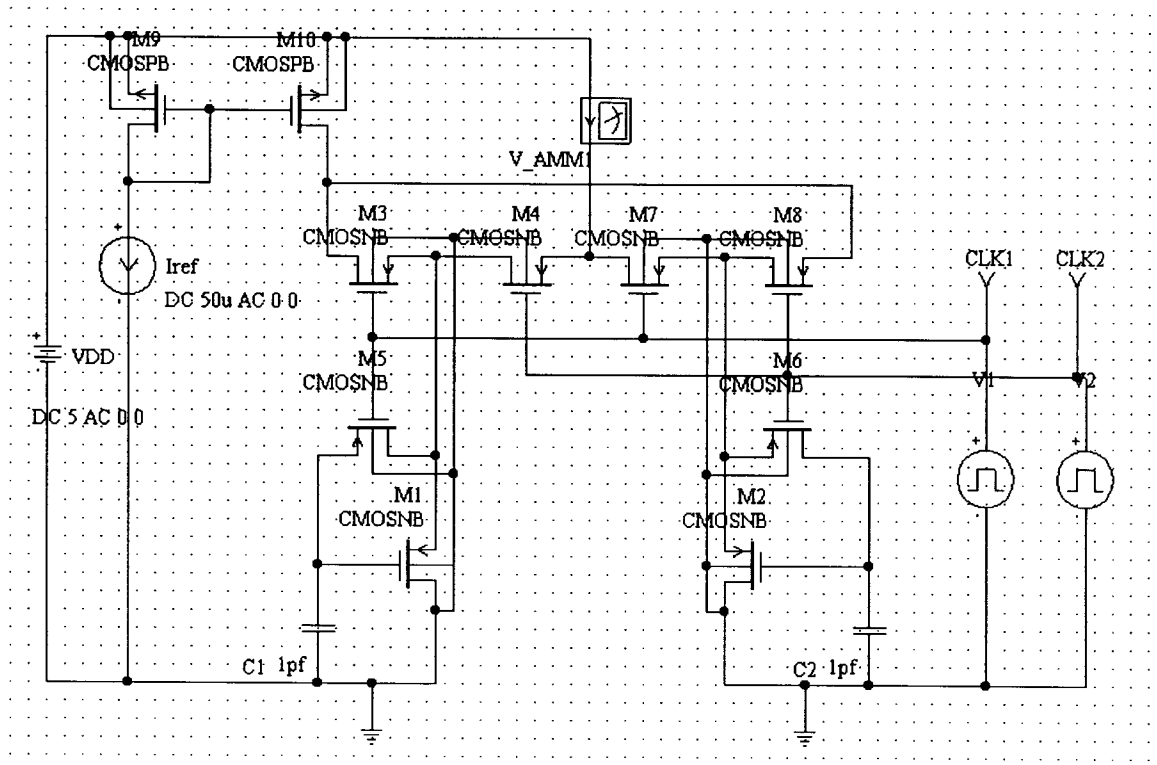



```
*** Top Level Netlist ***
M1      1 Vom Vop 0 CMOSNB  L=2u W=10u
M2      1 Vop Vom 0 CMOSNB  L=2u W=10u OFF
M3      0 VCLK 1 0 CMOSNB  L=2u W=10u OFF
M4      6 VCLK Vop 8 CMOSPB  L=2u W=3u
M5      Vom VCLK 7 8 CMOSPB  L=2u W=3u
M6      Vop Vom 8 8 CMOSPB  L=20u W=3u
M7      Vom Vop 8 8 CMOSPB  L=20u W=3u
V1      7 0     DC 2.4 AC 0 0
V2      6 0     DC 2.6 AC 0 0
VCLK    VCLK 0          DC 0 AC 0 0 PULSE(0 5 50n 1p 1p 100n 200n)
VDD     8 0     DC 5 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.OPTION ABSTOL=1m RELTOL=0.1 VNTOL=100mv
.tran 1ns 300ns 40ns 1ns uic
.end
```

The SPICE simulation result is shown below:



Problem 27.15




```
*** Top Level Netlist ***
C1        0 2 1pf
C2        0 4 1pf
Iref      10 0     DC 50u AC 0 0
M1        0 2 3 0 CMOSNB  L=5u W=15u
M10       6 10 11 11 CMOSPB  L=5u W=70u
M2        0 4 5 0 CMOSNB  L=5u W=15u
M3        6 CLK1 3 0 CMOSNB  L=5u W=15u
M4        3 CLK2 9 0 CMOSNB  L=5u W=15u
M5        3 CLK1 2 0 CMOSNB  L=5u W=15u
M6        4 CLK2 5 0 CMOSNB  L=5u W=15u
M7        9 CLK1 5 0 CMOSNB  L=5u W=15u
M8        5 CLK2 6 0 CMOSNB  L=5u W=15u
M9        10 10 11 11 CMOSPB  L=5u W=70u
V_AMM1          11 9 0V
V1        CLK1 0DC 0 AC 0 0 PULSE(5 0 10n 1ns 1ns 30ns 60ns)
V2        CLK2 0DC 0 AC 0 0 PULSE(0 5 10n 1ns 1ns 30ns 60ns)
VDD       11 0     DC 5 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
```

.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=1mv
.tran 1ns 300ns 100ns 1ns
.end

The SPICE simulation result is shown below: