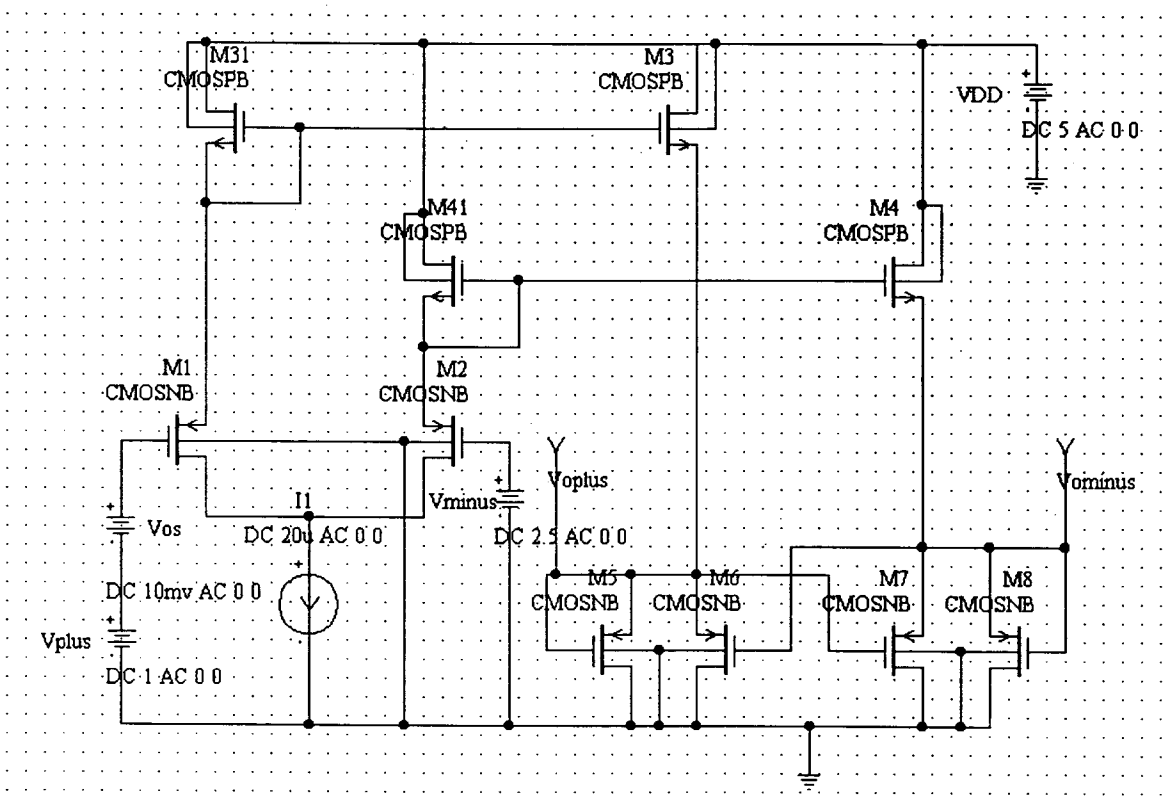
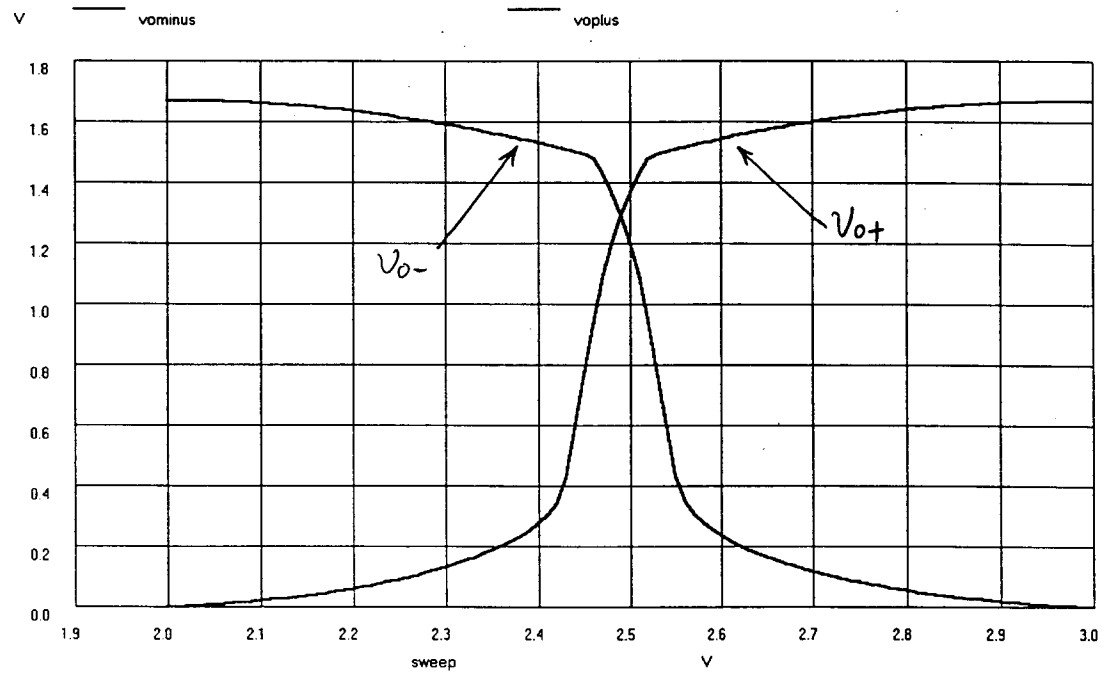
Problem 26.1




```
*** Top Level Netlist ***
I1        1 0       DC 20u AC 0 0
M1        1 10 3 0 CMOSNB  L=2u W=10u
M2        1 5 6 0 CMOSNB  L=2u W=10u
M3        7 3 Voplus 7 CMOSPB  L=2u W=3u
M31       7 3 3 7 CMOSPB  L=2u W=3u
M4        7 6 Vominus 7 CMOSPB  L=2u W=3u
M41       7 6 6 7 CMOSPB  L=2u W=3u
M5        0 Voplus Voplus 0 CMOSNB  L=2u W=3u
M6        0 Vominus Voplus 0 CMOSNB  L=2u W=3u
M7        0 Voplus Vominus 0 CMOSNB  L=2u W=3u
M8        0 Vominus Vominus 0 CMOSNB  L=2u W=3u
VDD       7 0       DC 5 AC 0 0
Vminus    5 0       DC 2.5 AC 0 0
Vos       10 2      DC 10mv AC 0 0
Vplus     2 0       DC 1 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.DC Vplus 2 3 .01
```

.end

The SPICE simulation result is shown below:



Problem 26.2

The input capacitance of the comparator of Fig 26.11 is approximately the C_{gs} of the input MOSFETs, that is,

$$C_{in} \simeq C_{gs(in)} = \frac{2}{3} C_{ox}' \times W \times L$$

(Assuming input MOSFETs are in saturation region and neglecting C_{gd}).

The hysteresis of the decision circuit causes the gain of the comparator to increase.

Problem 26.3

We use the circuit of Fig 26.5.

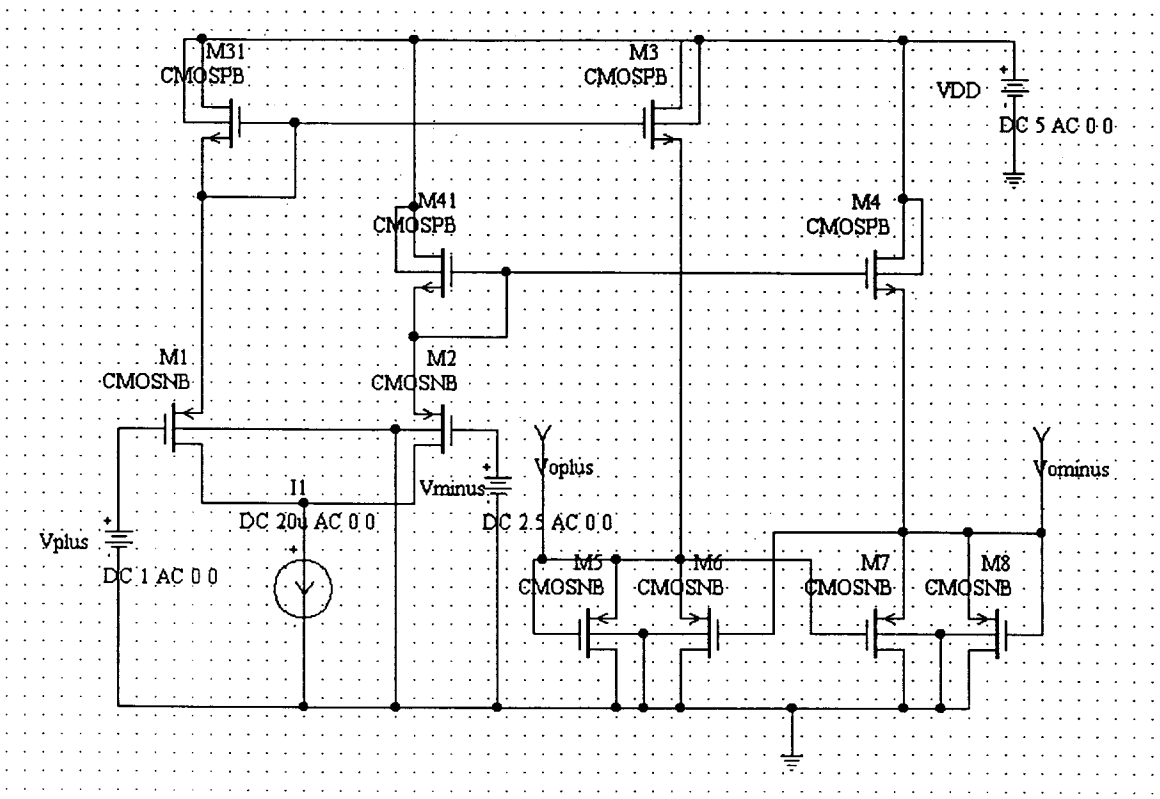
$$V_{sp_H} = 100mV = \frac{I_{SS}}{g_m} \cdot \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} = \frac{20\,\mu A}{71\,\mu A/V} \times \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1}$$

$$\Longrightarrow \frac{\beta_B}{\beta_A} = 2.1$$

Set the length of all devices $2\,\mu m$, $W_5 = W_8 = 3\,\mu m$ resulting in $W_6 = W_7 = \underline{6\,\mu m}$

The SPICE simulation results are shown on next page.

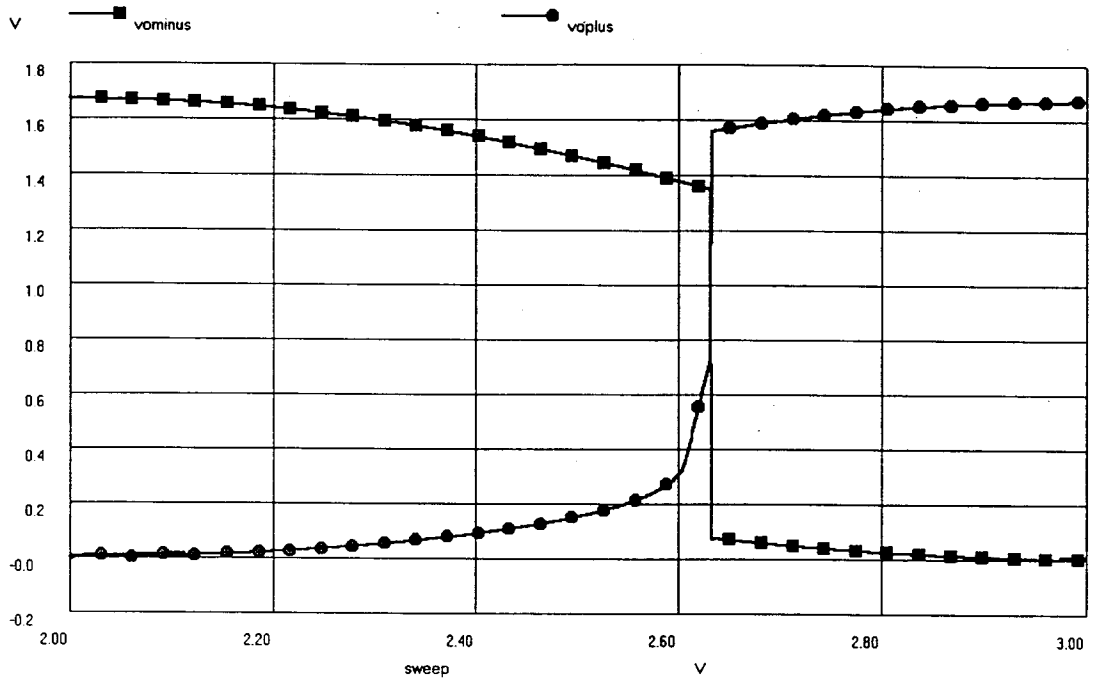
Problem 26.3

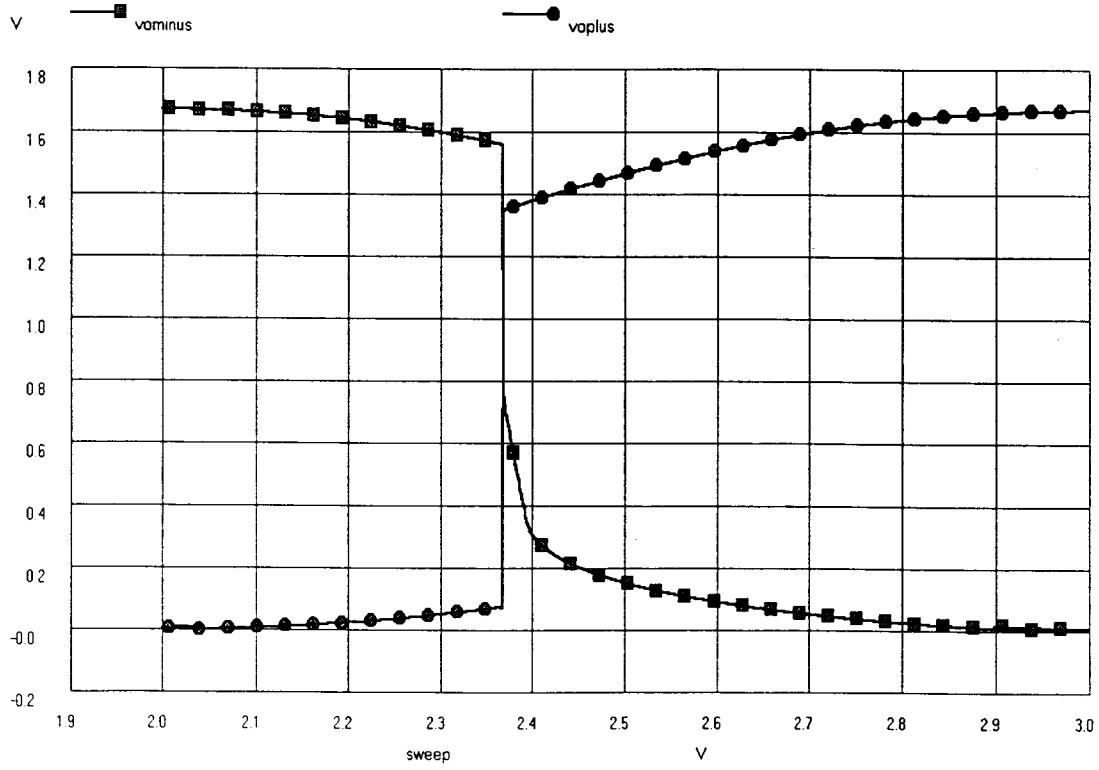



```
*** Top Level Netlist ***
I1        1 0       DC 20u AC 0 0
M1        1 2 3 0 CMOSNB  L=2u W=10u
M2        1 5 6 0 CMOSNB  L=2u W=10u
M3        7 3 Voplus 7 CMOSPB  L=2u W=3u
M31       7 3 3 7 CMOSPB  L=2u W=3u
M4        7 6 Vominus 7 CMOSPB  L=2u W=3u
M41       7 6 6 7 CMOSPB  L=2u W=3u
M5        0 Voplus Voplus 0 CMOSNB  L=2u W=3u
M6        0 Vominus Voplus 0 CMOSNB  L=2u W=6u
M7        0 Voplus Vominus 0 CMOSNB  L=2u W=6u
M8        0 Vominus Vominus 0 CMOSNB  L=2u W=3u
VDD       7 0       DC 5 AC 0 0
Vminus    5 0       DC 2.5 AC 0 0
Vplus     2 0       DC 1 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4


.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=10mv
```

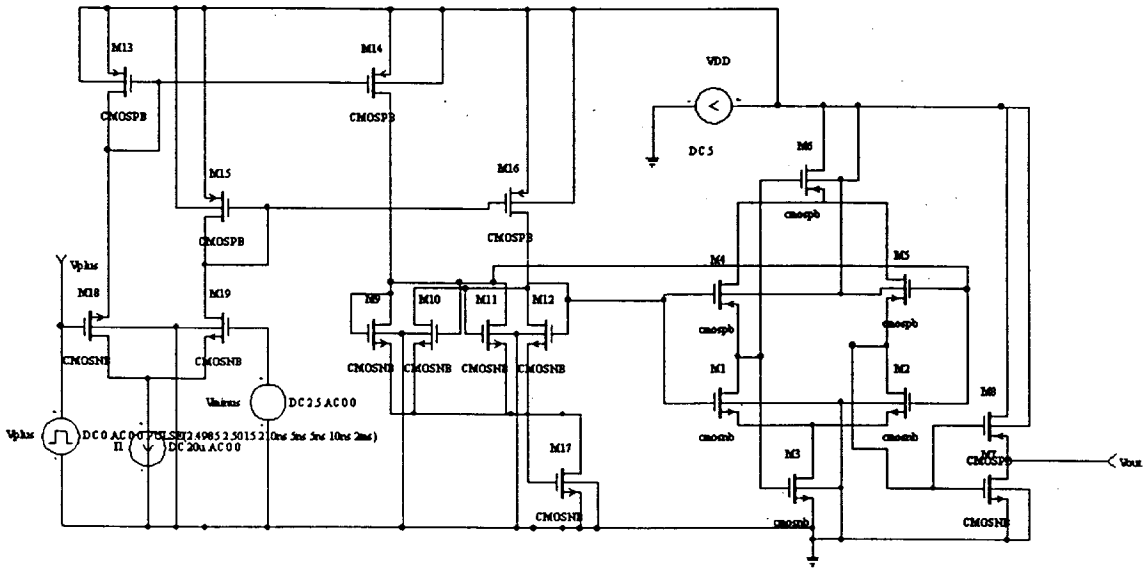
.DC Vplus 3 2 -.001
.end

The SPICE simulation result is shown below:





Problem 26.4

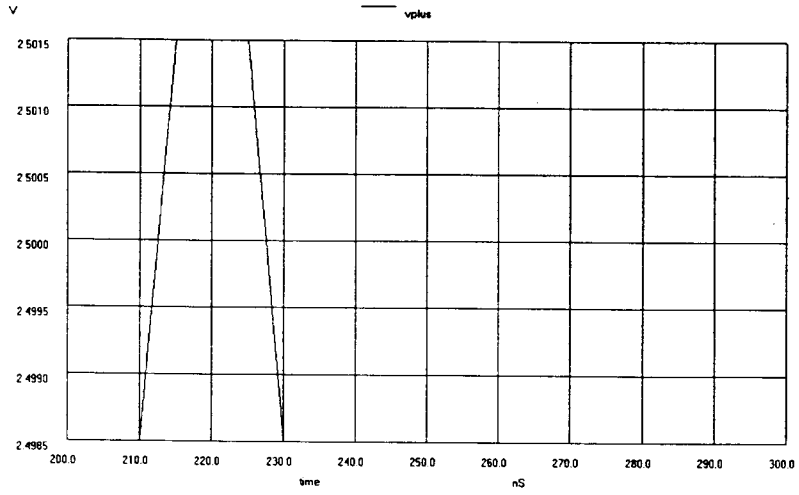


*** Top Level Netlist ***

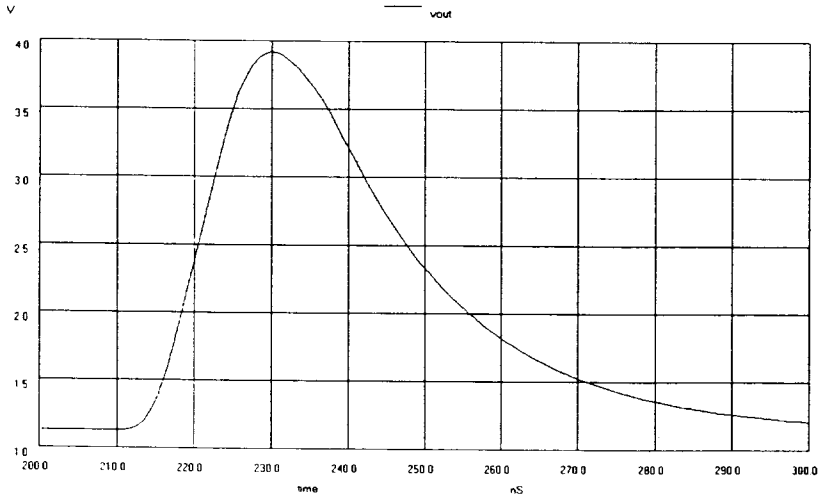
```
I1      13 0     DC 20u AC 0 0
M1      1 2 3 0 cmosnb  L=2u W=3u
M10     2 10 9 0 CMOSNB  L=2u W=3u
M11     10 2 9 0 CMOSNB  L=2u W=3u
M12     2 2 9 0 CMOSNB  L=2u W=3u
M13     11 11 6 6 CMOSPB  L=2u W=3u
M14     10 11 6 6 CMOSPB  L=2u W=3u
M15     12 12 6 6 CMOSPB  L=2u W=3u
M16     2 12 6 6 CMOSPB  L=2u W=3u
M17     9 9 0 0 CMOSNB  L=2u W=300u
M18     13 Vplus 11 0 CMOSNB  L=2u W=10u
M19     12 15 13 0 CMOSNB  L=2u W=10u
M2      7 10 3 0 cmosnb  L=2u W=3u
M3      3 1 0 0 cmosnb  L=2u W=3u
M4      5 2 1 6 cmospb  L=2u W=3u
M5      5 10 7 6 cmospb  L=2u W=3u
M6      6 1 5 6 cmospb  L=2u W=3u
M7      Vout 7 0 0 CMOSNB  L=2u W=3u
M8      6 7 Vout 6 CMOSPB  L=2u W=3u
M9      10 10 9 0 CMOSNB  L=2u W=3u
VDD     6 0      DC 5
Vminus  15 0     DC 2.5 AC 0 0
Vplus   Vplus 0 DC 0 AC 0 0 PULSE(2.4985 2.5015 210ns 5ns 5ns 10ns 2ms)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
```

```
.OPTION ABSTOL=1u CHGTOL=1.0E-13 ITL4=100 RELTOL=0.01 VNTOL=1mv
.probe
.tran 1n 300n 200n 1n uic
.plot tran all
.print tran all
.end
```

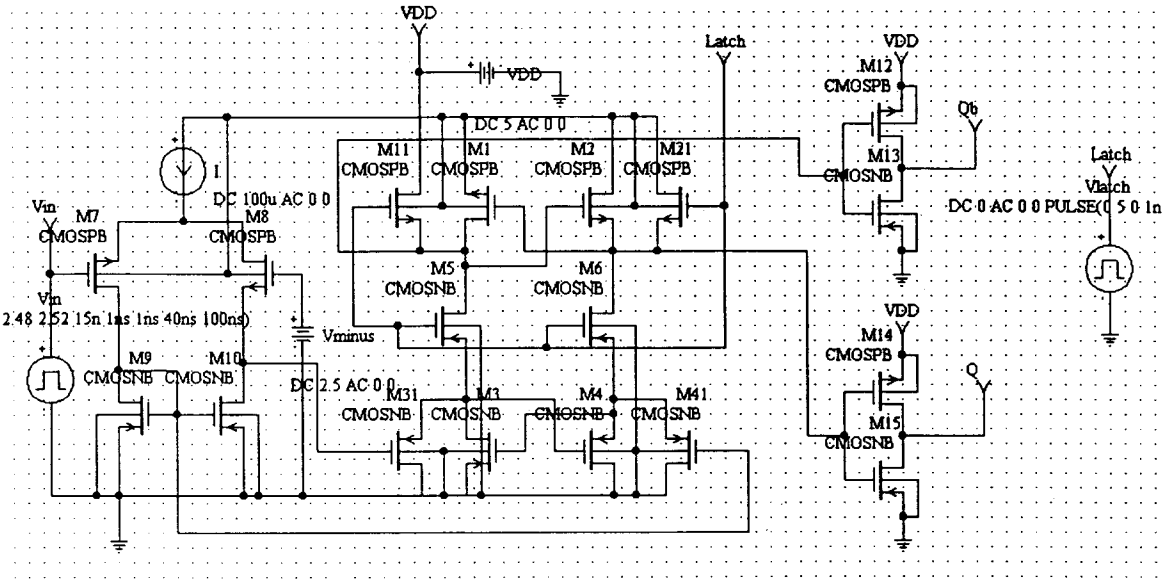
The SPICE simulation result is shown below:



The minimum sensitivity is 3 mV



Problem 26.5



*** Top Level Netlist ***

```
I        VDD 11          DC 100u AC 0 0
M1       1 2 VDD VDD CMOSPB
M10      8 9 0 0 CMOSNB  L=2u W=3u
M11      VDD Latch 1 VDD CMOSPB  L=2u W=3u
M12      Qb 1 VDD VDD CMOSPB  L=2u W=30u
M13      Qb 1 0 0 CMOSNB  L=2u W=10u
M14      Q 2 VDD VDD CMOSPB  L=2u W=30u
M15      Q 2 0 0 CMOSNB  L=2u W=10u
M2       VDD 1 2 VDD CMOSPB
M21      VDD Latch 2 VDD CMOSPB  L=2u W=3u
M3       4 5 0 0 CMOSNB
M31      0 8 4 0 CMOSNB  L=2u W=3u
M4       0 4 5 0 CMOSNB
M41      0 9 5 0 CMOSNB  L=2u W=3u
M5       1 Latch 4 0 CMOSNB  L=2u W=3u
M6       2 Latch 5 0 CMOSNB  L=2u W=3u
M7       9 Vin 11 VDD CMOSPB  L=2u W=10u
M8       11 12 8 VDD CMOSPB  L=2u W=10u
M9       9 9 0 0 CMOSNB  L=2u W=3u
VDD      VDD 0  DC 5 AC 0 0
Vin      Vin 0    DC 0 AC 0 0 PULSE(2.48 2.52 15n 1ns 1ns 40ns 100ns)
Vlatch   Latch 0 DC 0 AC 0 0 PULSE(0 5 0 1n 1n 20ns 40ns)
Vminus   12 0     DC 2.5 AC 0 0
```

***** Spice models and macro models *****

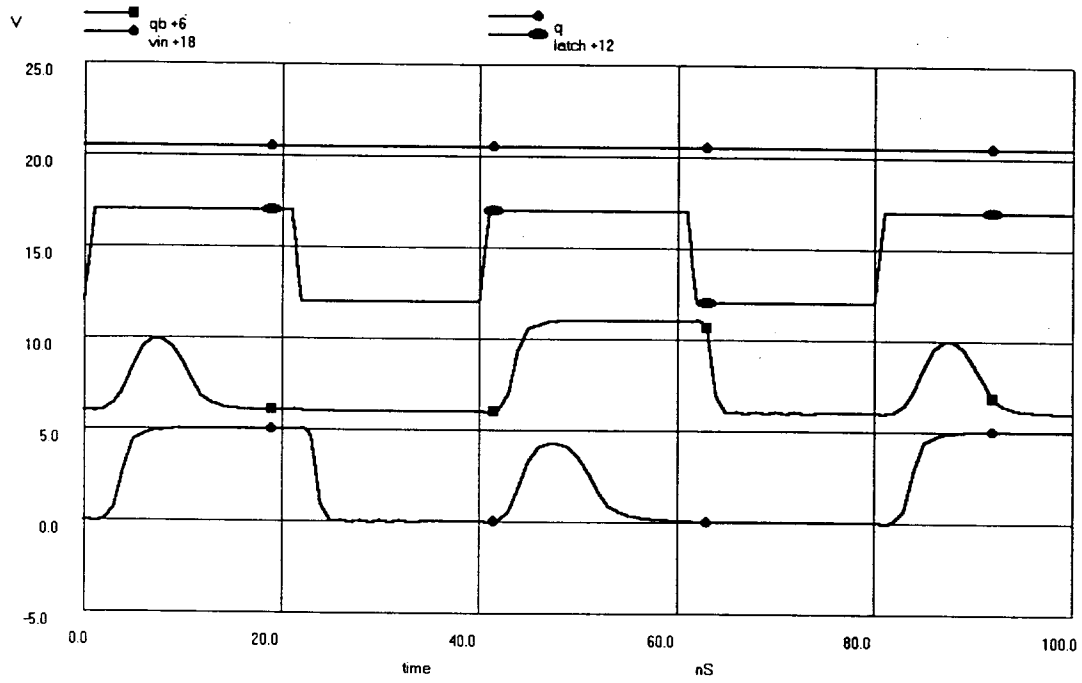
.MODEL CMOSPB PMOS LEVEL=4

.MODEL CMOSNB NMOS LEVEL=4

***** End of spice models and macro models *****

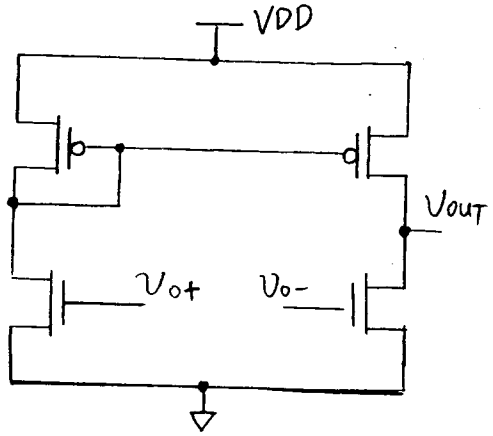
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=50mv
.tran 1n 200n 0 1n
.end

The following is the SPICE simulation result:



Note: The 4 MOSFETs connected to Latch don't turn on and off at the same rate causing a glitch in the output. Sizing can minimize the glitch.

Problem 26.6

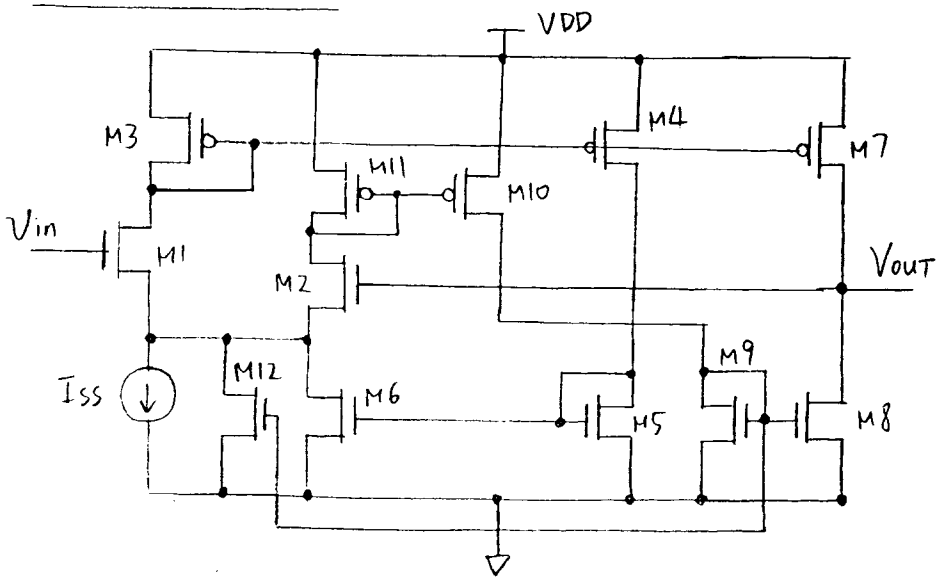


The advantage of this output buffer is the small layout size. The main problem of using this buffer is the low speed (caused by the small gain of the circuit). Also, this buffer does not exhibit the common mode rejection to its differatial inputs.

Problem 26.7

Since the self-biased comparator (see Fig 26.19) has a wide input common-mode runge, it can be used as a wide-swing op-amp. As there is only one high impedance node (out put node) in this configuration, compensating the circuit is just like that of an OTA, that is, selecting a mininum load capacitance for desired fu and phase margin, and the circuit is always stable.

Problem 26.8

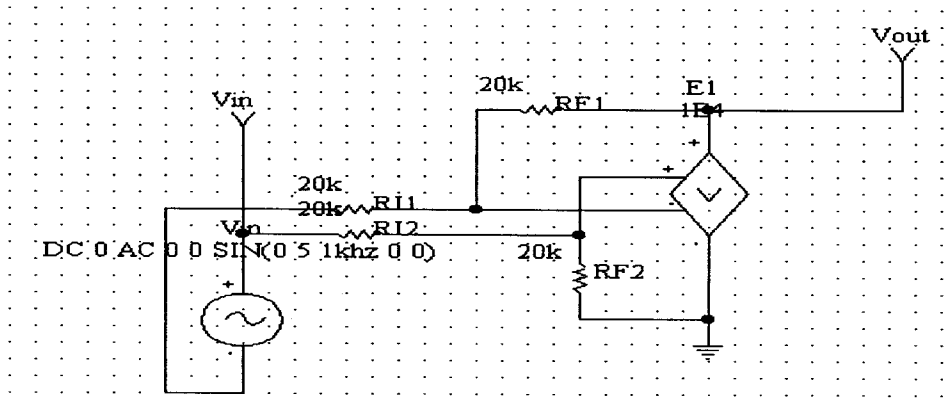


The DC biasing for this circuit is difficult to implement becau of the positive feedback. One might consider the OTA of Fig 26.24 for stable biasing.

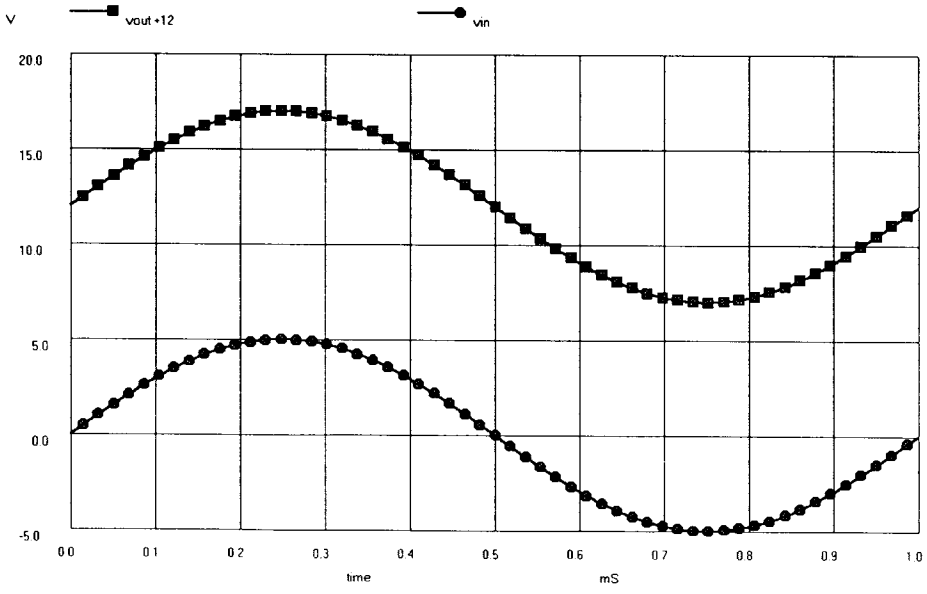
Problem 26.9

The benifits of using long channel length in the multiplying quad of Fig 26.30 is the reduced module length modulation effect, and ensuring devices operate follows Equation A.5. The long channel devices do not affect speed since they are part of the feedback of the op-amp. The problem of using long length devices, however, is that smaller W/L ratio of MOSFETs makes it more difficult to keep the quad in the triode region.

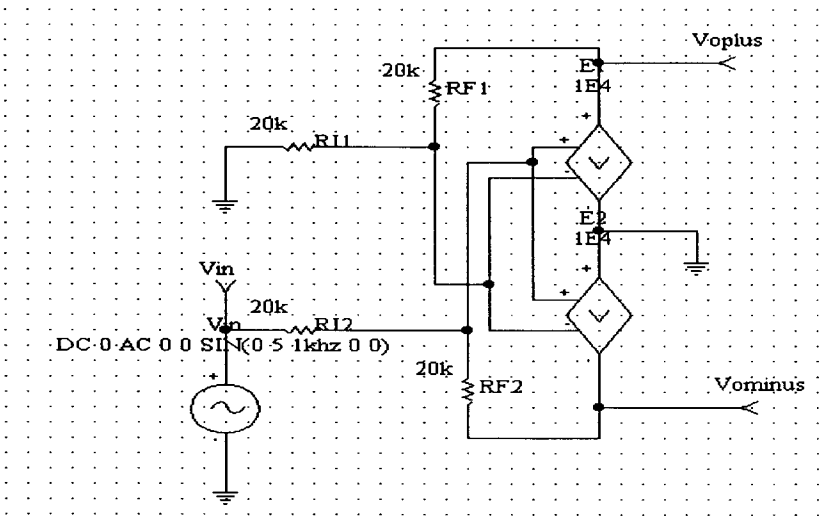
Problem 26.10




```
*** Top Level Netlist ***
E1        Vout 0 4 3        1E4
RF1       Vout 3 20k
RF2       0 4 20k
RI1       5 3 20k
RI2       4 Vin 20k
Vin       Vin 5    DC 0 AC 0 0 SIN(0 5 1khz 0 0)

***** Spice models and macro models *****


***** End of spice models and macro models *****

.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=1mv
.op
.tran 500n 1ms 0 500n
.end
```



Problem 26.10 (cont.)



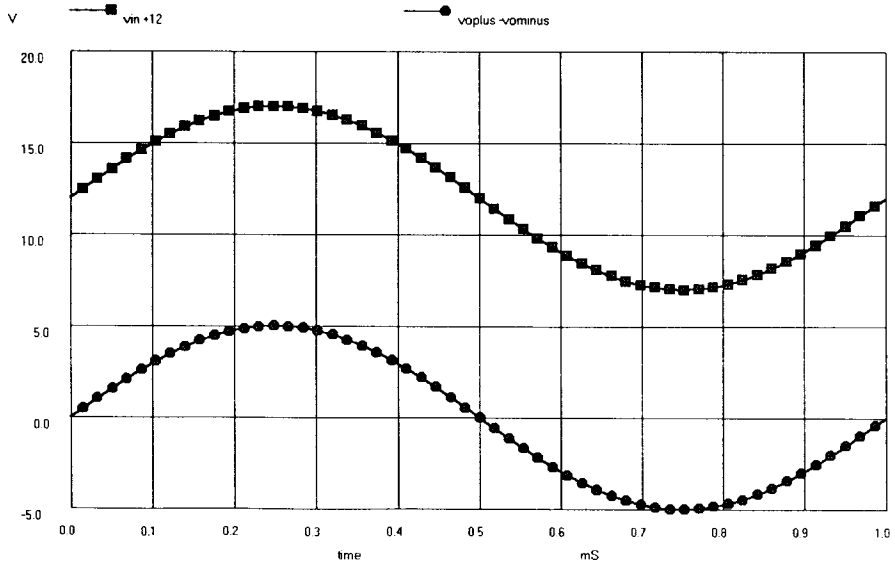
*** Top Level Netlist ***

E1	Voplus 0 4 5	1E4
E2	0 Vominus 4 5	1E4
RF1	Voplus 5 20k	
RF2	4 Vominus 20k	
RI1	0 5 20k	
RI2	4 Vin 20k	
Vin	Vin 0 DC 0 AC 0 0 SIN(0 5 1khz 0 0)	

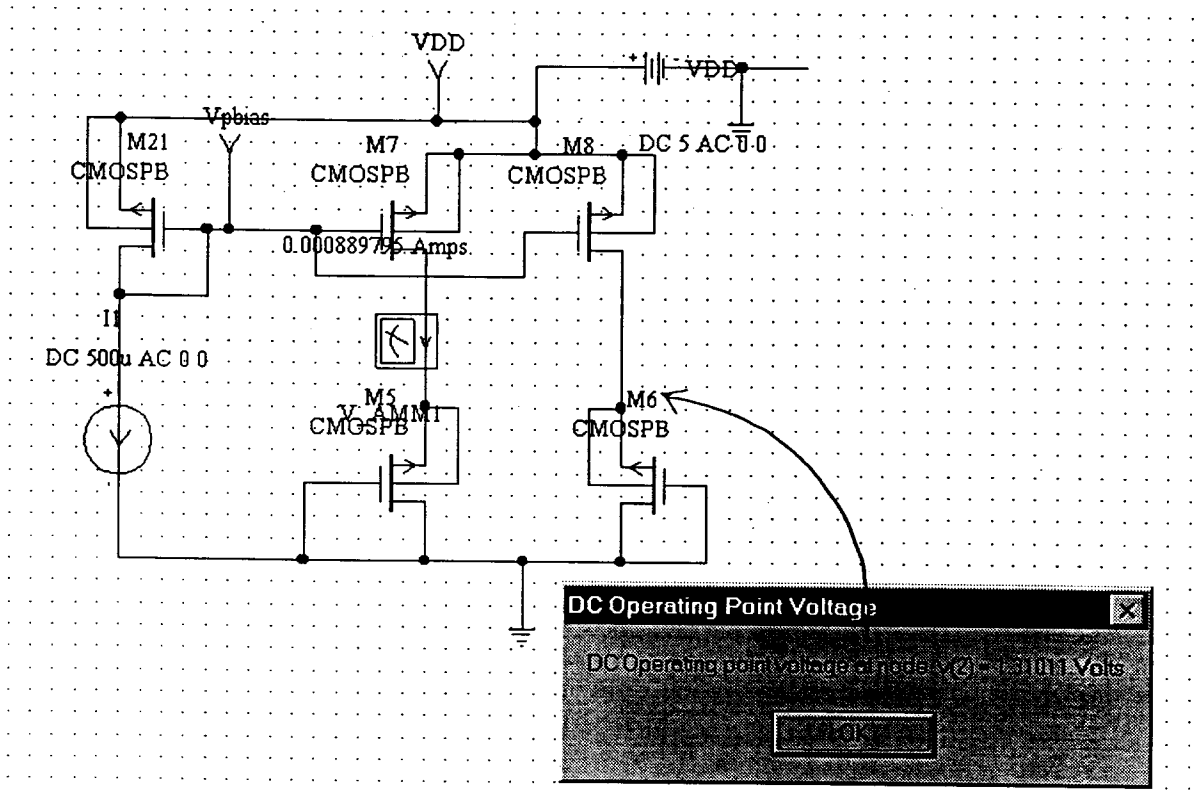
***** Spice models and macro models *****

***** End of spice models and macro models *****

.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=1mv
.op
.tran 500n 1ms 0 500n
.end



Problem 26.11




```
*** Top Level Netlist ***
I1          Vpbias 0          DC 500u AC 0 0
M21         Vpbias Vpbias VDD VDD CMOSPB  L=2u W=1000u
M5          0 0 3 3 CMOSPB  L=2u W=1000u
M6          0 0 2 2 CMOSPB  L=2u W=1000u
M7          1 Vpbias VDD VDD CMOSPB  L=2u W=1000u
M8          2 Vpbias VDD VDD CMOSPB  L=2u W=1000u
V_AMM1          1 3 0V
VDD         VDD 0  DC 5 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=1mv
.op
.end
```