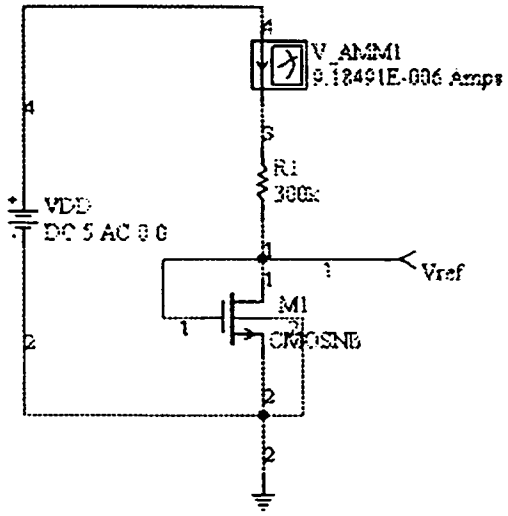
Problem 21.1

ANS: The schematic is shown in the following figure. To achieve Vref = 2V.
==> R = (VDD-Vref)/ID = (5-2)V/10uA = 300 kΩ.
and for 10uA through the transistor with VGS = 2V. ID = (KPn/2) (W/L) $(VGS-Vthn)^2$. Pluging ID=10uA, KPn= 50uA/V^2, VGS = 2V, and Vthn =0.83V. ==> W/L =0.29221. Chosing L=10um, ==> W=3um.

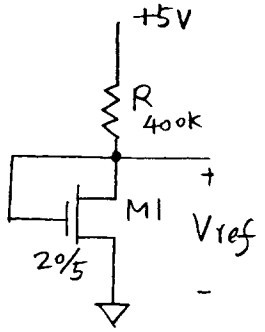
In Summation, R=300kΩ, W=3um, L=10um.



SPICE gives Vref = 2.2V and ID = 9.2uA, for details see the following simulation results.

```
Operating point information:

      Node   Voltage
      ----   -------
      vref   2.244527e+000
      V(3)   5.000000e+000
      V(4)   5.000000e+000
      m1#drain     2.244271e+000
      m1#source    2.562588e-004

      Source       Current
      ------       -------

      vdd#branch   -9.18491e-006
      v_amm1#branch      9.184909e-006
```

Problem 21.2



$$\frac{5 - V_{ref}}{400k} = \frac{50\mu A/V^2}{2} \times \frac{20}{5} \times (V_{ref} - V_{THN})^2$$

$$\Rightarrow V_{ref} \simeq \underline{1.14\ V}$$

$$TC(V_{ref}) = \frac{1}{V_{ref}} \times \left[V_{THN} \cdot TCV_{TH} - \frac{1}{2}\sqrt{\frac{2L}{W_1} \times \frac{VDD}{R \times KP(T)}} \cdot \left[\frac{1}{R}\frac{\partial R}{\partial T} - \frac{1.5}{T} \right] \right]$$

$TCV_{TH} \simeq -3{,}000\ ppm/^\circ C$ and $TCR = \frac{1}{R}\frac{\partial R}{\partial T} \simeq 10{,}000\ ppm/^\circ C$

$$\Rightarrow TC(V_{ref}) \simeq \underline{-3740\ ppm/^\circ C}$$

SPICE simulation result is shown on next page.

Problem 21.2 (Simulation)

*** (TurboSim V 1.87) Netlist for C:\TS\SOLUTION\21_2.CKT

*** Top Level Netlist ***
M1 Vref Vref 0 0 CMOSNB L=5u W=20u
R1 Vref 3 400k TC1=0.01
VDD 3 0 DC 5 AC 0 0

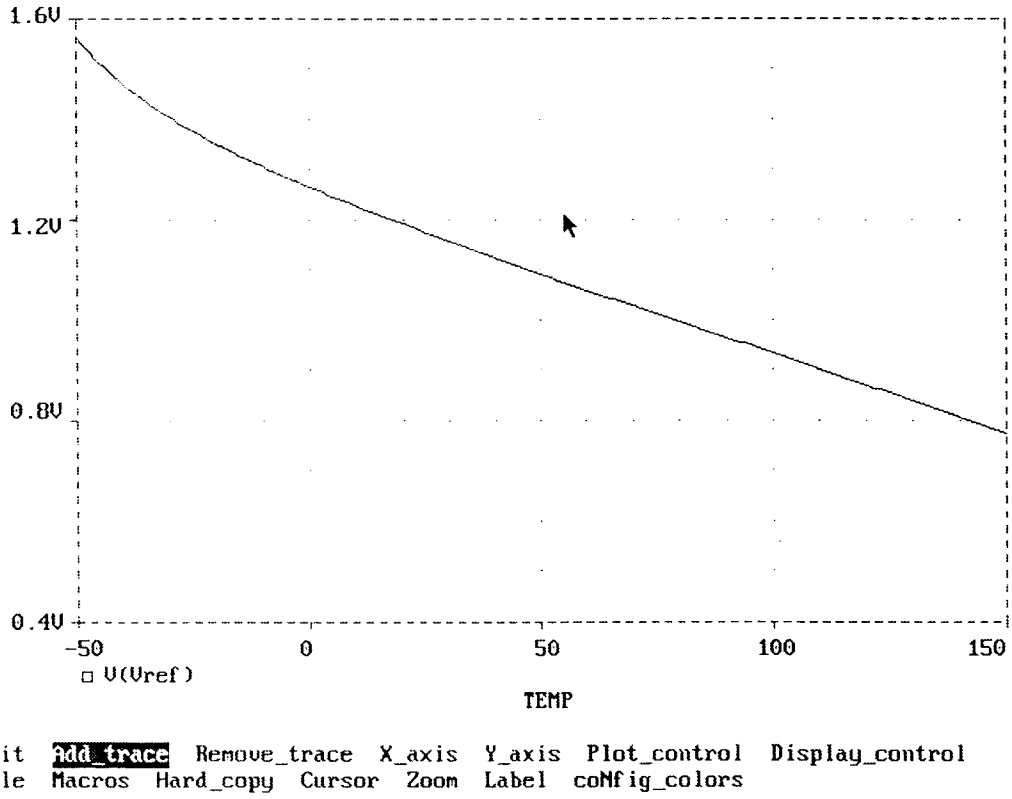
***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

***** End of spice models and macro models *****

.DC temp -50 150 1
.probe
.end

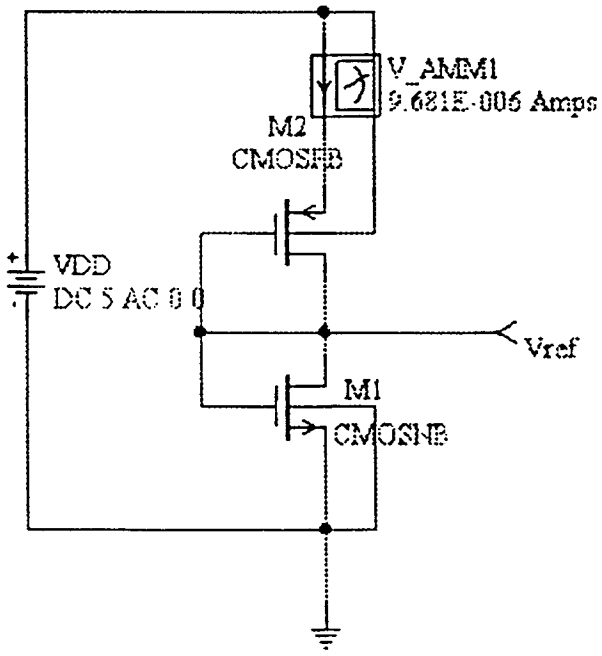
The SPICE simulation is shown below:



Problem 21.3

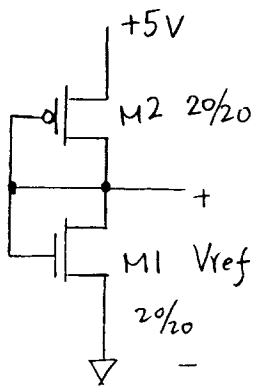
ANS: Same as problem 21.1, for M1, it will come out the design results W1 = 3um and L1=10um. For M2, solving the equation 10 uA = (17uA/V^2/2)*(W2/L2)*(3-0.916)^2, ==> W2/L2 = 0.27. Chosing W2=3um, ==>L2=11um.

For the sizes, SPICE simulation gives Iref = 2.05 V but the ID = 6.67uA. There is some deviation between hand calculation and SPICE simulation. Remember the two MOSFETs behave like two resistors. If we want to keep Vref as about 2V and increase ID to about 10uA, we need to decrease the two resistors in same ratio. The MOSFET resistor is propotional to L/W, so either increasing W or decreasing L will achieve the goal. The trial and error yields that ID = 9.68uA and Vref = 2.04V by keepping W1 = W2 = 3um but reducing L1 to 7um and L2 to 8um. See the following date list for the detail.




```
Operating point information:

      Node   Voltage
      ----   -------
      vref   2.036651e+000
      V(4)   5.000000e+000
      V(3)   5.000000e+000
      m2#drain     2.037180e+000
      m2#source    4.999470e+000
      m1#drain     2.036381e+000
      m1#source    2.700999e-004

      Source       Current
      ------       -------

      vdd#branch   -9.68101e-006
      v_amm1#branch      9.681000e-006
```

Problem 21.4 and 21.5



$$V_{ref} = \frac{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}}(VSS + V_{THN})}{\sqrt{\frac{\beta_1}{\beta_2}} + 1}$$

$$= \frac{5 - 0.91 + \sqrt{\frac{50}{17}}(0 + 0.83)}{\sqrt{\frac{50}{17}} + 1}$$

$$\simeq 2.03\ V.$$

$$TC(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{1}{\sqrt{\frac{\beta_1}{\beta_2}} + 1}\left[\frac{\partial(-V_{THP})}{\partial T} + \sqrt{\frac{\beta_1}{\beta_2}}\frac{\partial V_{THN}}{\partial T}\right]$$

$$= \frac{1}{2.03} \cdot \frac{1}{\sqrt{\frac{50}{17}} + 1} \cdot \left[2.7\times10^{-3}\ V/^{\circ}C + \sqrt{\frac{50}{17}} \cdot (-2.4\times10^{-3})\ V/^{\circ}C\right]$$

$$\simeq \underline{-256.9\ ppm/^{\circ}C}$$

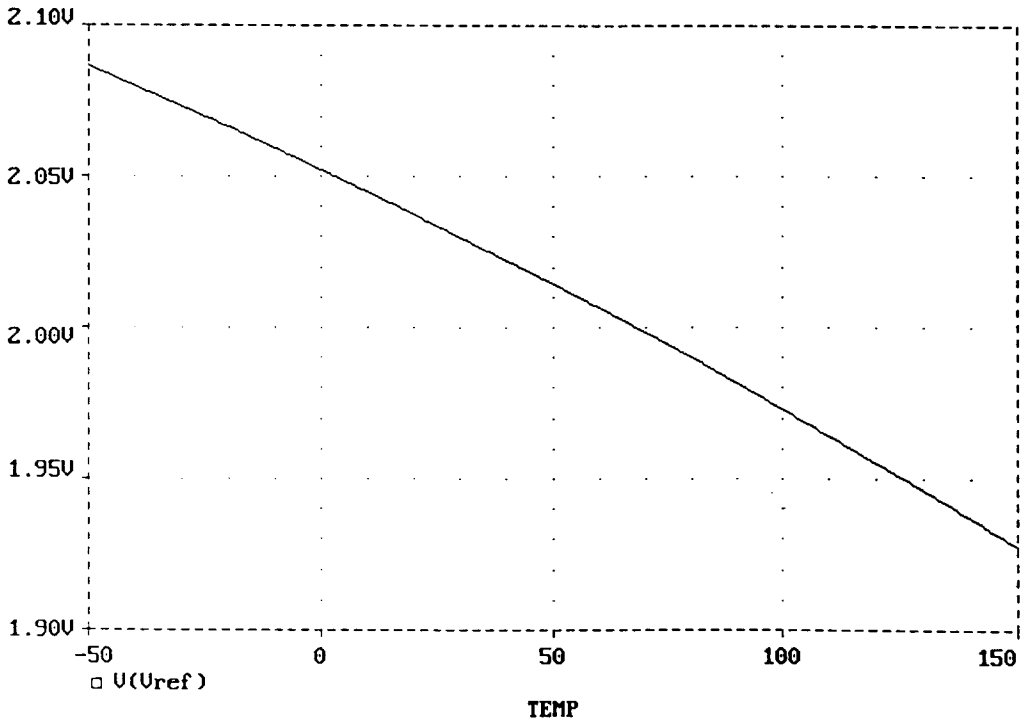
$$S_{V_{DD}}^{V_{ref}} = \frac{VDD}{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}}(VSS + V_{THN})}$$

$$= \frac{5}{5 - 0.91 + \sqrt{\frac{50}{17}}(0 + 0.83)} \simeq \underline{0.907}$$

Problem 21.4 (simulation)

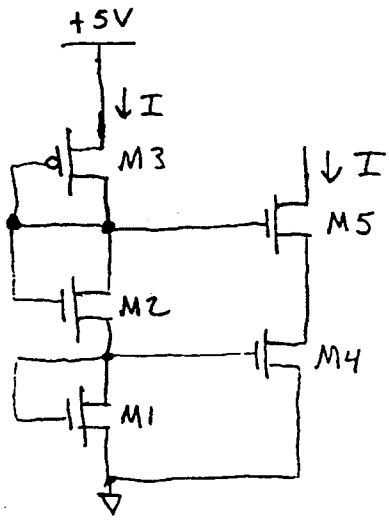
```
*** Top Level Netlist ***
M1      Vref Vref 0 0 CMOSNB  L=20u W=20u
M2      Vref Vref 3 3 CMOSPB  L=20u W=20u
VDD     3 0      DC 5 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.DC temp -50 150 1
.probe
.end
```

The SPICE simulation is shown below:



21.6.

Select the size of M3 in Fig. 21.6 so that 10 μA flows in all MOSFETS in the circuit. Assume that M5 and M4 are operating in the saturation region.



All n-channels are 15/5

Since all n-channel devices are the same size V_{GS} for the n-channel devices will be the same.

$$10\,\mu A = \frac{50\,\mu A/V^2}{2}\frac{15}{5}(V_{GS} - .83)^2$$

$$V_{GS}^2 - 1.66\,V_{GS} + 0.5556 = 0$$

$$V_{GS} = 1.195\ V$$

$$\therefore V_{SG3} = 5 - 2(1.195) = 2.61\ V$$

Now determine the size of M3

$$10\,\mu A = \frac{17\,\mu A/V^2}{2}\frac{W}{L}(2.61 - .91)^2$$

$$\frac{W}{L} = .407$$

$$W = 4\,\mu m$$

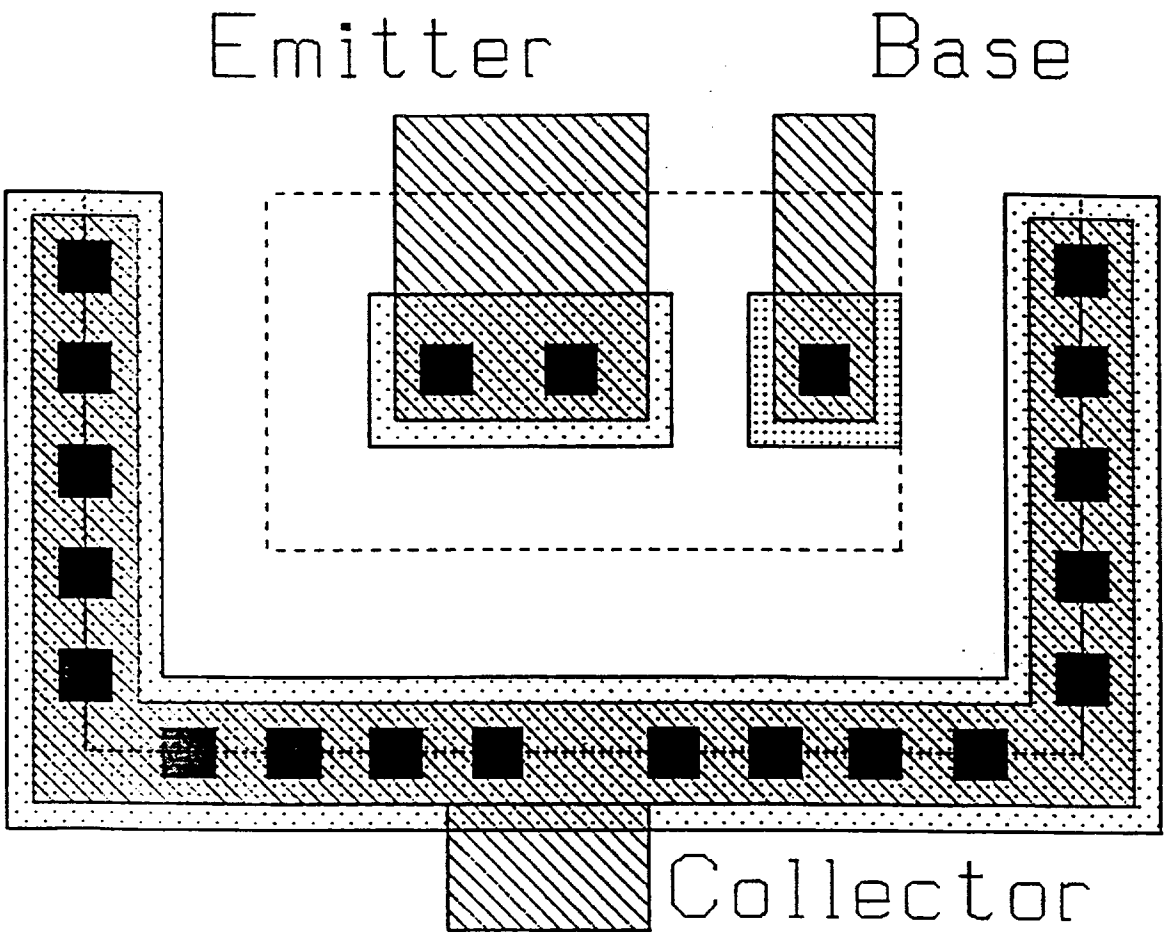
$$L = 10\,\mu m$$

Problem 21.7

ANS: The figure is shown in Figure P21.7 @page 462. For M1:
ID1=(KPn/2)*(W1/L1)*(VGS1-Vthn)^2 . Notice VGS1=ID2*830K = ID1*830k. i.e.
ID1=(50uA/V^2/2)*(100u/2u)*(ID1*830k-0.83)^2 , solving the equation ==> ID1≅1uA. Therefore,
==> I = 2xID1=2uA.

Problem 21.9

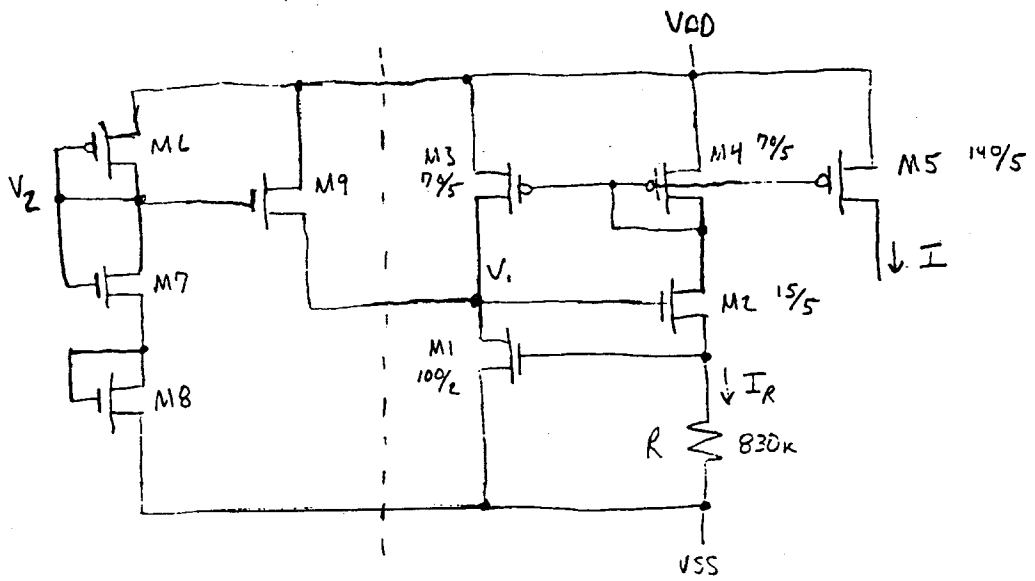
Layout of the PNP



The more realistic value for the scale current of the diode model is 10^{-15} A if the area specified for the diode is 1.

21.8

Sketch a startup circuit for the threshold-voltage referenced current source of Fig. P21.7. Assume the maximum current in the startup circuit is 1 μA.



$$I_R \simeq \frac{.83}{830K} \simeq 1\mu A$$

Find V_1 when the devices in the current source are saturated.

$$1\mu A = \frac{50\ \mu A/V^2}{2}\frac{15}{5}(V_{GS2} - .83)^2$$

$$V_{GS2}^2 - 1.66\,V_{GS2} + .6756$$

$$V_{GS2} = 0.9455\ V$$

$$\therefore V_1 = .83 + .9455 = 1.78V$$

To design the startup circuit, make V_{GS} of M9 less than V_{THN} when M1, M2, M3, & M4 are saturated.

Choose $V_2 = 2.0V$ so $V_{GS9} = 2 - 1.78 = .22V$

Make $V_{GS7} = V_{GS8} = 1.0V$

$$1\mu A = \frac{50\ \mu A/V^2}{2}\frac{W}{L}(1 - .83)^2$$

$$\frac{W}{L} = 1.384$$

$L = 5\mu m$
$W = 7\mu m$ for M7 & M8

Now size M6

$V_{SG6} = 5 - 2 = 3V$

$$1mA = \frac{17 \mu A/V^2}{2} \frac{W}{L} (3 - .91)^2$$

$$\frac{W}{L} = .02693$$

$L = 150 \mu m$

$W = 4 \mu m$

Now size M9

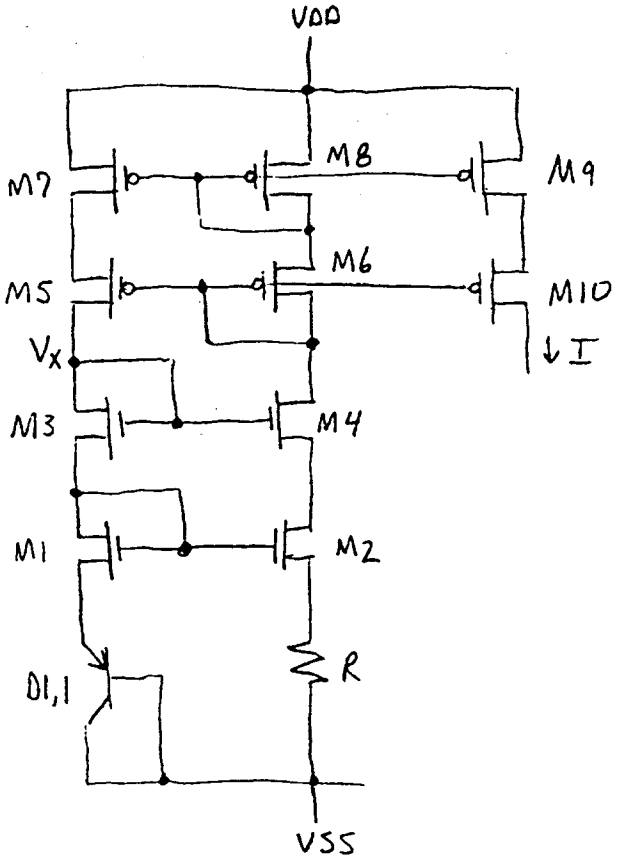
The size of M9 is not critical for the operation of the startup circuit since it only operates for a short period of time then turns off. We want M9 to be able to source current until V_1 is high enough to shut M9 off, and thus the current source will be operating at the correct point. To minimize layout area, make M9 minimum size.

$W = 3 \mu m$

$L = 2 \mu m$

21.10

Design a 5 mA current source using the diode referenced self-biasing circuit of Fig. 21.11. Verify the operation of your design using SPICE.



For the current source:

$$R = \frac{n \cdot V_T}{I} \ln \frac{I}{I_S}$$

$$= \frac{26mV}{5m} \ln \frac{5m}{10^{-15}}$$

$$= 116.1\ \Omega$$

Make V_{GS} the same for all n-channel devices.

$$V_{GS} = 1.2V$$

$$5mA = \frac{50mA/V^2}{2} \frac{W}{L} (1.2 - .83)^2$$

$$\frac{W}{L} = 1.46$$

$$W_1 = W_2 = W_3 = W_4 = 7\mu m$$
$$L_1 = L_2 = L_3 = L_4 = 5\mu m$$

For all p-channel devices

Make $V_{SG} = 1.2V$

$$5\mu A = \frac{17\mu A/V^2}{2} \frac{W}{L} (1.2 - .91)^2$$

$$\frac{W}{L} = 7$$

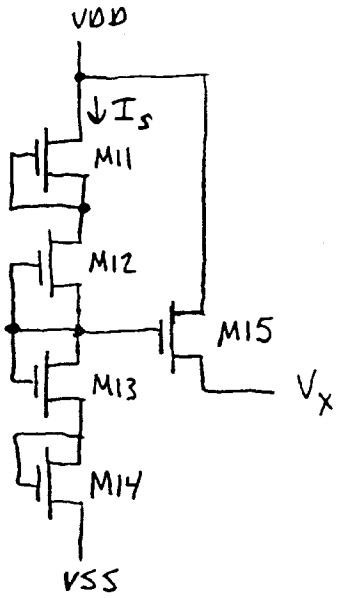
$$W_5 = W_6 = W_7 = W_8 = W_9 = W_{10} = 35\mu m$$
$$L_5 = L_6 = L_7 = L_8 = L_9 = L_{10} = 5\mu m$$

For the Start up circuit:

$$V_X = 5u(116.1k) + 2.4 = 2.98V$$

Make $V_{G15} < V_X$ $\quad V_{G15} = 2.5V$

and choose $I_S = 0.5\ mA$



Start up circuit

Make $V_{SG} = V_{GS} = 1.25\ V$

For M13 & M14

$$0.5\mu A = \frac{50\ \mu A/V^2}{2} \frac{W}{L} (1.25 - .83)^2$$

$$\frac{W}{L} = .1134$$

$W = 5\ \mu m$

$L = 45\ \mu m$

For M11 & M12

$$0.5\mu A = \frac{17\ \mu A/V^2}{2} \frac{W}{L} (1.25 - .91)^2$$

$$\frac{W}{L} = .5089$$

$W = 5\ \mu m$

$L = 10\ \mu m$

Design M6 to be minimum size

$W = 3\ \mu m$

$L = 2\ \mu m$

**** 02/22/98 19:36:27 ***** Win95 PSpice 6.3a (June 1996) **** ID# 90771 ****

* Problem 21.10

**** CIRCUIT DESCRIPTION

****

```
R1 3 0 116.1k
D1 1 0 PNPDIOD
M1 2 2 1 0 CMOSNB L=5u W=7u
M2 4 2 3 0 CMOSNB L=5u W=7u
M3 5 5 2 0 CMOSNB L=5u W=7u
M4 6 5 4 0 CMOSNB L=5u W=7u
M5 5 6 7 9 CMOSPB L=5u W=35u
M6 6 6 8 9 CMOSPB L=5u W=35u
M7 7 8 9 9 CMOSPB L=5u W=35u
M8 8 8 9 9 CMOSPB L=5u W=35u
M9 10 8 9 9 CMOSPB L=5u W=35u
M10 11 6 10 9 CMOSPB L=5u W=35u
M11 13 13 9 9 CMOSPB L=10u W=5u
M12 12 12 13 9 CMOSPB L=10u W=5u
M13 12 12 14 0 CMOSNB L=45u W=5u
M14 14 14 0 0 CMOSNB L=45u W=5u
M15 9 12 5 0 CMOSNB L=2u W=3u
VOUT 11 0 DC 2.2V
VDD 9 0 DC 5.0V
.OP
.MODEL PNPDIOD D(is=1E-15 n=1)

* BSIM model for n-channel CN20
* BSIM model for p-channel CN20
```

**** MOSFETS

NAME	M1	M2	M3	M4	M5
MODEL	CMOSNB	CMOSNB	CMOSNB	CMOSNB	CMOSPB
ID	4.93E-06	4.96E-06	4.93E-06	4.96E-06	-4.93E-06
VGS	1.51E+00	1.51E+00	1.82E+00	1.86E+00	-1.66E+00
VDS	1.51E+00	1.47E+00	1.82E+00	2.86E-01	-8.28E-02

NAME	M6	M7	M8	M9	M10
MODEL	CMOSPB	CMOSPB	CMOSPB	CMOSPB	CMOSPB
ID	-4.96E-06	-4.93E-06	-4.96E-06	-4.96E-06	-4.96E-06
VGS	-1.49E+00	-1.18E+00	-1.18E+00	-1.18E+00	-1.49E+00
VDS	-1.49E+00	-1.02E+00	-1.18E+00	-1.18E+00	-1.62E+00

NAME	M11	M12	M13	M14	M15
MODEL	CMOSPB	CMOSPB	CMOSNB	CMOSNB	CMOSNB
ID	-9.56E-08	-9.56E-08	9.56E-08	9.56E-08	5.01E-12
VGS	-1.05E+00	-1.32E+00	1.53E+00	1.09E+00	-1.27E+00
VDS	-1.05E+00	-1.32E+00	1.53E+00	1.09E+00	1.10E+00

Problem 21.11

For Fig 21.12, if we require the current is 5μA, and the gate-source voltages are 1.2V, we get,

For n-channel devices:

$$5\mu A = \frac{50\mu A/V^2 \times W}{2 \times L}(1.2v - 0.83v)^2 \Rightarrow \left(\frac{W}{L}\right)_n = 1.46$$

Set $L_n = \underline{5\mu m}$, $W_n = \underline{7\mu m}$.

For p-channel devices:

$$5\mu A = \frac{17\mu A/V^2 \times W}{2 \times L}(1.2 - 0.91)^2 \Rightarrow \left(\frac{W}{L}\right)_p \simeq 7$$

Set $L_p = \underline{5\mu m}$, $W_p = \underline{35\mu m}$.

Also, set $k = 8$, $(n = 1)$

$$R = \frac{nV_T \times \ln k}{I} = \frac{1 \times 26mv \times \ln 8}{5\mu A} \simeq \underline{10.8k\Omega}$$

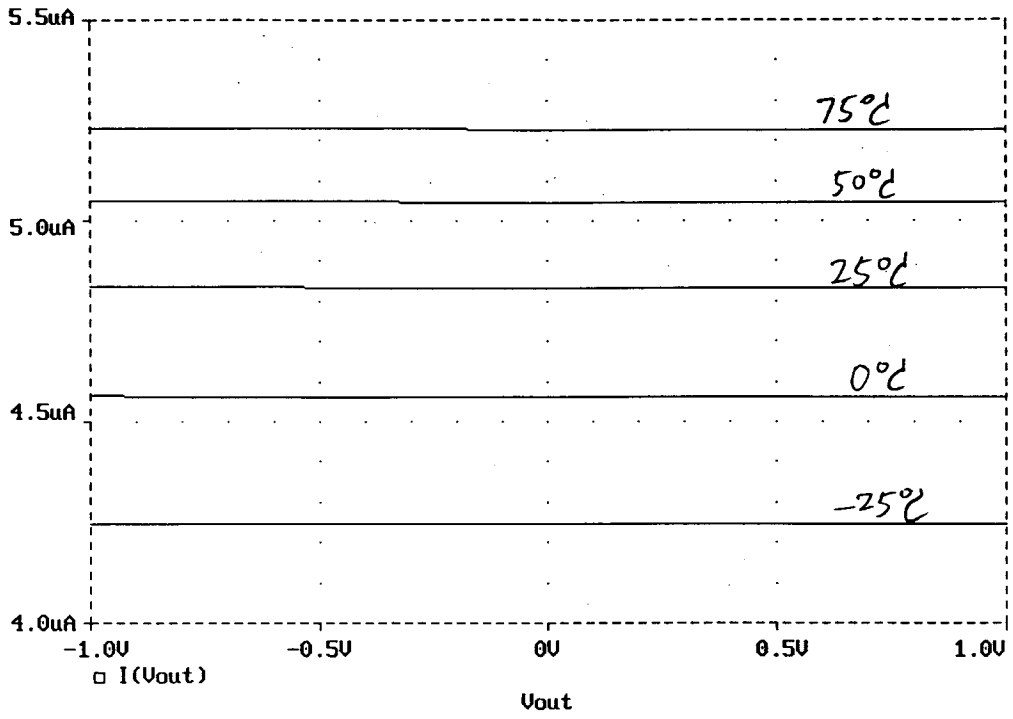
See next page for SPICE simulations.

Problem 21.11 (simulation)

```
*** Top Level Netlist ***
D1      7 3 pnpdiod
D2      8 3 pnpdiod 8
M1      4 4 7 3 CMOSNB  L=5u W=7u
M2      2 4 11 3 CMOSNB  L=5u W=7u
M3      1 1 4 3 CMOSNB  L=5u W=7u
M4      9 1 2 3 CMOSNB  L=5u W=7u
M5      1 9 12 6 CMOSPB  L=5u W=35u
M6      9 9 10 6 CMOSPB  L=5u W=35u
M7      12 10 6 6 CMOSPB  L=5u W=35u
M8      10 10 6 6 CMOSPB  L=5u W=35u
M9      13 10 6 6 CMOSPB  L=5u W=35u
M10     14 9 13 6 CMOSPB  L=5u W=35u
R1      8 11 10.8k TC1=0.002
VDD     6 0   DC 2.5v AC 0 0
Vout    14 0  DC 0 AC 0 0
VSS     3 0   DC -2.5v AC 0 0
.NODESET V(8)=0 V(2)=0 V(12)=0

***** Spice models and macro models *****

.MODEL PNPDIOD D
+IS=1E-15 n=1
.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
*.OPTION post=3 acct opts VZERO=2 $probe=1

.OPTION ABSTOL=1n RELTOL=0.01 VNTOL=1mv ITL1=100 ITL2=100
.probe
.DC Vout -1 1 .01 temp -25 75 25
*.print DC all
.end
```

The SPICE simulation is shown on next page:

Problem 21.11 (simulation, cont.)



Problem 21.12

ANS: The figure is shown in figure 21.14 @Page454.

$$Vd1 = IR + Vd2 \quad (1)$$

From $Id1 = Is * Exp(Vd1/nVt) \Rightarrow Vd1 = nVt * \ln(I/Is)$ (2)

$Id2 = K * Is * Exp(Vd2/nVt) \Rightarrow Vd2 = nVt * \ln[I/(K*Is)]$ (3)

$$IR = Vd1 - Vd2 = nVt * [\ln(I/Is) - \ln[I/(K*Is)]] = nVt * \ln K \quad (4)$$

$\Rightarrow$ $I = nVt * \ln K / R$ (5)

Since $Vref = I * R * L + Vd3$ (6)

From $Id3 = K * IsExp(Vd1/nVt) \Rightarrow Vd3 = nVt * \ln[I/(K*Is)]$ (7)

Pluging (5) and (7) into (6)

$$Vref = L * n * Vt * \ln K + nVt * \ln[I/(K*Is)] \quad (8)$$

Pluging n=1, K=8, T=300K, I=10uA and $Is=10^{-15}$ A into equation (8) $\Rightarrow$

@L=11.3 Vref = 1.15V

@L=12 Vref = 1.20V

So, the reference voltage increases with L increasing.

Problem 21.13

ANS: The figure is shown in figure P21.13. Assuming the current through D1 is ID1 and through D2 is ID2. Since the voltage at '+' and '-' terminals of the Op-amp with infinite open loop gain is equal, i.e.

$$Vref-ID1*LR=Vref-ID2*LR \quad ==> \quad ID1=ID2=I \qquad (1)$$

Also

$$I*R + Vd1 = Vd2 \qquad (2)$$

As shown in problem 21.12, $Vd1= nVt*\ln[I/(K*Is)]$ and $Vd2 = nVt*\ln(I/Is)$ (3)
Pluging (3) into (2), ==>

$$I = (nVt*\ln K)/R \qquad (4)$$

$$Vref = I*R*L + Vd2 = (L*n*\ln K)Vt + nVt*\ln(I/Is) \qquad (5)$$

By definition of TC from ch.7, $TCVref = (1/Vref)*dVref/dT = *1/Vreg)*[L*n*\ln K*(dVt/dT) + dVd2/dT]$
Let TCVref = 0, and pluging dVt/dT = 0.085mV/C, dVd2/dT = -2mV/C, ==>

$$L*n*\ln K = 2/0.085 = 23.5$$

Problem 21.15

Solution: Select M4 5u/5u, M3 and M5 15u/5u, Select K=4, ==> M6 20u/5u. Same start-up circuit as figure 21.17 of Textbook, and the rest PMOS with size 70u/5u. Plugging the values into equation (21.46) and @ T =300 K, It comes out the TC expression of Vref which was chosed as VGS4 is:

$$dVref/dT = -2400 + 3000/(R\beta 4)$$
$$= -2400 + 6x10^7/R \qquad (1)$$

Note: $\beta 1$ in the equation becomes $\beta 4$, see the schematic below.

By definition of TC in Ch.7,

$$TCVref = (1/Vref)*dVref/dT \qquad (2)$$

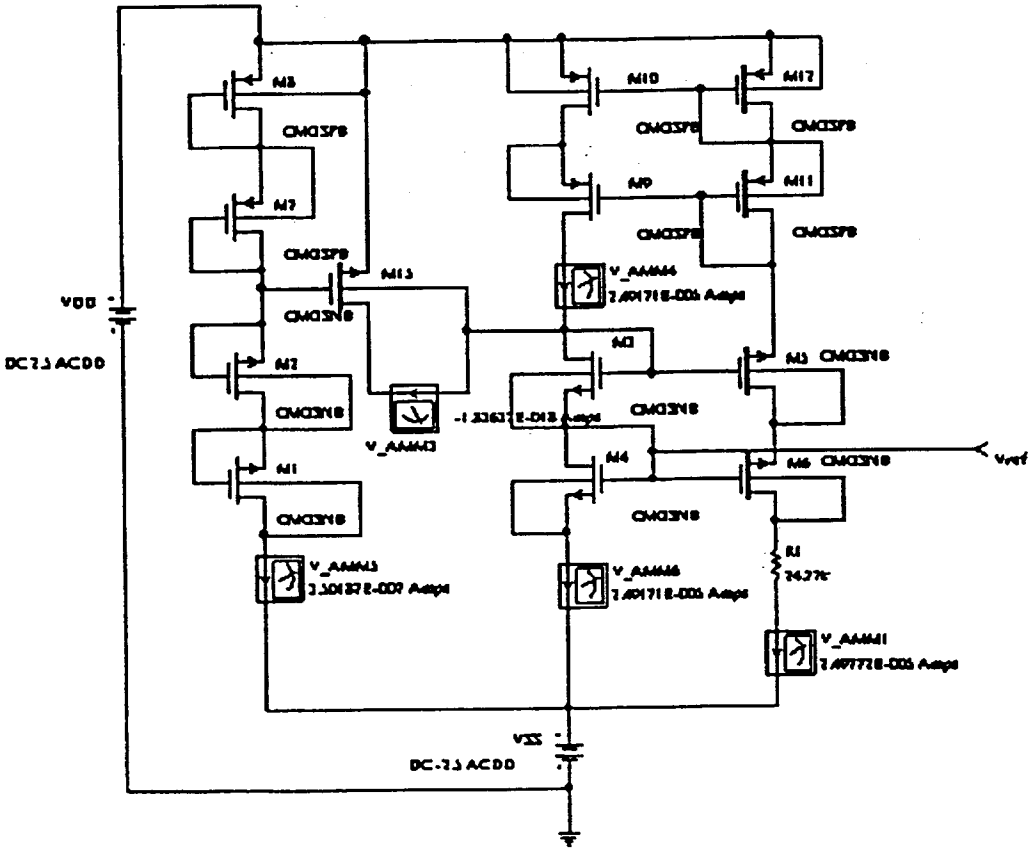
Notice: $Vref = VGS4 = Vthn + SQRT(2*ID/\beta 4)$ (3)

ID is the current through MOSFETs M3, M4, M5, M6, and M9 ~ M12. By neglecting the body effect of M6, ==> (see equation (21.39) to (21.41)

$$ID = [2/(R^2*\beta 4)]*[1-SQRT(1/K)]^2 = 1000/R^2 \qquad (4)$$

Pluging equation (4) into (3), ==> $Vref = Vthn + 20000/R$ (5)
Pluging equation (1), (5) into (2), Let TCVref equals to **1000ppm/°C**, get **$R = 8x10^7/3230 = 24.77\ k\Omega$.**
The circuit design is shown below which was simulated in Turbosim. VSS = -2.55 V, VDD =2.5V.

Notice equation (3) gives hand calculation of Vref is about 1.63V. But TurboSim gives about -0.5 - (-2.5) = 2V. The error mainly due to the body effect of M6.



The following netlist was generated:

*** (TurboSim V 1.1) Netlist for C:\TS\P2115V4.CKT

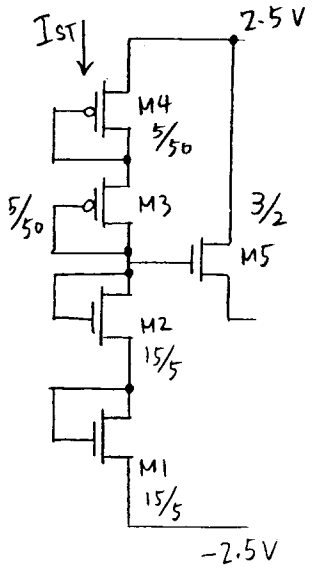
*** Top Level Netlist ***

```
M1        1 2 2 1 CMOSNB  L=5u W=15u
M10       13 14 18 18 CMOSPB  L=5u W=70u
M11       9 9 14 14 CMOSPB  L=5u W=70u
M12       14 14 18 18 CMOSPB  L=5u W=70u
M15       15 3 18 4 CMOSNB  L=2u W=3u
M2        2 3 3 2 CMOSNB  L=5u W=15u
M3        4 4 Vref Vref CMOSNB  L=5u W=15u
M4        Vref Vref 7 7 CMOSNB  L=5u W=5u
M5        8 4 9 8 CMOSNB  L=5u W=15u
M6        10 Vref 8 10 CMOSNB  L=5u W=20u
M7        3 3 11 11 CMOSPB  L=50u W=5u
M8        11 11 18 18 CMOSPB  L=50u W=5u
M9        12 9 13 13 CMOSPB  L=5u W=70u
R1        10 17 24.77k
V_AMM1    17 6 0V
V_AMM3    4 15 0V
V_AMM4    12 4 0V
V_AMM5    1 6 0V
V_AMM6    7 6 0V
VDD       18 0      DC 2.5 AC 0 0
VSS       6 0       DC -2.5 AC 0 0
***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
*BSIM model*
.MODEL CMOSPB PMOS LEVEL=4
*BSIM model*
***** End of spice models and macro models *****
.OPTION ABSTOL=1u CHGTOL=1p RELTOL=0.01 VNTOL=1mv
.op
.end
```

Operating Point Analysis gives the following results:

```
Operating point information:

        Node    Voltage
        ----    -------
        V(1)    -2.50000e+000
        V(2)    -1.64389e+000
        V(13)   1.213438e+000
        V(14)   1.138767e+000
        V(18)   2.500000e+000
        V(9)    -2.22467e-001
        V(15)   9.795691e-001
        V(3)    -7.87785e-001
        V(4)    9.795691e-001
        vref    -4.96132e-001
        V(7)    -2.50000e+000
        V(8)    -5.62917e-001
        V(10)   -1.88132e+000
        V(11)   8.561073e-001
        V(12)   9.795691e-001
        V(17)   -2.50000e+000
        V(6)    -2.50000e+000
        m9#drain          9.809321e-001
        m9#source         1.212075e+000
        m8#drain          8.561265e-001
        m8#source         2.499981e+000
        m7#drain          -7.87766e-001
        m7#source         8.560881e-001
        m12#drain         1.140133e+000
        m12#source        2.498634e+000
        m11#drain         -2.21101e-001
        m11#source        1.137400e+000
        m10#drain         1.214801e+000
        m10#source        2.498637e+000
        m6#drain          -1.88062e+000
        m6#source         -5.63614e-001
        m5#drain          -5.62220e-001
        m5#source         -2.23164e-001
        m4#drain          -4.96827e-001
        m4#source         -2.49930e+000
        m3#drain          9.788739e-001
        m3#source         -4.95437e-001
        m2#drain          -1.64388e+000
        m2#source         -7.87795e-001
        m15#drain         9.795691e-001
        m15#source        2.500000e+000
        m1#drain          -2.49999e+000
        m1#source         -1.64390e+000

        Source  Current
        ------  -------

        vss#branch      5.024445e-005
        vdd#branch      -5.02445e-005
        v_amm6#branch   2.491711e-005
        v_amm5#branch   3.501874e-007
        v_amm4#branch   2.491711e-005
        v_amm3#branch   -1.83637e-018
        v_amm1#branch   2.497715e-005
```

Problem 21.14



The power dissipation of the startup circuit is

$$P_{ST} = I_{ST} \times (2.5v - (-2.5v)) = I_{ST} \times 5(v)$$

We first calculate V_{GSN} and V_{SGP},

$$\begin{cases} 2(V_{GSN} + V_{SGP}) = 5 \\ \frac{50\mu A/V^2 \times 15}{2 \times 5}(V_{GSN} - 0.83)^2 = \frac{17\mu A/V^2 \times 5}{2 \times 50}(V_{SGP} - 0.91)^2 \end{cases}$$

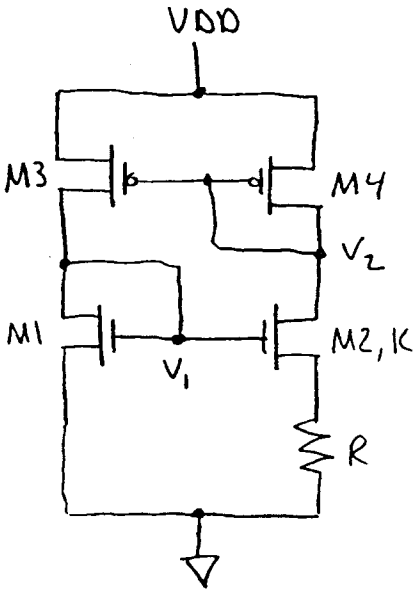
$$\Longrightarrow V_{GSN} \simeq 0.9v \text{ and } V_{SGP} \simeq 1.6\,V.$$

$$I_{ST} = \frac{17\mu A/V^2 \times 5}{2 \times 50} \times (1.6 - 0.91)^2 \simeq \underline{\underline{0.4\,\mu A}}$$

$$\therefore P_{ST} = I_{ST} \times (V_{DD} - V_{SS}) = 5v \times 0.4\mu A = \underline{\underline{2\mu W}}.$$

21.16

The β multiplier reference is an example of a circuit that uses positive feedback. Discuss methods of ensuring a stable operating point for the circuit.



Since the gain from V_1 to V_2 is negative and the gain from V_2 to V_1 is negative, the loop has positive feedback. For a stable circuit the feedback, the feed back gain must be less than 1.

$$\text{Gain} = \frac{V_2}{V_1}\cdot\frac{V_1}{V_2} = \left(\frac{-\frac{1}{g_{m4}}}{\frac{1}{g_{m4}}+R}\right)\left(-\frac{g_{m3}}{g_{m1}}\right)$$

since $g_{m3} = g_{m4}$

$$\text{Gain} = \frac{1}{\frac{g_{m1}}{g_{m2}} + g_{m1}R}$$

also $g_{m2} = \sqrt{K}\, g_{m1}$

$$\text{Gain} = \frac{1}{\frac{1}{\sqrt{K}} + g_{m1}R}$$

$$g_{m1} = \sqrt{2\beta_1 I_0}$$

$$I_0 = \frac{2}{R^2\beta_1}\cdot\left(1-\sqrt{\frac{1}{K}}\right)^2$$

Substituting I_0 into the equation for g_{m1} yields

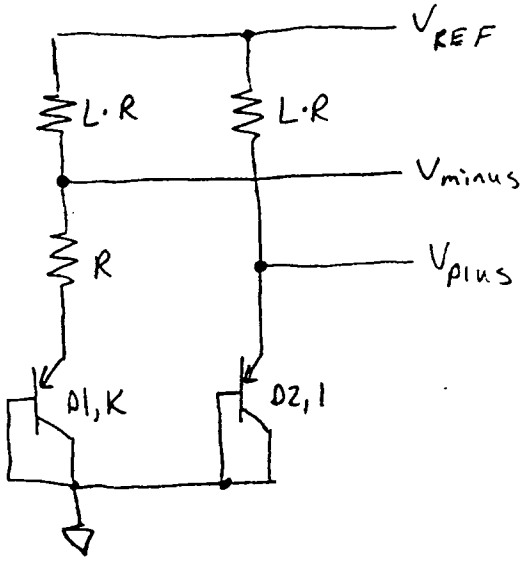
$$g_{m1} = \frac{2}{R}\left(1-\sqrt{\frac{1}{K}}\right)$$

$$\therefore \quad \text{Gain} = \frac{1}{2-\sqrt{\frac{1}{K}}}$$

For the Gain < 1, $K > 1$!

21.17

An important consideration in the design of a voltage or current reference is the design of the startup circuit. Consider the portion of the bandgap reference of Fig. P21.13 shown in Fig. 21.17a. Using SPICE, plot V_{REF} against V_{plus} and V_{minus}. The result should look similiar to Fig. P21.17b. Design a start up circuit for the bandgap of Fig. 21.13



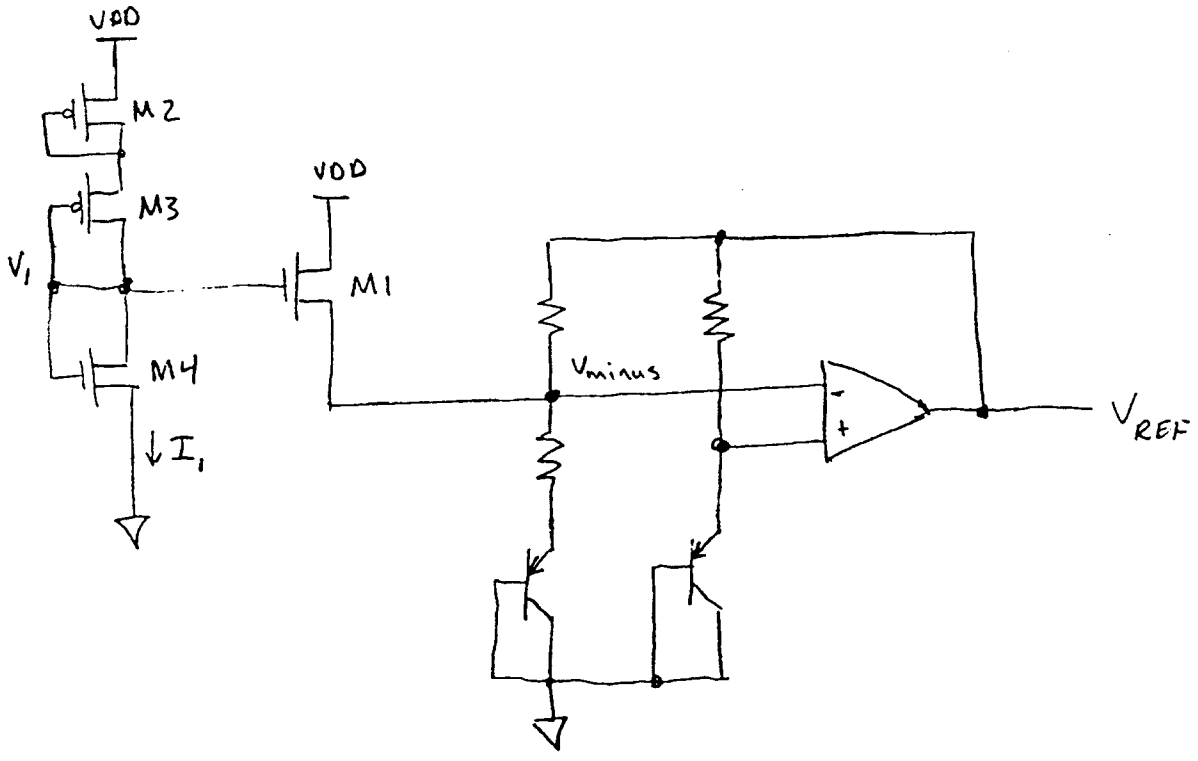
For the simulation use the values calculated for a TC = 0 on p. 479.

$K = 8$

$L = 12$

$R = 65\,k\Omega$

The startup circuit should look similiar to the following:



To design the start up circuit want to make V_{minus} large than V_{plus}. From the simulation results we can see that when V_{minus} is larger than 0.55V it will be larger than V_{plus}. V_{REF} must be larger than 1.2V.

For designing the start up circuit, ideally we would like to make V_1 less than V_{minus} once the circuit is table, but in this case $V_{minus} > .55V$ so it's impossible to make $V_1 < .55V$. For this case make $V_{GS1} < V_{THN}$. Design M4 so $V_1 = 1.2V$,

$$1\mu A = \frac{50\mu A/V^2}{2} \frac{W_4}{L_4}(1.2 - .83)^2$$

$$\frac{W_4}{L_4} = .292$$

$$W_4 = 6\,\mu m$$

$$L_4 = 20\,\mu m$$

$$\text{Make } V_{SG2} = V_{SG3} = \frac{5 - 1.2}{2} = 1.9\,V$$

$$1\mu A = \frac{17\mu A/V^2}{2} \frac{W}{L}(1.9 - .91)^2$$

$$\frac{W}{L} = .12$$

$$W_2 = W_3 = 6\,\mu m$$

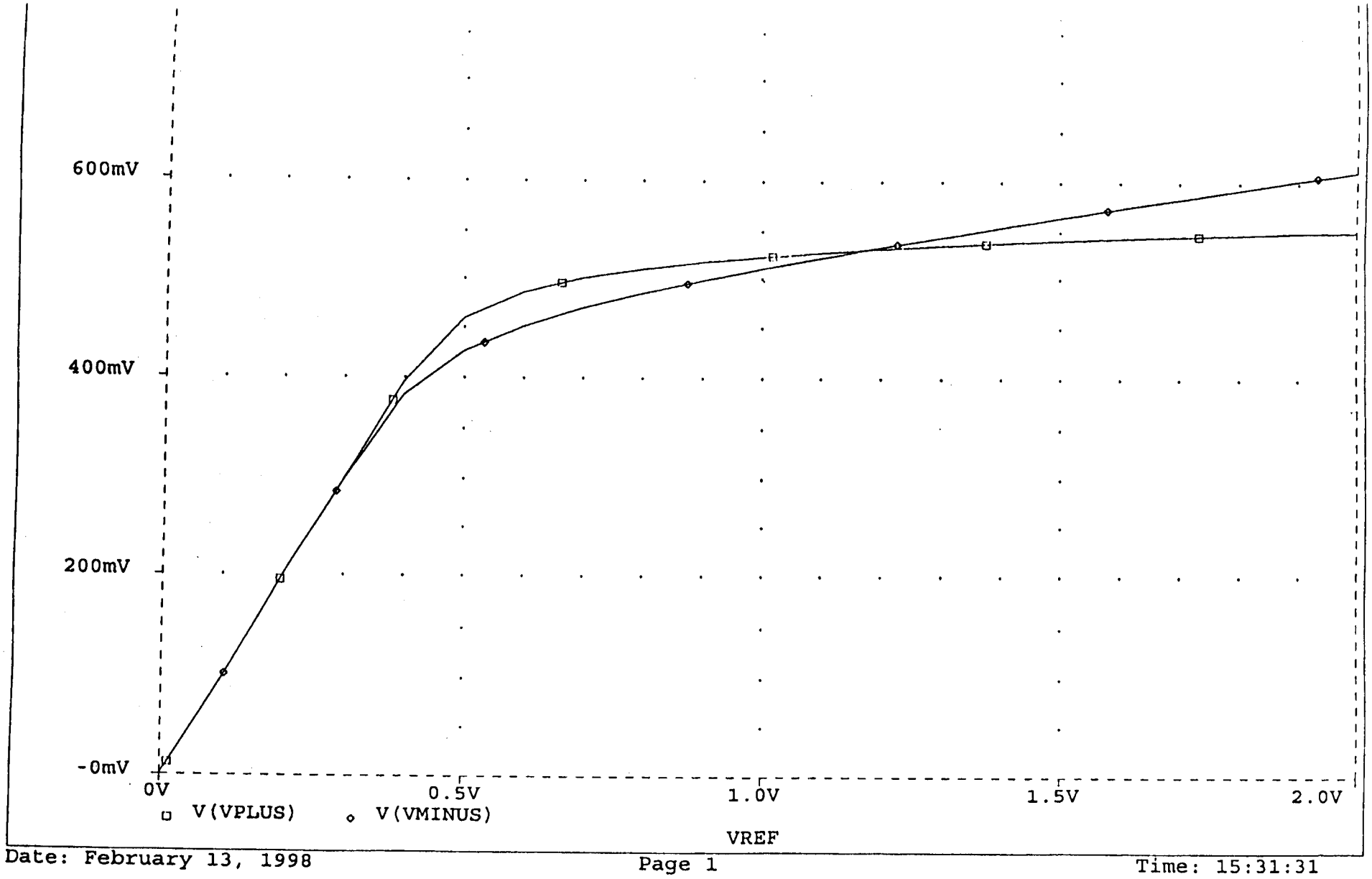
$$L_2 = L_3 = 50\,\mu m$$

Make M1 minimum size

$$W_1 = 3\,\mu m$$

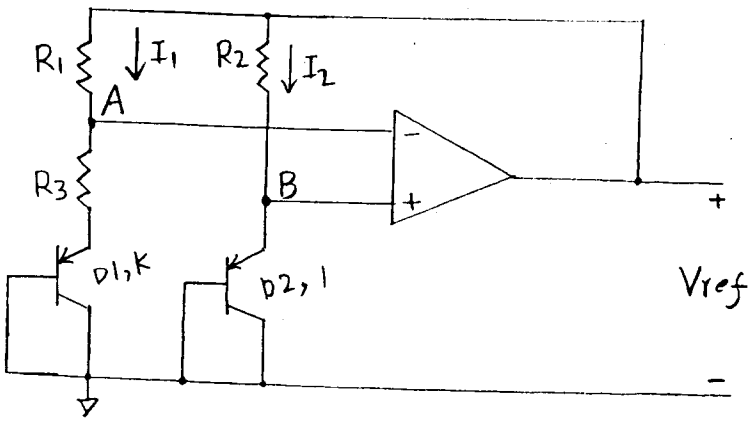
$$L_2 = 2\,\mu m$$

```
* Problem 21.17
D1 1 0 PNPDIOD  8
D2 VPLUS 0 PNPDIOD
R1 VMINUS 1 65k
R2 2 VMINUS 780K
R3 2 VPLUS 780K
VREF 2 0  DC 0V
.DC  VREF 0 2V 0.1V
.MODEL PNPDIOD D(is=1E-15 n=1)
.PROBE
.END
```



Problem 21.17 (simulation)

Problem 21.18



$$V_{ref} = I_2 R_2 + V_{d2} \qquad (1)$$

$\because V_A = V_B$

$\therefore I_1 R_1 = I_2 R_2 \Longrightarrow \frac{I_1}{I_2} = \frac{R_2}{R_1} \qquad (2)$

Also, $I_1 R_3 + V_{d1} = V_{d2}$

$$\Longrightarrow I_1 R_3 + n V_T \ln \frac{I_1}{I_S} = n V_T \ln \frac{I_2}{I_S}$$

$$\Longrightarrow I_1 = \frac{1}{R_3} n V_T \ln \frac{I_2}{I_1} = \frac{1}{R_3} n V_T \ln \frac{R_1}{R_2} \text{ (inserting (2))} \qquad (3)$$

Plugging (3) into (1), we get

$$V_{ref} = I_2 R_2 + V_{d2} = I_1 R_1 + V_{d2} = \underline{\underline{\frac{R_1}{R_3} n V_T \ln \frac{R_1}{R_2} + V_{d2}}}$$

Problem 21.19

$$R = \frac{nV_T}{I_D} \ln k \quad , \text{ where } k = 8,\ n = 1,\ V_T = 26mV \text{ @ } 300k$$

$$\Rightarrow R = \frac{1 \times 26 \times 10^{-3}\ V}{0.1\ \mu A} \ln 8 \quad = 540k.$$

SPICE simulation is shown below:

```
*** Top Level Netlist ***
M1      3 3 0 0 CMOSNB  L=5u W=5u
M10     12 5 9 4 cmospb  L=5u W=70u
M2      2 3 7 0 CMOSNB  L=5u W=40u
M3      1 1 3 0 CMOSNB  L=5u W=15u
M4      5 1 2 0 CMOSNB  L=5u W=15u
M5      1 5 8 4 cmospb  L=5u W=70u
M6      5 5 6 4 cmospb  L=5u W=70u
M7      8 6 4 4 cmospb  L=5u W=70u
M8      6 6 4 4 cmospb  L=5u W=70u
M9      9 6 4 4 cmospb  L=5u W=70u
R1      0 7 540k
V_Iout   12 10 0V
VDD     4 0   DC 5 AC 0 0
Vout    10 0   DC 0 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.probe
.DC Vout 0 5 .01
*.plot dc all
*.print dc all
.end
```

The SPICE simulation result is shown below: