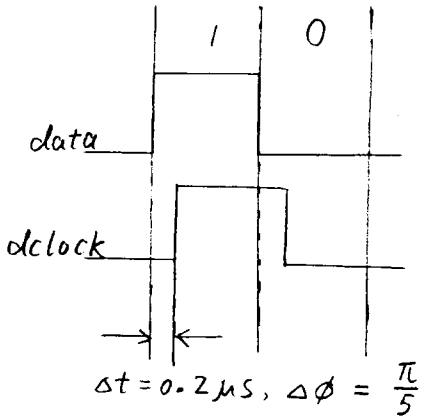
Chapter 19

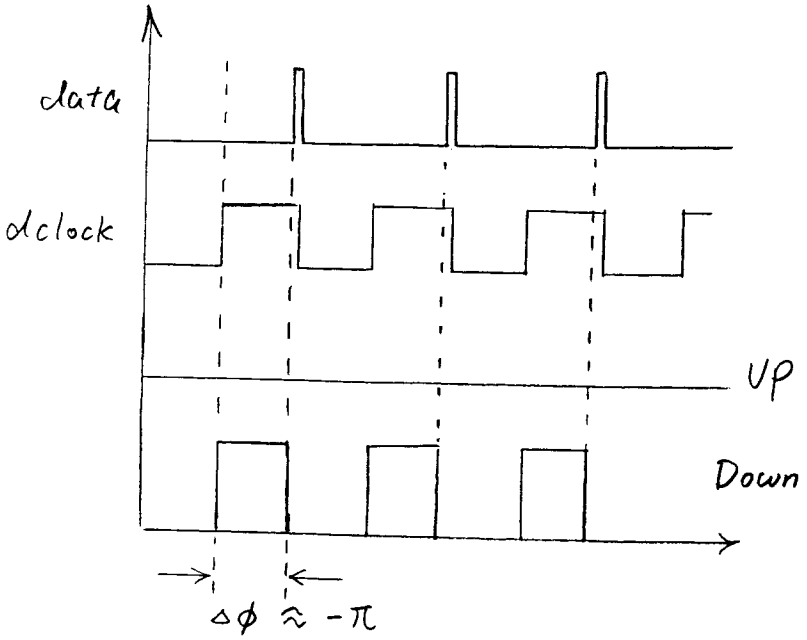
Problem 19.1



$$\Delta\phi = \frac{0.2\mu s}{1\mu s} \times \pi = \frac{1}{5}\pi$$

$$V_{P\,Dout} = VDD \times \frac{\Delta\phi}{\pi} = \frac{V_{DD}}{5} = 1V.$$

Problem 19.2



Problem 19.3

Using 5 stages. Assuming the MOSFETs of inverters, M2 & M3, are sized for equal drive; $L_n = L_p = 2\mu m$, $W_n = 3\mu m$, $W_p = 9\mu m$, we get

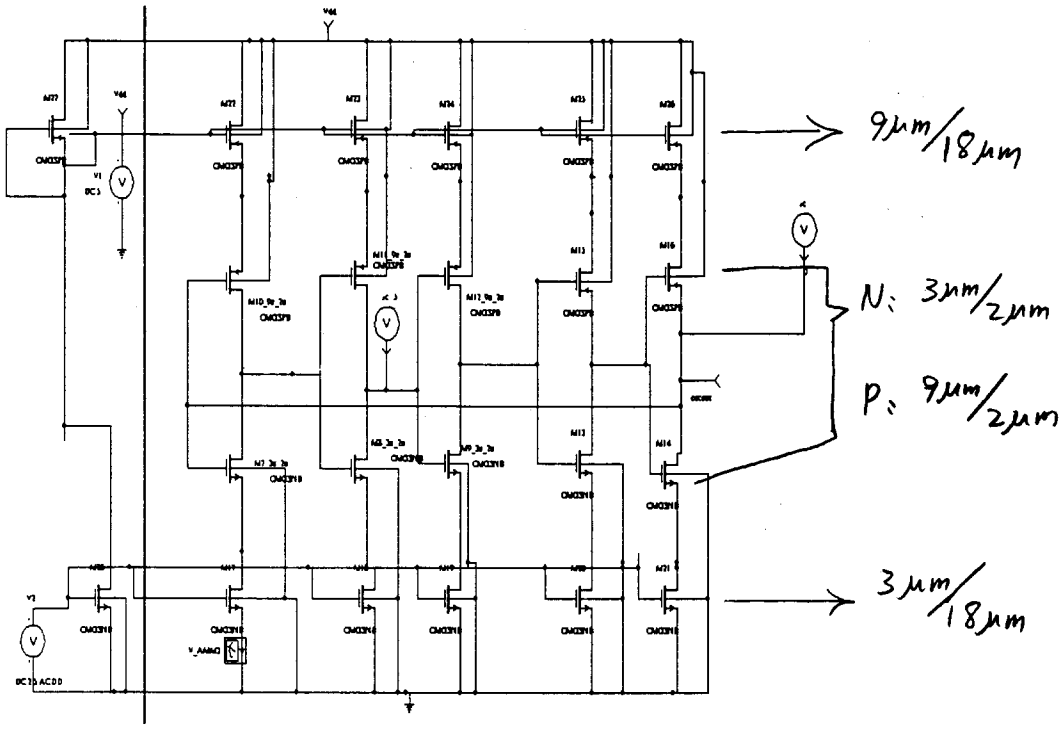
$$C_{TOT} = 48fF$$

$$f_{osc} = \frac{I_D}{N \cdot C_{TOT} \cdot VDD} \Rightarrow I_D = f_{osc} \times N \times C_{TOT} \times V_{DD} = 10MHz \times 5 \times 48fF \times 5V$$

$$= 12\mu A$$

$$I_D = \frac{\beta_5}{2} \times (V_{GS} - V_{THN})^2 \Rightarrow \left(\frac{W}{L}\right)_5 = 0.172. \quad \text{Choose } \frac{W_5}{L_5} = \frac{3\mu m}{18\mu m}.$$

Problem 19.3 *(cont.)*

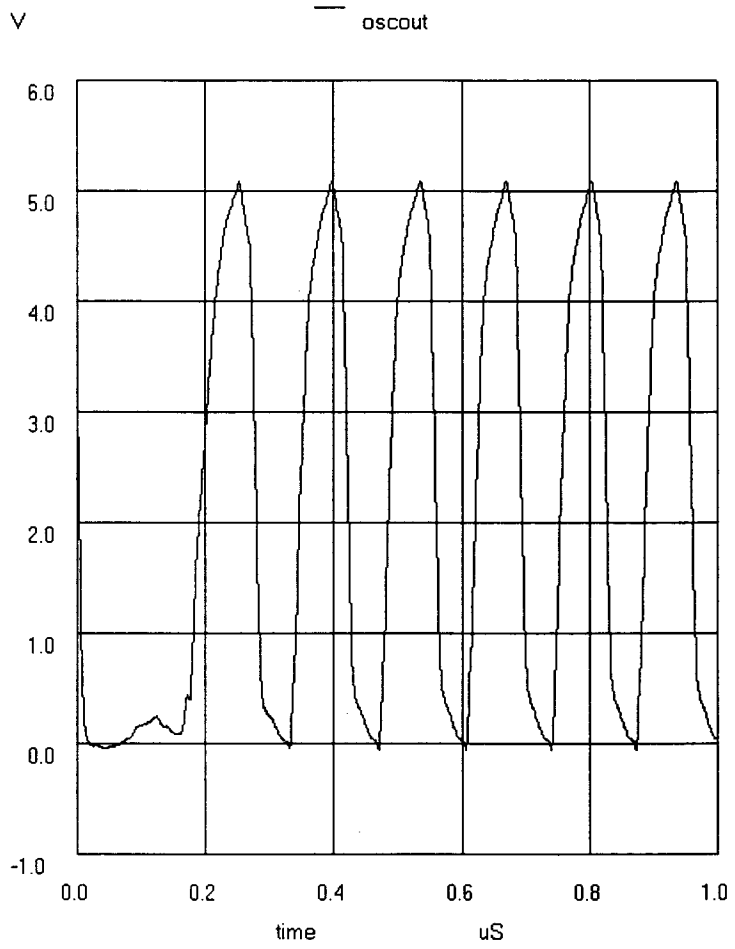



```
*** Top Level Netlist ***
.ic        V(2)=5
.ic        V(oscout)=0
M10_9u_2u        1 oscout 6 Vdd CMOSPB  L=2u W=9u
M11_9u_2u        2 1 9 Vdd CMOSPB  L=2u W=9u
M12_9u_2u        5 2 10 Vdd CMOSPB  L=2u W=9u
M13      4 5 17 0 CMOSNB  L=2u W=3u
M14      oscout 4 12 0 CMOSNB  L=2u W=3u
M15      11 5 4 Vdd CMOSPB  L=2u W=9u
M16      8 4 oscout Vdd CMOSPB  L=2u W=9u
M17      14 20 19 0 CMOSNB  L=18u W=3u
M18      13 20 0 0 CMOSNB  L=18u W=3u
M19      16 20 0 0 CMOSNB  L=18u W=3u
M20      17 20 0 0 CMOSNB  L=18u W=3u
M21      12 20 0 0 CMOSNB  L=18u W=3u
M22      Vdd 15 6 Vdd CMOSPB  L=18u W=9u
M23      Vdd 15 9 Vdd CMOSPB  L=18u W=9u
M24      Vdd 15 10 Vdd CMOSPB  L=18u W=9u
M25      Vdd 15 11 Vdd CMOSPB  L=18u W=9u
M26      Vdd 15 8 Vdd CMOSPB  L=18u W=9u
M27      Vdd 15 15 Vdd CMOSPB  L=18u W=9u
M28      15 20 0 0 CMOSNB  L=18u W=3u
M7_3u_2u         1 oscout 14 0 CMOSNB  L=2u W=3u
M8_3u_2u         2 1 13 0 CMOSNB  L=2u W=3u
M9_3u_2u         5 2 16 0 CMOSNB  L=2u W=3u
V_AMM3           19 0 0V
V1       Vdd 0   DC 5
V2       20 0    DC 2.5 AC 0 0
```

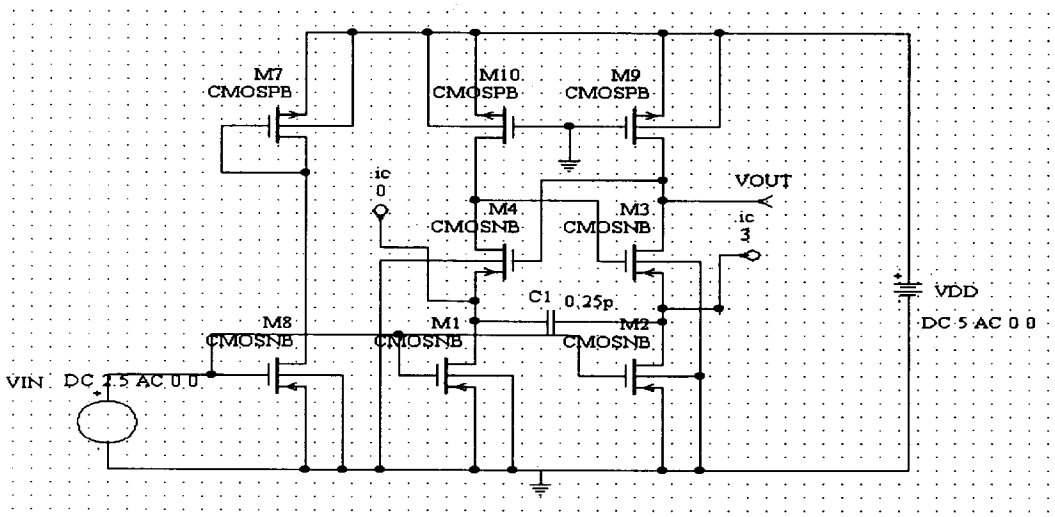
***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
.OPTION ABSTOL=10u ITL4=1000 RELTOL=0.1 VNTOL=10mv
.probe
.tran 1n 1000n 0n 1n uic
.plot tran all
.print tran all
.end

The SPICE simulation is shown below:



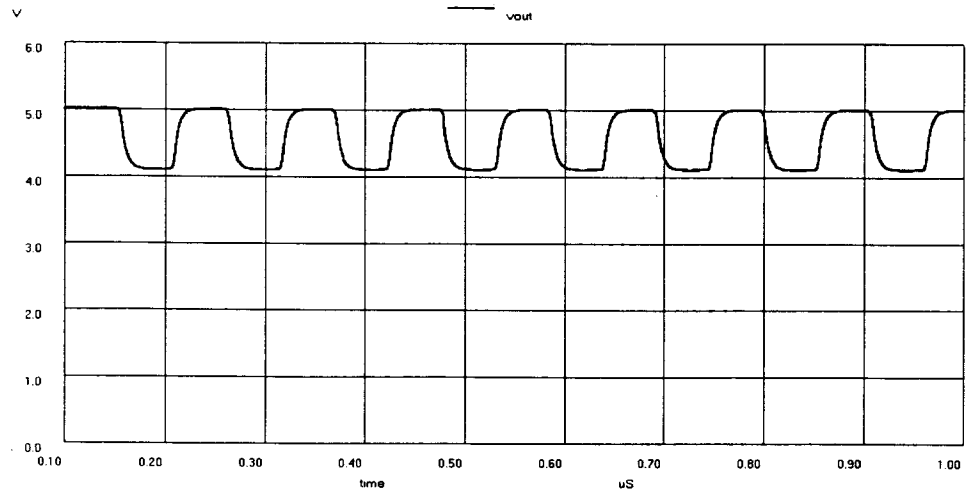
Problem 19.4



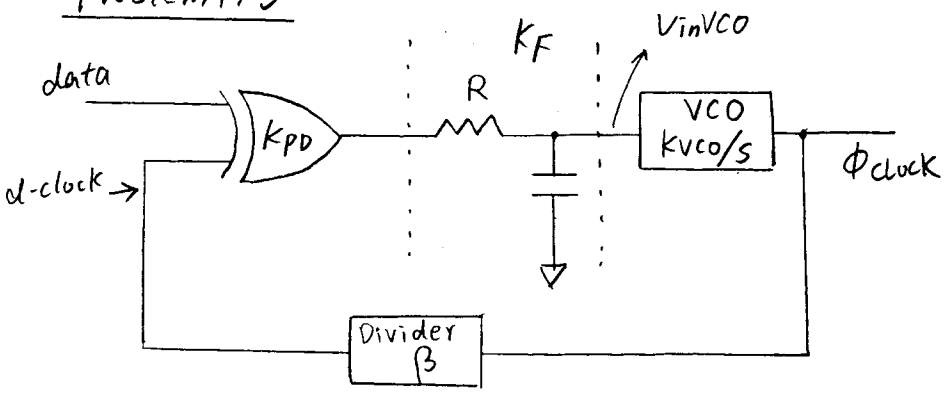

```
*** Top Level Netlist ***
.ic       V(3)=3
.ic       V(1)=0
C1        1 3 0.25p
M1        1 8 0 0 CMOSNB  L=21u W=3u
M10       6 0 7 7 CMOSPB  L=10u W=3u
M2        3 8 0 0 CMOSNB  L=21u W=3u
M3        VOUT 6 3 0 CMOSNB  L=2u W=30u OFF
M4        6 VOUT 1 0 CMOSNB  L=2u W=30u
M7        5 5 7 7 CMOSPB  L=21u W=9u
M8        5 8 0 0 CMOSNB  L=21u W=3u
M9        VOUT 0 7 7 CMOSPB  L=10u W=3u
VDD       7 0       DC 5 AC 0 0
VIN       8 0       DC 2.5 AC 0 0

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=5mv
.tran 1n 1000n 0 1n uic
.end
```



Problem 19.5



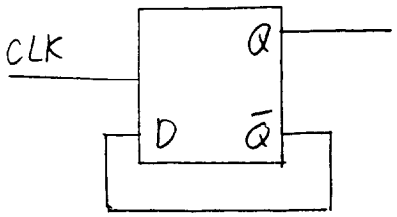
$$H(s) = \frac{A(s)}{1 + A(s)F(s)}$$

$$A(s) = K_{PD} \times K_F \times K_{VCO}/s \quad , \quad F(s) = \beta$$

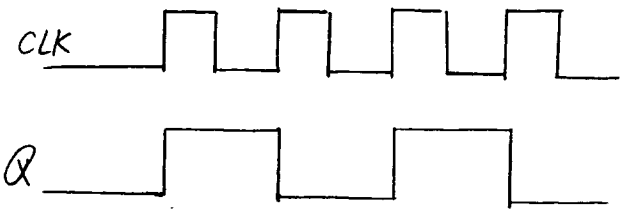
$$\therefore H(s) = \frac{K_{PD} \times K_F \times K_{VCO}/s}{1 + K_{PD} \times K_F \times K_{VCO} \times \beta/s} = \frac{K_{PD} K_F K_{VCO}}{s + \beta K_{PD} K_F K_{VCO}}$$

Problem 19.6

One of the implementation of divide by 2 is shown below:

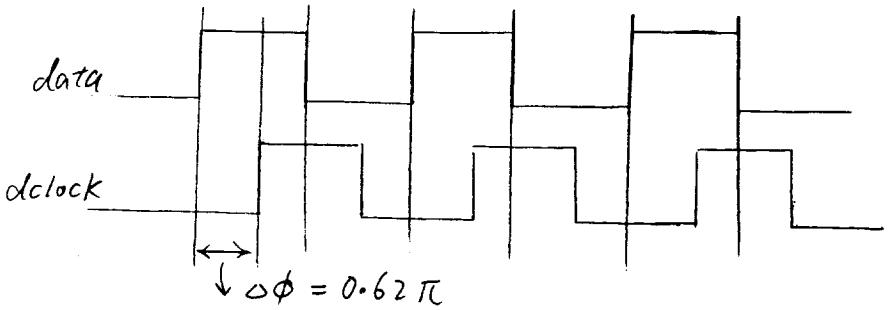


(positive edge-triggered D FF)

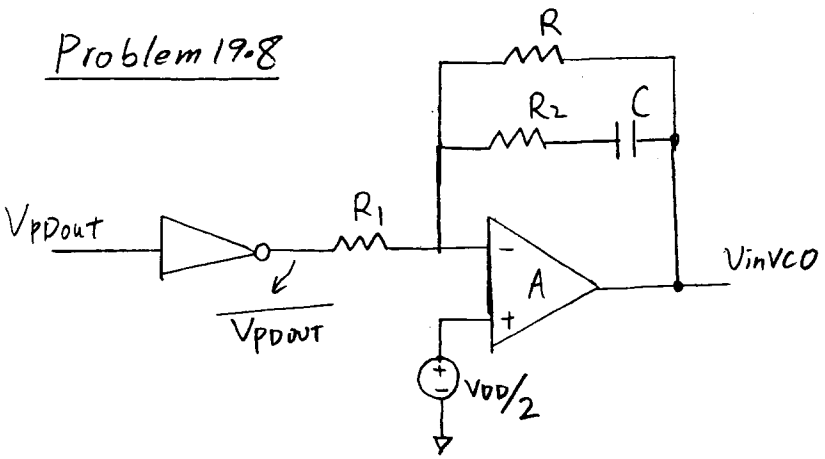


Problem 19.7

When input data rate is 9.04Mbits/s, the clock is aligned slightly off center of the data, and $\Delta\phi = 0.62\pi$.



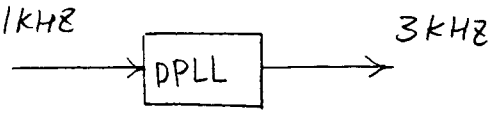
Problem 19.8



Assume $R \gg R_1$ & R_2, and ideal op-amp A is used,

$$K_F = \frac{V_{inVCO}}{V_{PDOUT}} = \frac{-V_{inVCO}}{\overline{V_{PDOUT}}} = \frac{R_2 + \frac{1}{CS}}{R_1} = \frac{1 + SR_2C}{SR_1C}$$

Problem 19.9



Assume VCO oscillates from 6kHz to DC for input voltages (V_{inVCO}) from 0 to 5V.

$$K_{VCO} = 2\pi \times \frac{6000 - 0\ (Hz)}{5\ V} = 7536\ rad/V\cdot S$$

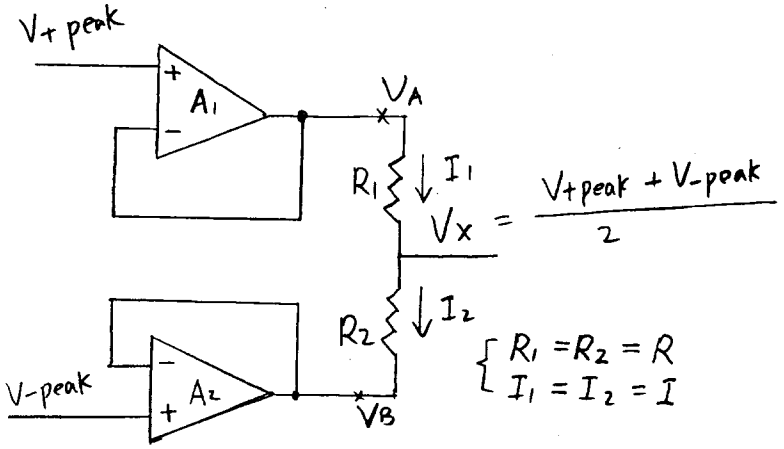
The lock range, Δf_L, is set to 200Hz (800 ~ 1200 Hz).

Assume $\xi = 0.7$, $\omega_n = \frac{2\pi \times 200}{4\pi \times 0.7} = 143\ rad/S$

$$\begin{cases} \omega_n = \sqrt{\dfrac{K_{PDtri}\, K_{VCO}}{N(R_1 + R_2)C}} \\ \xi = \dfrac{\omega_n}{2} R_2 C \end{cases}$$

Insert the data, we get $\underline{\underline{R_2C \approx 9.7\,mS}}$; $\underline{\underline{R_1C \approx 39.2\,mS}}$.

Problem 19.10



For unity feedback op-amps A_1 and A_2, we have

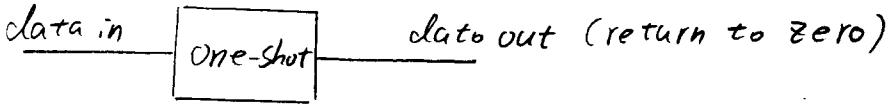
$V_A = V_{+peak}$, $V_B = V_{-peak}$

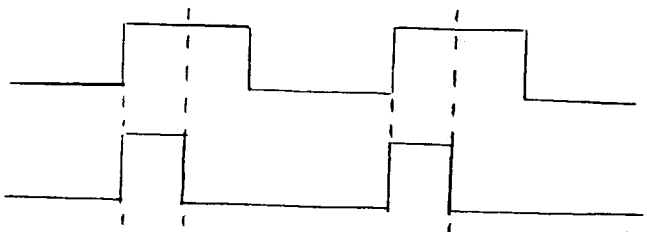
Since $I_1 = I_2 = I$, we have

$$\frac{V_A - V_x}{R} = \frac{V_x - V_B}{R} \Rightarrow V_x = \frac{V_A + V_B}{2} = \frac{V_{+peak} + V_{-peak}}{2}$$

Problem 19.11

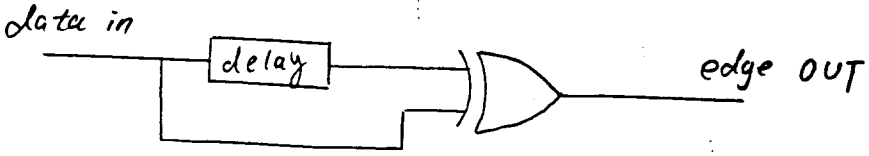
Mono-stable (one-shot) circuit can be used for implementing return to zero data format, as shown below:



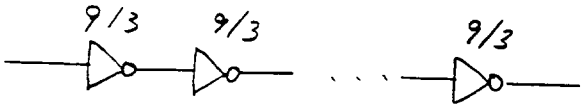


The pulse width of the mon-stable circuit is adjusted to be half of the data width.

Problem 19.12



The key point in the design of edge dectector is designing of the delay element. Assume we use invertor chain for delay element and we use the equal-drive size, that is, $3\mu m/2\mu m$ for N-channel, and $9\mu m/2\mu m$ for p-channel.



The total propagation delay $t_{TOT} = N \times [R_n (C_{out} + C_{IN})]$

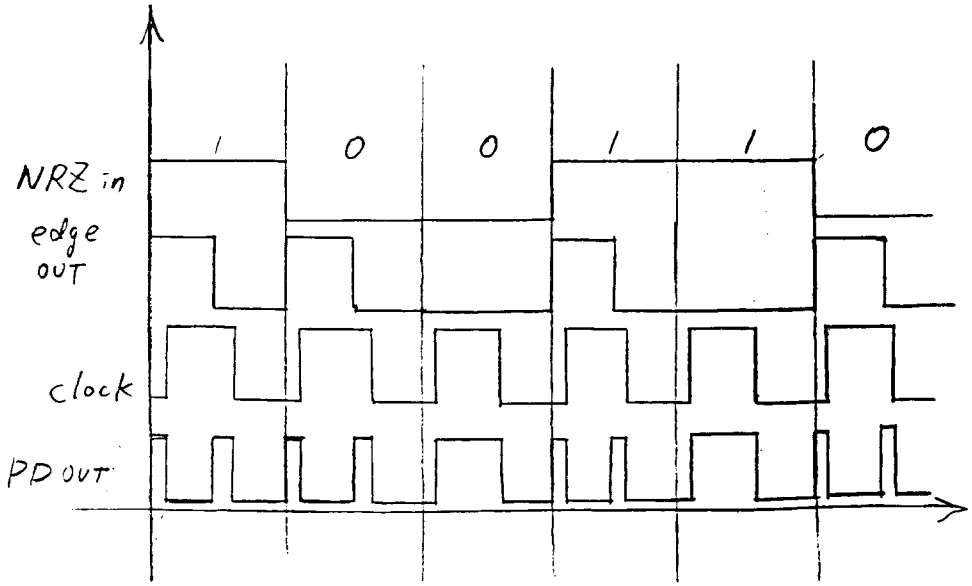
$$t_{TOT} = N \times \left[8k \times \frac{5}{2} \times C_{ox}' \times (3 \times 2\mu m^2 + 9 \times 2\mu m^2) \right] = 5\ nS$$

$$\Longrightarrow N \approx 13.02$$

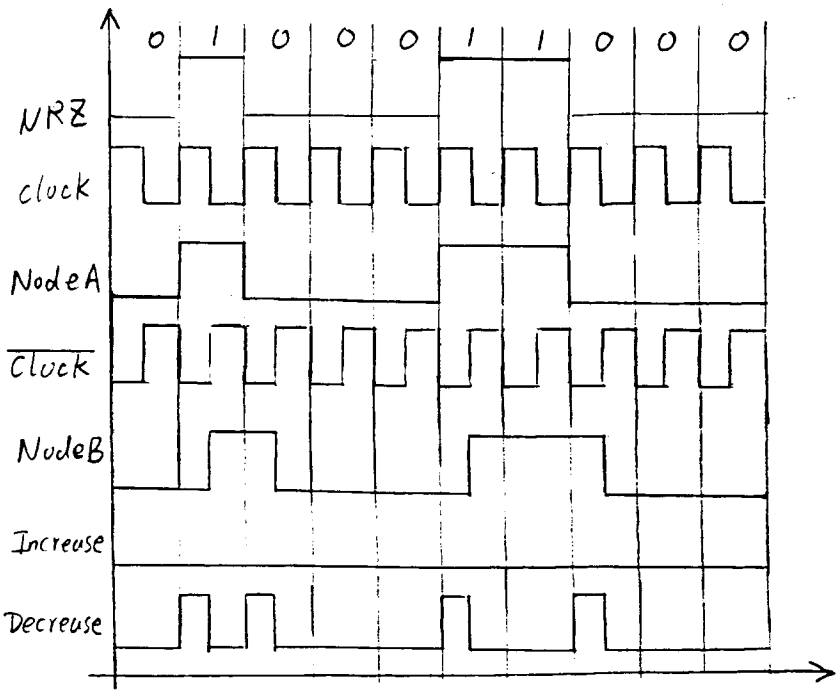
In order to keep the non-inverting function of the delay element, we choose $N = 12$. The resulting output width is approximately 4.6 nS.

Problem 19.13

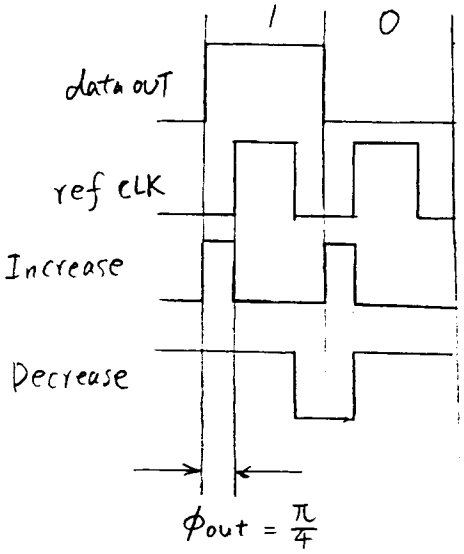
The optimum delay for using in an edge detector should be close to one-half of the bit-interval time.



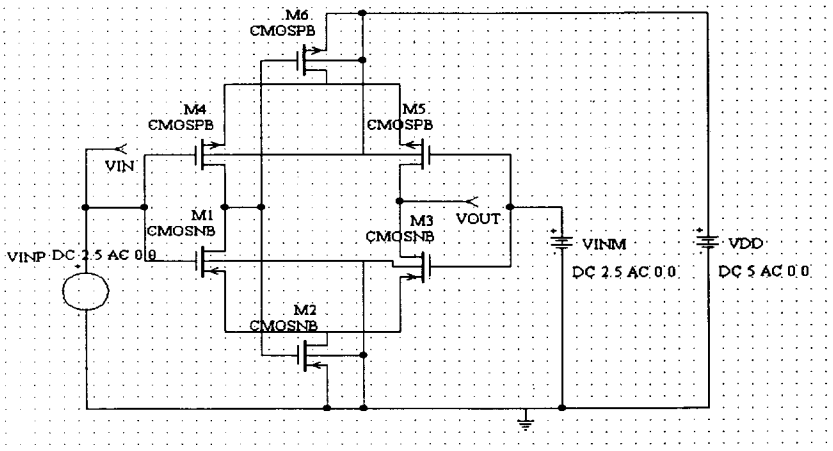
Problem 19.14



Problem 19.15



Problem 19.16




```
*** Top Level Netlist ***
M1      1 VIN 3 0 CMOSNB  L=2u W=10u
M2      3 1 0 0 CMOSNB  L=2u W=10u
M3      VOUT 10 3 0 CMOSNB  L=2u W=10u
M4      1 VIN 15 16 CMOSPB  L=2u W=30u
M5      VOUT 10 15 16 CMOSPB  L=2u W=30u
M6      15 1 16 16 CMOSPB  L=2u W=30u
VDD     16 0    DC 5 AC 0 0
VINM    10 0    DC 2.5 AC 0 0
VINP    VIN 0   DC 2.5 AC 0 0

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=5mv
.DC VINP 0 5 0.1
.end
```