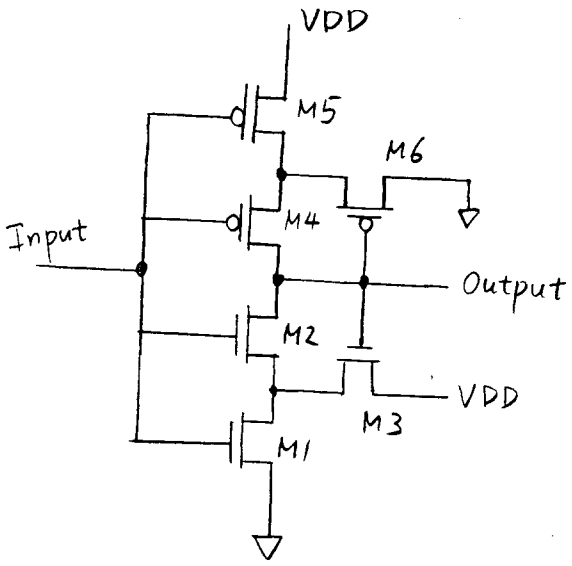
Chapter 18

Problem 18.1



$$\frac{\beta_1}{\beta_3} = \left[\frac{V_{DD} - V_{SPH}}{V_{SPH} - V_{THN}}\right]^2 = \left[\frac{5-3}{3-0.83}\right]^2 = 0.85$$

$$\frac{\beta_5}{\beta_6} = \left[\frac{V_{SPL}}{V_{DD} - V_{SPL} - V_{THP}}\right]^2 = \left[\frac{2.5}{5-2.5-0.91}\right]^2 = 2.47$$

$$\Rightarrow \begin{cases} \frac{W_1}{L_1} = \frac{W_6}{L_6} = \frac{3\,\mu m}{3\,\mu m} \\ \frac{W_3}{L_3} = \frac{7\,\mu m}{6\,\mu m}, \quad \frac{W_5}{L_5} = \frac{5\,\mu m}{2\,\mu m} \end{cases}$$

Also, $\beta_2 > 5\beta_1$ and $5\beta_3 \Rightarrow \frac{W_2}{L_2} = \frac{10\,\mu m}{2\,\mu m}$

$\beta_4 > 5\beta_5$ and $5\beta_6 \Rightarrow \frac{W_4}{L_4} = \frac{25\,\mu m}{2\,\mu m}$.

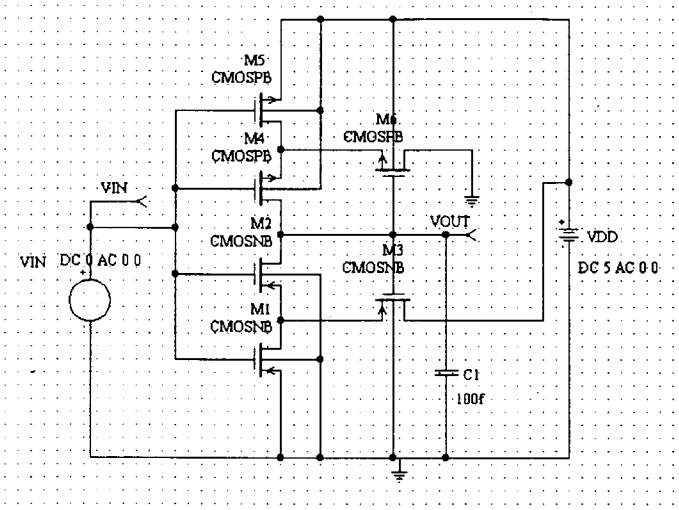
See next page for SPICE simulations.

Problem 18.2

$$t_{PHL} \approx (R_{n1} + R_{n2}) \cdot C_{load}$$
$$= \left(12k \times \frac{3}{3} + 12k \times \frac{2}{10}\right) \times 100fF = 1.44\,nS.$$

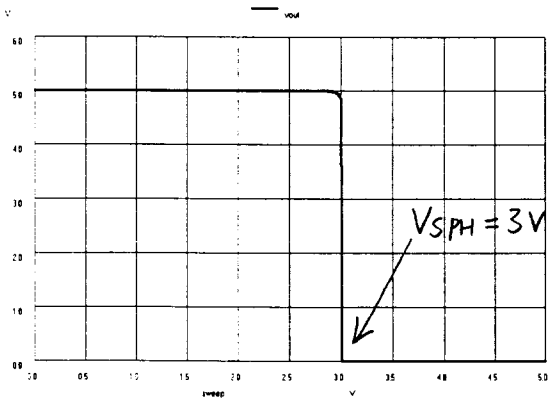
$$t_{PLH} \approx (R_{p4} + R_{p5}) \cdot C_{load}$$
$$= \left(36k \times \frac{3}{3} + 36k \times \frac{2}{10}\right) \times 100fF = 4.32\,nS$$

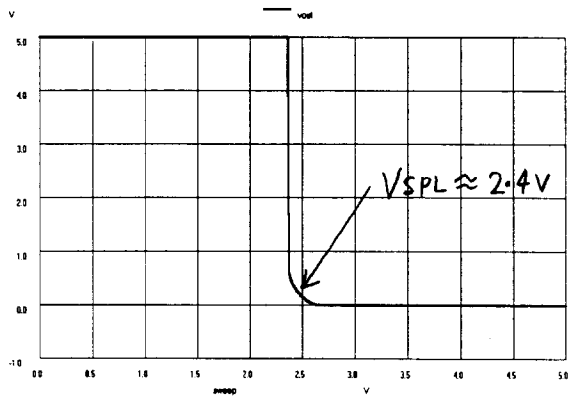
Problem 18.1 (Simulation)



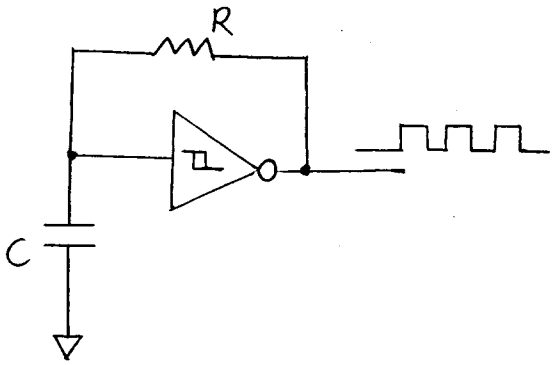

```
*** Top Level Netlist ***
C1        0 VOUT 100f
M1        1 VIN 0 0 CMOSNB  L=3u W=3u
M2        VOUT VIN 1 0 CMOSNB  L=2u W=10u
M3        12 VOUT 1 0 CMOSNB  L=6u W=7u
M4        VOUT VIN 11 12 CMOSPB  L=2u W=25u
M5        11 VIN 12 12 CMOSPB  L=2u W=5u
M6        0 VOUT 11 12 CMOSPB  L=3u W=3u
VDD       12 0     DC 5 AC 0 0
VIN       VIN 0   DC 0 AC 0 0

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=5mv
.DC VIN 0 5 0.01
.end
```

The SPICE simulation is shown below:





Problem 18.3



$$f_{osc} = \frac{1}{t_1 + t_2} = 10\,MHz \Rightarrow t_1 + t_2 = 100\,ns$$

Using the Schmitt trigger of Ex 18.11, $V_{SPL} = 2V$, $V_{SPH} = 3V$

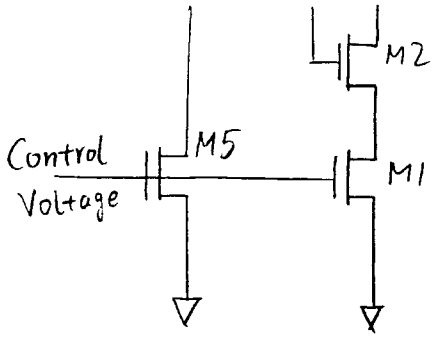
$$t_1 = RC \ln \frac{V_{SPH}}{V_{SPL}}, \quad t_2 = RC \ln \frac{V_{DD} - V_{SPL}}{V_{DD} - V_{SPH}}$$

$$\therefore 100ns = RC\left[\ln \frac{3V}{2V} + \ln \frac{5-2V}{5-3V}\right] \Rightarrow \underline{RC = 123.3ns}$$

We can set $R = 100k$ and $C = 1.2pF$.

See next page for SPICE simulation.

Problem 18.4

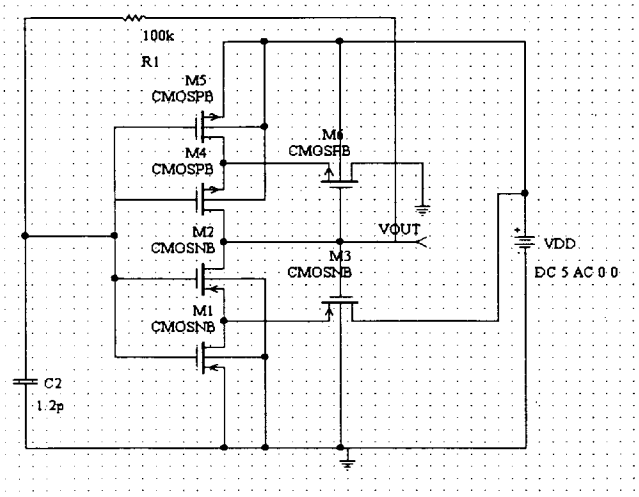


The total input capacitance on the control voltage input for VCO is,

$$C_{TOT} = C_{inn5} + C_{inn1}$$

$$= \frac{3}{2} C_{ox}' (W_5 L_5 + W_1 L_1)$$

Problem 18.3 (Simulation)

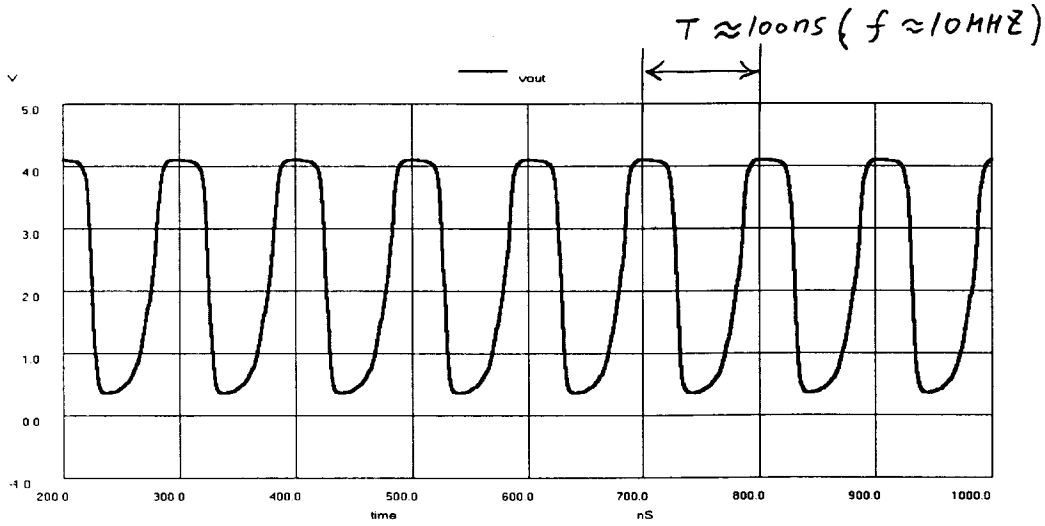


*** Top Level Netlist ***
C2 2 0 1.2p
M1 1 2 0 0 CMOSNB L=3u W=3u
M2 VOUT 2 1 0 CMOSNB L=2u W=10u
M3 12 VOUT 1 0 CMOSNB L=6u W=7u
M4 VOUT 2 11 12 CMOSPB L=2u W=10u
M5 11 2 12 12 CMOSPB L=3u W=3u
M6 0 VOUT 11 12 CMOSPB L=11u W=12u
R1 2 VOUT 100k
VDD 12 0 DC 5 AC 0 0

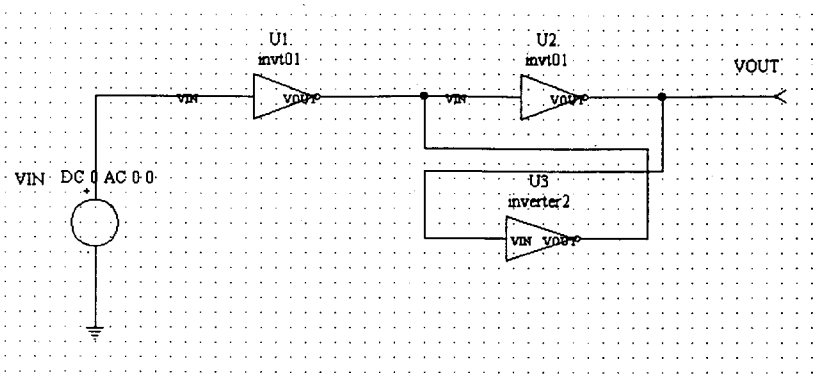
***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=5mv
.tran 1n 1000n 0 1n uic
.end

The SPICE simulation is shown below:



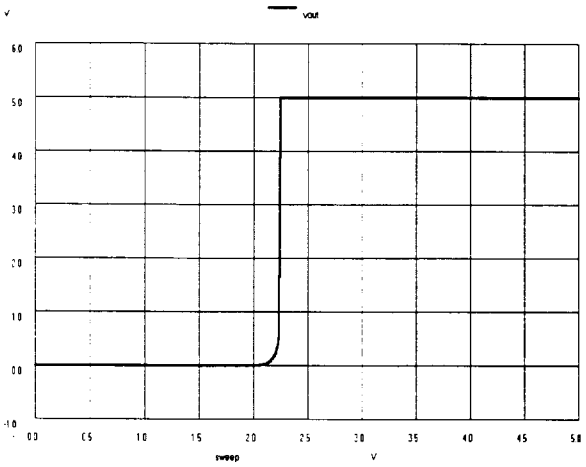
Problem 18.5

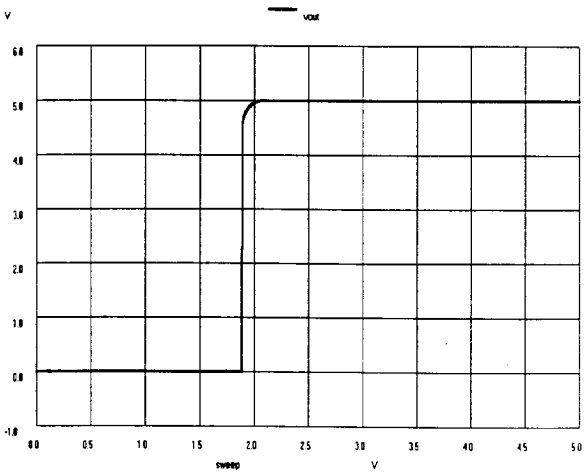



```
.subckt invt01.sub 4 1
M1      1 4 0 0 CMOSNB  L=2u W=3u
M2      1 4 3 3 CMOSPB  L=2u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt01.sub

.subckt invt02.sub 4 1
M1      1 4 0 0 CMOSNB  L=15u W=3u
M2      1 4 3 3 CMOSPB  L=15u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt02.sub

*** Top Level Netlist ***
XU1     1 2     invt01.sub
XU2     2 VOUT          invt01.sub
XU3     VOUT 2          invt02.sub
VIN     1 0     DC 0 AC 0 0

***** Spice models and macro models *****

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=5mv
.DC VIN 0 5 0.01
.end
```

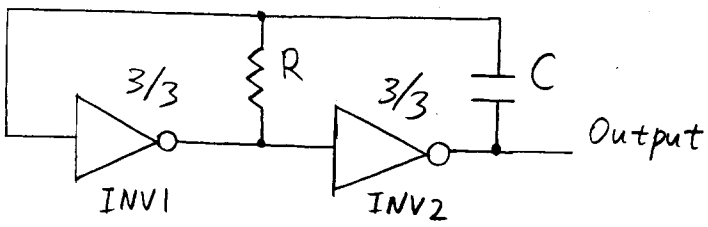
Simulation results:
$V_{SPH} \approx 2.2V$
$V_{SPL} \approx 1.8V$

The SPICE simulation is shown below:





Problem 18.6



Since the minimum-size inverters are used, the V_{sp} of the inverters is about 2V.

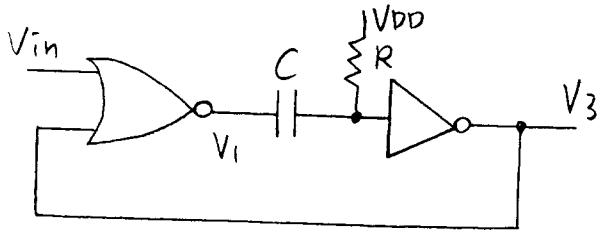
$$t_1 = t_2 = RC \cdot \ln \frac{V_{DD} + V_{SP1}}{V_{SP1}} \simeq 1.25\,RC$$

$$f_{osc} = \frac{1}{t_1 + t_2} = \frac{1}{2.5\,RC} = 20MHz$$

$$\Longrightarrow \underline{\underline{RC = 20 \times 10^{-9}\ (s)}}$$

If we choose $R = 1k$, then $C = 20pF$.

Problem 18.7



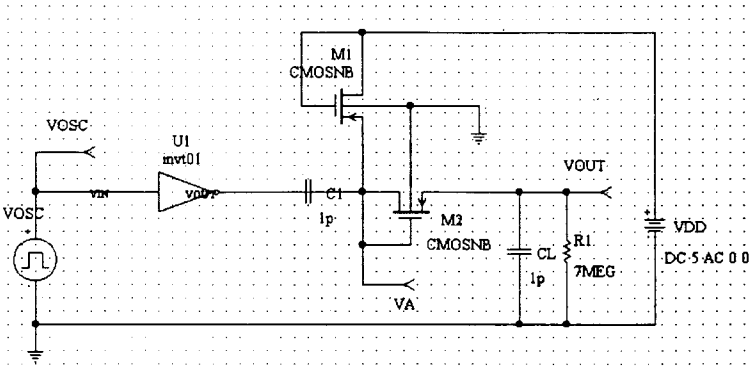
For NOR gate, we use minimum size devices, and for inverter, equal-drive size is used, that is, N-channel: 3μm/2μm, P-Channel: 9μm/2μm. (V_{sp} of the inverter is $V_{DD}/2$)

The pulse width of the one-shot circuit is:

$$t = RC \ln \frac{V_{DD}}{V_{DD} - V_{SP}} \approx 0.7RC,\quad t = 100nS \Longrightarrow RC = 143 \times 10^{-9}(s)$$

set $R = 100k$ and $C = 1.4pF$.

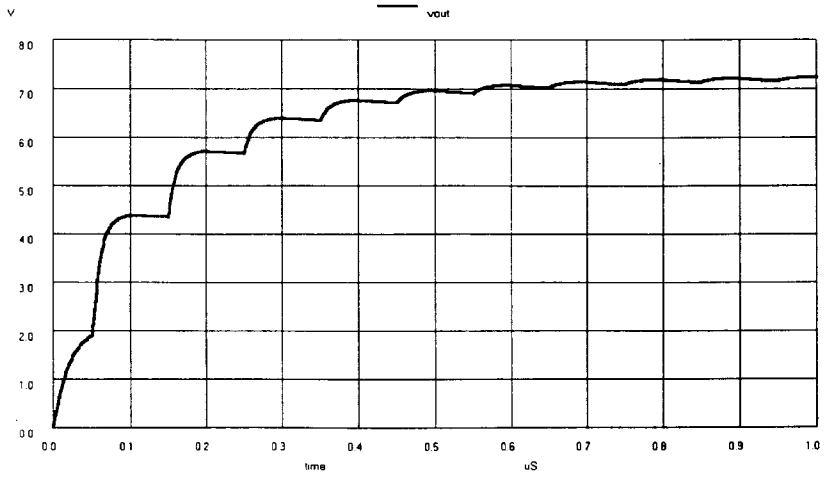
Problem 18.9



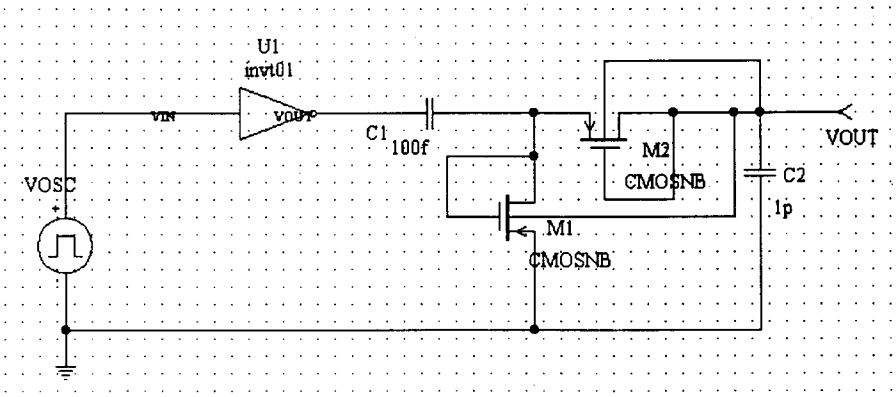

```
.subckt invt01.sub 4 1
M1      1 4 0 0 CMOSNB  L=2u W=3u
M2      1 4 3 3 CMOSPB  L=2u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt01.sub

*** Top Level Netlist ***
C1      VA 2 1p
CL      0 VOUT 1p  IC=0
M1      6 6 VA 0 CMOSNB  L=2u W=9u
M2      VA VA VOUT 0 CMOSNB  L=2u W=9u
R1      VOUT 0 7MEG
XU1     VOSC 2          invt01.sub
VDD     6 0     DC 5 AC 0 0
VOSC    VOSC 0          DC 0 AC 0 0 PULSE(0 5 0 0.1n 0.1n 50n 100n)

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
.tran 1n 1000n 0 1n uic
.end
```

Note the size of M1 and M2 is increased to 9μ/2μ for driving DC load.

The SPICE simulation is shown below:

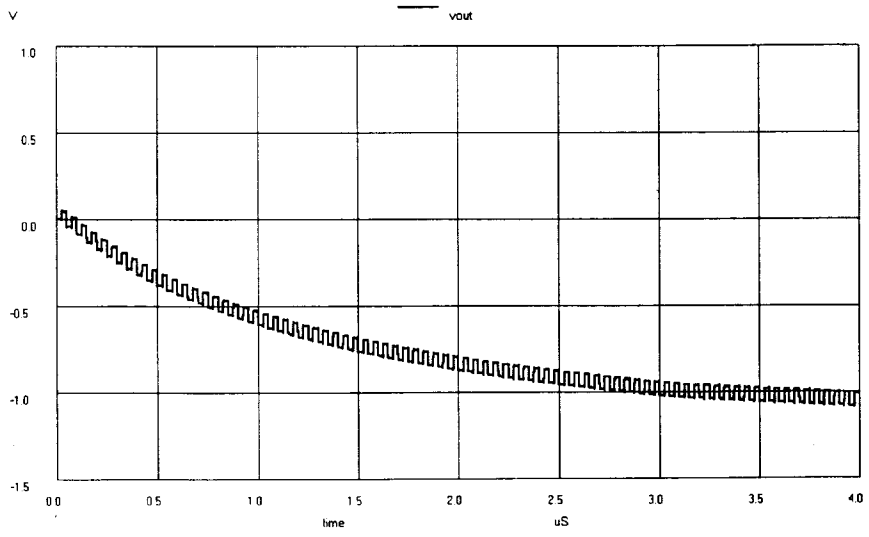


Problem 18.10




```
.subckt invt01.sub 4 1
M1      1 4 0 0 CMOSNB  L=2u W=3u
M2      1 4 3 3 CMOSPB  L=2u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt01.sub

*** Top Level Netlist ***
C1      2 5 100f
C2      0 VOUT 1p
M1      5 5 0 VOUT CMOSNB  L=30u W=3u
M2      VOUT VOUT 5 VOUT CMOSNB  L=30u W=3u
XU1     1 2     invt01.sub
VOSC    1 0     DC 0 AC 0 0 PULSE(0 5 0 0.1ns 0.1ns 25n 50n)

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=1mv
.tran 5n 4000n 0 5n uic
.end
```

The SPICE simulation is shown below:



Problem 18.11

The circuit in this problem is different than the multiplier of Fig 18.18 in that it has feedback connection from capacitors (C_2, C_3 ...) to the gates of N-MOSFETs of their previous stages. Since the voltages of these capacitors are about two times than those drain voltages of MOSFETs of their previous stages, the capacitors will be charged to VDD, 2VDD, 3VDD instead of $V_{DD} - V_{THN}$, $2V_{DD} - 2V_{THN}$, $3V_{DD} - 3V_{THN}$, i.e., without threshold voltage drop. Therefore, this circuit is more efficient than the one of Fig 18.18 of the text.