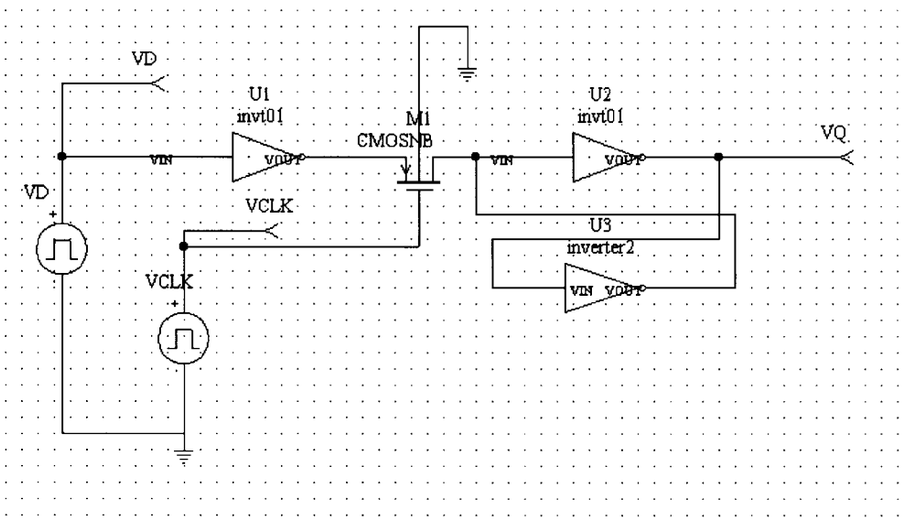
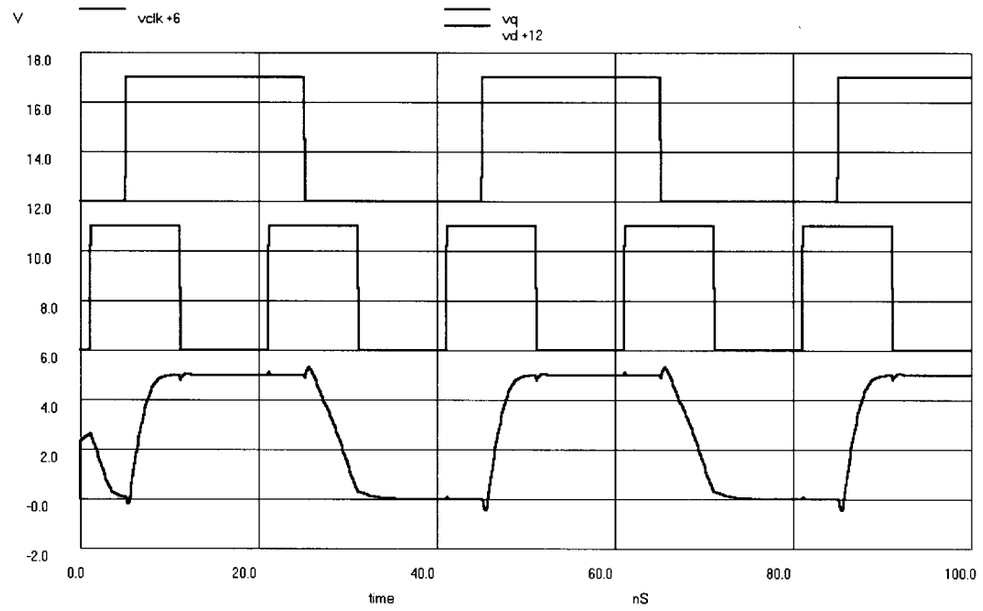
Chapter 15

Problem 15.7

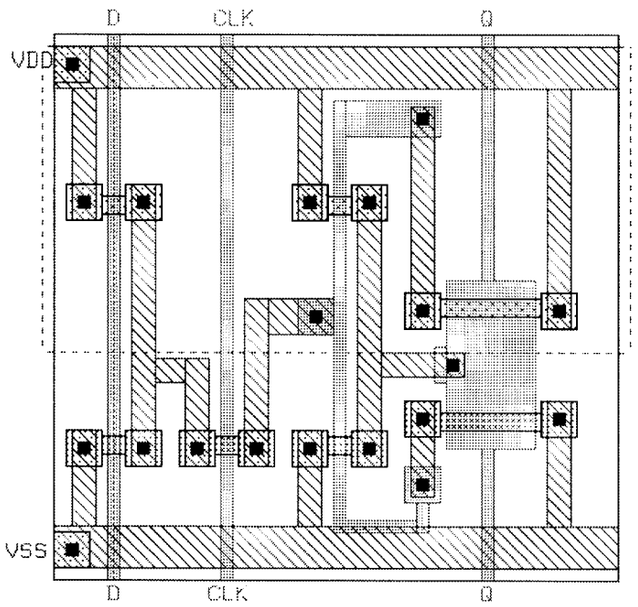



```
.subckt invt01.sub 4 1
M1      1 4 0 0 CMOSNB  L=2u W=3u
M2      1 4 3 3 CMOSPB  L=2u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt01.sub

.subckt invt02.sub 4 1
M1      1 4 0 0 CMOSNB  L=15u W=3u
M2      1 4 3 3 CMOSPB  L=15u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt02.sub

*** Top Level Netlist ***
M1      5 VCLK 2 0 CMOSNB  L=2u W=3u
XU1     VD 2    invt01.sub
XU2     5 VQ    invt01.sub
XU3     VQ 5    invt02.sub
VCLK    VCLK 0          DC 0 AC 0 0 PULSE(0 5 1n 0.1n 0.1n 10n 20n)
VD      VD 0    DC 0 AC 0 0 PULSE(0 5 5n 0.1n 0.1n 20n 40n)

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=5mv
.tran 0.1n 100n 0 0.1n uic
.end
```

The SPICE simulation is shown below:

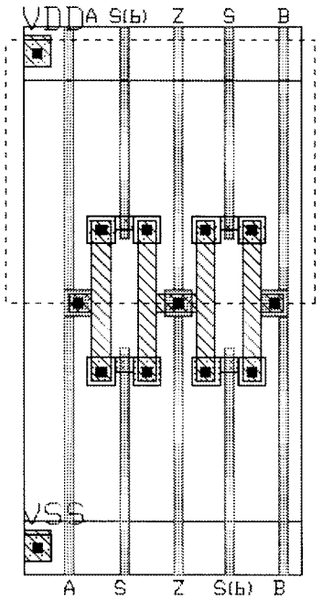


The layout of the D-FF is as following:



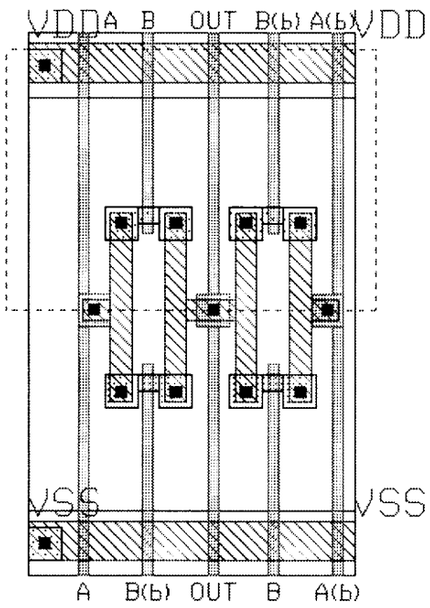
Problem 15.8

The layout of the two-input MUX is shown below:

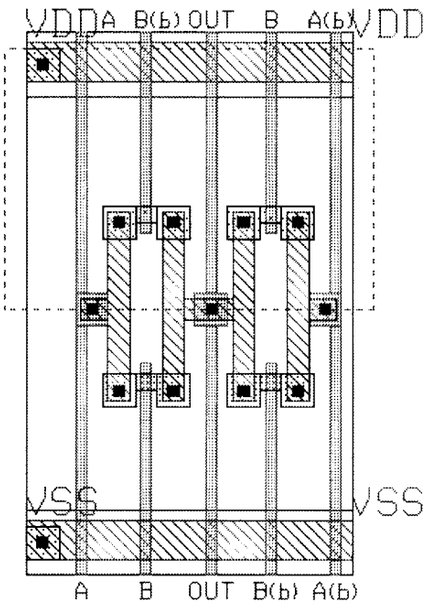


Problem 15.9

The layout of XOR/XNOR using reduced standard-cell frame height is shown below:



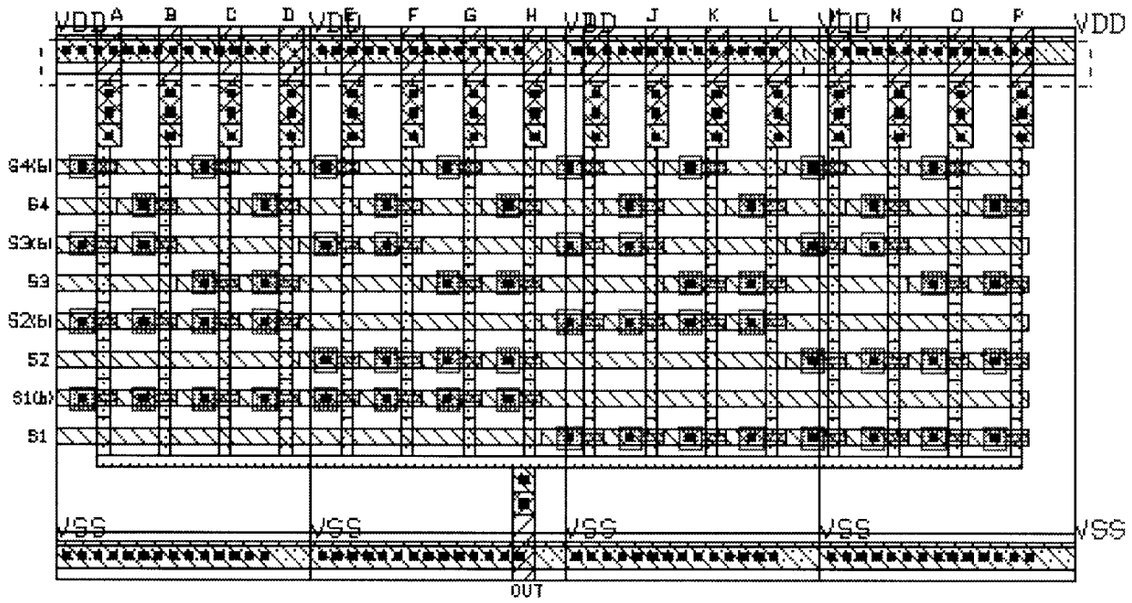
XOR



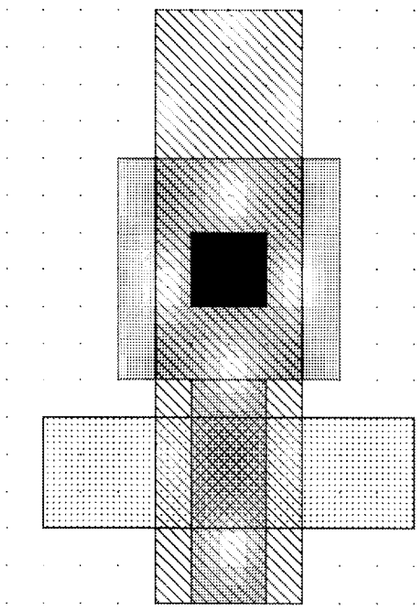
XNOR

Problem 15.10

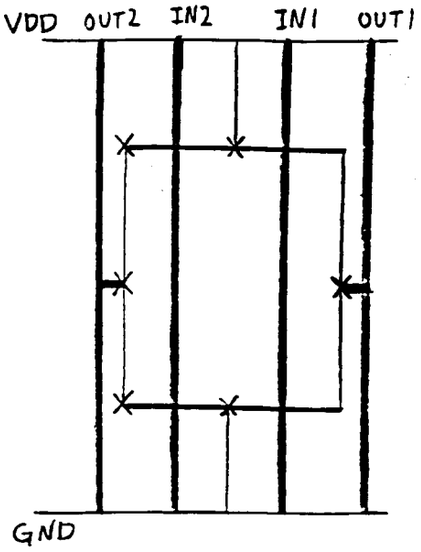
The layout of a 16-to-1 MUX/DEMUX is shown below:



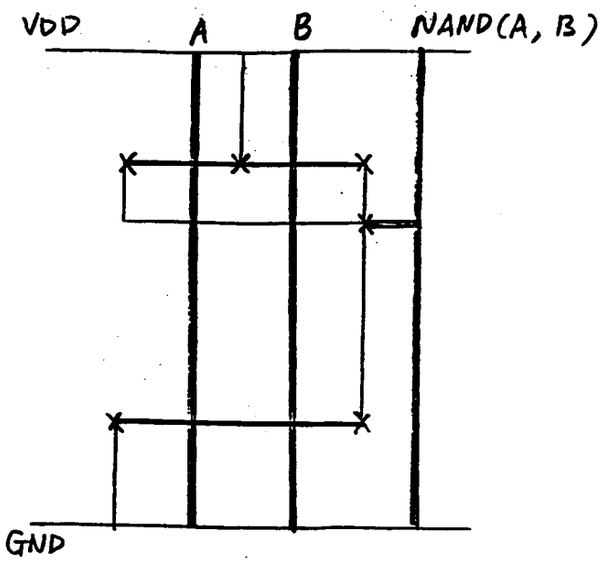
Cell used to make the MUX/DEMUX:



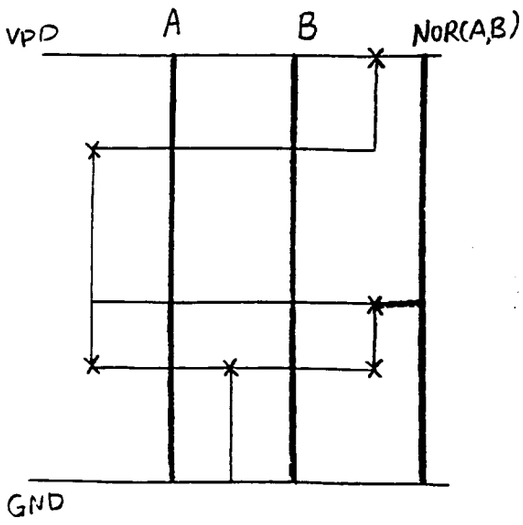
Problem15.11



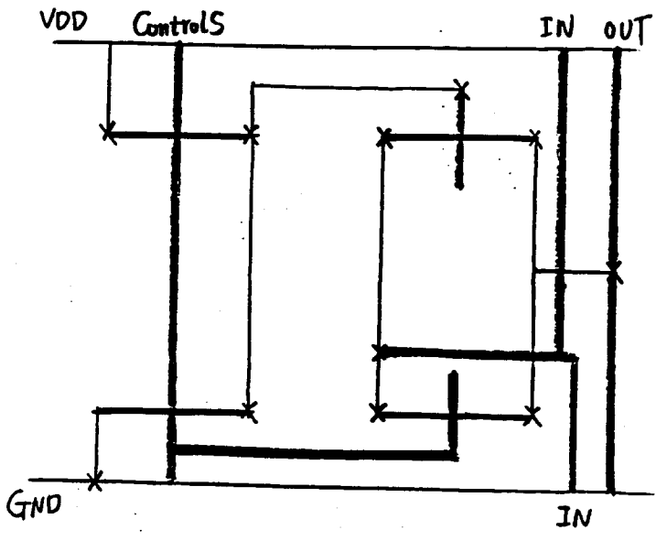
(a)



(b)

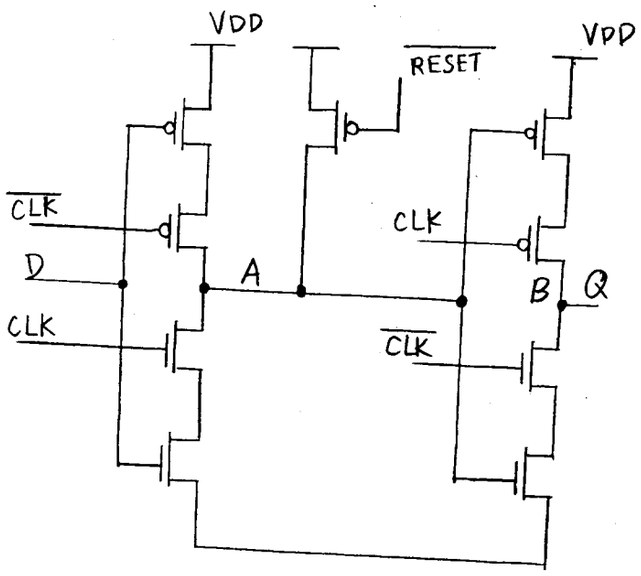


(c)



(d)

Problem 15.12.



Node A and Node B are high-impedance nodes. When laying out a circuit with high-impedance node, we should try to make the parasic capacitance of these nodes as small as possible to keep the speed of the circuit from going too low.

Problem 15.13

The reasons why we want small layout size are:

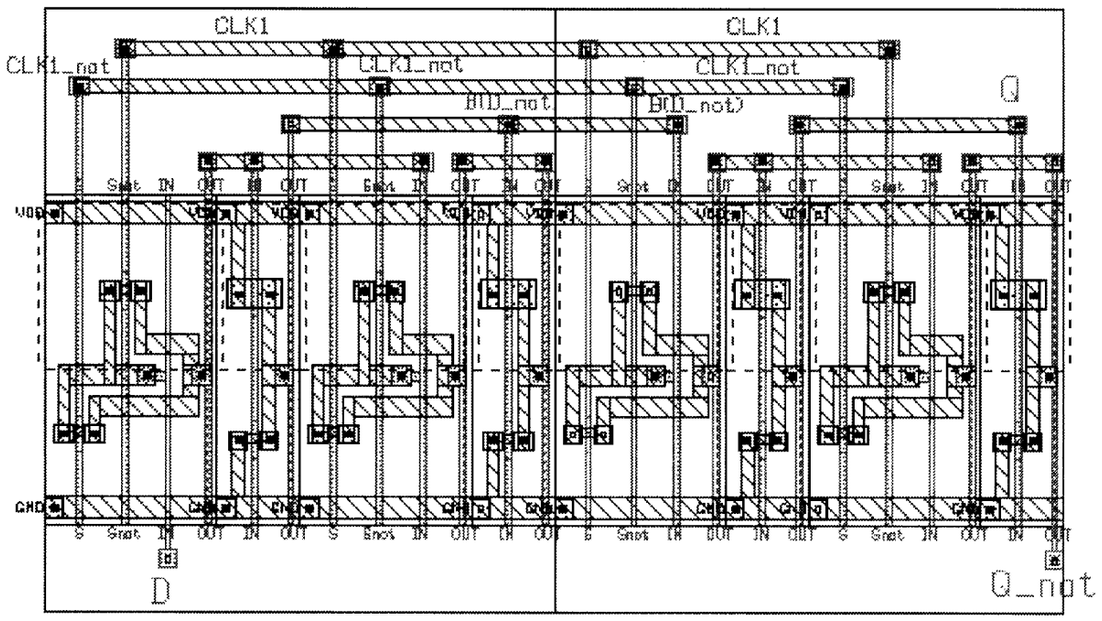
(1) The yield (number of good die / total number of die on wafer) is increased with smaller die size. The result is more die/wafer available for sale.

(2) Increasing the number of die on a wafer decreases the cost per die, since the processing costs per wafer are constant, whether it is blank or as tightly packed with circuitry as possible.

(3) From technical point, smaller layout size results in shorter interconnecting wires, thereby reducing parasitic loading and crosstalk effects.

Problem 15.14

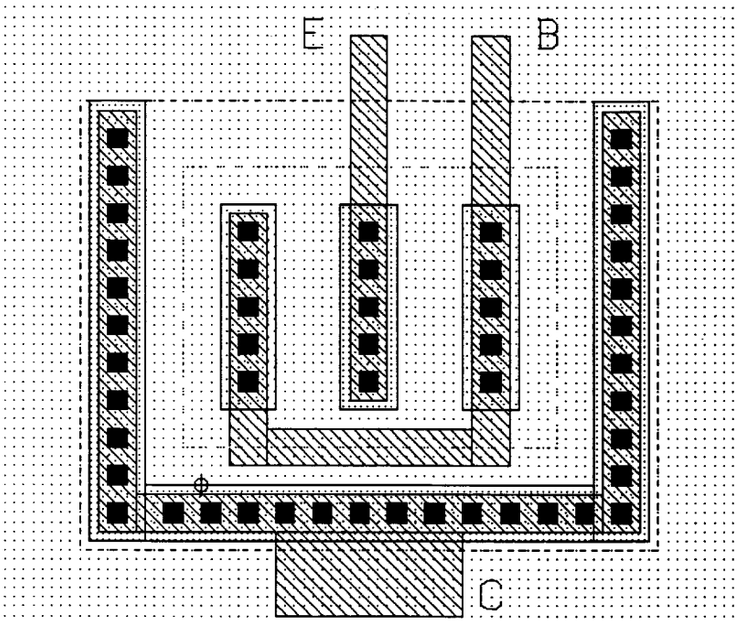
The layout of the D-FF is shown below:



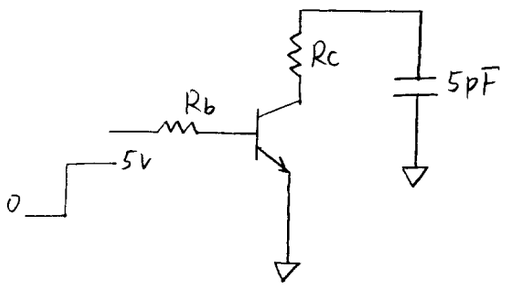
Chapter 16

Problem 16.1

The layout of a lateral 5 X 1 NPN BJT is shown below:



Problem 16.2

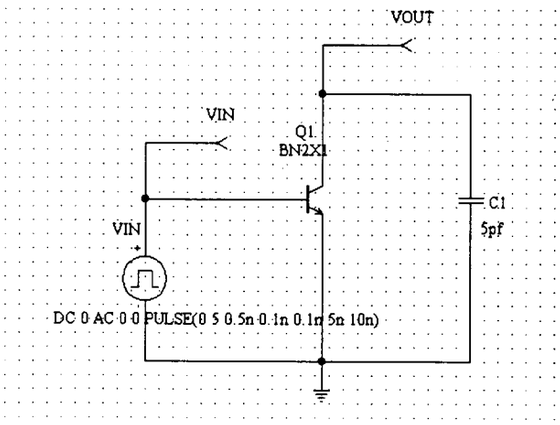


For a 5×1 BJT, $A = 2.5$

$$R_{npn} = \frac{R_C}{A} = \frac{420\Omega}{2.5} = 168\Omega$$

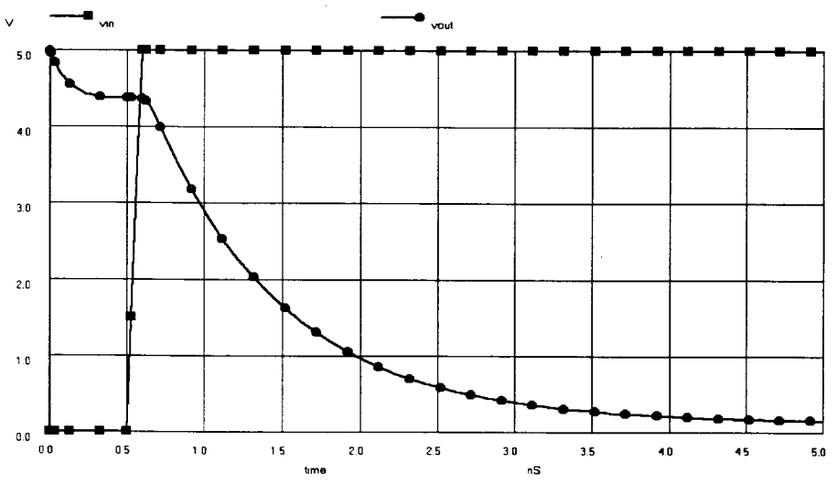
$$t_{PHL} = R_{npn} \cdot C_{Load} = 168\Omega \times 5pF = \underline{0.84nS}$$

Problem 16.2 (Simulation)




```
*** Top Level Netlist ***
C1        0 VOUT 5pf  IC=5
Q1        VOUT VIN 0 BN2X1  2.5
VIN       VIN 0   DC 0 AC 0 0 PULSE(0 5 0.5n 0.1n 0.1n 5n 10n)

***** Spice models and macro models *****
.MODEL BN2X1 NPN
+ BF=82 IS=1.588E-16 NF=9.9563E-01 NE=1.3356 VAF=57.1
+ IKF=2.3067E-02 ISE=1.267E-16 RE=12.7 RC=420.00 RB=1.213E+03
+ RBM=7.53 ISC=3.363E-15 NC=1.0202
+ CJE=0.1952E-12 MJE=0.5050 VJE=0.85 CJC=0.18815E-12 MJC=0.4990 VJC=0.80
+ CJS=0.2326E-12 MJS=0.2033 VJS=0.70
***** End of spice models and macro models *****

.OPTION ABSTOL=1m RELTOL=0.1 VNTOL=100mv
.tran 0.1n 5n 0 0.1n uic
.end
```

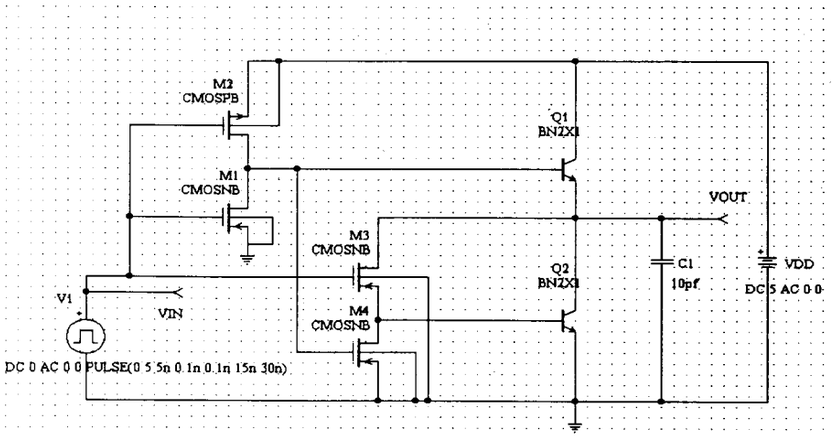
The SPICE simulation is shown below:



Simulation result:

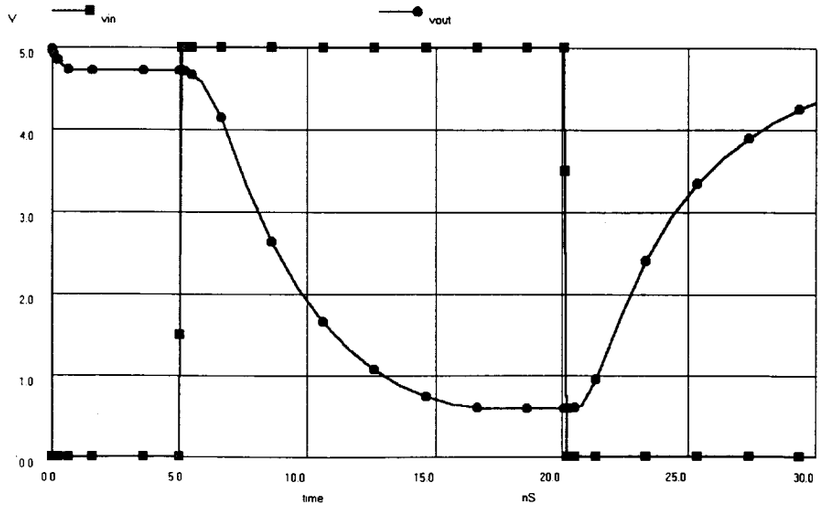
$T_{PHL} \approx 0.62nS$

Problem 16.3




```
*** Top Level Netlist ***
C1      0 VOUT 10pf  IC=-5
M1      4 VIN 0 0 CMOSNB  L=2u W=10u
M2      4 VIN 10 10 CMOSPB  L=2u W=16u
M3      VOUT VIN 18 0 CMOSNB  L=2u W=10u
M4      18 4 0 0 CMOSNB  L=2u W=10u
Q1      10 4 VOUT BN2X1
Q2      VOUT 18 0 BN2X1
V1      VIN 0   DC 0 AC 0 0 PULSE(0 5 5n 0.1n 0.1n 15n 30n)
VDD     10 0    DC 5 AC 0 0

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4
.MODEL BN2X1 NPN

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=1mv
.tran 1n 30n 0 1n uic
.end
```

The SPICE simulation is shown below:

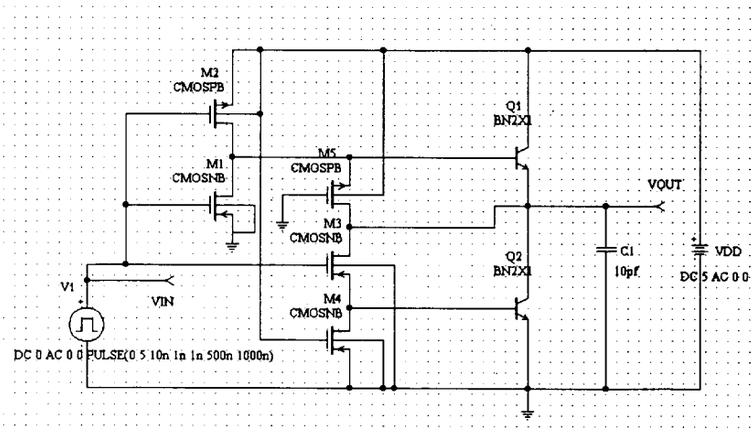


Simulation results:

$T_{PHL} \approx 3.8$ nS

$T_{PLH} \approx 3.5$ nS

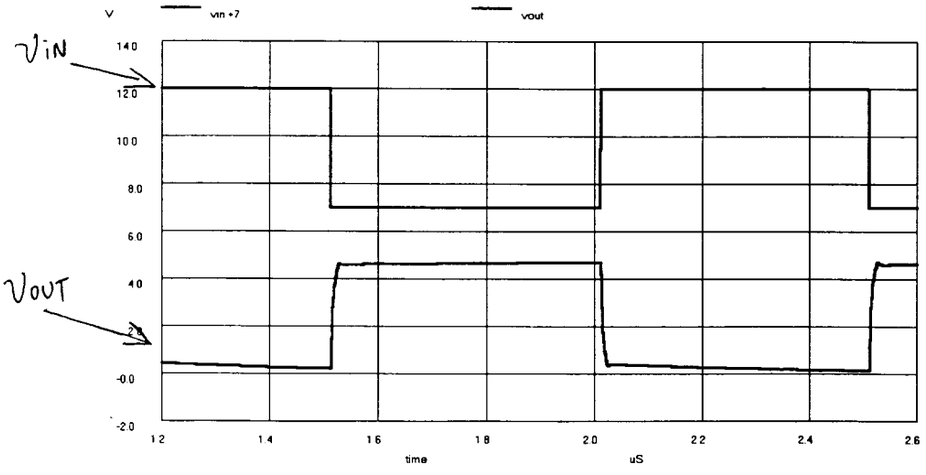
Problem 16.4



*** Top Level Netlist ***

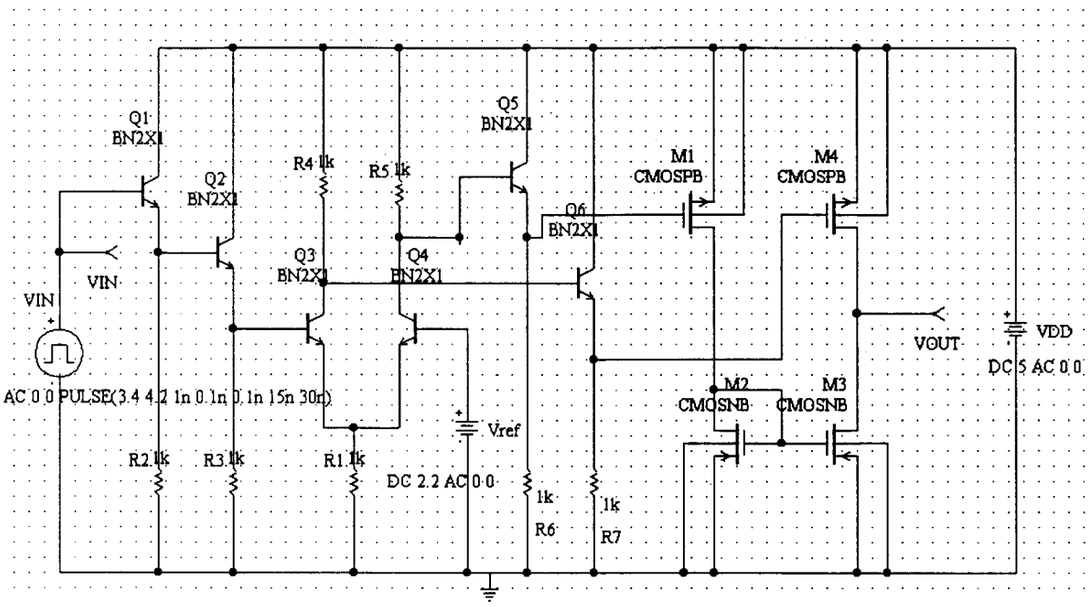
```
C1      0 VOUT 10pf  IC=-5
M1      6 VIN 0 0 CMOSNB  L=2u W=10u
M2      6 VIN 1 1 CMOSPB  L=2u W=16u
M3      VOUT VIN 5 0 CMOSNB  L=2u W=10u
M4      5 1 0 0 CMOSNB  L=20u W=3u
M5      VOUT 0 6 1 CMOSPB  L=20u W=3u
Q1      1 6 VOUT BN2X1
Q2      VOUT 5 0 BN2X1
V1      VIN 0   DC 0 AC 0 0 PULSE(0 5 10n 1n 1n 500n 1000n)
VDD     1 0     DC 5 AC 0 0

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4
.MODEL BN2X1 NPN

***** End of spice models and macro models *****
.OPTION ABSTOL=1m RELTOL=0.1 VNTOL=10mv
.tran 1n 1100n 0 1n uic
.end
```

The SPICE simulation is shown below:



Simulation result:
$t_{PHL} + t_{PLH} \approx 5.5\,ns$

Problem 16.5



*** Top Level Netlist ***

M1	19 15 1 1 CMOSPB L=2u W=3u
M2	19 19 0 0 CMOSNB L=2u W=3u
M3	VOUT 19 0 0 CMOSNB L=2u W=3u
M4	VOUT 18 1 1 CMOSPB L=2u W=3u
Q1	1 VIN 3 BN2X1
Q2	1 3 6 BN2X1
Q3	7 6 9 BN2X1
Q4	10 11 9 BN2X1
Q5	1 10 15 BN2X1
Q6	1 7 18 BN2X1
R1	0 9 1k
R2	0 3 1k
R3	0 6 1k
R4	7 1 1k
R5	10 1 1k
R6	0 15 1k
R7	0 18 1k
VDD	1 0 DC 5 AC 0 0
VIN	VIN 0 DC 0 AC 0 0 PULSE(3.4 4.2 1n 0.1n 0.1n 15n 30n)
Vref	11 0 DC 2.2 AC 0 0

***** Spice models and macro models *****

.MODEL BN2X1 NPN

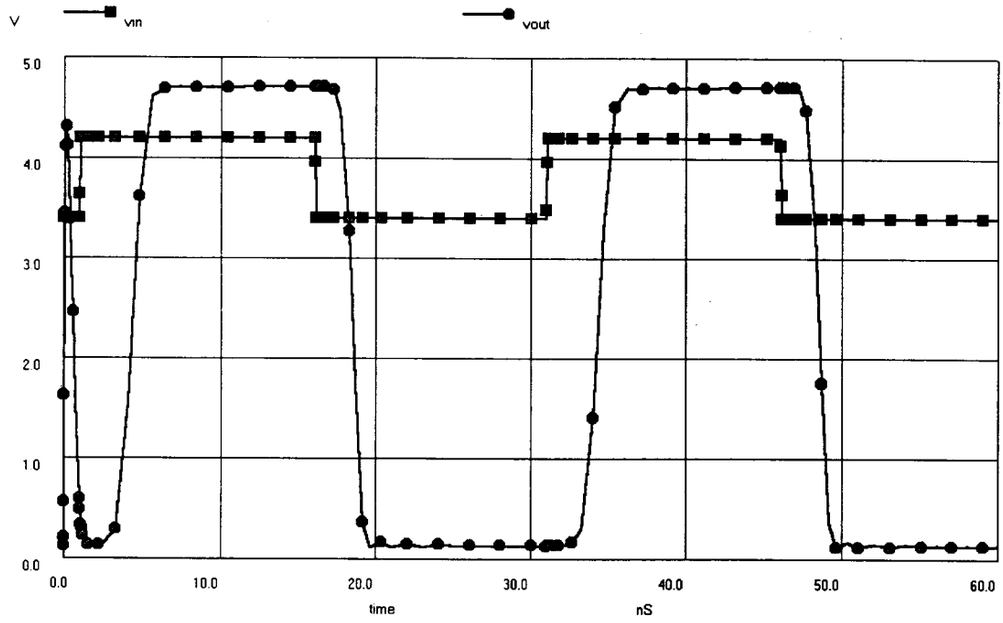
.MODEL CMOSPB PMOS LEVEL=4

.MODEL CMOSNB NMOS LEVEL=4

***** End of spice models and macro models *****

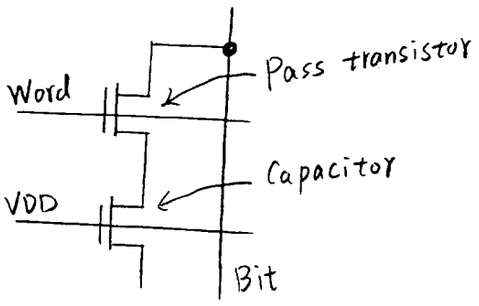
.tran 1n 60n 0 1n uic
.end

The SPICE simulation is shown below:



Chapter 17

Problem 17.1



The capacitance that the pass transistor contributes to the word line is:

$$C_p = \frac{3}{2} C_{ox}' \times W_p \times L_p = \frac{3}{2} \times 800 \frac{aF}{\mu m^2} \times 3 \times 2 \mu m^2$$

$$= 7.2 fF$$

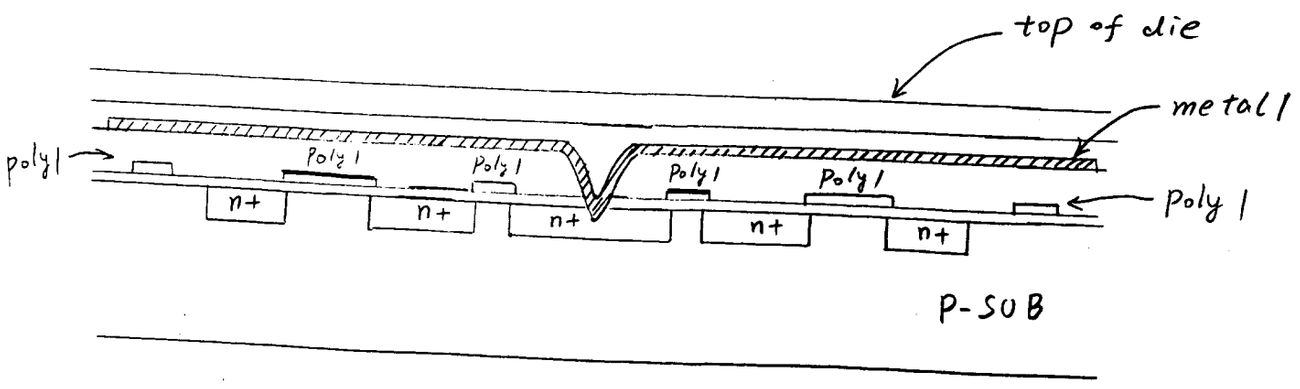
Problem 17.2

See next page for SPICE simulations.

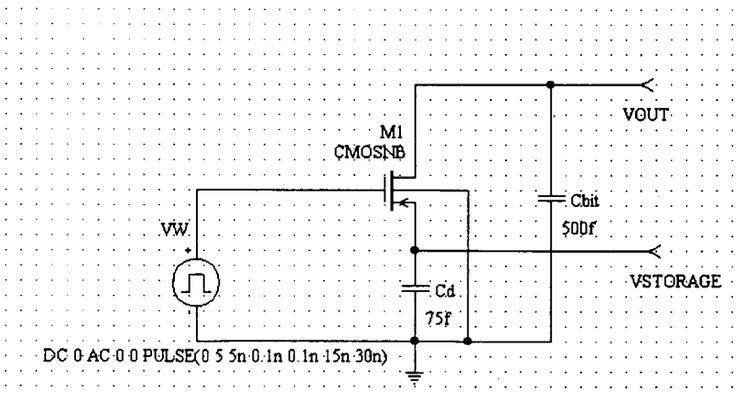
Problem 17.3

Poly 1 is used in CN20 process for word lines. Metal 1 is used for bit lines. We can not use metal 1 for word lines because word lines and bit lines cross each other in the layout. If we could use metal 1 for word lines, however, the delay through the line will be significantly decreased due to smaller metal 1 to substrate capacitance and sheet resistance.

Problem 17.4



Problem 17.2



*** Top Level Netlist ***
Cbit 0 VOUT 500f IC=-2.5
Cd 0 VSTORAGE 75f IC=-4
M1 VOUT 2 VSTORAGE 0 CMOSNB
VW 2 0 DC 0 AC 0 0 PULSE(0 5 5n 0.1n 0.1n 15n 30n)

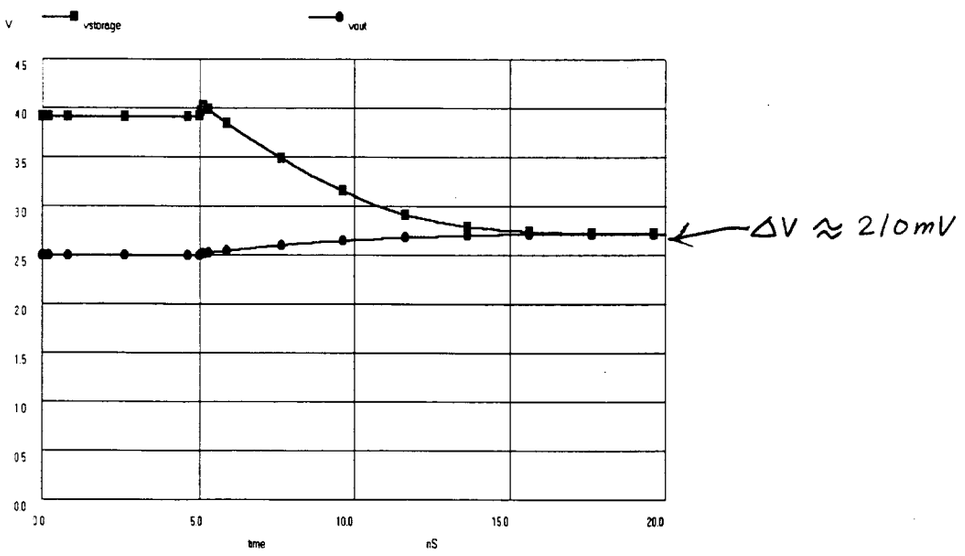
***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

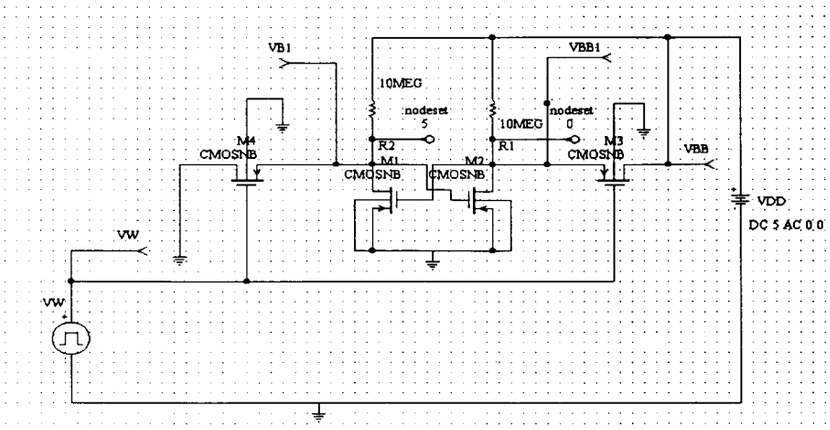
***** End of spice models and macro models *****

.tran 1n 20n 0 1n uic
.end

The SPICE simulation is shown below:



Problem 17.5

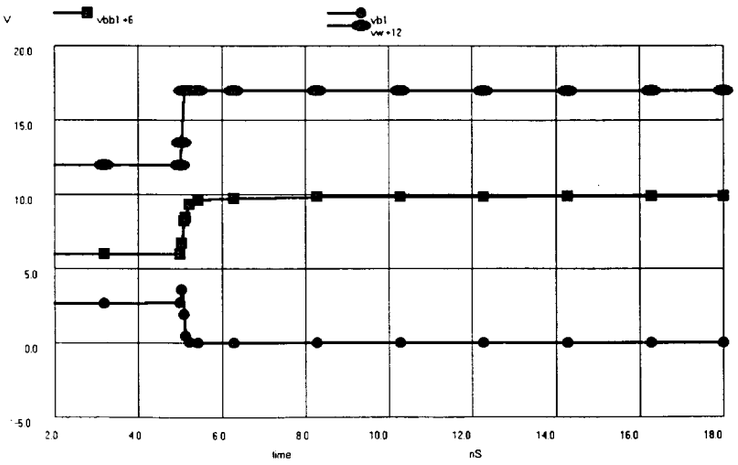


*** Top Level Netlist ***
.nodeset V(VBB1)=0
.nodeset V(VB1)=5
M1 VB1 VBB1 0 0 CMOSNB L=2u W=3u
M2 VBB1 VB1 0 0 CMOSNB L=2u W=3u OFF
M3 VBB VW VBB1 0 CMOSNB L=2u W=12u
M4 0 VW VB1 0 CMOSNB L=2u W=12u
R1 VBB1 VBB 10MEG
R2 VB1 VBB 10MEG
VDD VBB 0 DC 5 AC 0 0
VW VW 0 DC 0 AC 0 0 PULSE(0 5 5n 0.1n 0.1n 15n 30n)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

***** End of spice models and macro models *****
.OPTION RELTOL=0.01 VNTOL=1mv
.tran 1n 20n 0 1n uic
.end



Problem 17.6

For the correct operation of the sense amps, we must turn the two MOSFETs in Fig 17.9 on prior to a read operation, to set both bit lines (bit and $\overline{bit}$) to VDD/2. When row address decoder selects a word line, the corresponding bit line will slightly increase or decrease from VDD/2, depending on the data the memory cell has. This slight voltage change is detected by sen amps and set the bit line to high or low, according to the data stored in the memory cell. Equilibrating the bit line before read operation is very important since sense amp must discriminate less than 100mV voltage changes on the bit line.

Problem 17.7

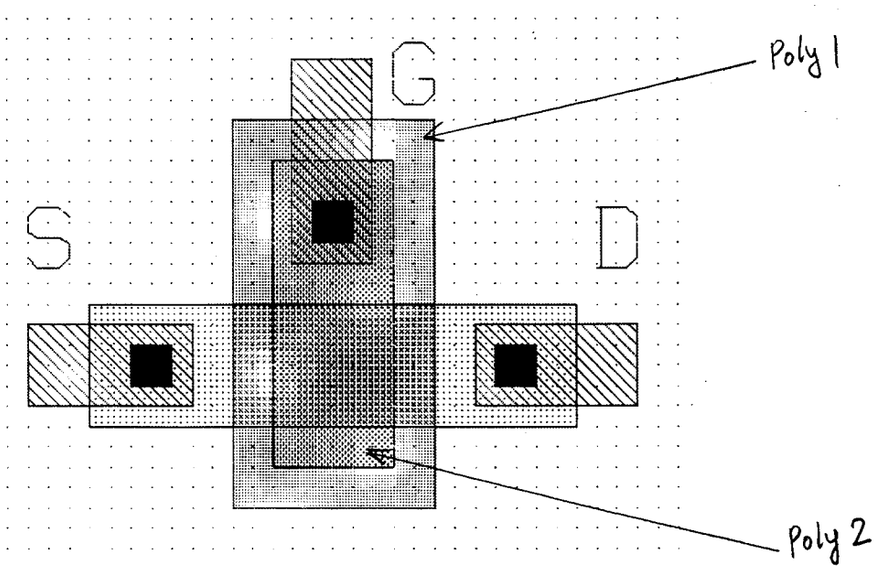
Open DRAM architecture results in smaller memory bit layout size. However, it is more susceptible to noise, since noise from sub and adjacent word/bit lines does not couple equally into the sense amp's inputs. Folded architecture has a better noise immunity but leads to bigger mbit layout size.

Problem 17.8

Since the sheet resistance of n+/p+ poly resistor is very high, using poly resistors as pull-ups would lower the speed of the circuit. The advantage of using poly resistor is the smaller layout size. (P-channel MOSFET pull-ups need N-well, which is area-consuming).

Problem 17.9

A possible EEPROM layout in CN20 is shown below:



Please note that poly 1 is floating in this configuration.