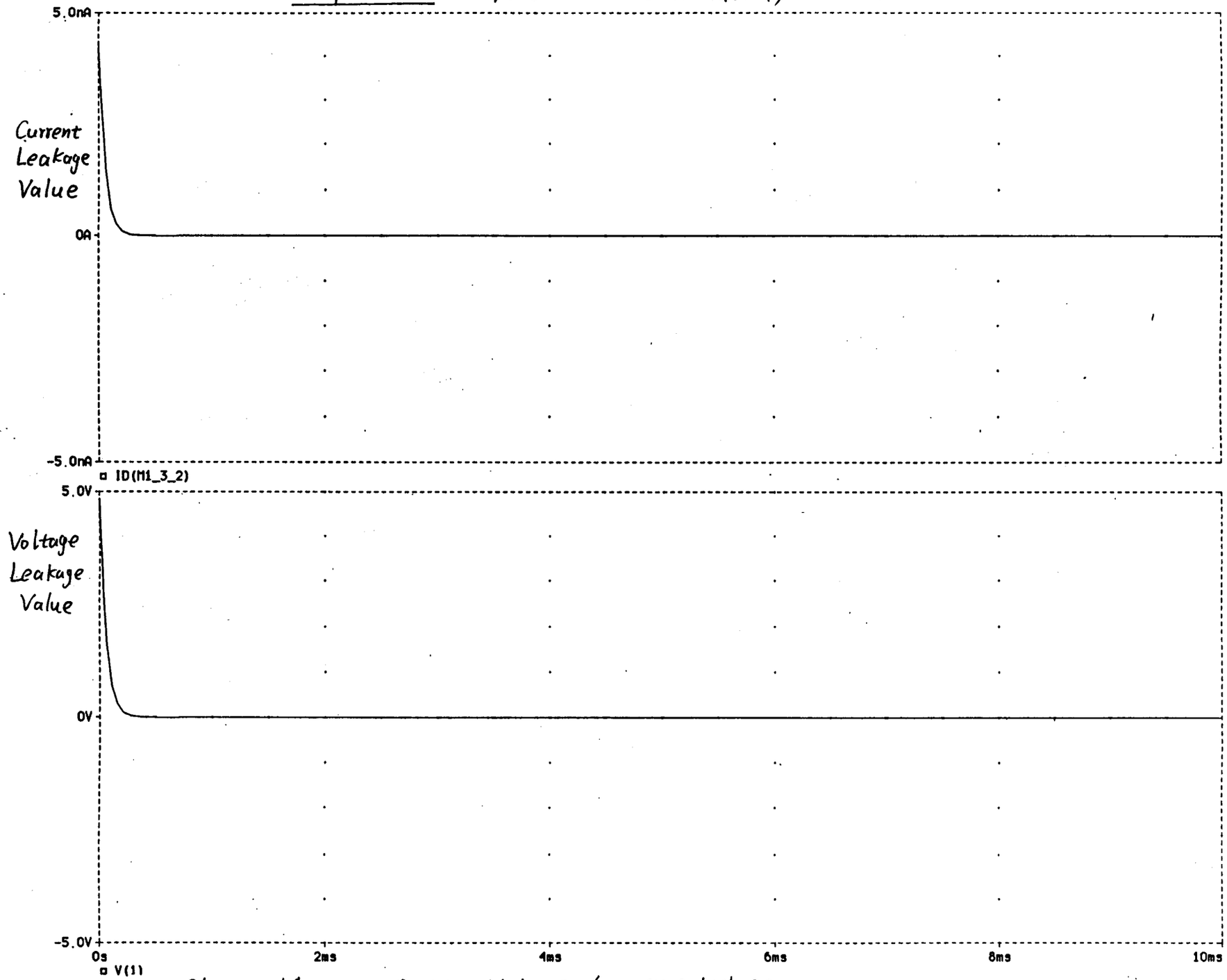
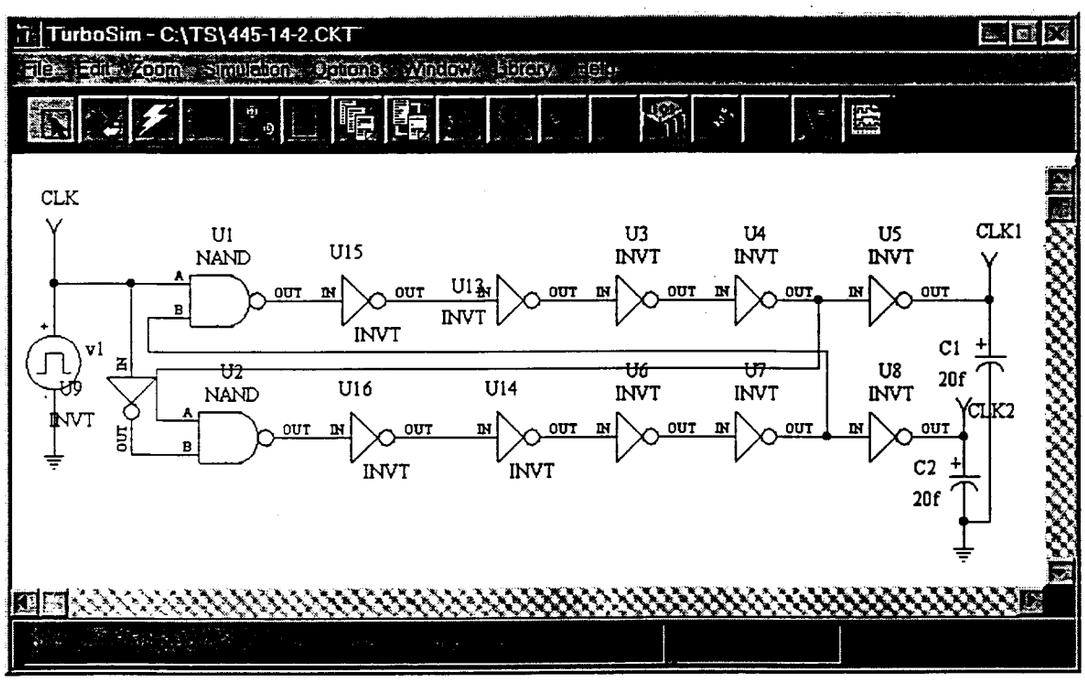
Chapter 14 Problem 14.1 (Simulation)



Chapter 14 Problem 14.1 3μ/2μ NMOS leakage

Problem 14.2

Simulation the nonoverlapping clock generator circuit. In order to increase the dead time between the nonoverlapping clocks, two more inverters are added to increase the delay time.

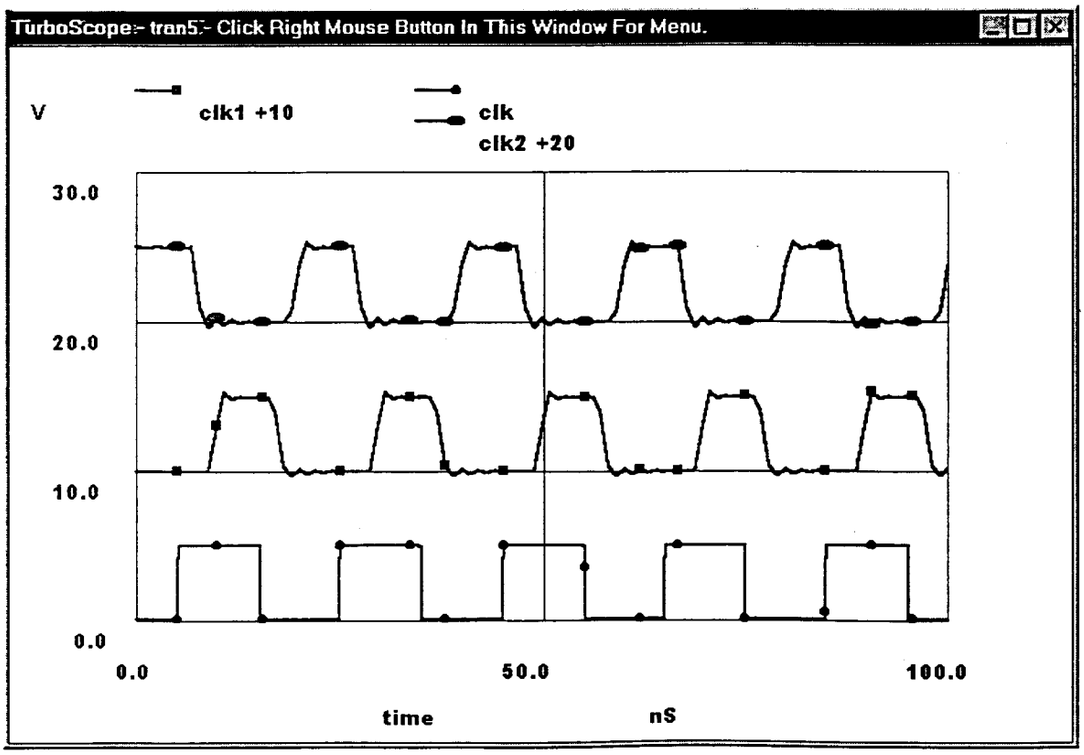


Netlist of SPICE simulation:

```
*** (TurboSim V 1.87) Netlist for C:\TS\445-14-2.CKT
* --
.subckt NAND.sub 6 4 5
M10     2 6 5 2 CMOSPB  L=2u W=3u
M11     2 4 5 2 CMOSPB  L=2u W=3u
M7      1 6 5 0 CMOSNB  L=2u W=3u
M8      0 4 1 0 CMOSNB  L=2u W=3u
V1      2 0     DC 5 AC 0 0
.ends NAND.sub

* --
.subckt inverter.sub 2 3
M1      0 2 3 0 CMOSNB  L=2u W=3u
M2      4 2 3 4 CMOSPB  L=2u W=3u
VDD     4 0     DC 5 AC 0 0
.ends inverter.sub


*** Top Level Netlist ***
C1      CLK1 0 20f
C2      CLK2 0 20f
```

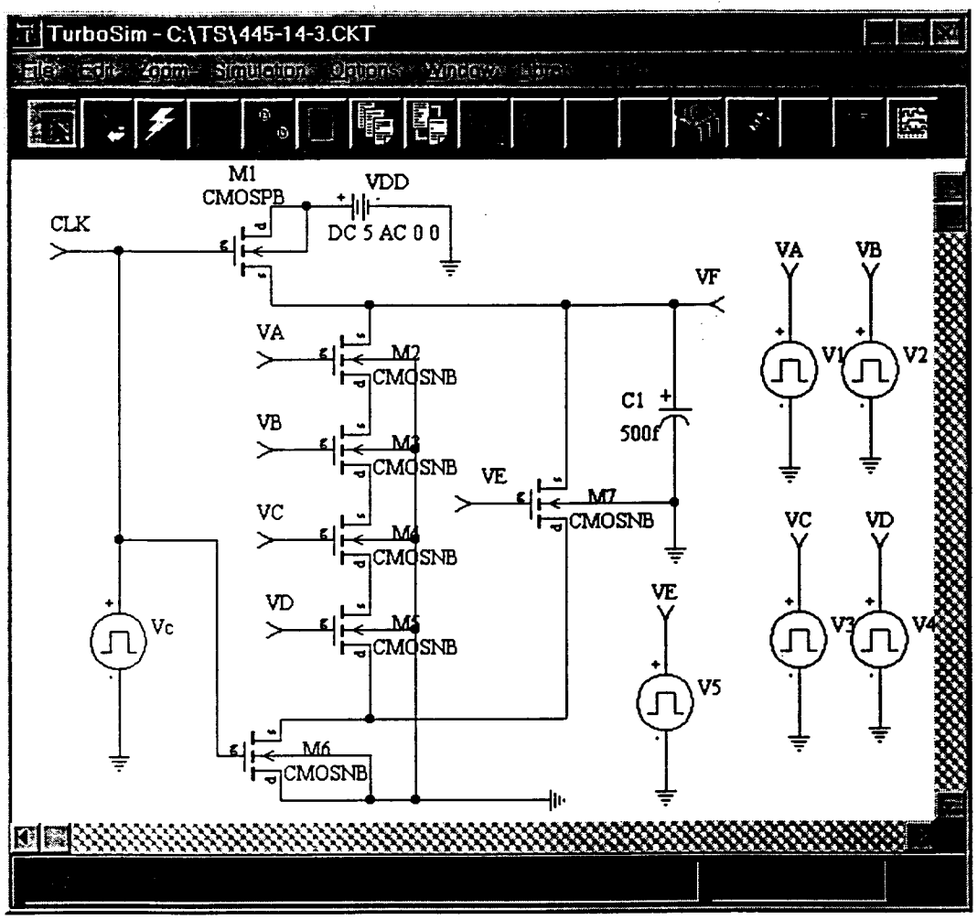
```
XU1     CLK 2 27        NAND.sub
XU13    23 3    inverter.sub
XU14    24 9    inverter.sub
XU15    27 23   inverter.sub
XU16    28 24   inverter.sub
XU2     7 8 28  NAND.sub
XU3     3 12    inverter.sub
XU4     12 7    inverter.sub
XU5     7 CLK1 inverter.sub
XU6     9 17    inverter.sub
XU7     17 2    inverter.sub
XU8     2 CLK2 inverter.sub
XU9     CLK 8   inverter.sub
vl      CLK 0   DC 0 AC 0 0 PULSE(0.1 5 5n .1n .1n 10n 20n)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.OPTION ABSTOL=1u ITL4=100 RELTOL=.01 VNTOL=2m
.tran .1n 100n 0 1n
.end
```

SPICE simulation result:



Problem 14.3

Use PE gate to realize some logic functions. The SPICE circuit and simulation results are shown below.



Netlist of this circuit:

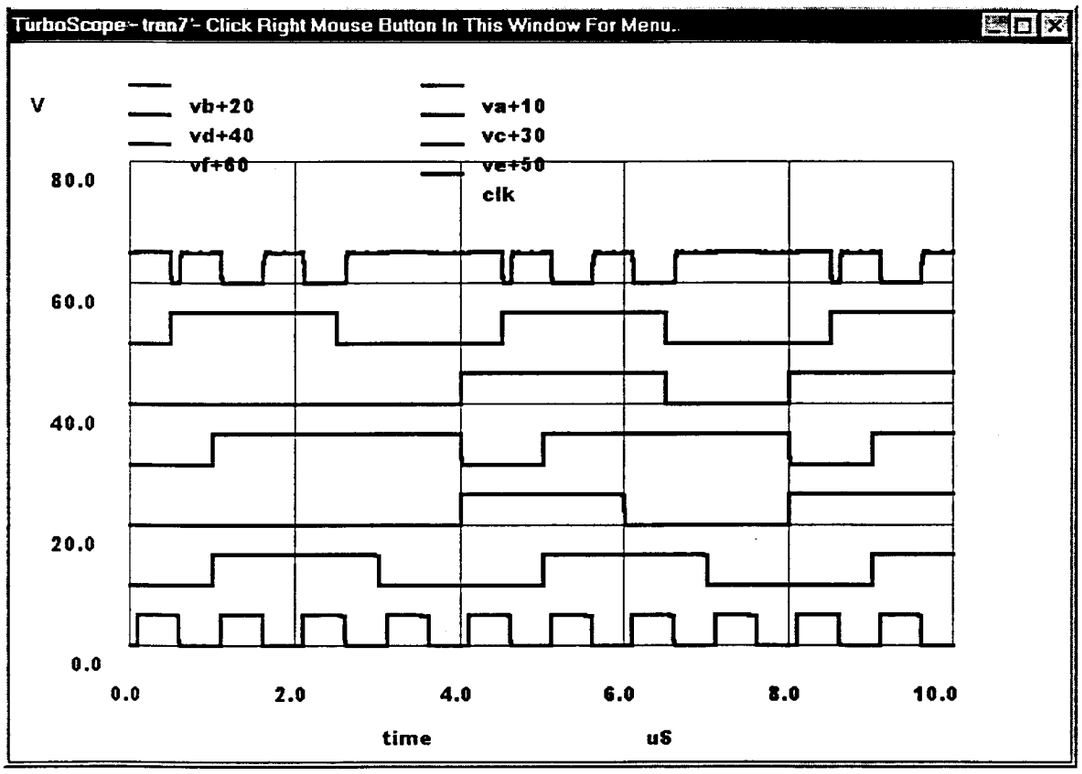
*** (TurboSim V 1.87) Netlist for C:\TS\445-14-3.CKT

*** Top Level Netlist ***

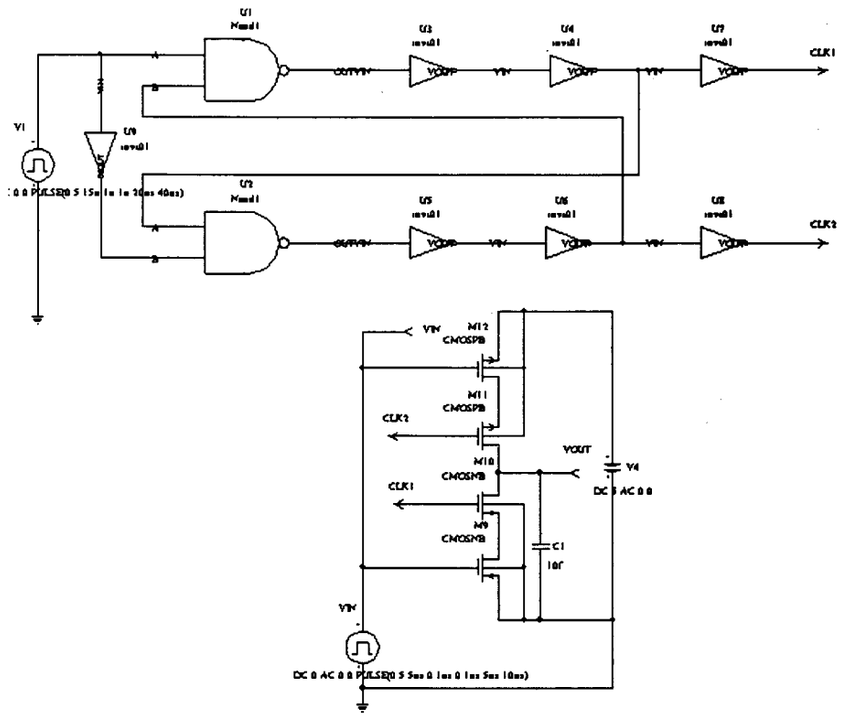
```
C1      VF 0 500f
M1      1 CLK VF 1 CMOSPB  L=2u W=3u
M2      3 VA VF 0 CMOSNB  L=2u W=3u
M3      6 VB 3 0 CMOSNB  L=2u W=3u
M4      8 VC 6 0 CMOSNB  L=2u W=3u
M5      13 VD 8 0 CMOSNB  L=2u W=3u
M6      0 CLK 13 0 CMOSNB  L=2u W=3u
M7      13 VE VF 0 CMOSNB  L=2u W=3u
V1      VA 0    DC 0 AC 0 0 PULSE(0 5 1u 5ns 5ns 2u 4u)
V2      VB 0    DC 0 AC 0 0 PULSE(0 5 4u 5ns 5ns 2u 4u)
V3      VC 0    DC 0 AC 0 0 PULSE(0 5 1u 5ns 5ns 3u 4u)
```

```
V4      VD 0    DC 0 AC 0 0 PULSE(0 5 4u 5ns 5ns 2.5u 4u)
V5      VE 0    DC 0 AC 0 0 PULSE(0 5 .5u 5ns 5ns 2u 4u)
Vc      CLK 0   DC 0 AC 0 0 PULSE(0 5 100n 5ns 5ns .5u 1u)
VDD     1 0     DC 5 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSPB PMOS LEVEL=4 ...
.MODEL CMOSNB NMOS LEVEL=4 ...

***** End of spice models and macro models *****

.OPTION ABSTOL=1u ITL4=100 RELTOL=.01 VNTOL=2m
.tran 100n 10u 0 100n
.end
```

Simulation result:



Problem 14.4



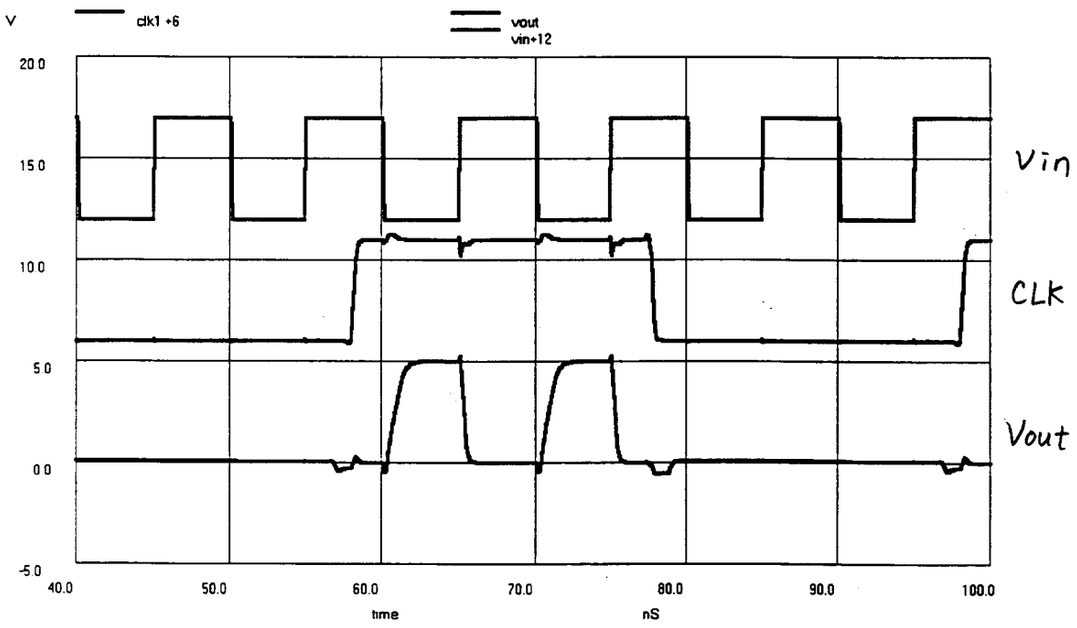
*** (TurboSim V 1.87) Netlist for C:\TURBOSIM\EE445\144.CKT
* --
.subckt nand1.sub 2 5 4
M1 1 2 0 0 CMOSNB L=2u W=3u
M2 4 5 1 0 CMOSNB L=2u W=3u
M3 4 5 6 6 CMOSPB L=2u W=3u
M4 4 2 6 6 CMOSPB L=2u W=3u
VDD 6 0 DC 5 AC 0 0
.ends nand1.sub

* --
.subckt invt01.sub 4 1
M1 1 4 0 0 CMOSNB L=2u W=3u
M2 1 4 3 3 CMOSPB L=2u W=3u
VDD 3 0 DC 5 AC 0 0
.ends invt01.sub

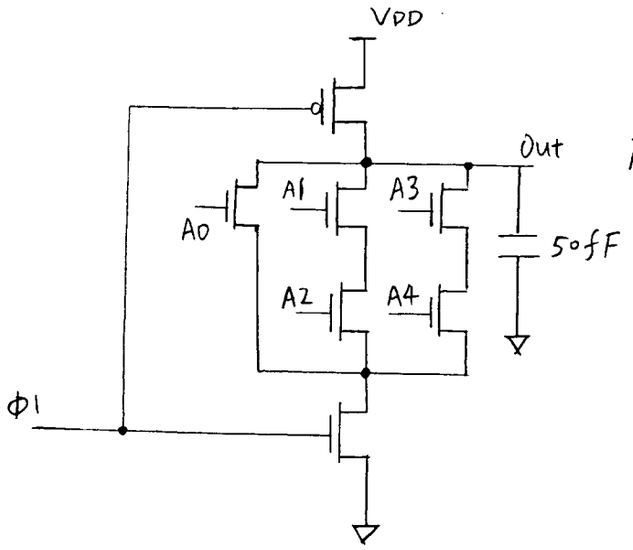
*** Top Level Netlist ***
C1 0 VOUT 10f
M10 VOUT CLK1 31 0 CMOSNB L=2u W=3u
M11 VOUT CLK2 34 35 CMOSPB L=2u W=3u
M12 34 VIN 35 35 CMOSPB L=2u W=3u
M9 31 VIN 0 0 CMOSNB L=2u W=3u

```
XU1     22 25 6 nand1.sub
XU2     3 13 16 nand1.sub
XU3     6 10    invt01.sub
XU4     10 13   invt01.sub
XU5     16 19   invt01.sub
XU6     19 22   invt01.sub
XU7     13 CLK1         invt01.sub
XU8     22 CLK2         invt01.sub
XU9     25 3    invt01.sub
V1      25 0    DC 0 AC 0 0 PULSE(0 5 15n 1n 1n 20ns 40ns)
V4      35 0    DC 5 AC 0 0
VIN     VIN 0   DC 0 AC 0 0 PULSE(0 5 5ns 0.1ns 0.1ns 5ns 10ns)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.OPTION ABSTOL=1m RELTOL=0.01 VNTOL=10mv
.tran .1ns 100ns 0 .1ns uic
.end
```

SPICE simulation is shown below:



Problem 14.5



$F = \overline{A0 + A1 \cdot A2 + A3 \cdot A4}$

Assuming minimum size is adopted (3μm/2μm). The worst-case t_{PHL}

$$t_{PHL} \approx 3 R_N \times C_{load} = 3 \times 8k \times 50fF = \underline{\underline{1.2nS}}$$

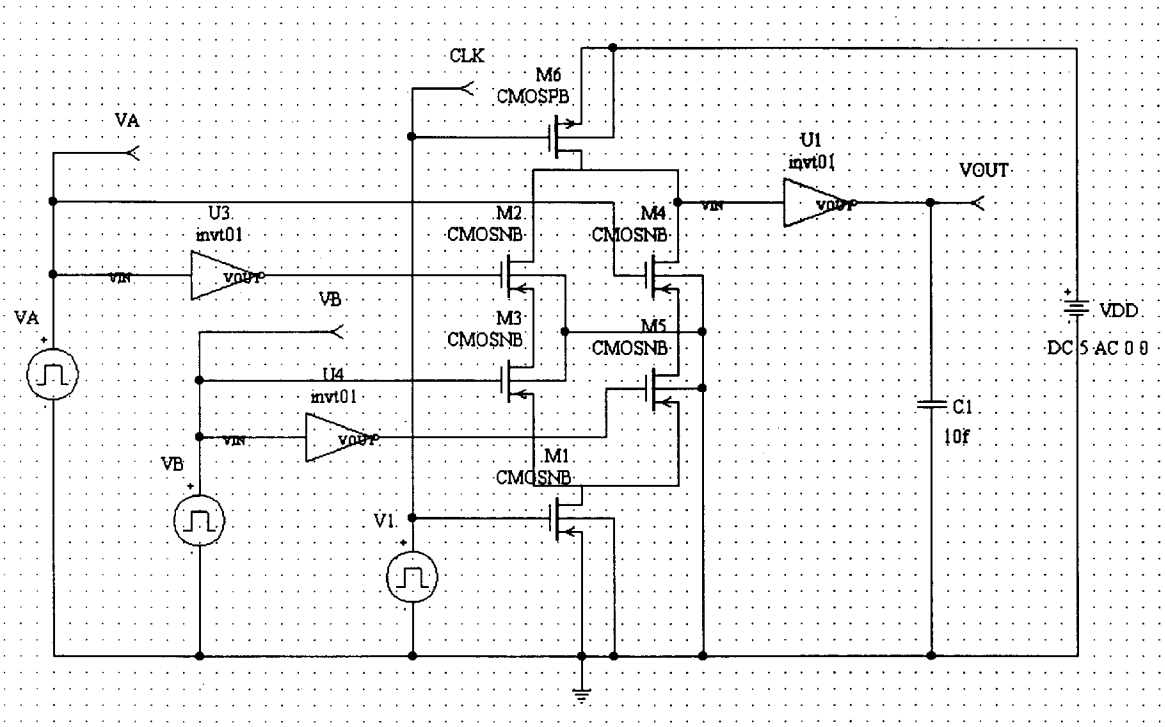
Problem 14.6

See next page for implementation and simulation.

Problem 14.7

The circuit is implemented by N-P logic. When $\phi = '0'$ ($\overline{\phi} = '1'$), both "C_{n+1}" and "S_n" logic are in pre-charge phase. Note that $\overline{C_{n+1}}$ is logic '1' and shut the corresponding P-MOS of second stage off. When $\phi = '1'$ ($\overline{\phi} = '0'$), both stages are in evaluation phase, and C_{n+1} and S_n are set by A_n, B_n and C_n.

Problem 14.6



***** (TurboSim V 1.87) Netlist for C:\TURBOSIM\EE445\146.CKT**
*** --**

```
.subckt invt01.sub 4 1
M1      1 4 0 0 CMOSNB  L=2u W=3u
M2      1 4 3 3 CMOSPB  L=2u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt01.sub


*** Top Level Netlist ***
C1      0 VOUT 10f
M1      1 CLK 0 0 CMOSNB  L=2u W=3u
M2      4 5 6 0 CMOSNB  L=2u W=3u
M3      6 VB 1 0 CMOSNB  L=2u W=3u
M4      4 VA 9 0 CMOSNB  L=2u W=3u
M5      9 10 1 0 CMOSNB  L=2u W=3u
M6      4 CLK 11 11 CMOSPB  L=2u W=3u
XU1     4 VOUT          invt01.sub
XU3     VA 5    invt01.sub
XU4     VB 10   invt01.sub
V1      CLK 0  DC 0 AC 0 0 PULSE(0 5 6n 0.1ns 0.1ns 10ns 20ns)
VA      VA 0    DC 0 AC 0 0 PULSE(0 5 1n 0.1n 0.1n 20n 40n)
VB      VB 0    DC 0 AC 0 0 PULSE(0 5 5n 0.1n 0.1n 30n 60n)
VDD     11 0    DC 5 AC 0 0

***** Spice models and macro models *****
```

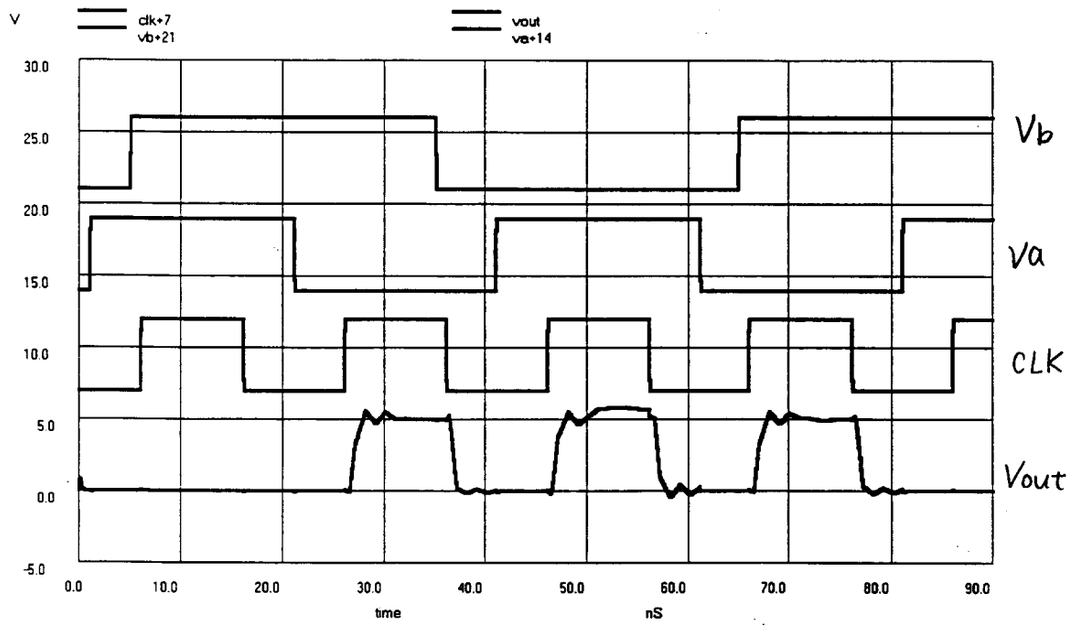
.MODEL CMOSNB NMOS LEVEL=4

.MODEL CMOSPB PMOS LEVEL=4

******* End of spice models and macro models *******

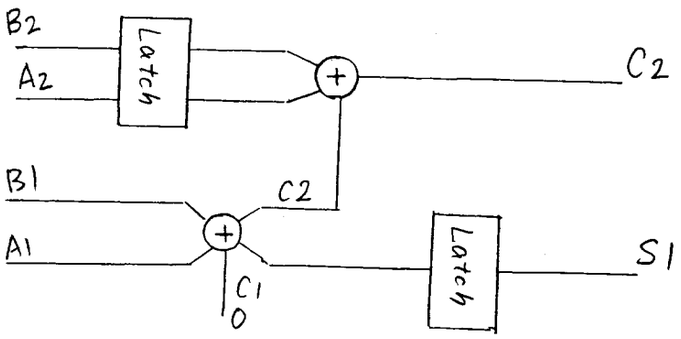
.OPTION ABSTOL=1m RELTOL=0.1 VNTOL=10mv
.tran 1n 100ns 0 1n uic
.end

The SPICE simulation is shown below:



Problem 14.8

A two-bit adder using adder cell of Fig P14.7 and pipelining is shown below:



If a clock running at 20MHz is used with the two-bit adder, the time it takes to add two two-bit words is $t = 2T = 2\frac{1}{f} = 2\times\frac{1}{20\,MHz} = 0.1\,\mu s$

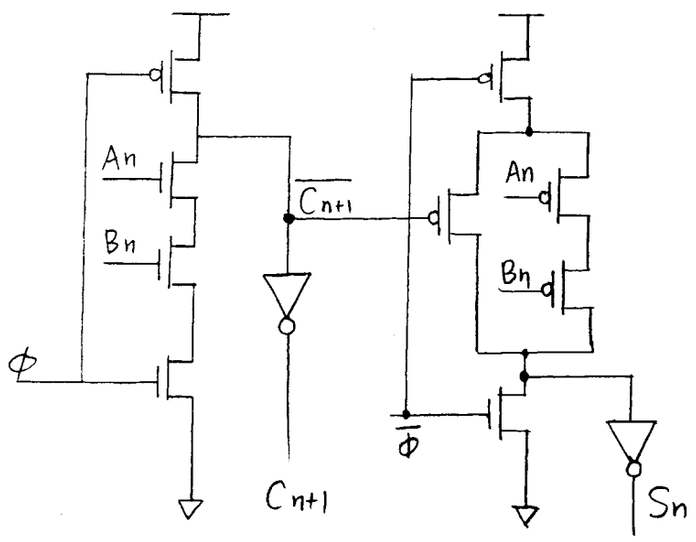
The time it takes to add two 32-bit words is $t = 32T = 1.6\,\mu s$.

Problem 14.9

For half adder, we have

$$\begin{cases} S_n = A_n \oplus B_n = (A_n + B_n)(\bar{A}_n + \bar{B}_n) = (A_n + B_n)\overline{C_{n+1}} \\ C_{n+1} = A_n B_n \end{cases}$$

The implementation using NP logic is as follows:



Problem 14.10

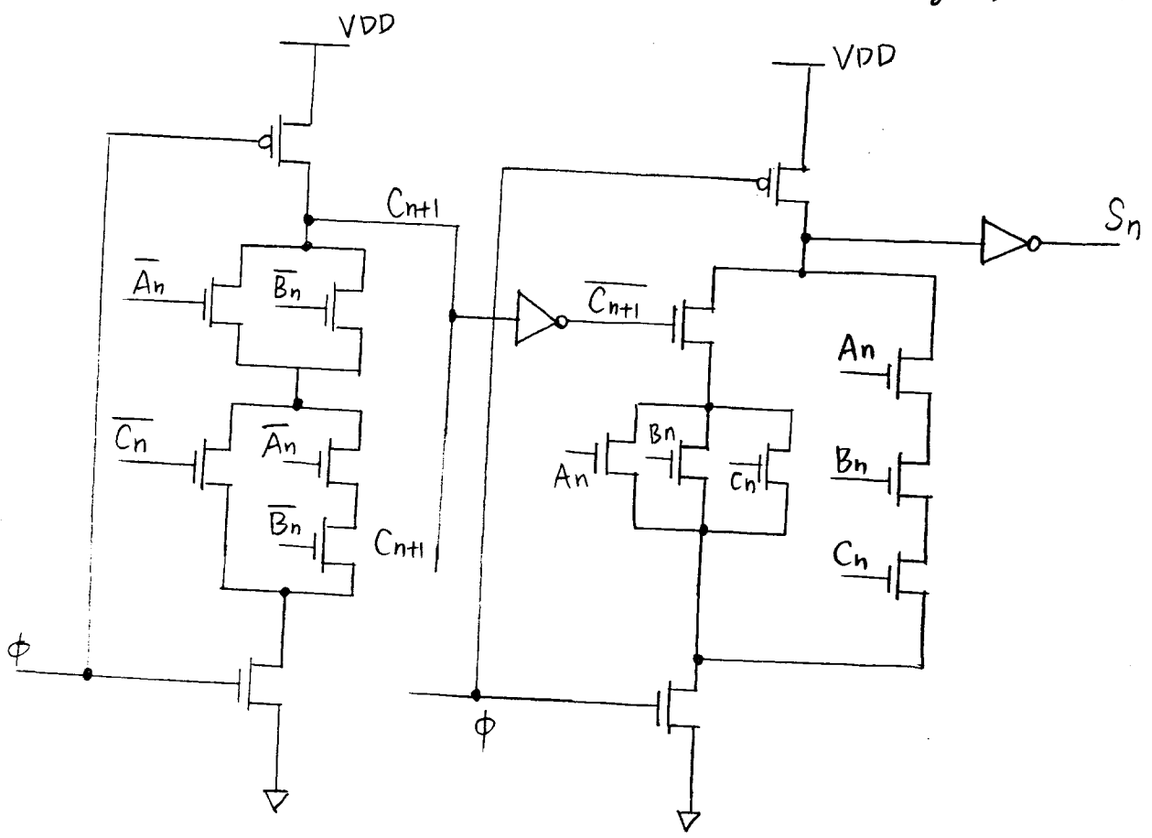
The logic functions of a full adder are:

$$S_n = \bar{A}_n \bar{B}_n C_n + \bar{A}_n B_n \bar{C}_n + A_n \bar{B}_n \bar{C}_n + A_n B_n C_n$$

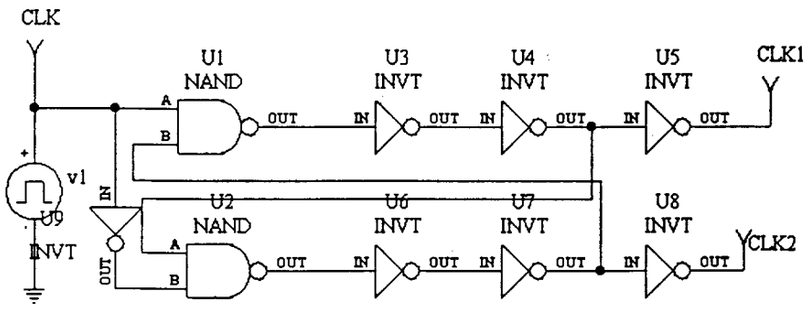
$$= (A_n + B_n + C_n)\overline{C_{n+1}} + A_n B_n C_n$$

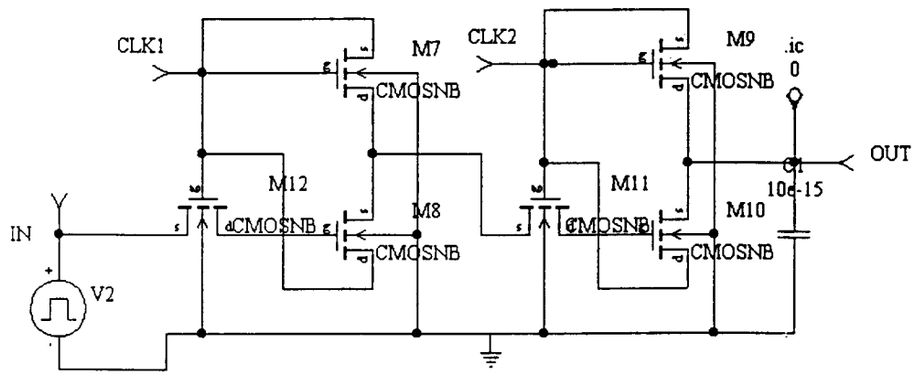
$$C_{n+1} = A_n B_n + C_n (A_n + B_n)$$

The implementation using PE gate (domino logic) is shown below:



Problem 14.12



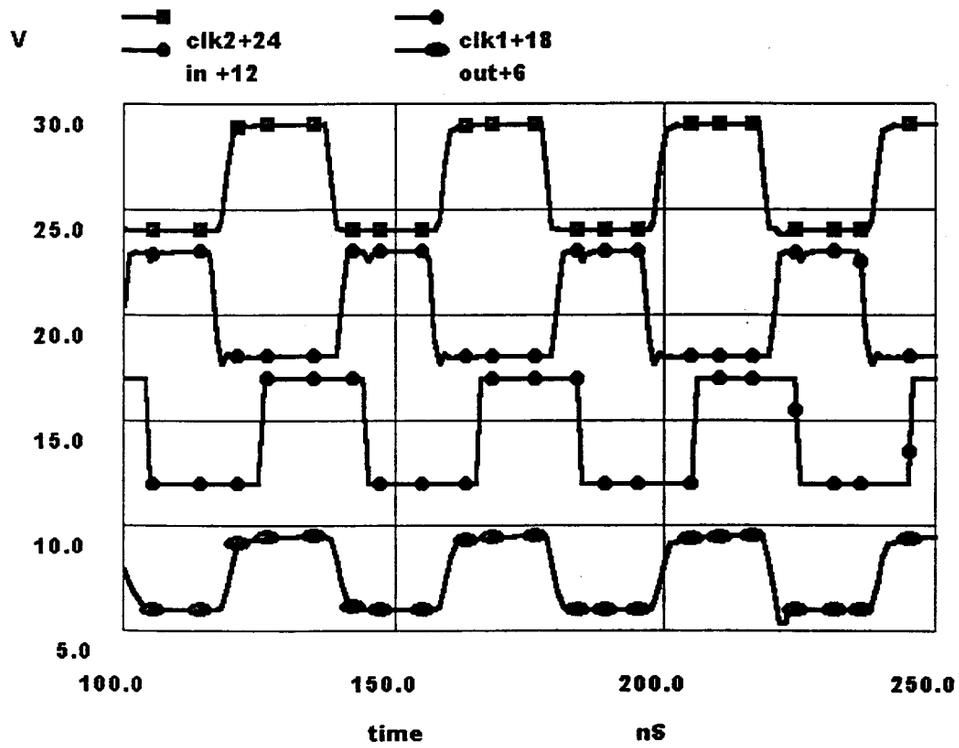


*** (TurboSim V 1.87) Netlist for C:\TS\CIRCUITS\445-1412.CKT
* --
.subckt NAND.sub 6 4 5
M10 2 6 5 2 CMOSPB L=2u W=3u
M11 2 4 5 2 CMOSPB L=2u W=3u
M7 1 6 5 0 CMOSNB L=2u W=3u
M8 0 4 1 0 CMOSNB L=2u W=3u
V1 2 0 DC 5 AC 0 0
.ends NAND.sub

* --
.subckt inverter.sub 2 3
M1 0 2 3 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
M2 4 2 3 4 CMOSPB L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
VDD 4 0 DC 5 AC 0 0
.ends inverter.sub

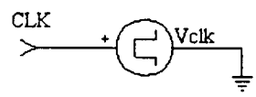
*** Top Level Netlist ***
.ic V(OUT)=0
C1 OUT 0 10e-15
M10 CLK2 10 OUT 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
M11 10 CLK2 7 0 CMOSNB L=2u W=6u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
M12 9 CLK1 IN 0 CMOSNB L=2u W=6u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
M7 7 CLK1 CLK1 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1

```
M8      CLK1 9 7 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
M9      OUT CLK2 CLK2 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
XU1     CLK 17 20       NAND.sub
XU2     16 4 29 NAND.sub
XU3     20 22   inverter.sub
XU4     22 16   inverter.sub
XU5     16 CLK1         inverter.sub
XU6     29 33   inverter.sub
XU7     33 17   inverter.sub
XU8     17 CLK2         inverter.sub
XU9     CLK 4  inverter.sub
v1      CLK 0  DC 0 AC 0 0 PULSE(0 5 15n 1n 1n 18n 40n)
V2      IN 0    DC 0 AC 0 0 PULSE(0 5 5n 1n 1n 18n 40n)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4 ..
.MODEL CMOSPB PMOS LEVEL=4 ..


***** End of spice models and macro models *****

.OPTION ABSTOL=100u CHGTOL=1.0E-12 ITL4=100 RELTOL=.1 VNTOL=5m
.tran .1n 250n 100n 1n
.end
```

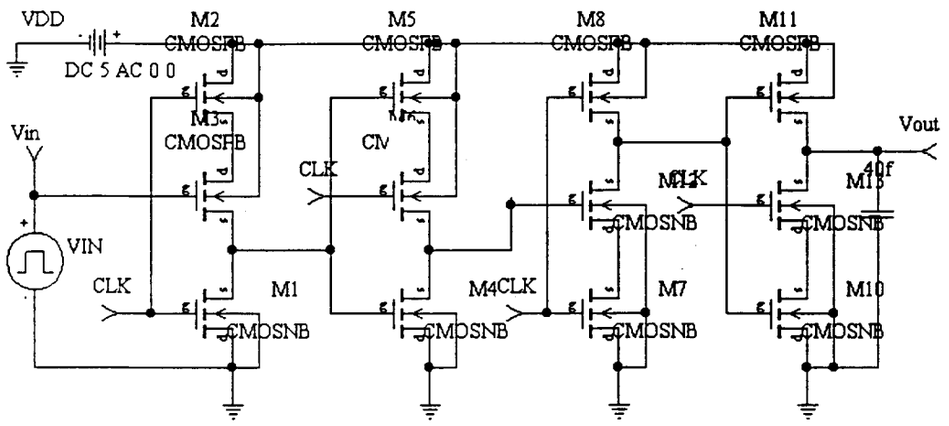


The logic high voltage is about 3.5V.

Problem 14.13



DC 0 AC 0 0 PULSE(0 5 15n 100p 100p 10n 20n)



*** (TurboSim V 1.87) Netlist for C:\TS\CIRCUITS\445-1413.CKT

*** Top Level Netlist ***

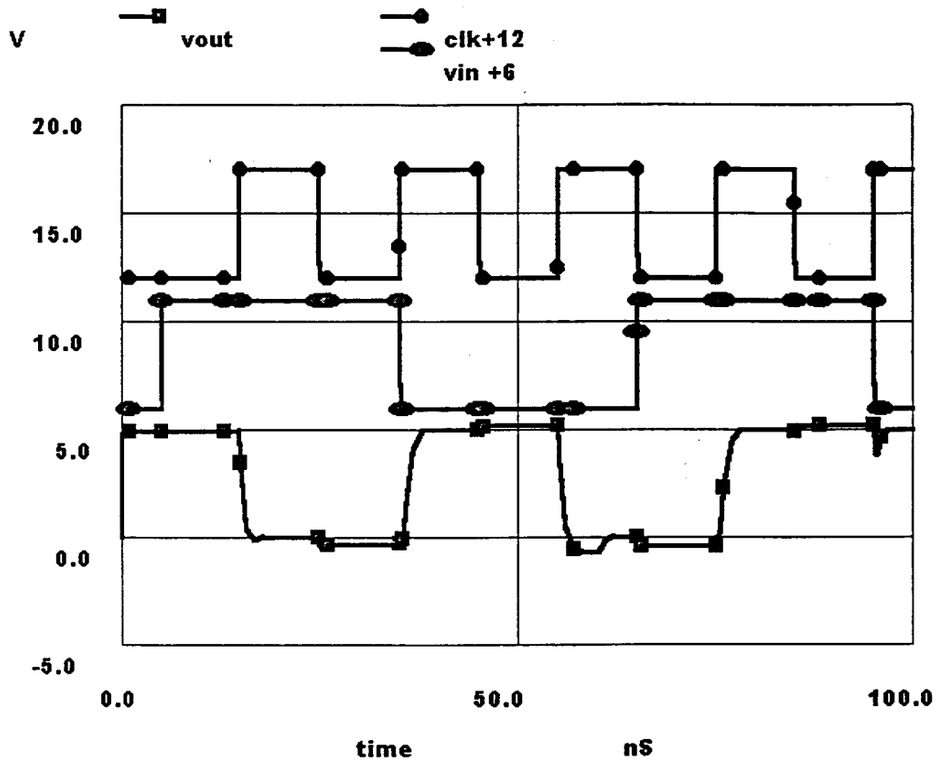
```
C1      Vout 0 40f  IC=5
M1      0 CLK 2 0 CMOSNB  L=2u W=3u
M10     0 9 8 0 CMOSNB  L=2u W=3u
M11     3 9 Vout 3 CMOSPB  L=2u W=3u
M12     7 10 9 0 CMOSNB  L=2u W=3u
M13     8 CLK Vout 0 CMOSNB  L=2u W=3u
M2      3 CLK 4 3 CMOSPB  L=2u W=3u
M3      4 Vin 2 3 CMOSPB  L=2u W=3u
M4      0 2 10 0 CMOSNB  L=2u W=3u
M5      3 2 6 3 CMOSPB  L=2u W=3u
M6      6 CLK 10 3 CMOSPB  L=2u W=3u
M7      0 CLK 7 0 CMOSNB  L=2u W=3u
M8      3 CLK 9 3 CMOSPB  L=2u W=3u
Vclk    CLK 0  DC 0 AC 0 0 PULSE(0 5 15n 100p 100p 10n 20n)
VDD     3 0    DC 5 AC 0 0
VIN     Vin 0  DC 0 AC 0 0 PULSE(0 5 5n 100p 100p 30n 60n)
```

***** Spice models and macro models *****

```
.MODEL CMOSNB NMOS LEVEL=4 ..
.MODEL CMOSPB PMOS LEVEL=4 ..
```

***** End of spice models and macro models *****

```
.OPTION ABSTOL=100u ITL4=100 RELTOL=.1 VNTOL=5mv
.tran .1n 100n 0 1n uic
.end
```


V
vout
clk+12
vin +6
20.0
15.0
10.0
5.0
0.0
-5.0
0.0
50.0
100.0
time
nS