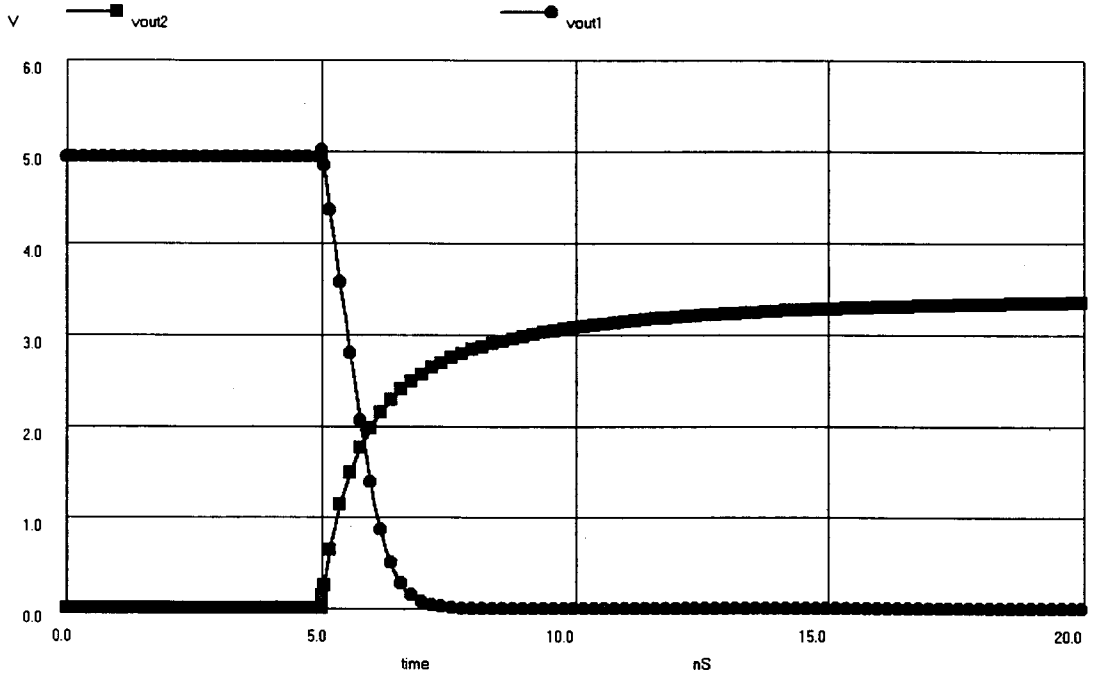
Chapter 13

Problem 13.1

```
*** Top Level Netlist ***
C2      0 VOUT2 100f  IC=0
C3      VOUT1 0 100f  IC=5v
M2      2 VG VOUT2 0 CMOSNB  L=2u W=3u OFF
M3      VOUT1 VG 0 0 CMOSNB  L=2u W=3u
VDD     2 0     DC 5 AC 0 0
VG      VG 0    DC 0 AC 0 0 PULSE(0 5 5n 1p 1p 20n 40n)

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
+VFB=-9.73820E-01, LVFB=3.67458E-01,WVFB=-4.72340E-02
... ...
+pbsw=0.8   mj=0.66036   mjsw=0.178543   wdf=0   dell=0

***** End of spice models and macro models *****
.OPTION ABSTOL=1m RELTOL=0.1 VNTOL=10mv
.tran 0.1n 20n 0 0.1n uic
.end
```

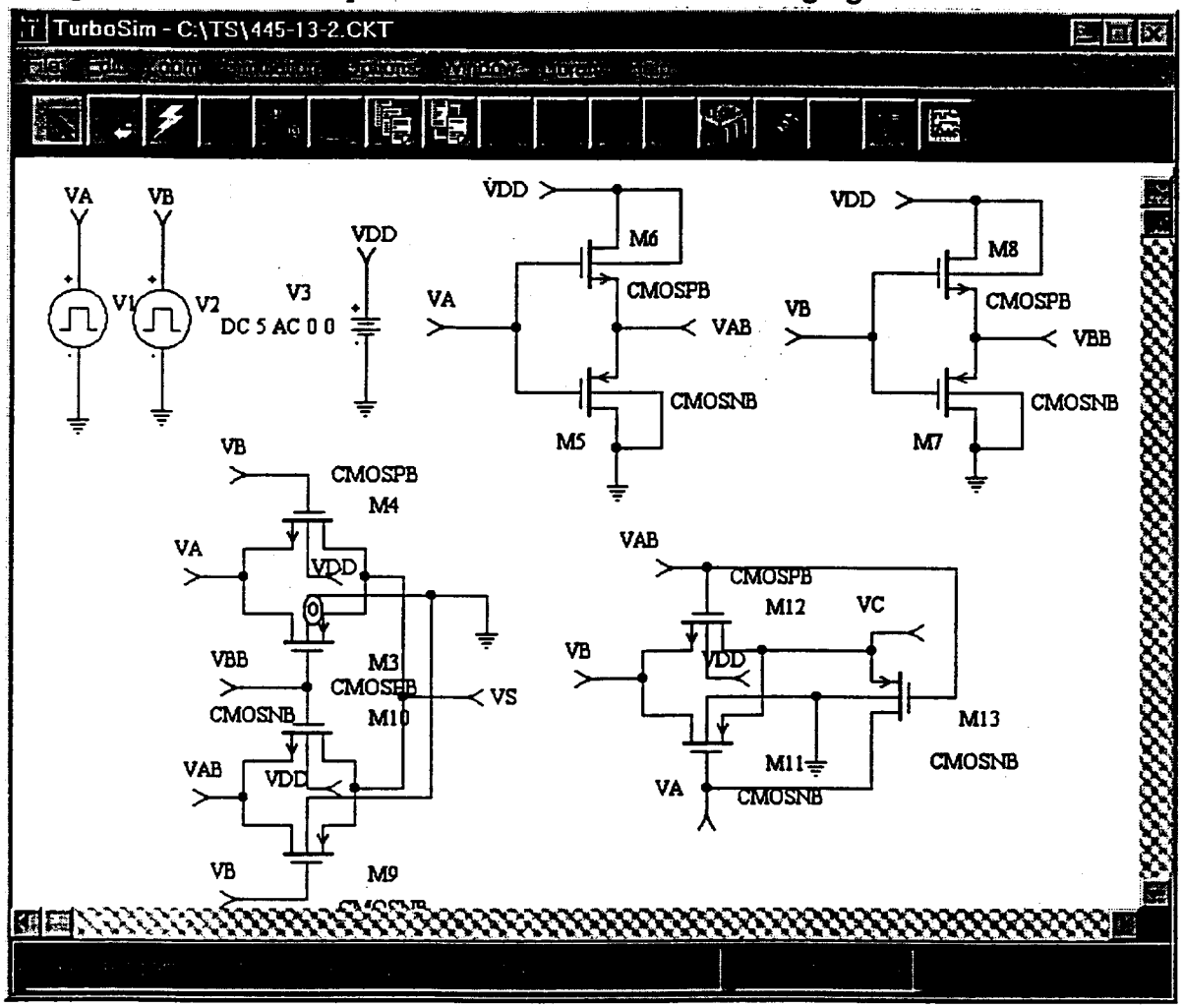
The SPICE simulation result is shown below:



SPICE simulation showed Tplh is about 0.58nS and Tphl is about 0.6nS. If we increase the width of the MOSFETs, since the load capacitance is relatively larger than the parasitic capacitance of MOSFET, although parasitic capacitance increases along with resistance of MOSFET decreasing, the total delay time will decrease. However, the internal logic driving this circuit will see an increase of its load capacitance.

Problem 13.2

Design and simulate the operation of a half adder circuit using Tgs.



*** Top Level Netlist ***

```
M10     VS VBB VAB VDD CMOSPB  L=2u W=3u
M11     VB VA VC 0 CMOSNB  L=2u W=3u
M12     VC VAB VB VDD CMOSPB  L=2u W=3u
M13     VA VAB VC 0 CMOSNB
M3      VA VBB VS 0 CMOSNB  L=2u W=3u
M4      VS VB VA VDD CMOSPB  L=2u W=3u
M5      0 VA VAB 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M6      VDD VA VAB VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M7      0 VB VBB 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M8      VDD VB VBB VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M9      VAB VB VS 0 CMOSNB  L=2u W=3u
V1      VA 0    DC 0 AC 0 0 PULSE(0 5 1u 5ns 5ns 2u 4u)
V2      VB 0    DC 0 AC 0 0 PULSE(0 5 4u 5ns 5ns 2u 4u)
V3      VDD 0  DC 5 AC 0 0
```

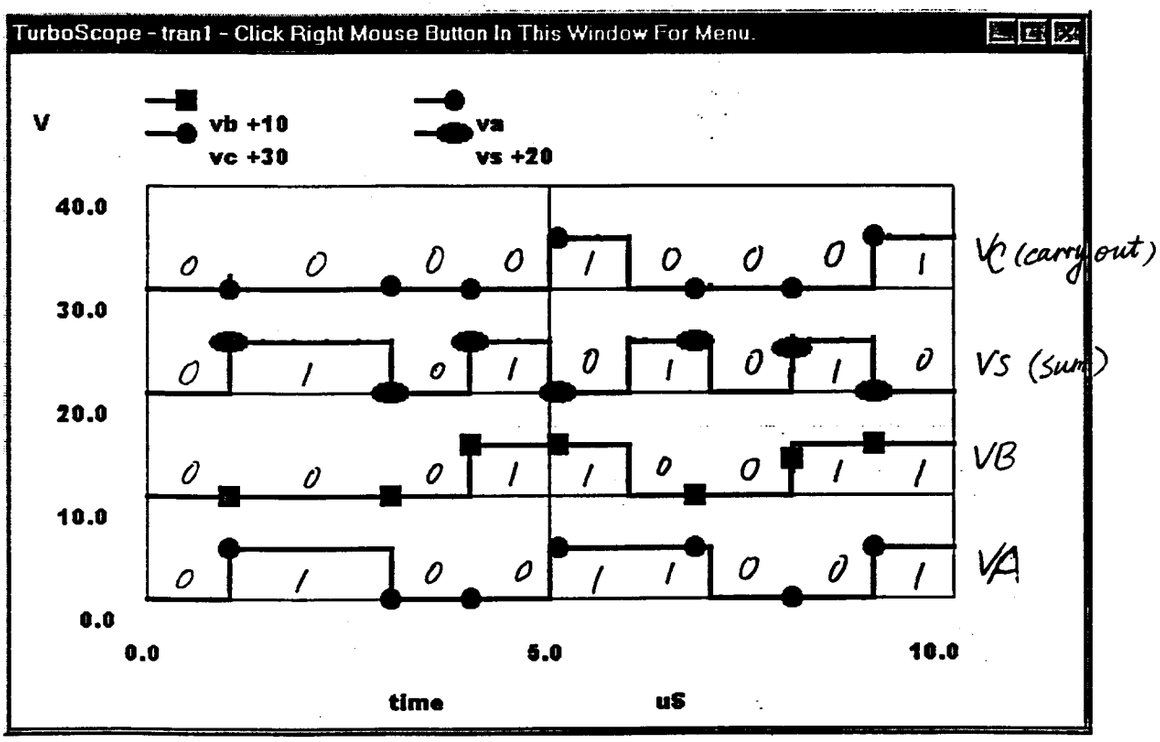
***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4 ...
.MODEL CMOSPB PMOS LEVEL=4 ...

***** End of spice models and macro models *****

.OPTION ABSTOL=1u ITL4=100 RELTOL=.1 VNTOL=2mv
.tran 10n 10u 0
.end

Simulation results:

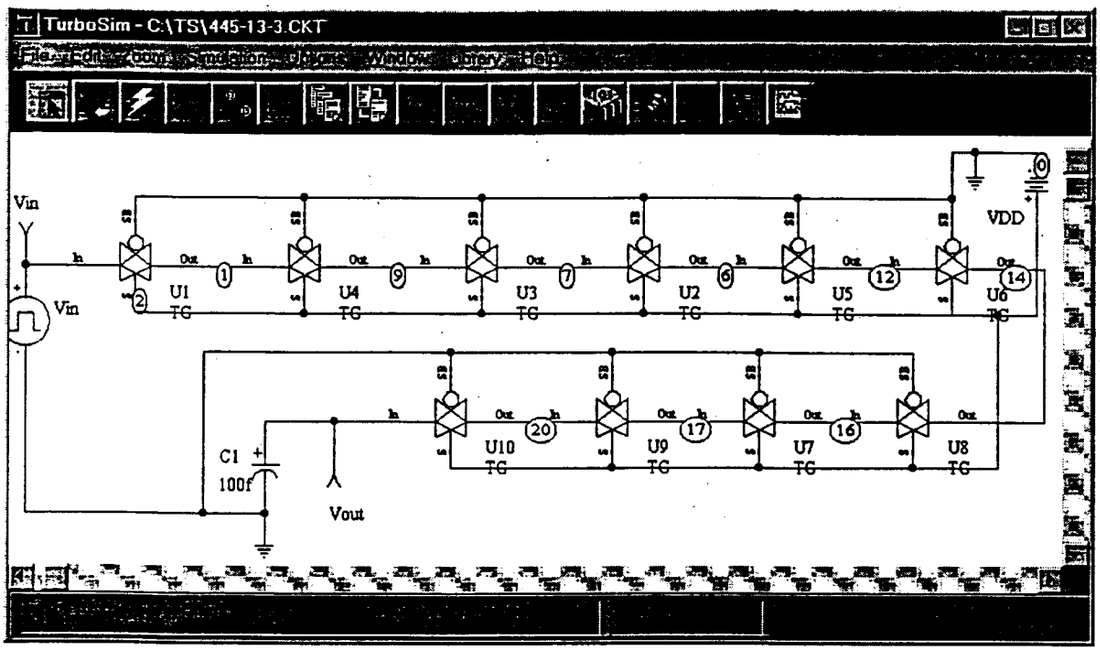


Problem 13.3

Series connection of 10 TGs, the delay to drive a 100fF load capacitance can be estimated: (using minimum size MOSFETs)

$$t_{PHL} = t_{PLH} = 10 \times (8k\Omega \| 24k\Omega) \times 100fF + .35 \times (8k\Omega \| 24k\Omega) \times (4.8fF + 4.8fF) \times 1.5 \times 100$$
$$\approx 9 \text{ ns}$$

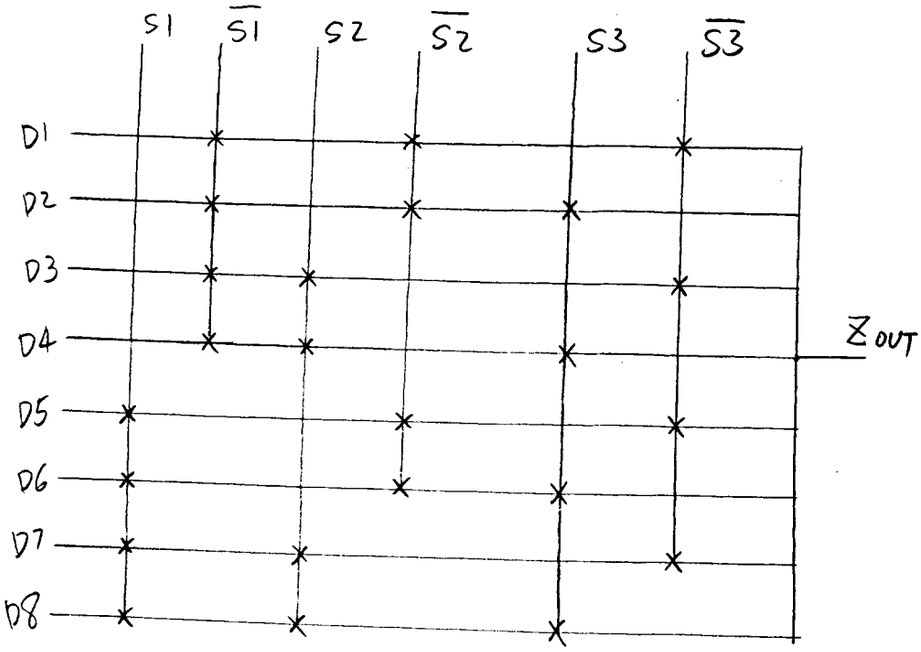
SPICE simulation results:



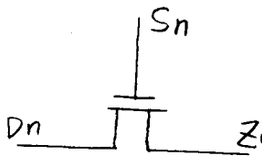

```
.subckt tg.sub 3 2 6 1
M1      1 2 3 0 CMOSNB  L=2u W=3u
M2      3 6 1 8 CMOSPB  L=2u W=3u
VDD     8 0     DC 5 AC 0 0
.ends tg.sub

*** Top Level Netlist ***
C1      Vout 0 100f
XU1     1 2 0 Vin       tg.sub
XU10    20 2 0 Vout     tg.sub
XU2     6 2 0 7  tg.sub
XU3     7 2 0 9  tg.sub
XU4     9 2 0 1  tg.sub
XU5     12 2 0 6tg.sub
XU6     14 2 0 12       tg.sub
XU7     16 2 0 17       tg.sub
XU8     14 2 0 16       tg.sub
XU9     17 2 0 20       tg.sub
VDD     2 0     DC 5 AC 0 0
Vin     Vin 0   DC 0 AC 0 0 PULSE(0 5 5n .1n .1n 80n 160n)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4 ...
.MODEL CMOSPB PMOS LEVEL=4 ...

***** End of spice models and macro models *****

.OPTION ABSTOL=1u ITL4=100 RELTOL=.1 VNTOL=8mv
.tran .1n 150n 0
.end
```

see next page for SPICE simulation results of problem 13.3

Problem 13.4



where X =



Z_{OUT} or Source (Drain) of next passing transistor.

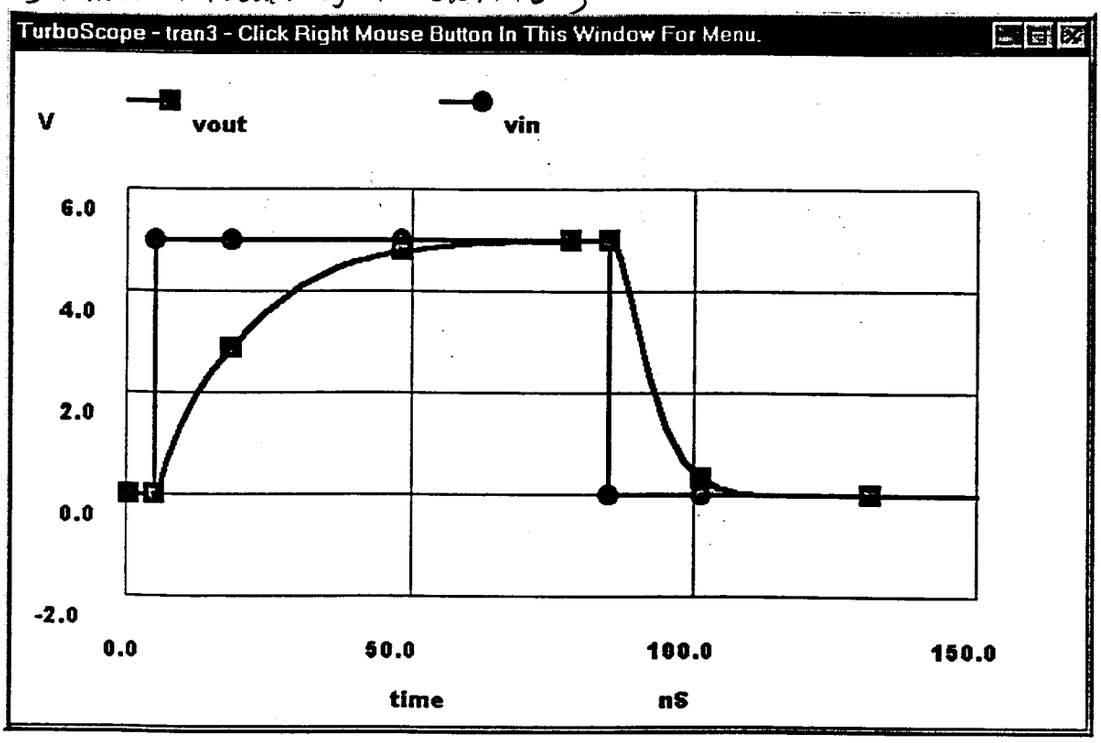
If $C_{load} = 50fF$, the total delay is (assuming minimum size)

$$t_d = 0.35 \times 2.5\, C_{ox} \times R_n \times N^2 + N \times R_n \times C_{Load}$$

$$= 0.35 \times 2.5 \times 800aF/\mu m^2 \times 6\mu m^2 \times 8k \times 9 + 3 \times 8k \times 50fF$$

$$\simeq 1.5nS.$$

Simulation result of Problem 13-3



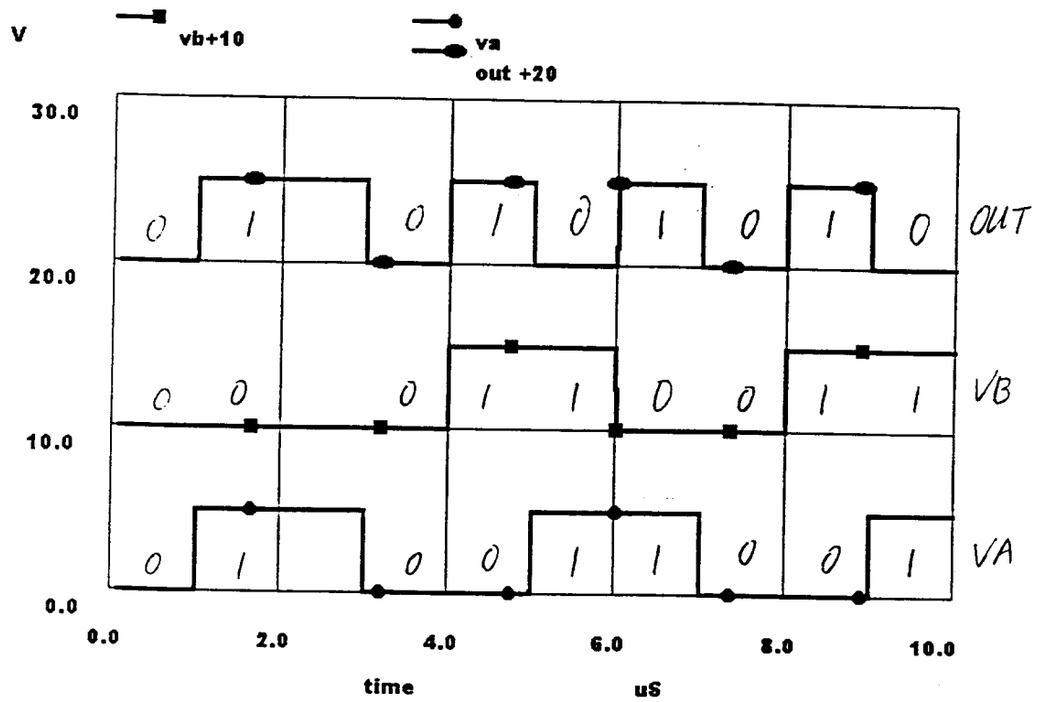
From SPICE simulation, the delay is about 10ns.

Problem 13.5

SPICE simulation for XORgate used Tgs.

```
*** (TurboSim V 1.87) Netlist for C:\TS\445-13-4.CKT
* --
.subckt tg.sub 3 2 6 1
M1      1 2 3 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
M2      3 6 1 8 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
VDD     8 0     DC 5 AC 0 0
.ends tg.sub


*** Top Level Netlist ***
M5      0 VA VAB 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M6      VDD VA VAB VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M7      0 VB VBB 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M8      VDD VB VBB VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
XU1     OUT VBB VB VA       tg.sub
XU2     OUT VB VBB VAB      tg.sub
V1      VA 0    DC 0 AC 0 0 PULSE(0 5 1u 5ns 5ns 2u 4u)
V2      VB 0    DC 0 AC 0 0 PULSE(0 5 4u 5ns 5ns 2u 4u)
V3      VDD 0  DC 5 AC 0 0

***** Spice models and macro models *****
```

```
.MODEL CMOSNB NMOS LEVEL=4 ...
.MODEL CMOSPB PMOS LEVEL=4 ...

***** End of spice models and macro models *****

.OPTION ABSTOL=50u RELTOL=.1 VNTOL=5m
.tran 10n 10u 100n 50n
.end
```

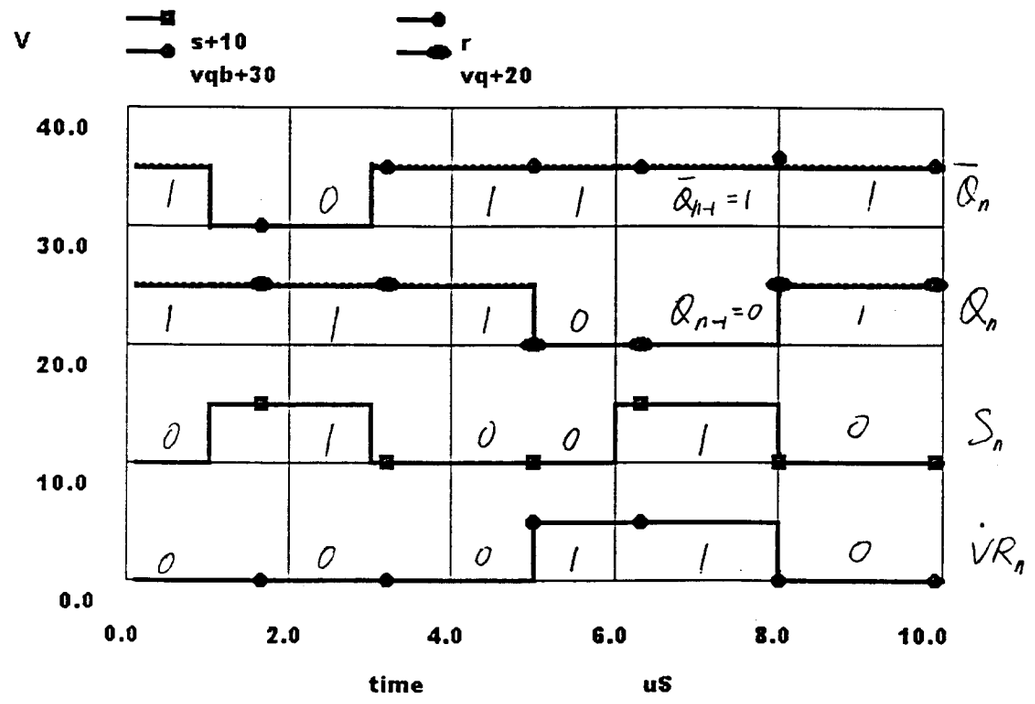


Problem 13.6

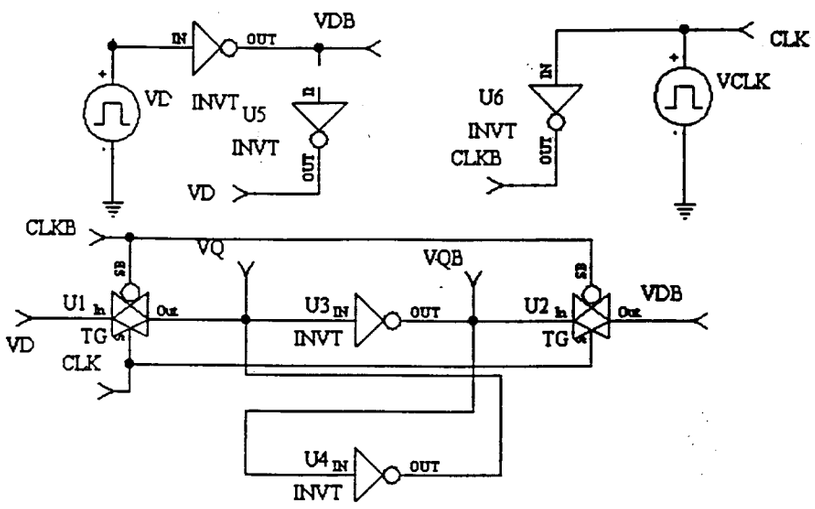
Using minimum-size MOSFETs NAND gates to realize the SR FF. the netlist and simulation results are followed.

```
*** (TurboSim V 1.87) Netlist for C:\TS\445-13-6.CKT
* --
.subckt NAND.sub 6 4 5
M10     2 6 5 2 CMOSPB  L=2u W=3u
M11     2 4 5 2 CMOSPB  L=2u W=3u
M7      1 6 5 0 CMOSNB  L=2u W=3u
M8      0 4 1 0 CMOSNB  L=2u W=3u
V1      2 0     DC 5 AC 0 0
.ends NAND.sub


*** Top Level Netlist ***
```

```
XU1     S VQ VQB      NAND.sub
XU2     R VQB VQ      NAND.sub
VR      R 0     DC 0 AC 0 0 PULSE(0 5 5u 5ns 5ns 3u 6u)
VS      S 0     DC 0 AC 0 0 PULSE(0 5 1u 5ns 5ns 2u 5u)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4 ...
.MODEL CMOSPB PMOS LEVEL=4 ...

***** End of spice models and macro models *****

.OPTION ABSTOL=50u RELTOL=.1 VNTOL=5m
.tran 10n 10u 100n 50n
.end
```



Problem 13.7

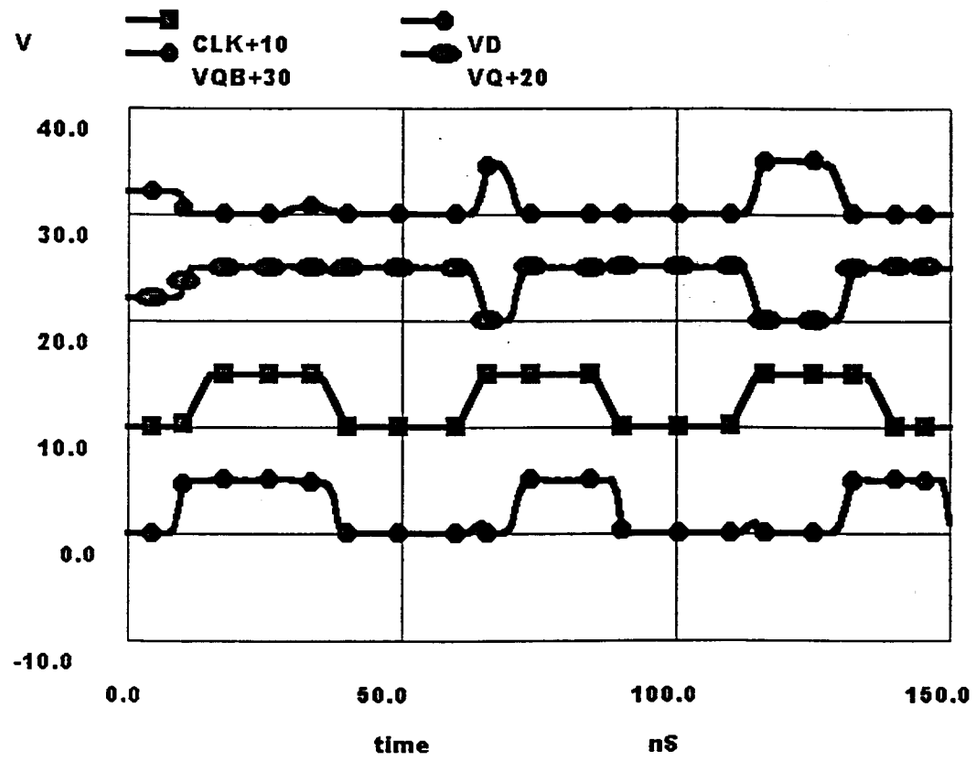


*** (TurboSim V 1.87) Netlist for C:\TS\CIRCUITS\445-13-7.CKT

```
* _
.subckt tg.sub 3 2 6 1
M1      1 2 3 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
M2      3 6 1 8 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
VDD     8 0     DC 5 AC 0 0
.ends tg.sub

* _
.subckt inverter.sub 2 3
M1      0 2 3 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
M2      4 2 3 4 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u NRD=1 NRS=1
VDD     4 0     DC 5 AC 0 0
.ends inverter.sub

*** Top Level Netlist ***
XU1     VQ CLK CLKB VD      tg.sub
XU17    13 VDB          inverter.sub
XU2     VDB CLK CLKB VQB    tg.sub
XU3     VQ VQB          inverter.sub
XU4     VQB VQ          inverter.sub
XU5     VDB VD          inverter.sub
XU6     CLK CLKB        inverter.sub
VCLK    CLK 0  DC 0 AC 0 0 PULSE(0 5 10n 5ns 5ns 20n 50n)
VD      13 0    DC 0 AC 0 0 PULSE(0 5 5n 5ns 5ns 15n 60n)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4
```

***** End of spice models and macro models *****

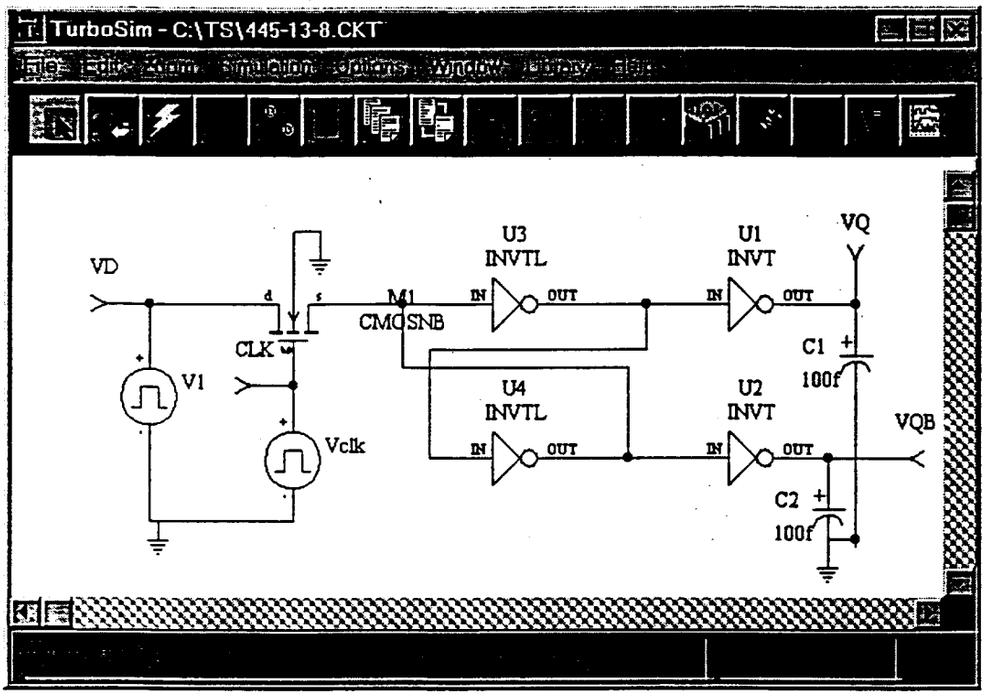
.OPTION ABSTOL=10u RELTOL=.01 VNTOL=5m
.tran 1n 150n 0 1n
.end



Problem 13.8

In order to change the voltage at outputs of U4, the effective digital resistances of this inverters is made large and sinks small current which is provided by the input driver and pass transistor, in another words, make U4 the long L inverter.

The circuit for SPICE simulation is shown below

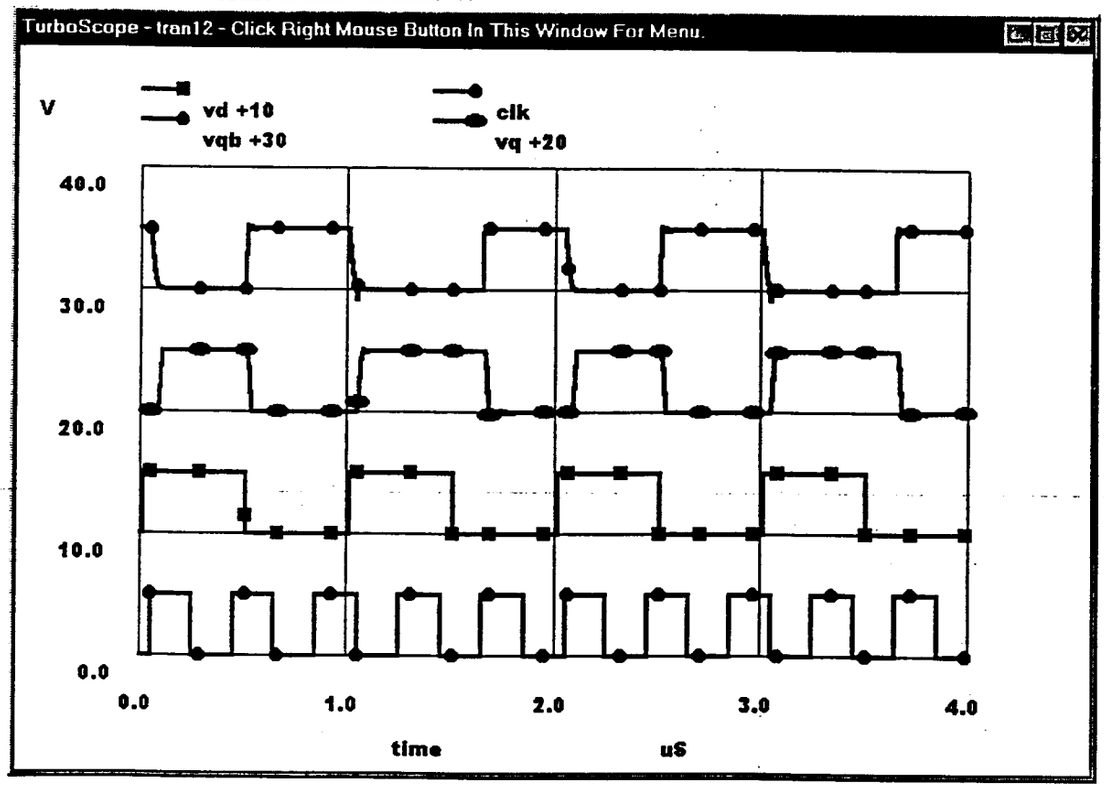


The netlist of this design is shown below.

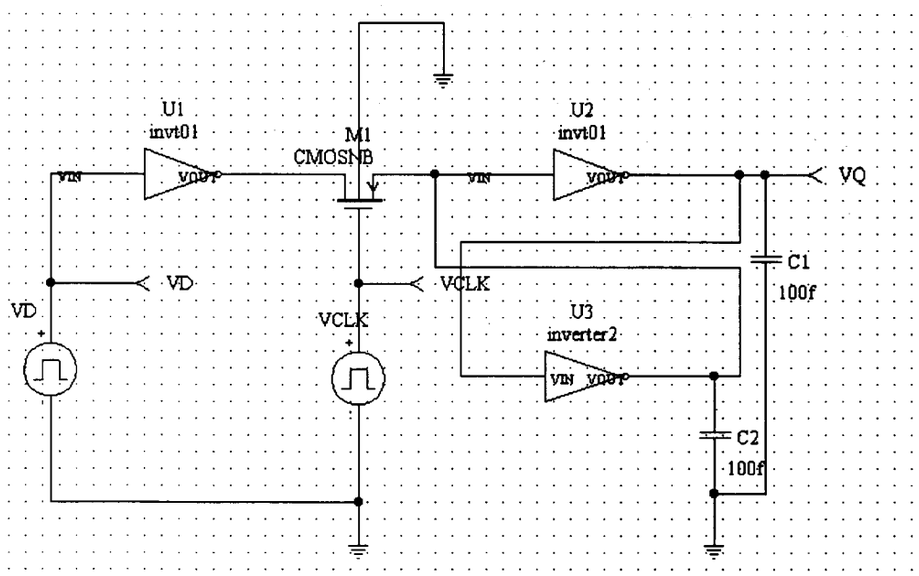
```
*** (TurboSim V 1.87) Netlist for C:\TS\445-13-8.CKT
* --
.subckt invtl.sub 2 3
M1      0 2 3 0 CMOSNB  L=15u W=3u
M2      4 2 3 4 CMOSPB  L=15u W=3u
VDD     4 0     DC 5 AC 0 0
.ends invtl.sub

* --
.subckt inverter.sub 2 3
M1      0 2 3 0 CMOSNB  L=2u W=3u
M2      4 2 3 4 CMOSPB  L=2u W=3u
VDD     4 0     DC 5 AC 0 0
.ends inverter.sub

*** Top Level Netlist ***
C1      VQ 0 100f
C2      VQB 0 100f
M1      VD CLK 13 0 CMOSNB  L=6u W=9u
XU1     10 VQ  inverter.sub
XU2     13 VQB         inverter.sub
XU3     13 10   invtl.sub
XU4     10 13   invtl.sub
V1      VD 0   DC 0 AC 0 0 PULSE(0 5 10n .1n .1n .5u 1u)
Vclk    CLK 0  DC 0 AC 0 0 PULSE(0 5 50n .1n .1n 200n 400n)

***** Spice models and macro models *****
```

```
.MODEL CMOSNB NMOS LEVEL=4 ...
.MODEL CMOSPB PMOS LEVEL=4 ...

***** End of spice models and macro models *****

.OPTION ABSTOL=1u ITL4=100 RELTOL=.1 VNTOL=5mv
.tran 1n 4u 0 10n
.end
```

The simulation result is shown below.



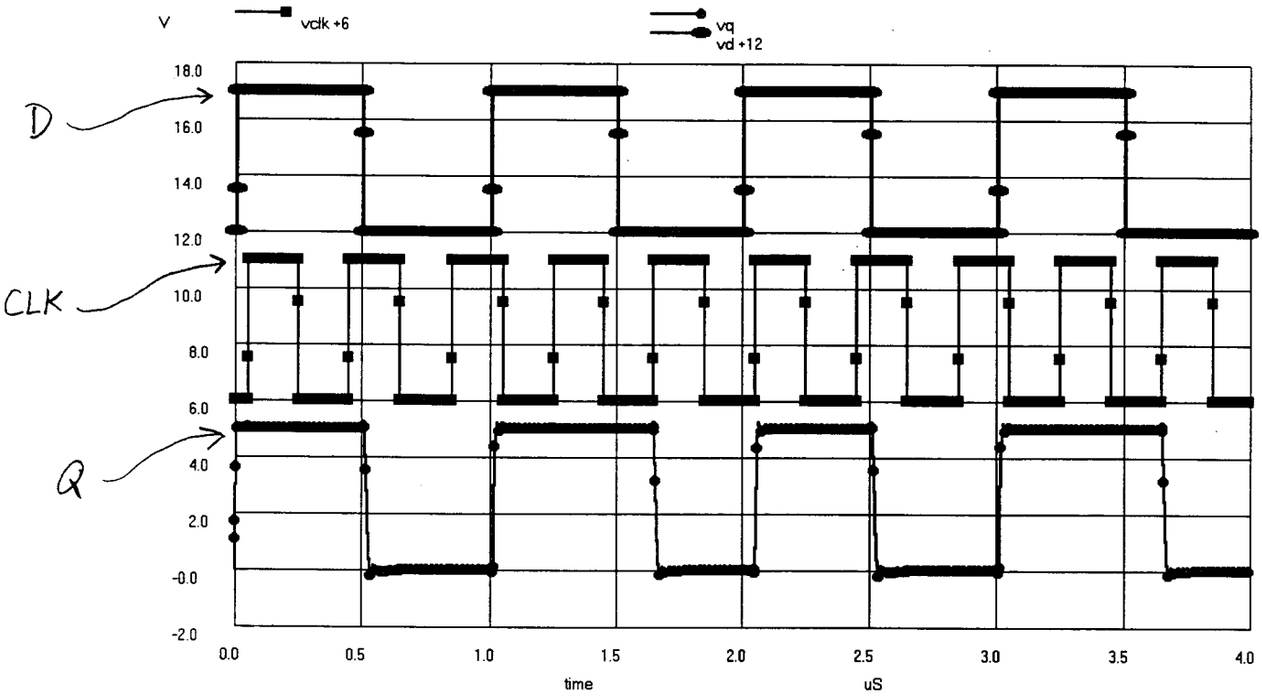
Problem 13.9




```
.subckt invt01.sub 4 1
M1      1 4 0 0 CMOSNB  L=2u W=3u
M2      1 4 3 3 CMOSPB  L=2u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt01.sub

.subckt invt02.sub 4 1
M1      1 4 0 0 CMOSNB  L=15u W=3u
M2      1 4 3 3 CMOSPB  L=15u W=3u
VDD     3 0     DC 5 AC 0 0
.ends invt02.sub

*** Top Level Netlist ***
C1      0 VQ 100f
C2      0 5 100f
M1      2 VCLK 5 0 CMOSNB  L=2u W=3u
XU1     VD 2    invt01.sub
XU2     5 VQ    invt01.sub
XU3     VQ 5    invt02.sub
VCLK    VCLK 0          DC 0 AC 0 0 PULSE(0 5 50n 0.1n 0.1n 200n 400n)
VD      VD 0    DC 0 AC 0 0 PULSE(0 5 10n 0.1n 0.1n 0.5u 1u)

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****
```

.OPTION ABSTOL=1m RELTOL=0.1 VNTOL=50mv
.tran 10n 4u 0 10n uic
.end

The SPICE simulation is shown below:



Problem 13.10

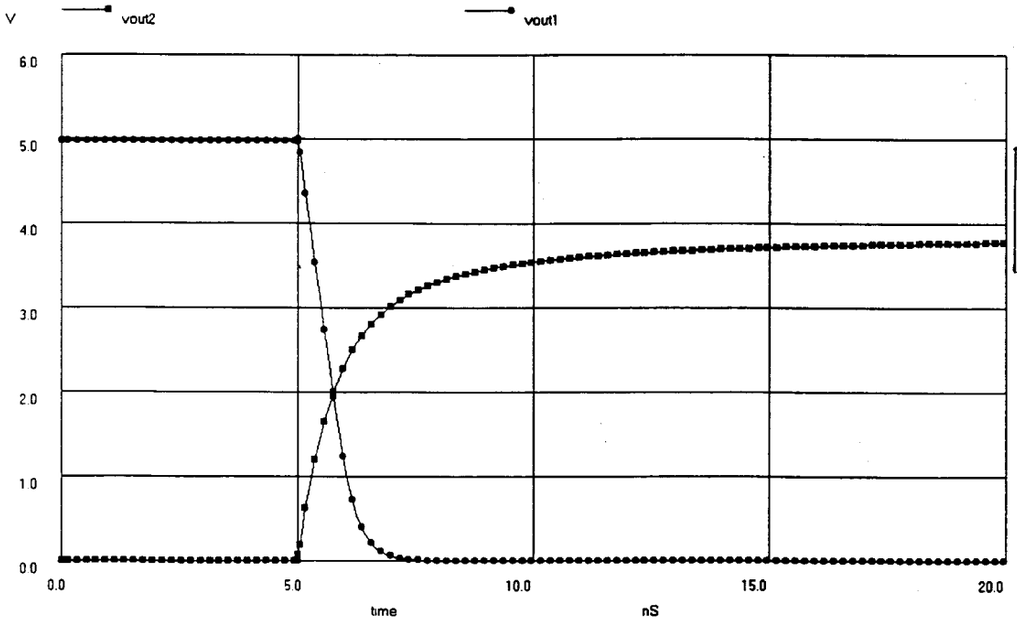
For minimum-size (0.9/0.6) MOSFETs using CMOS14TB process,

$$R_n = \frac{9k\Omega \cdot \mu m}{0.9\mu m} = 10k\Omega$$

$$t_{PHL} = t_{PLH} \cong R_n C_{Load} = 10k\Omega \times 100fF = \underline{\underline{1nS}}$$

```
*** Top Level Netlist ***
C2      0 VOUT2 100f  IC=0
C3      VOUT1 0 100f  IC=5v
M2      2 VG VOUT2 0 CMOSNB5  L=0.6u W=0.9u OFF
M3      VOUT1 VG 0 0 CMOSNB5  L=0.6u W=0.9u
VDD     2 0     DC 5 AC 0 0
VG      VG 0    DC 0 AC 0 0 PULSE(0 5 5n 1p 1p 20n 40n)

***** Spice models and macro models *****

.MODEL CMOSNB5 NMOS LEVEL=4
+ vfb=-9.65360E-01        lvfb= 4.11254E-02        wvfb=-1.21737E-01
... ...
+ pbsw=0.99   mj=0.805   mjsw=0.761   wdf=0   dell=0

***** End of spice models and macro models *****

.OPTION ABSTOL=1m RELTOL=0.1 VNTOL=10mv
.tran 0.1n 20n 0 0.1n uic
.end
```

The SPICE simulation is shown below:



$t_{PHL} \approx 0.62nS$

$t_{PLH} \approx 1.15nS$

Problem 13.11

ANS: The netlist is shown as below:

$R_n = \frac{9\,k\Omega\cdot\mu m}{0.9\,\mu m} = 10\,k\Omega$

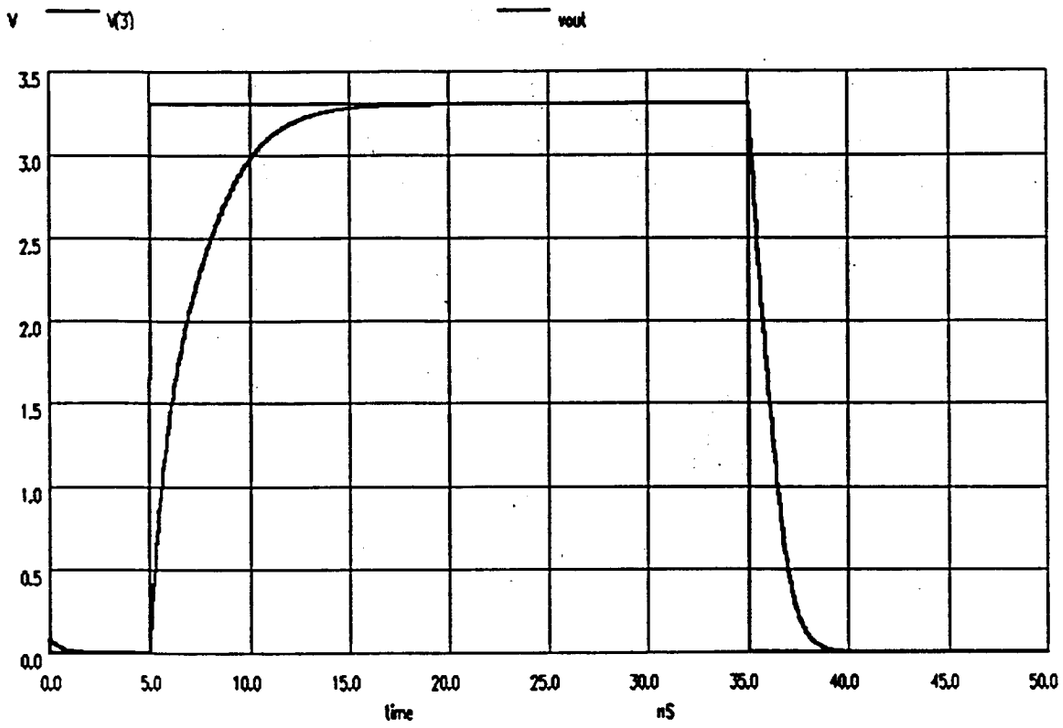
$R_p = \frac{18\,k\Omega\cdot\mu m}{0.9\,\mu m} = 20\,k\Omega$.

$t_{PLH} = t_{PHL} = (R_n \| R_p)150$

$= 1\,ns$

```
*** (TurboSim V 1.87) Netlist for C:\TS\E504\P1311.CKT
*** Top Level Netlist ***
.ic          V(Vout)=0
C1           0 Vout 150f
M1           Vout 2 3 0 CMOSNB5  L=0.6u W=0.9u AD=3.24p AS=3.24p PD=7.2u PS=7.2u NRD=1 NRS=1
M2           3 0 Vout 2 CMOSPB5  L=0.6u W=0.9u AD=3.24p AS=3.24p PD=7.2u PS=7.2u NRD=1 NRS=1
VDD          2 0          DC 3.3 AC 0 0
Vin          3 0          DC 0 AC 0 0 PULSE(0 3.3 5ns 0.05ns 0.05ns 30ns 60ns)
***** Spice models and macro models *****
.MODEL CMOSNB5 NMOS LEVEL=4
+ vfb=-9.65360E-01  lvfb= 4.11254E-02    wvfb=-1.21737E-01
+ phi= 9.02436E-01  lphi= 0.00000E+00    wphi= 0.00000E+00
+ k1= 9.33674E-01   lk1= -8.15872E-02    wk1= 2.03526E-01
+ k2= 7.39228E-02   lk2= 1.48295E-02     wk2= 5.89097E-02
+ eta=-2.77969E-03  leta= 1.12296E-02    weta= 1.25263E-03
+ muz= 4.71133E+02              dl= 1.57937E-001    dw= 4.09563E-001
+ u0= 1.98427E-01   lu0= 1.54850E-01     wu0= -1.05429E-01
+ u1= 3.39403E-02   lu1= 3.59469E-02     wu1= -5.00497E-03
+ x2mz=1.25728E+01              lx2mz=-1.24115E+01              wx2mz=1.77657E+01
+ x2e=-9.95217E-05              lx2e=-5.16949E-03    wx2e= 2.83253E-03
+ x3e=-4.27269E-04              lx3e=-1.62632E-03    wx3e=-1.60797E-03
+ x2u0=-9.02747E-04             lx2u0=-1.66946E-02   wx2u0=2.48458E-02
+ x2u1=-7.29822E-04             lx2u1=2.38803E-03    wx2u1=-9.76918E-04
+ mus=5.36631E+02               lmus=2.18647E+01     wmus=4.43373E+00
+ x2ms=5.97403E+00              lx2ms=-7.67105E+00              wx2ms=2.19614E+01
+ x3ms=7.60054E+00              lx3ms=4.73779E+00               wx3ms=2.59952E+00
+ x3u1=1.75532E-02              lx3u1=-1.21628E-03   wx3u1=-5.95548E-04
+ tox=9.60000E-003              temp=2.70000E+01     vdd=3.30000E+00
+ cgdo=4.26077E-010             cgso=4.26077E-010    cgbo=4.01709E-010
+ xpart=1.00000E+000
+ n0=1.00000E+000               ln0=0.00000E+000     wn0=0.00000E+000
+ nb=0.00000E+000               lnb=0.00000E+000     wnb=0.00000E+000
+ nd=0.00000E+000               lnd=0.00000E+000     wnd=0.00000E+000
+ rsh=2  cj=6.02e-04  cjsw=2.0e-11  js=1e-08  pb=0.99
+ pbsw=0.99  mj=0.805  mjsw=0.761  wdf=0  dell=0

.MODEL CMOSPB5 PMOS LEVEL=4
+ vfb=-2.80568E-01  lvfb=5.70163E-02     wvfb=-6.17493E-02
+ phi=8.14689E-01   lphi=0.00000E+00     wphi=0.00000E+00
+ k1=4.52973E-01    lk1=-9.19899E-02     wk1=1.20834E-01
+ k2=-9.42157E-03   lk2=-2.25562E-03     wk2=3.13315E-02
+ eta=-7.03956E-03  leta=1.92833E-02     weta=5.45445E-05
+ muz=1.36047E+02               dl=1.85988E-001     dw=4.32366E-001
+ u0=1.93813E-01    lu0=6.02231E-02      wu0=-4.90734E-02
+ u1=8.52399E-03    lu1=2.60545E-02      wu1=-6.34371E-03
+ x2mz=7.96258E+00              lx2mz=-2.15761E+00              wx2mz=2.30663E+00
+ x2e=4.37912E-04               lx2e=-1.60046E-03    wx2e=-3.86750E-04
+ x3e=-3.52725E-04              lx3e=-4.09096E-04    wx3e=-2.53471E-03
+ x2u0=1.18873E-02              lx2u0=-4.81760E-03   wx2u0=8.80040E-03
+ x2u1=2.26591E-03              lx2u1=7.96828E-04    wx2u1=-4.70527E-04
+ mus=1.44421E+02               lmus=1.63665E+01     wmus=-7.31189E-01
+ x2ms=8.18970E+00              lx2ms=-1.25158E+00              wx2ms=3.62233E+00
+ x3ms=7.29640E-01              lx3ms=1.15206E+00               wx3ms=1.02833E+00
+ x3u1=-3.51521E-03             lx3u1=-3.12374E-03   wx3u1=3.48134E-03
+ tox=9.60000E-003              temp=2.70000E+01     vdd=3.30000E+00
+ cgdo=5.01753E-010             cgso=5.01753E-010    cgbo=4.14187E-010
+ xpart=1.00000E+000
+ n0=1.00000E+000               ln0=0.00000E+000     wn0=0.00000E+000
+ nb=0.00000E+000               lnb=0.00000E+000     wnb=0.00000E+000
+ nd=0.00000E+000               lnd=0.00000E+000     wnd=0.00000E+000
+ rsh=2.1  cj=9.34e-04  cjsw=2.41e-10  js=1e-08  pb=0.90
+ pbsw=0.90  mj=0.491  mjsw=0.222  wdf=0  dell=0

***** End of spice models and macro models *****
.OPTION ABSTOL=10u VNTOL=1mv
.tran 0.05ns 50ns 0 0.05ns uic
.end
```

The plot indicates that the t_{PLH} is about 1ns and the t_{PHL} is about 0.8ns.

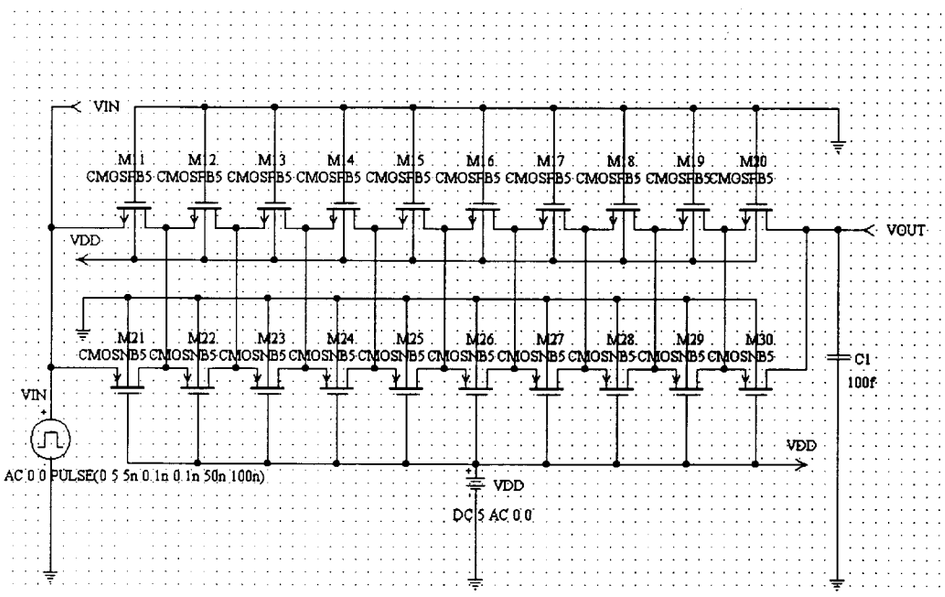


Problem 13.12

$$t_{PHL} = t_{PLH} = N \times (R_n // R_p) \times (C_{Load}) + 0.35 (R_n // R_p)(C_{inn} + C_{inp}) N^2$$

$$= 10 \times (10k // 20k) \times 100fF + 0.35 \times (10k // 20k) \times \frac{3}{2} \times 3.7 \frac{fF}{\mu m^2} \times (0.6 \times 0.9) \times 2 \mu m^2 \times 10^2$$

$$\simeq 8.07 nS$$

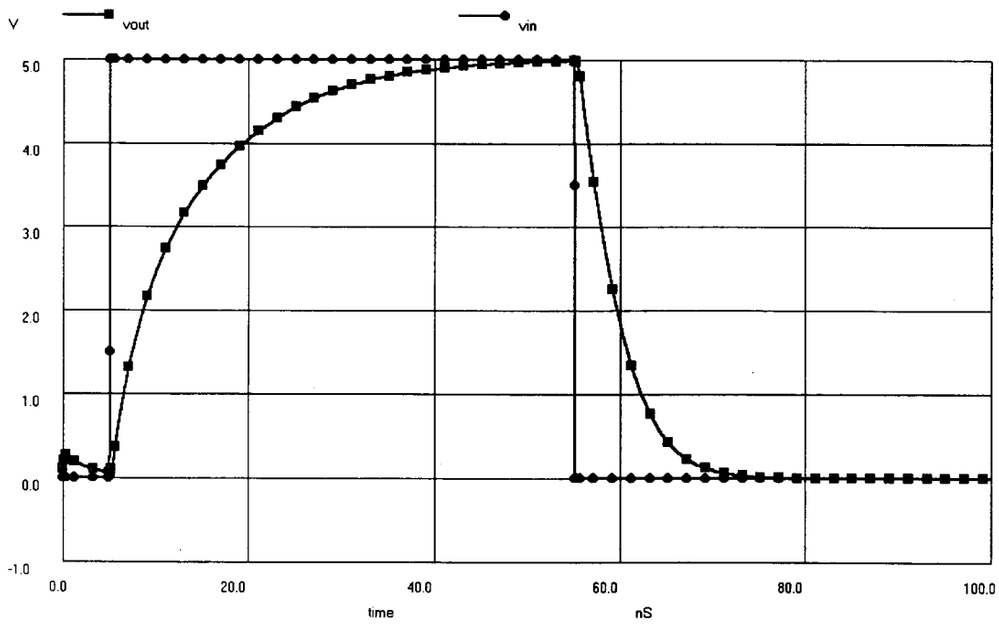


*** Top Level Netlist ***

```
C1      0 VOUT 100f  IC=0
M11     1 0 VIN VDD CMOSPB5  L=0.6u W=0.9u
M12     4 0 1 VDD CMOSPB5  L=0.6u W=0.9u
M13     5 0 4 VDD CMOSPB5  L=0.6u W=0.9u
M14     6 0 5 VDD CMOSPB5  L=0.6u W=0.9u
M15     7 0 6 VDD CMOSPB5  L=0.6u W=0.9u
M16     8 0 7 VDD CMOSPB5  L=0.6u W=0.9u
M17     9 0 8 VDD CMOSPB5  L=0.6u W=0.9u
M18     10 0 9 VDD CMOSPB5  L=0.6u W=0.9u
M19     11 0 10 VDD CMOSPB5  L=0.6u W=0.9u
M20     VOUT 0 11 VDD CMOSPB5  L=0.6u W=0.9u
M21     1 VDD VIN 0 CMOSNB5  L=0.6u W=0.9u
M22     4 VDD 1 0 CMOSNB5  L=0.6u W=0.9u
```

```
M23     5 VDD 4 0 CMOSNB5  L=0.6u W=0.9u
M24     6 VDD 5 0 CMOSNB5  L=0.6u W=0.9u
M25     7 VDD 6 0 CMOSNB5  L=0.6u W=0.9u
M26     8 VDD 7 0 CMOSNB5  L=0.6u W=0.9u
M27     9 VDD 8 0 CMOSNB5  L=0.6u W=0.9u
M28     10 VDD 9 0 CMOSNB5  L=0.6u W=0.9u
M29     11 VDD 10 0 CMOSNB5  L=0.6u W=0.9u
M30     VOUT VDD 11 0 CMOSNB5  L=0.6u W=0.9u
VDD     VDD 0  DC 5 AC 0 0
VIN     VIN 0   DC 0 AC 0 0 PULSE(0 5 5n 0.1n 0.1n 50n 100n)

***** Spice models and macro models *****

.MODEL CMOSPB5 PMOS LEVEL=4

.MODEL CMOSNB5 NMOS LEVEL=4

***** End of spice models and macro models *****

.OPTION ABSTOL=1m RELTOL=0.1 VNTOL=50mv
.tran 1n 100n 0 1n uic
.end
```

The SPICE simulation is shown below:



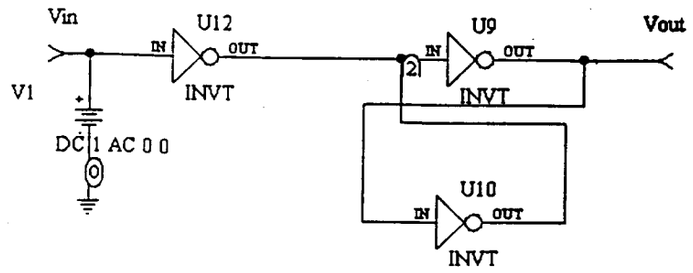
Simulation results

$t_{PLH} \simeq 5.2nS$

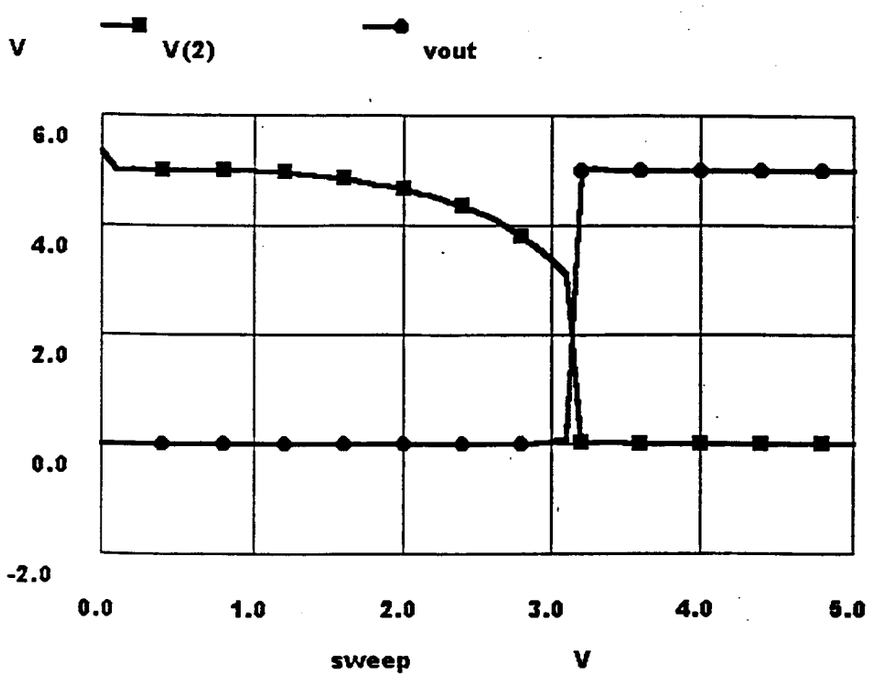
$t_{PHL} \simeq 4.0nS$

Problem 13.13.

Since voltage source used in SPICE can provide infinite current, we use an inverter to simulate the more practical condition.



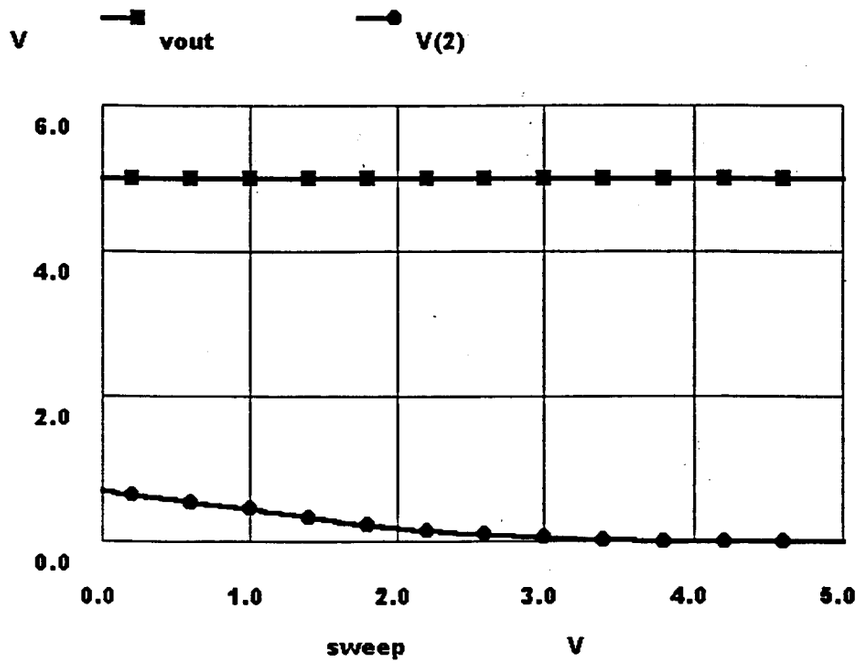
1) Vin from 0 to 5v



The switching point is moved to about 3.2v and has bad noise performance.

2) Vin from 5 to 0

In this case, for all minimum size inverters, this circuit doesn't work. The reason is the inverter U10 will sink a lot of current (through the nmos transistor) and pull down the node 2 before inverter U9 far below the switching point of U9, and U9 can never change state. From the simulation results, the output stays in 5V (High) and node voltage V2 is just around threshold voltage. Use long L device of U10 will make this circuit work.


V
vout
V(2)
6.0
4.0
2.0
0.0
0.0
1.0
2.0
3.0
4.0
5.0
sweep
V