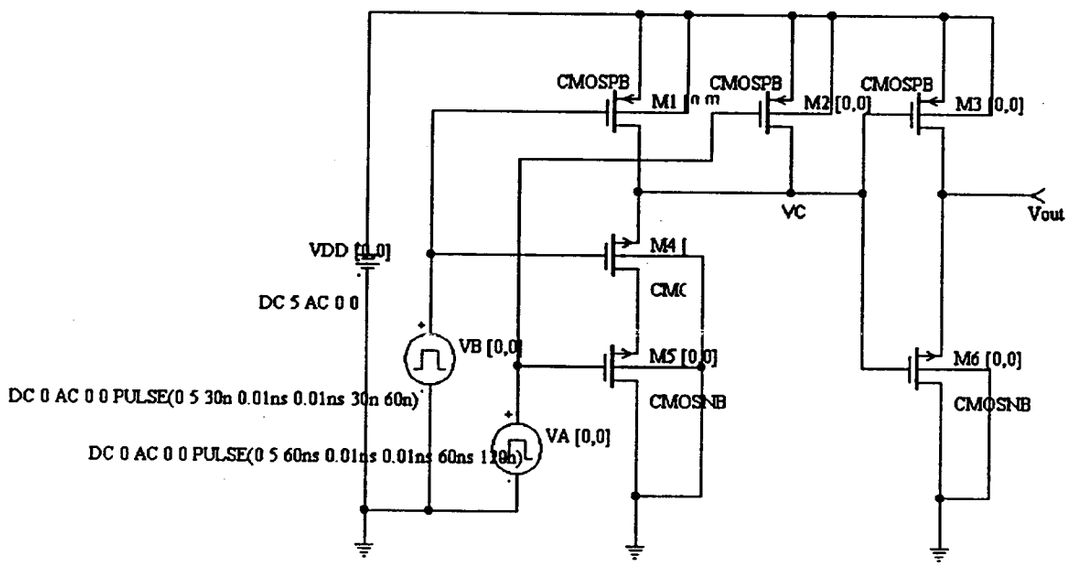
Problem 12.1

Solution: a) Design and hand-cal: The 2-input CMOS AND gate circuit diagram is shown below which consists of two parts NAND and INVERTOR cascaded:



To find Vsp, tie input A and B together as Vin. From NAND gate part, ignoring the body effect, we have

$$Vc = Vin = Vsp = \frac{\sqrt{\frac{\beta n}{4\beta p}}Vthn + (Vdd - Vthp)}{1 + \sqrt{\frac{\beta n}{4\beta p}}} \qquad (12.1a)$$

$$Vout = Vc = Vsp = \frac{\sqrt{\frac{\beta n}{\beta p}}Vthn + (Vdd - Vthp)}{1 + \sqrt{\frac{\beta n}{\beta p}}} \qquad (12.1b)$$

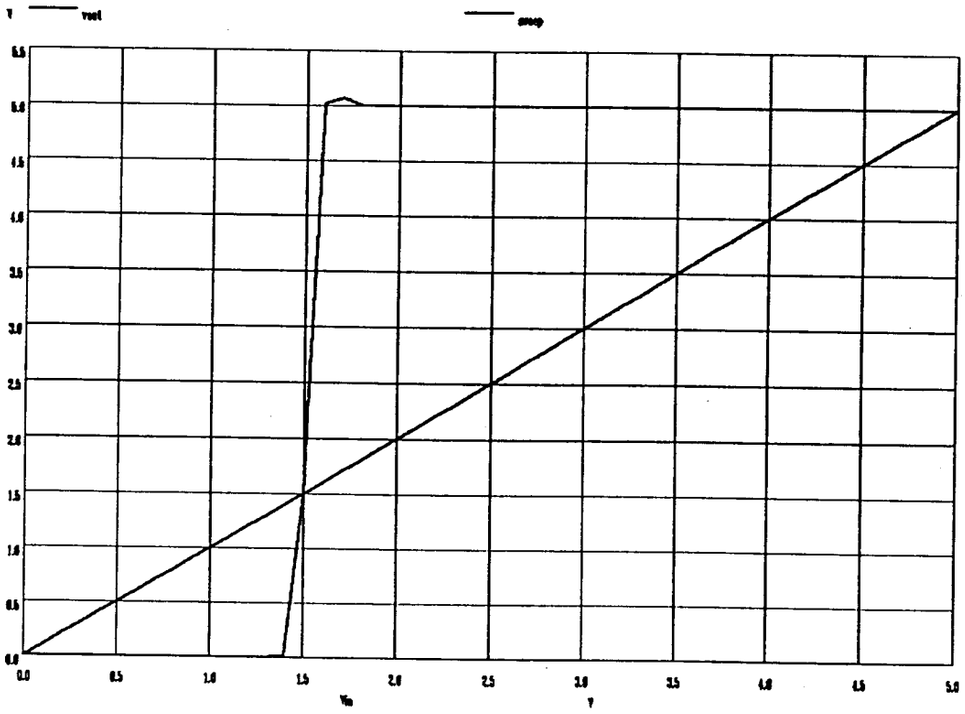
Vthn=0.83V, Vthp=0.91V, chosing all the length of CMOS L=2u, all Wp=3u for p-channel. Let both Vsp expression equals to 1.5 V, ==>> W4=W5=60u, W6=15u.

b) Spice simulation: The following netlist was simulated on TurboSim:

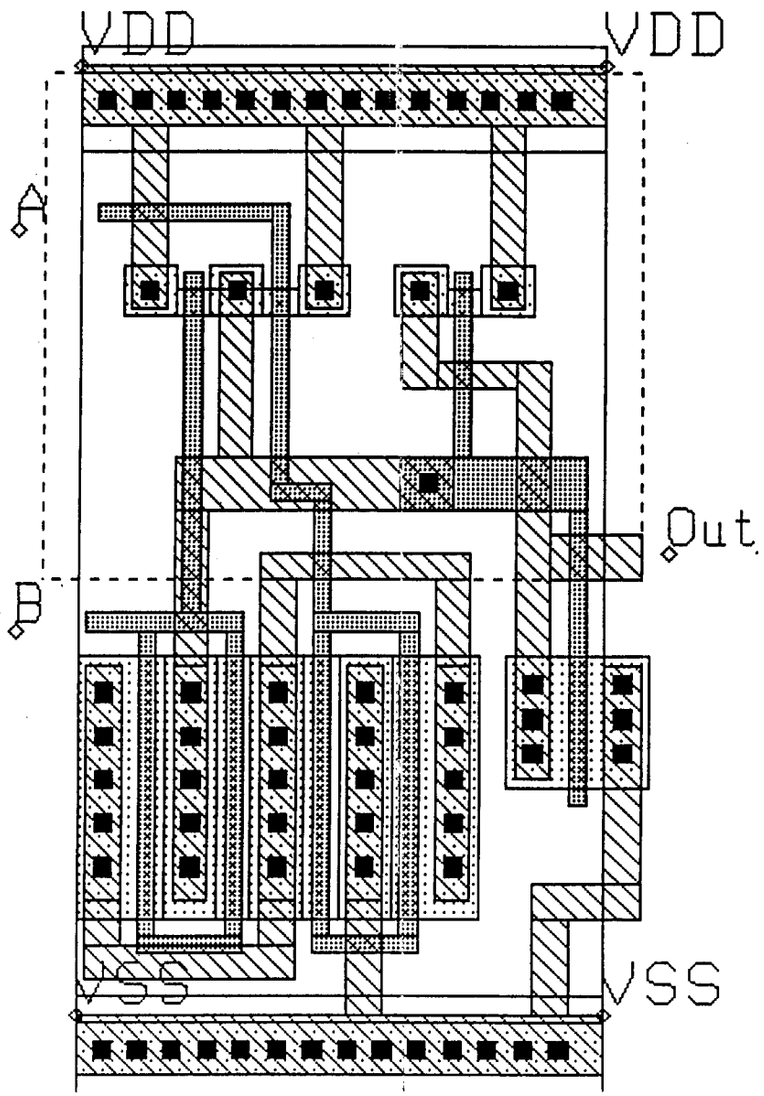
Problem 12.1 (cont.)

```
*** (TurboSim V 1.1) Netlist for C:\TS\E504\P1201DC.CKT

*** Top Level Netlist ***
M1        1 6 2 2 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M2        1 6 2 2 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M3        Vout 1 2 2 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M4        4 6 1 0 CMOSNB  L=2u W=60u AD=3600p AS=360p PD=132u PS=132u
M5        0 6 4 0 CMOSNB  L=2u W=60u AD=360p AS=360p PD=132u PS=132u
M6        0 1 Vout 0 CMOSNB  L=2u W=15u AD=90p AS=90p PD=42u PS=42u
VDD       2 0       DC 5 AC 0 0
Vin       6 0       DC 1 AC 0 0

***** Spice models and macro models *****

.MODEL CMOSPB PMOS LEVEL=4
** PMOS BSIM parameters **

.Model CMOSNB NMOS LEVEL=4
** NMOS BSIM parameters **

***** End of spice models and macro models *****

.OPTION ABSTOL=1m CHGTOL=1n ITL1=1000 ITL2=1000 ITL4=10 RELTOL=0.1
+ VNTOL=10mv
.DC Vin 0 5 0.1
.end
```

which produce the following plot. It gives Vsp 1.5V exact same as the hand calculation.

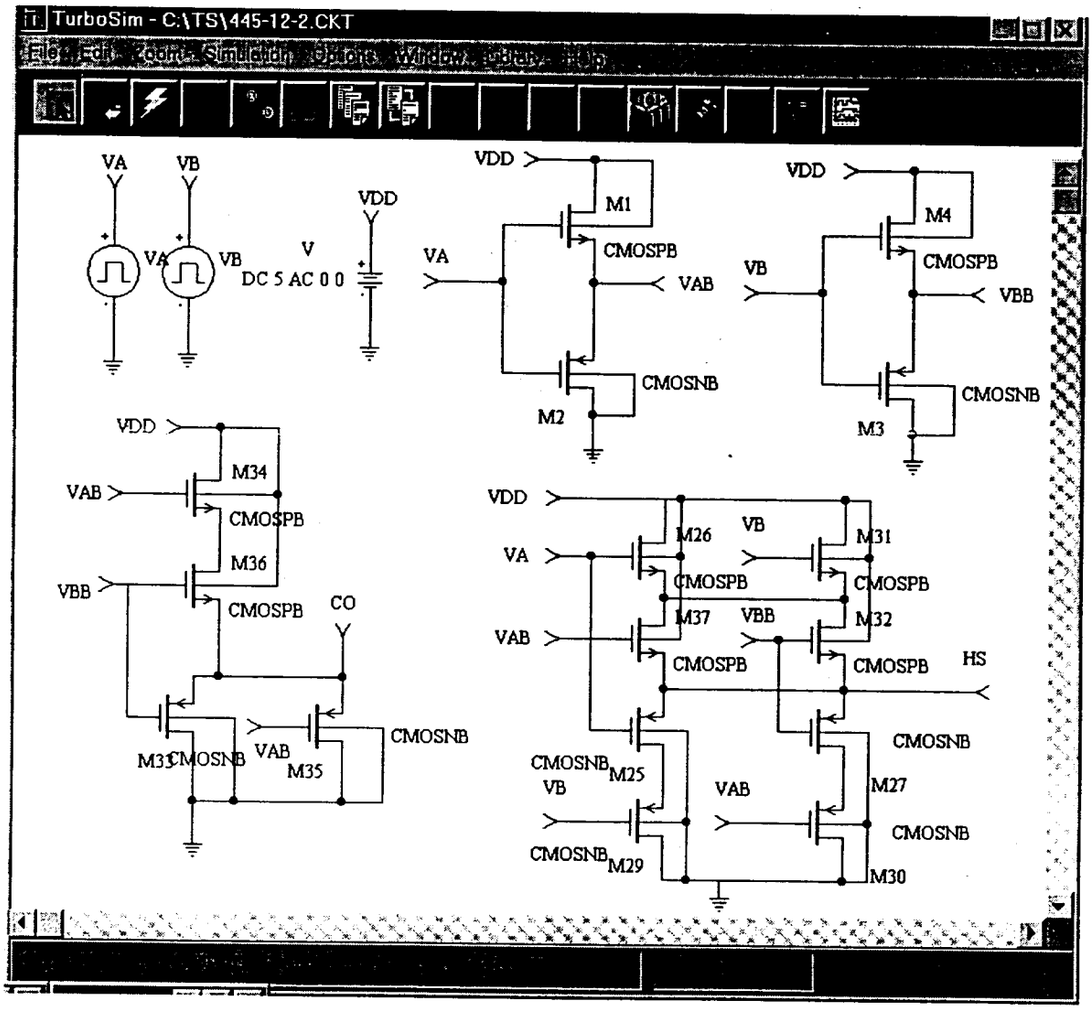


Problem 12-1 (cont.)



Problem 12.2

Solution: The following schematic using AOI to build a half adder is simulated on TurboSim:

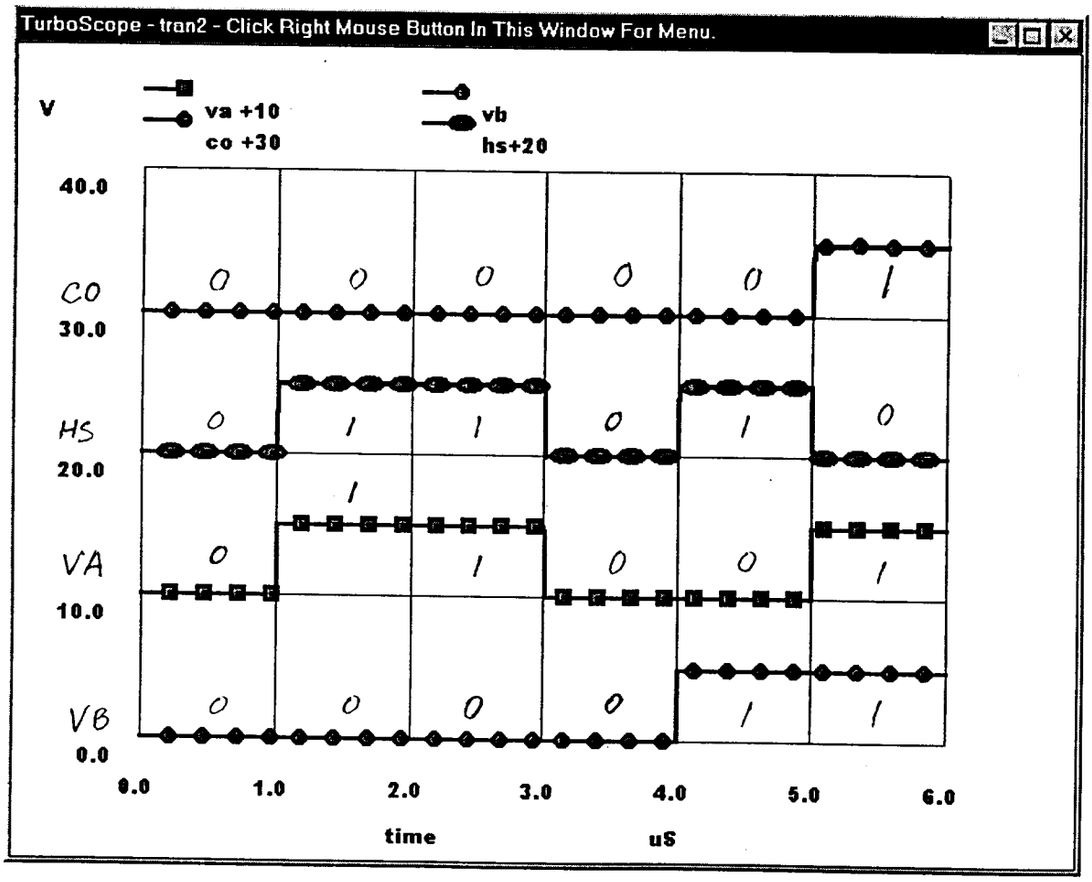


*** (TurboSim V 1.87) Netlist for C:\TS\445-12-2.CKT

*** Top Level Netlist ***

M1 VDD VA VAB VDD CMOSPB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M2 0 VA VAB 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M25 8 VA HS 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M26 VDD VA 7 VDD CMOSPB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M27 6 VBB HS 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M29 0 VB 8 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M3 0 VB VBB 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M30 0 VAB 6 0 CMOSNB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M31 VDD VB 7 VDD CMOSPB L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M32 7 VBB HS VDD CMOSPB L=2u W=3u AD=36p AS=36p PD=24u PS=24u

```
M33     0 VBB CO 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M34     VDD VAB 10 VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M35     0 VAB CO 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M36     10 VBB CO VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M37     7 VAB HS VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M4      VDD VB VBB VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
V       VDD 0  DC 5 AC 0 0
VA      VA 0    DC 0 AC 0 0 PULSE(0 5 1u 5ns 5ns 2u 4u)
VB      VB 0    DC 0 AC 0 0 PULSE(0 5 4u 5ns 5ns 2u 4u)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4
.MODEL CMOSPB PMOS LEVEL=4

***** End of spice models and macro models *****

.OPTION ABSTOL=1u CHGTOL=1p ITL2=500 ITL4=400 RELTOL=0.01 VNTOL=5m
.tran 5ns 6u 0 5n
.end
```



Problem 12.3

Solution: For N-input NOR gate, we have:

$t_{PLH} = NRp(Coutp / N + NCoutn + Cload) + 0.35RpCinp(N-1)^2$ (12.3a)

$t_{PHL} = (Rn / N)(NCoutn + Coutp / N + Cload)$ (12.3b)

With minimum size MOSFEF, Rn=8kΩ, Rp=24kΩ, Coutn=Coutp=4.8fF, Cinp=7.2fF. and 3input.

a) With Cload=0:

$t_{PLH} = 3x24k(4.8f / 3 + 3x4.8f + 0) + 0.35x24kx7.2f(3-1)^2 = 1.394ns$

$t_{PHL} = (8k / 3)(3x4.8f + 4.8f / 3 + 0) = 42.67ps$

b) With Cload=100fF:

$t_{PLH} = 3x24k(4.8f / 3 + 3x4.8f + 100) + 0.35x24kx7.2f(3-1)^2 = 8.594ns$

$t_{PHL} = (8k / 3)(3x4.8f + 4.8f / 3 + 100) = 309ps$

It can be seen that for 3-input NOR gate, the $t_{PLH} > t_{PHL}$, while for 3-input NAND gate, the $t_{PLH} < t_{PHL}$, also that the maximum delay time of NOR is bigger than the maximum delay time of NAND. Plus we already know that NAND gate has better Vsp and better noise margins. That is why in CMOS digital design, the NAND gate is used most often.

c) SPICE simulation is shown in the next page.

Problem 12.4

Solution: For N-input NOR gate, a more useful, but not as precise, equations to estimate the delay are:

$t_{PLH} = NRpCload$ (12.4a)

$t_{PHL} = RnCload$ (12.4b)

With minimum size MOSFEF, Rn=8kΩ, Rp=24kΩ, Cload=100fF. and 3input.

$t_{PLH} = 3x24kx100 = 7.2ns$

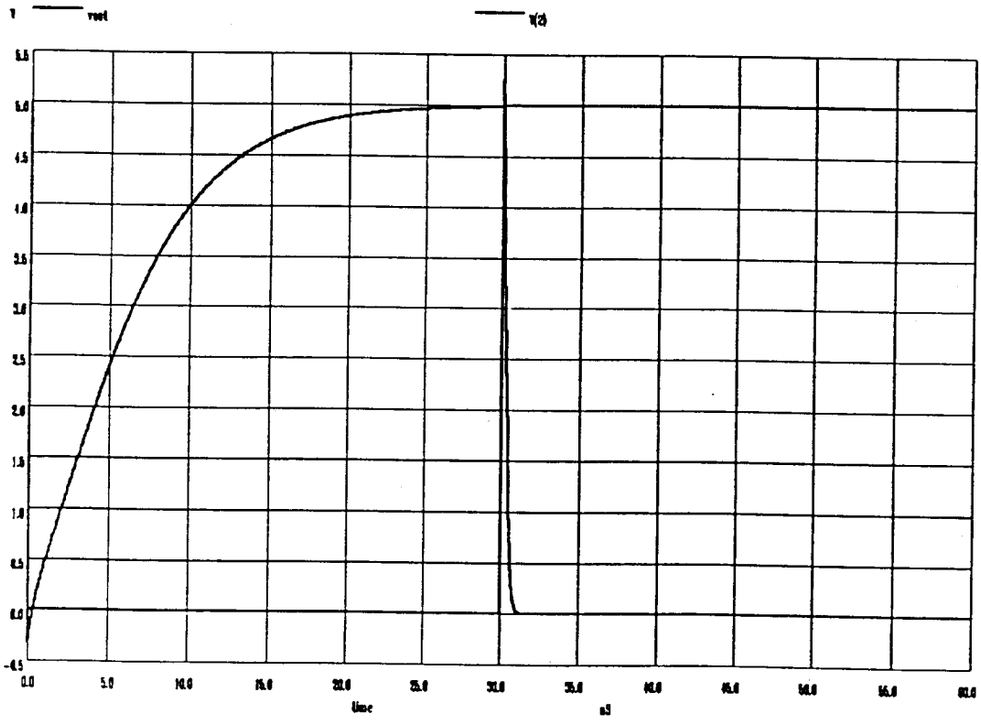
$t_{PHL} = 8kx100 = 800ps$

Problem 12.3 SPICE simulation:

Netlist:

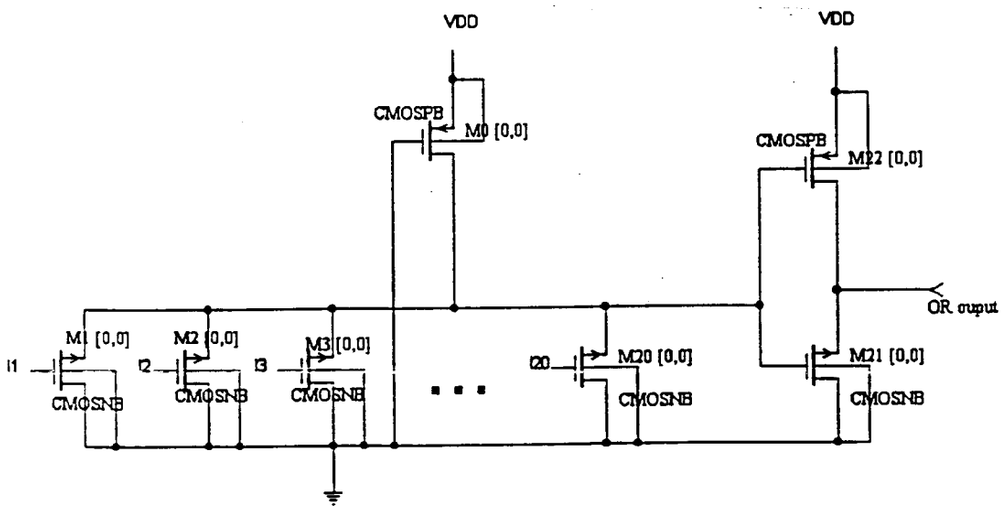
```
*** (TurboSim V 1.1) Netlist for C:\TS\E504\H5\P1203.CKT

*** Top Level Netlist ***
C1      Vout 0 100f
M1      0 2 Vout 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M2      0 2 Vout 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M3      0 2 Vout 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M4      Vout 2 4 5 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M5      4 2 6 5 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M6      6 2 5 5 CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
V2      2 0       DC 0 AC 0 0 PULSE(5 0 0 5ps 5ps 30ns 60ns)
VDD     5 0       DC 5 AC 0 0

***** Spice models and macro models *****
.Model CMOSNB NMOS LEVEL=4
...BSIM Parameters of Appendix A...
.MODEL CMOSPB PMOS LEVEL=4
...BSIM Parameters of Appendix A...
***** End of spice models and macro models *****
.OPTION ABSTOL=1u CHGTOL=1n ITL1=500 ITL2=500 ITL4=500 RELTOL=0.1
+ VNTOL=10mv
.tran 0.1n 60n 0 0.1n
.end
```

Plot is as below, simulation gives t_{PLH} about 5ns, t_{PHL} about 300ps(when zoom in):



Problem 12.5

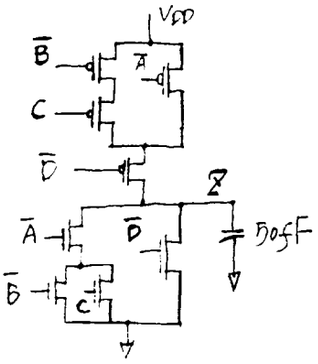
Solution: The 20-input OR gate is consist of an 20-input NOR and an INVERTOR. For 20 input, the scheme of NOR shown in figure 12.4 is not practical because of the long delay time associated with the 20 p-channel MOSFET in series and requiring total 40 MOSFETs. So, the scheme of NOR shown in figure 12.11 is needed. The schematic of an OR gate with 20 inputs is shown below which uses 23 MOSFETs:



For all the n-channel MOSFET, chose Wn=3u, Ln=2u, for p-channel, chose W22p=3u, L22p=2u. By using equation (12.21), set VOL about 500mv, get W0p=L0n=3u. When the ouput is low, the static power dissipation of the OR gate is about zero, but static power is dissipated when the output is high due to both n- and p-channel of NOR part conducting.

Ploblem 12.6

$$Z = (A + B\cdot\bar{C})\cdot D \;,\quad \bar{Z} = \bar{A}(\bar{B}+C)+\bar{D} \Rightarrow Z = \overline{\bar{A}(\bar{B}+C)+\bar{D}}$$



Chosing minimum size ($^{34}/_{2u}$) for all MOSFETs.

$R_n = 8k\Omega$, $R_p = 24k\Omega$, $C_{outn} = C_{outp} = C = 4.8fF$.

Worst-case delay: $\bar{B}, C, \bar{D}$ ON, for t_{pLH}

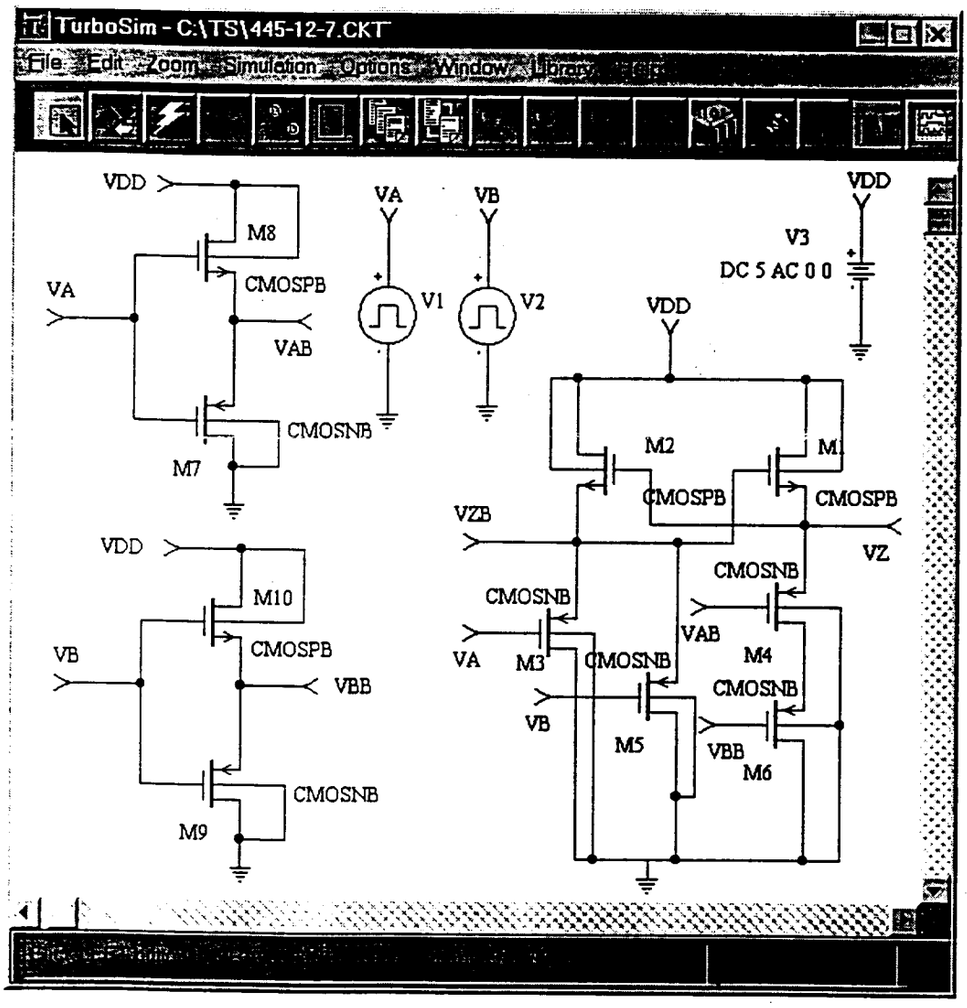
$$t_{pLH} = 3R_p\cdot C_{load} + 3R_p\left[C_{outn}(\bar{D}) + \frac{C_{outn}(\bar{A})\times 2C}{C_{outn}(\bar{A})+2C} + \frac{C_{outp}(\bar{D})\times\frac{3}{2}C}{C_{outp}(\bar{D})+\frac{3}{2}C}\right]$$

$$= 3R_p\left[C_{load} + C + \frac{2}{3}C + \frac{3}{5}C\right]$$

$$= 3\times 24k\Omega \times \left(50 + \frac{34}{15}\times 4.8\right)fF \approx \underline{\underline{44ns}}.$$

Problem 12.7

The following schematic using CSVL to build a OR gate with minimum-size devices.



*** Top Level Netlist ***

```
M1      VDD VZB VZ VDD CMOSPB  L=2u W=3u
M10     VDD VB VBB VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M2      VDD VZ VZB VDD CMOSPB  L=2u W=3u
M3      0 VA VZB 0 CMOSNB  L=2u W=3u
M4      6 VAB VZ 0 CMOSNB  L=2u W=3u
M5      0 VB VZB 0 CMOSNB  L=2u W=3u
M6      0 VBB 6 0 CMOSNB  L=2u W=3u
M7      0 VA VAB 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M8      VDD VA VAB VDD CMOSPB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
M9      0 VB VBB 0 CMOSNB  L=2u W=3u AD=36p AS=36p PD=24u PS=24u
V1      VA 0    DC 0 AC 0 0 PULSE(0 5 1u 5ns 5ns 2u 4u)
V2      VB 0    DC 0 AC 0 0 PULSE(0 5 4u 5ns 5ns 2u 4u)
V3      VDD 0  DC 5 AC 0 0
```

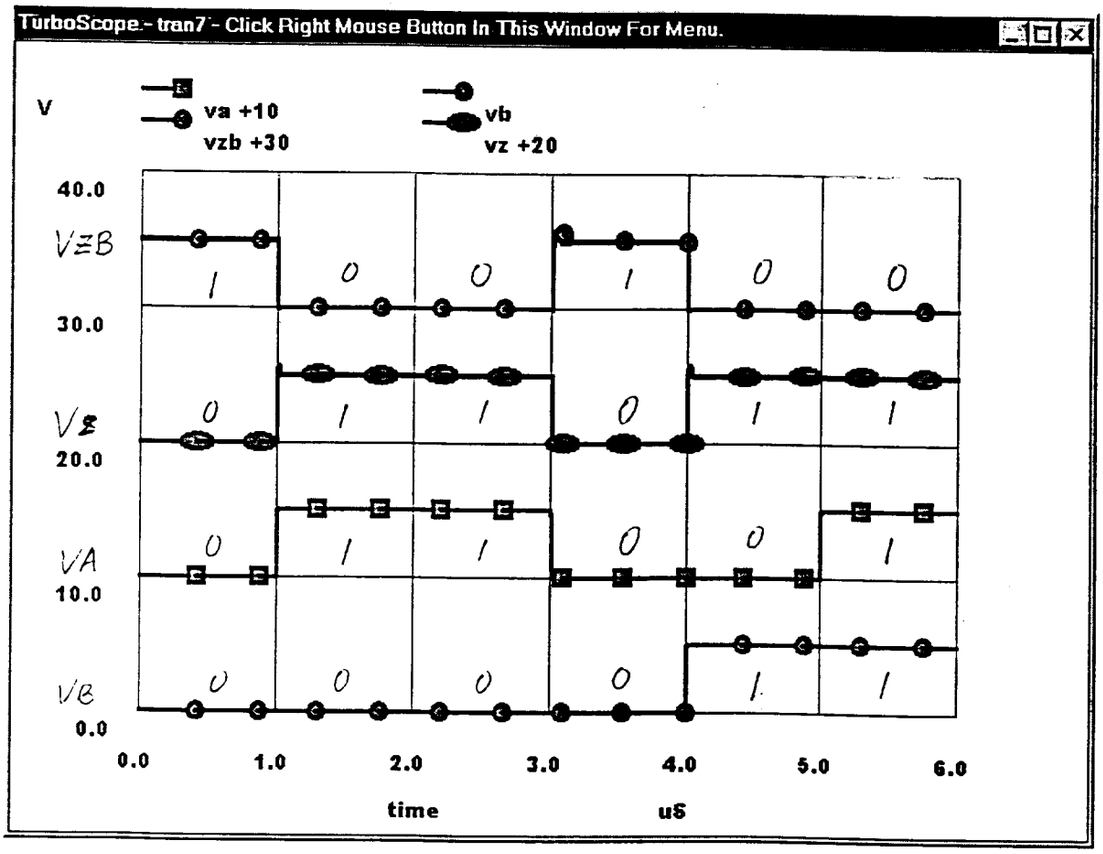
***** Spice models and macro models *****

.MODEL CMOSPB PMOS LEVEL=4
.MODEL CMOSNB NMOS LEVEL=4

***** End of spice models and macro models *****

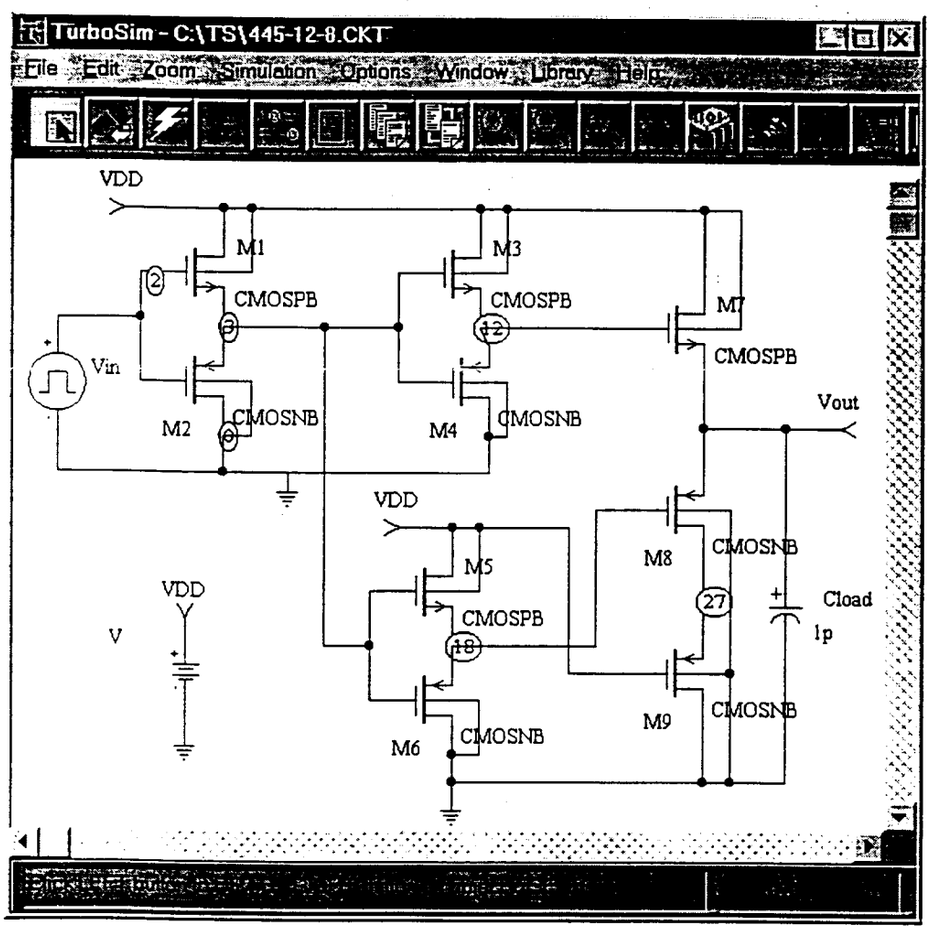
.OPTION ABSTOL=1u ITL4=100 RELTOL=.1 VNTOL=5mv
.tran 5n 6u 0 5n
.end

The simulation produced the following plot with labels.



Problem 12.8

Using tri-state inverting buffer (Fig 12.24), assume Enable at logic high. Design the circuit as following. The input capacitance is 48fF and the propagation delay is under 10ns.



*** Top Level Netlist ***

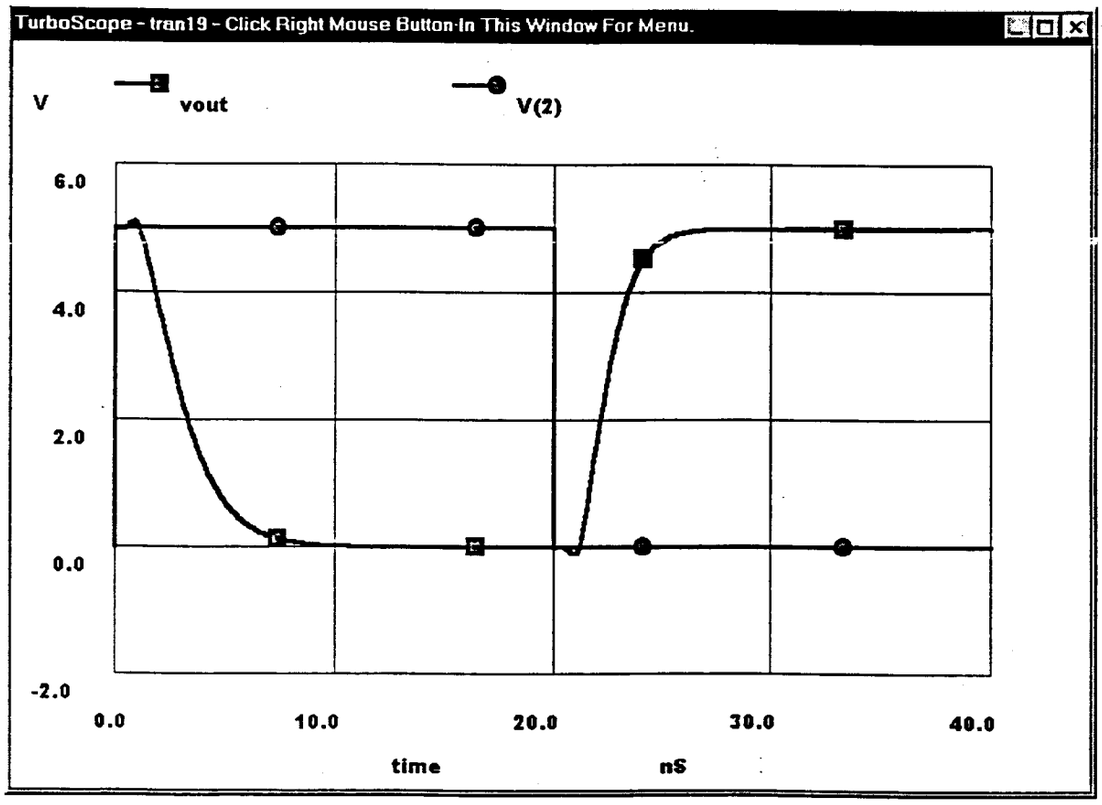
```
Cload   Vout 0 1p
M1      VDD 2 3 VDD CMOSPB  L=2u W=10u
M2      0 2 3 0 CMOSNB  L=2u W=10u
M3      VDD 3 12 VDD CMOSPB  L=2u W=20u
M4      0 3 12 0 CMOSNB  L=2u W=20u
M5      VDD 3 18 VDD CMOSPB  L=2u W=20u
M6      0 3 18 0 CMOSNB  L=2u W=20u
M7      VDD 12 Vout VDD CMOSPB  L=2u W=40u
M8      27 18 Vout 0 CMOSNB  L=4u W=40u
M9      0 VDD 27 0 CMOSNB  L=4u W=40u
V       VDD 0  DC 5 AC 0 0
Vin     2 0     DC 0 AC 0 0 PULSE(0 5 0 1p 1p 20n 40n)
```

***** Spice models and macro models *****

.MODEL CMOSPB PMOS LEVEL=4 ...
.MODEL CMOSNB NMOS LEVEL=4 ...

***** End of spice models and macro models *****

.OPTION ABSTOL=1u ITL4=100 RELTOL=.1 VNTOL=8m
.tran .1 40n 0 .1n
.end

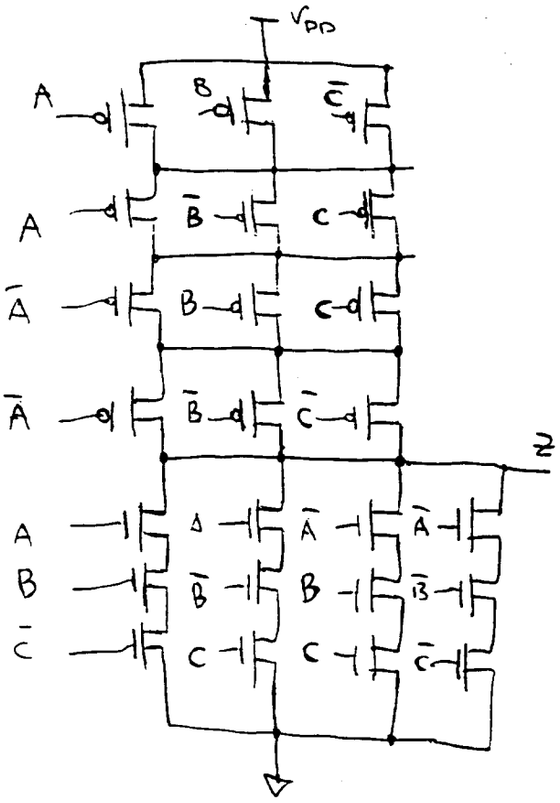


Problem 12.9

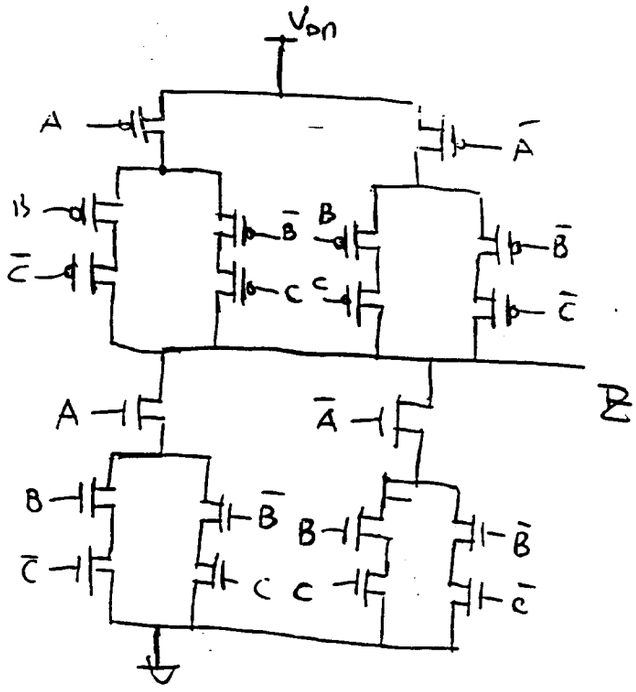
$$Z = A \oplus B \oplus C = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$\bar{Z} = AB\bar{C} + A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}\bar{C}$$

$$Z = \overline{AB\bar{C} + A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}\bar{C}}$$



another implementation.



Problem 12.10:

$$Z=\overline{A(BD+CE)}.$$

Problem 12.11:

This is a NOR gate, and the logic function is: $OUT=\overline{(A+B)}$.
If we tie A and B together, it becomes a inverter. When $V_{SP}=V_{in}=V_{out}$, all of these n-MOSFET are operated in saturation region. If we named them as M1(3/10), M2(3/2) and M3(3/2), we have(neglecting body effect):

$$\frac{\beta_1}{2}\cdot(VDD-V_{SP}-V_{THN})^2=\frac{\beta_2+\beta_3}{2}\cdot(V_{SP}-V_{THN})^2$$

$$\therefore V_{SP}=\frac{\left(\sqrt{\frac{\beta_2+\beta_3}{\beta_1}}-1\right)\cdot V_{THN}+VDD}{1+\sqrt{\frac{\beta_2+\beta_3}{\beta_1}}}$$

Because $\beta=KP_n\cdot\frac{W}{L}$, $\frac{\beta_2+\beta_3}{\beta_1}=1$. Using VDD=5V, V_{THN}=0.83V,

$V_{SP}\cong 1.632V$.

Problem 12.12:

$V_{out(MAX)}=VDD-V_{THN}\cong 3.5V$(Body-effect).

For minimum ouput voltage, the $V_{out(MIN)}\approx 0$. If using current equations, the ouput voltage is slightly higher than 0.

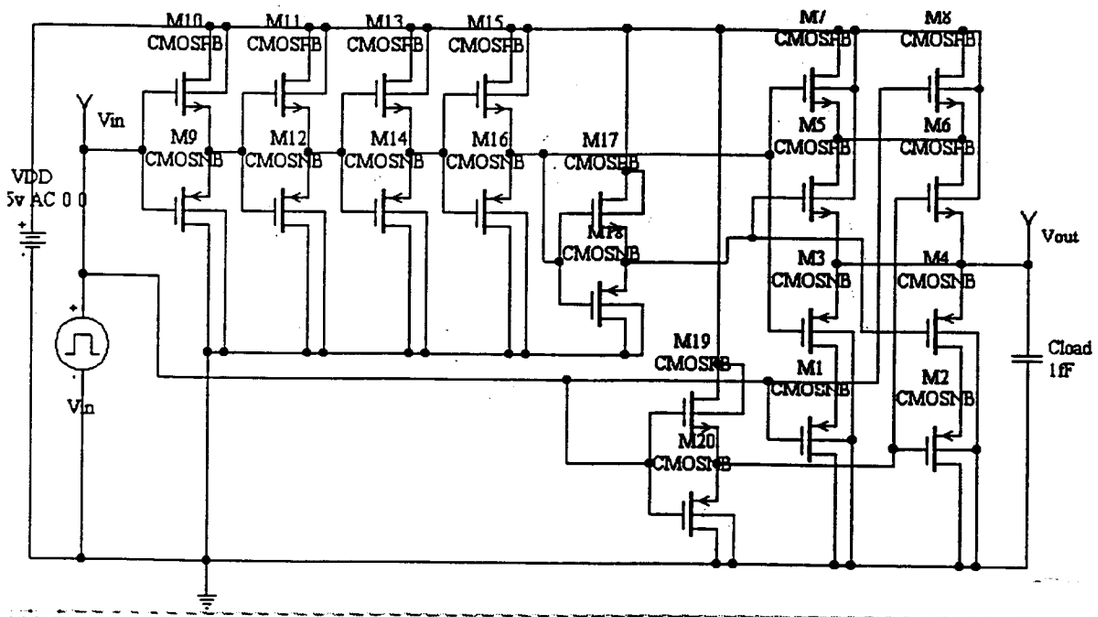
Problem 12.13:

If we use 4 basic CMOS inverter(assume each MOSFET has same size) to form the delay buffer, the delay time of this buffer,

$t_d=2(t_{PHL}+t_{PLH})=2(R_n+R_p)C_{tot}=2(12k+36k)\times(L/W)\times 5\times C'_{ox}\times W\times L$

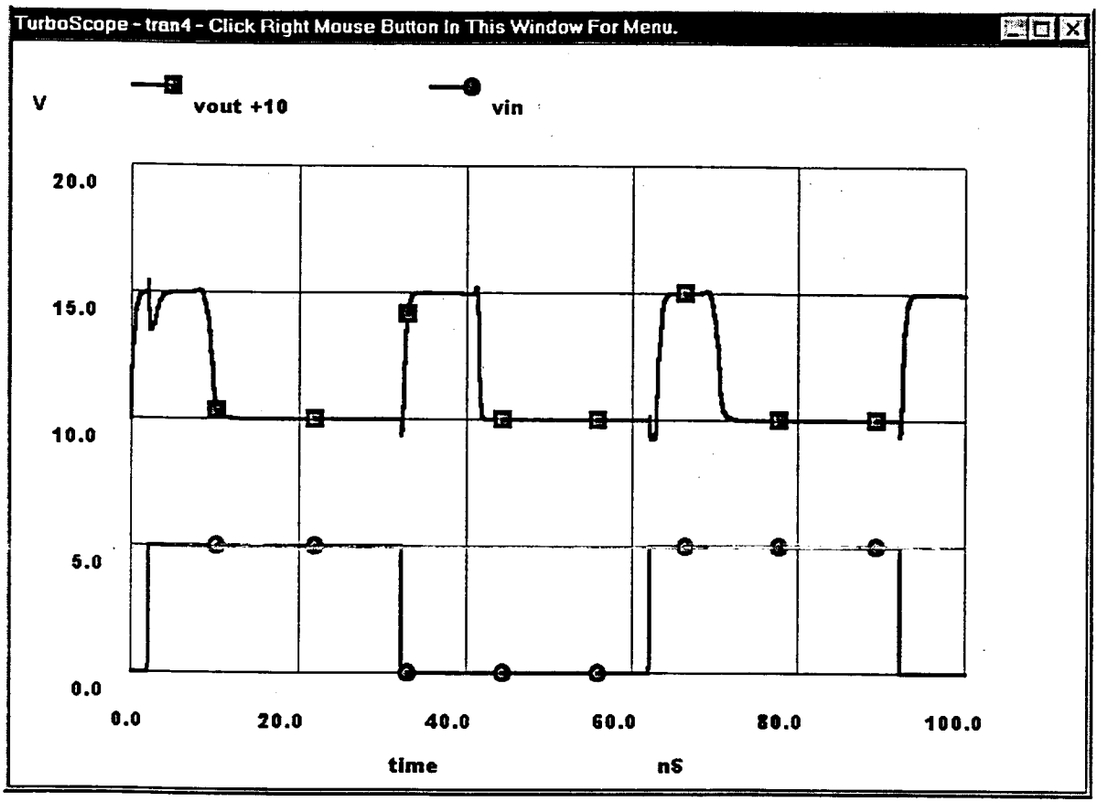
$t_d=0.384\times L^2(ns)$.

If t_d=10ns, we can get $L\cong 5.1\mu m$. If we use L=6μm,W=3μm for the delay buffer, we use minimum size(3/2) in other MOSFET, the BISM simulating circuit is shown below:



*** Top Level Netlist ***

```
Cload    Vout 0 1fF
M1       0 Vin 1 0 CMOSNB  L=2u W=3u
M10      5 Vin 6 5 CMOSPB  L=6u W=3u
M11      5 6 7 5 CMOSPB  L=6u W=3u
M12      0 6 7 0 CMOSNB  L=6u W=3u
M13      5 7 8 5 CMOSPB  L=6u W=3u
M14      0 7 8 0 CMOSNB  L=6u W=3u
M15      5 8 9 5 CMOSPB  L=6u W=3u
M16      0 8 9 0 CMOSNB  L=6u W=3u
M17      5 9 10 5 CMOSPB  L=2u W=3u
M18      0 9 10 0 CMOSNB  L=2u W=3u
M19      5 Vin 3 5 CMOSPB  L=2u W=3u
M2       0 3 2 0 CMOSNB  L=2u W=3u
M20      0 Vin 3 0 CMOSNB  L=2u W=3u
M3       1 9 Vout 0 CMOSNB  L=2u W=3u
M4       2 10 Vout 0 CMOSNB  L=2u W=3u
M5       4 10 Vout 5 CMOSPB  L=2u W=3u
M6       4 3 Vout 5 CMOSPB  L=2u W=3u
M7       5 9 4 5 CMOSPB  L=2u W=3u
M8       5 Vin 4 5 CMOSPB  L=2u W=3u
M9       0 Vin 6 0 CMOSNB  L=6u W=3u
VDD      5 0      DC 5v AC 0 0
Vin      Vin 0    DC 0 AC 0 0 PULSE(0 5v 2n .1n .1n 30n 60n)

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4 ...
.MODEL CMOSPB PMOS LEVEL=4 ...

***** End of spice models and macro models *****
.OPTION ABSTOL=1u ITL4=1000 RELTOL=0.1 VNTOL=8mv
.tran .1ns 100ns 0 .1ns uic
.end
```



If the width of the input pulse is less than 10ns, the output cannot trigger the rise and fall edges of input pulse exactly. The result is shown below with input pulse width = 5ns.