Chapter 11

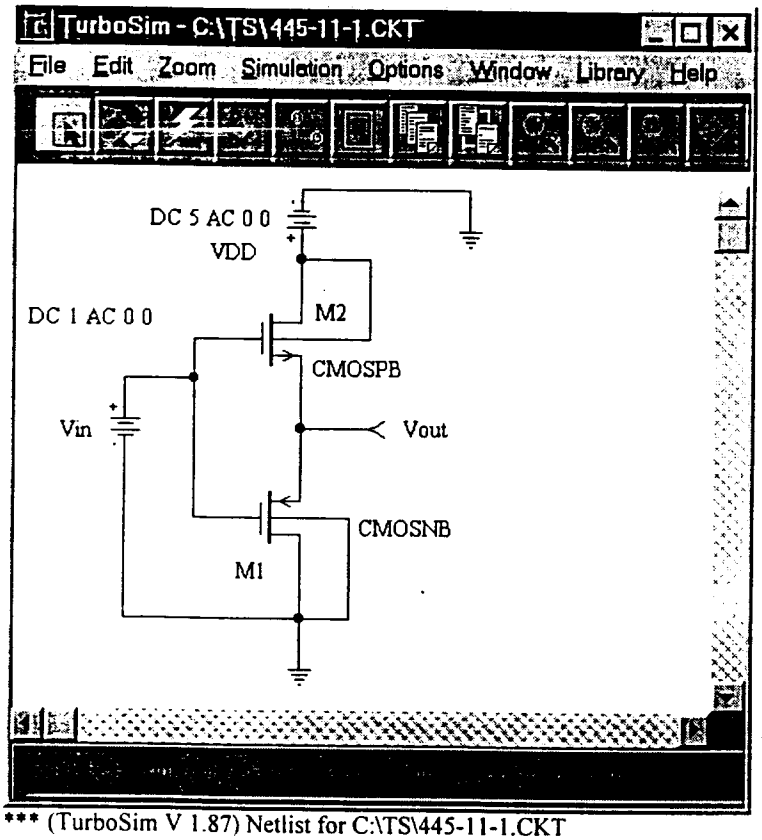
Problem 11.1

From equation (11.4), with $V_{SP}$ approximately equal to VTHN, βn should be far larger than βp. In a basic inverter, for both NMOS and PMOS, the length of devices is same and Wn = 400μm, Wp=3μm. Assume KPn = 3KPp, VDD = 5V, $V_{THN}=V_{THP}=0.9V$ ,

$V_{SP} = (20\ V_{THN} + VDD-V_{THP})/ (1+20) \approx 1.05V$

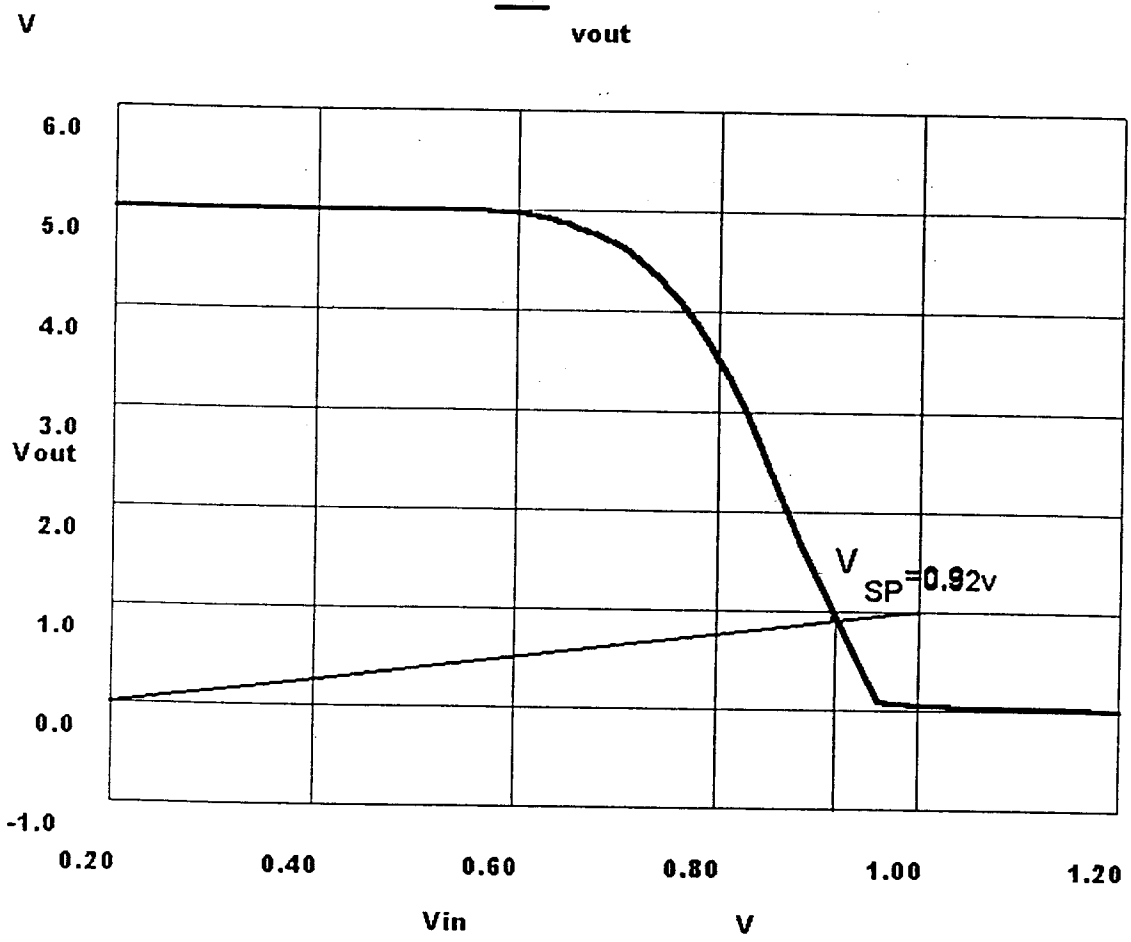
SPICE simulation:

1) Circuit and netlist:




```
*** (TurboSim V 1.87) Netlist for C:\TS\445-11-1.CKT
*** Top Level Netlist ***
M1      0 2 Vout 0 CMOSNB  L=2u W=400u
M2      5 2 Vout 5 CMOSPB  L=2u W=3u
VDD     5 0      DC 5 AC 0 0
Vin     2 0      DC 1 AC 0 0

***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4 (refer to Appendix A)
.MODEL CMOSPB PMOS LEVEL=4 (refer to Appendix A)

***** End of spice models and macro models *****
.OPTION ABSTOL=1u ITL4=100 RELTOL=0.01 VNTOL=.5m
.DC Vin 0 2 0.01
.end
```

2) Simulation results




3) The noise margins:

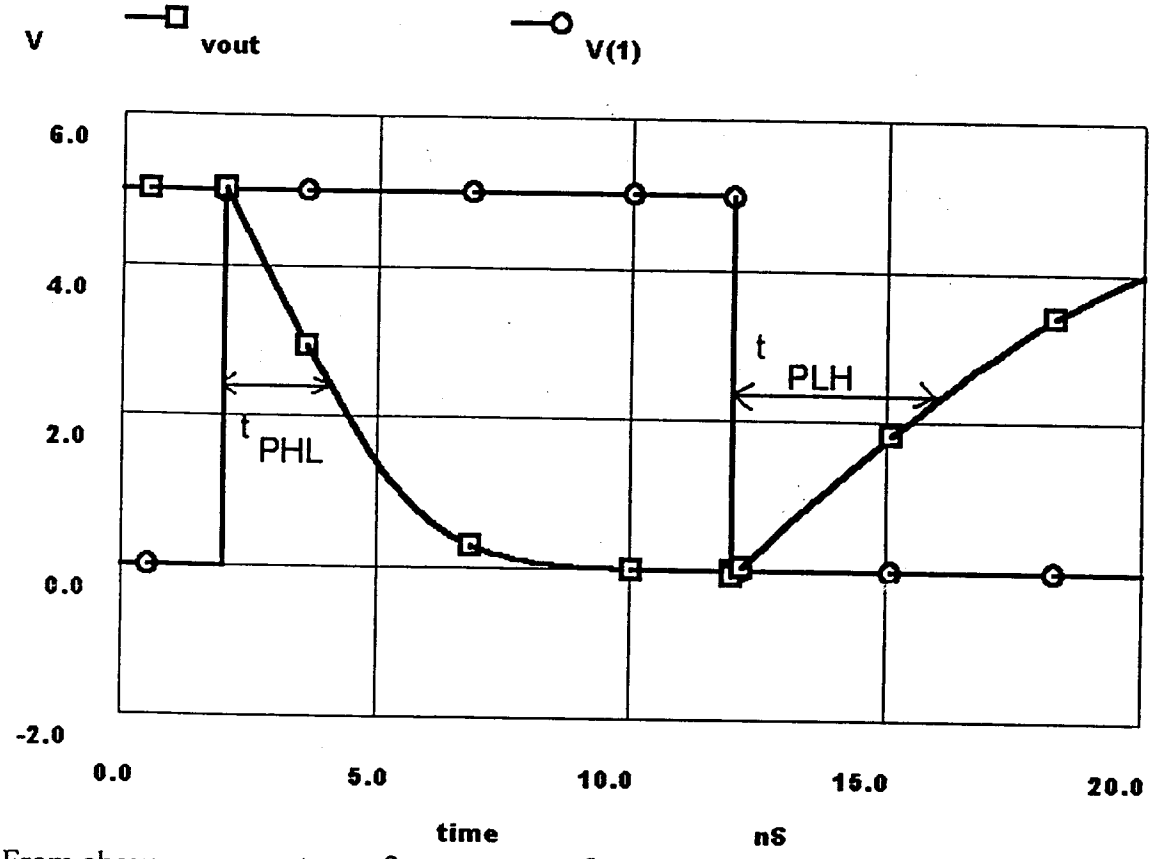
NMH = 5V-0.95V = 4.05V, NML = 0.7V - 0V= 0.7V

Problem 11.2

With W=10μm and a load capacitance of 1pF, $C_{tot}$ = 1pF+2×10 ×2 ×800aF = 1.032pF. Rn1=12KΩ×2/10=2.4KΩ, Rp2=7.2KΩ. The propagation delay times are

$t_{PHL}$=2.4kΩ×1.032pF ≈ 2.5ns , $t_{PLH}$=7.2kΩ×1.032pF ≈ 7.43ns

SPICE Simulation Results:




From above curve, $t_{PHL} \approx \underline{2ns}$ , $t_{PLH} \approx \underline{5ns}$

Problem 11.3

For minimum size inverter, $t_{PHL} + t_{PLH} = 160k \times C_{ox} = 160k\Omega \times 4.8fF = 768ps$. Using 31 inverters, the oscillation frquency is

fosc = $1/(31 \times 768ps) \approx \underline{42MHz}$.

Problem 11.4

The layout of standard-cell frame is shown in figure p11.4.
The adding implants in this layout can reduce the distance from the connection of n-well (by n+ to VDD) and p-substrate (by p+ to VSS); therefore, reduce the parasitic resistance which will cause latch-up.

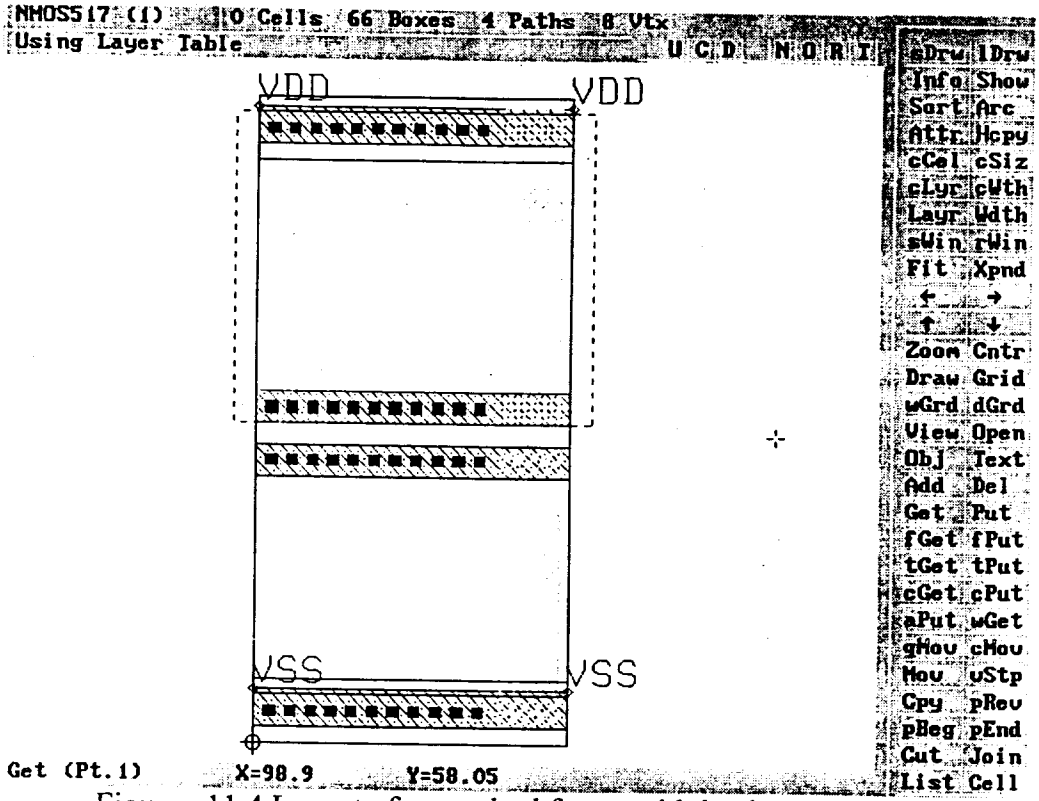


Figure p11.4 Layout of a standard frame with latch-up prtection

Problem 11.5

For the first inverter with size of 150/50, the total resistance is (assume 2μm in length)

$R = (12k\Omega \times 2/50 + 36k\Omega \times 2/150) = 0.96k\Omega$, and the output capacitance is

$C = 2\times50\times800aF+2\times150\times800aF = 320fF=0.32pF$

To drive 50pF load capacitance, try three stages buffer, i.e. N=3.

$A = [50pF/(.32\times3/2)pF]1/3 = 4.705$

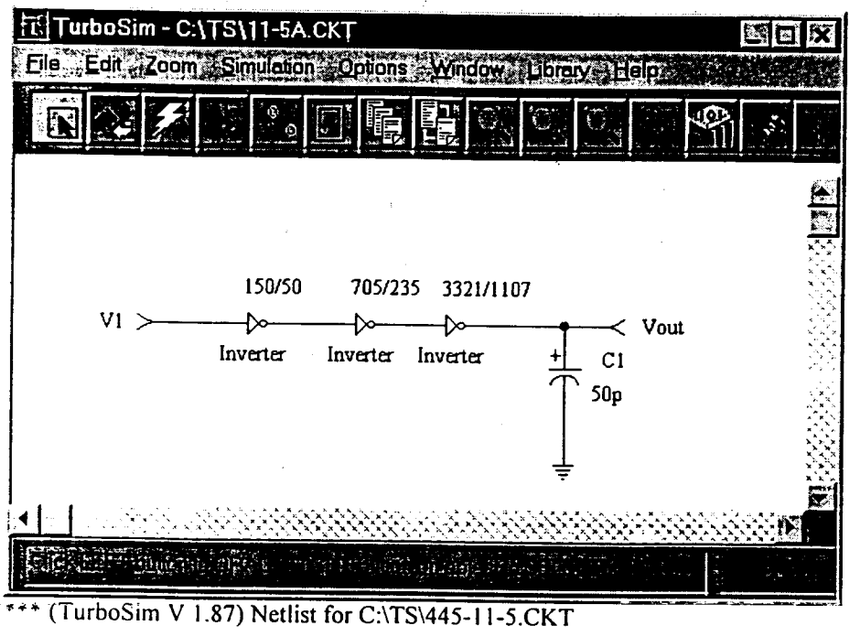
Using Eq.(11.25), the delay is

$t_{PHL}+ t_{PLH}= 3\times(.96k\Omega)\times(.32pF + 4.705\times0.48pF) =7.426ns < 10ns$

Using two stages buffer, A=10.206.

$t_{PHL}+ t_{PLH}= 2\times(.96k\Omega)\times(.32pF + 10.206\times0.48pF) =10.02ns > 10ns$

Therefore, use three-stage buffer to drive a 50pF capacitive load. SPICE simulation is followed.




*** (TurboSim V 1.87) Netlist for C:\TS\445-11-5.CKT

*** Top Level Netlist ***

```
C1      Vout 0 50p
M3      0 1 3 0 CMOSNB  L=2u W=50u
M4      6 1 3 6 CMOSPB  L=2u W=150u
M5      0 3 2 0 CMOSNB  L=2u W=235u
M6      6 3 2 6 CMOSPB  L=2u W=705u
M7      0 2 Vout 0 CMOSNB  L=2u W=1107u
M8      6 2 Vout 6 CMOSPB  L=2u W=3321u
V2      6 0     DC 5 AC 0 0
Vin     1 0     DC 0 AC 0 0 PULSE(0 5 0 1p 1p 15ns 30ns)
```

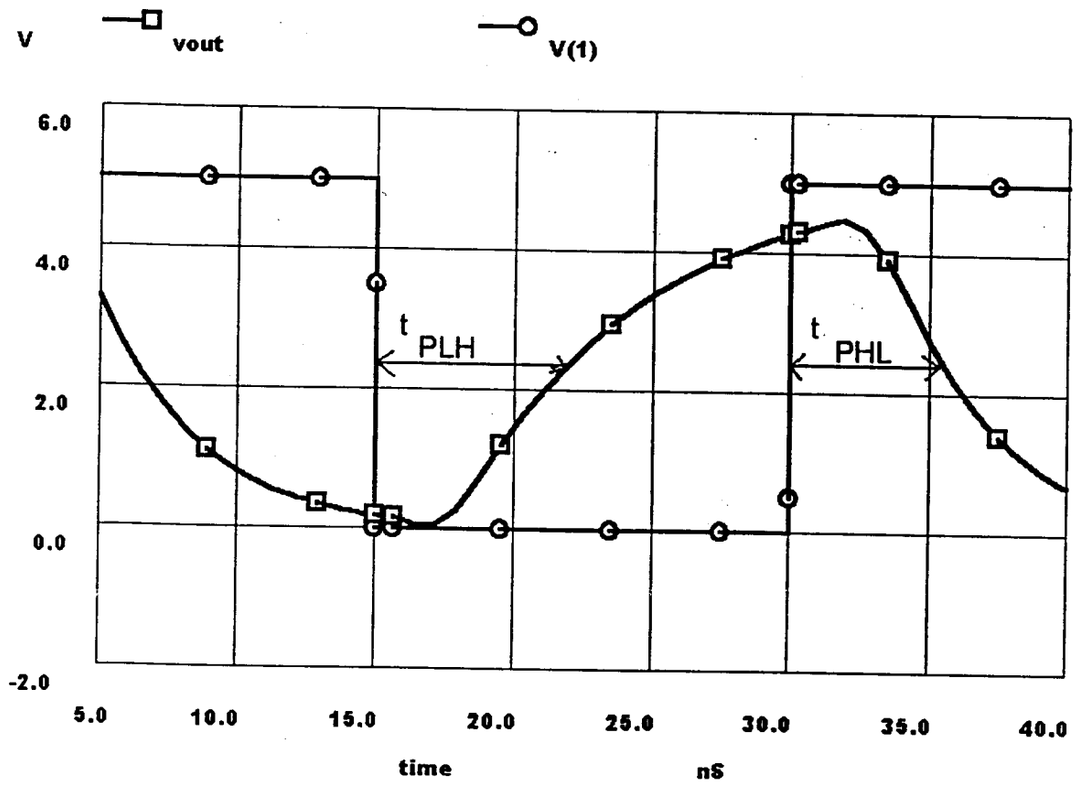
***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4 ...

.MODEL CMOSPB PMOS LEVEL=4 ...

***** End of spice models and macro models *****

```
.OPTION ABSTOL=1u ITL4=100 RELTOL=.1 VNTOL=5m
.tran 1n 40n 0
.end
```




Problem 11.6

For the first inverter with size of 3/3, the total resistance is (assume 2μm in length)

$R = (12k\Omega \times 2/3 + 36k\Omega \times 2/3) = 32k\Omega$, and the output capacitance is

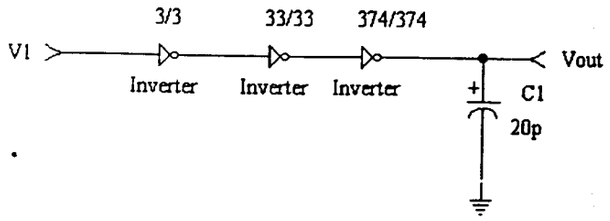
$C = 2\times3\times800aF + 2\times3\times800aF = 9.6fF$

To drive 20pF load capacitance, try three stages buffer, i.e. N=3.

$A = [20pF/(9.6\times3/2)fF]1/3 \approx 11.16$

Using Eq.(11.25), the delay is

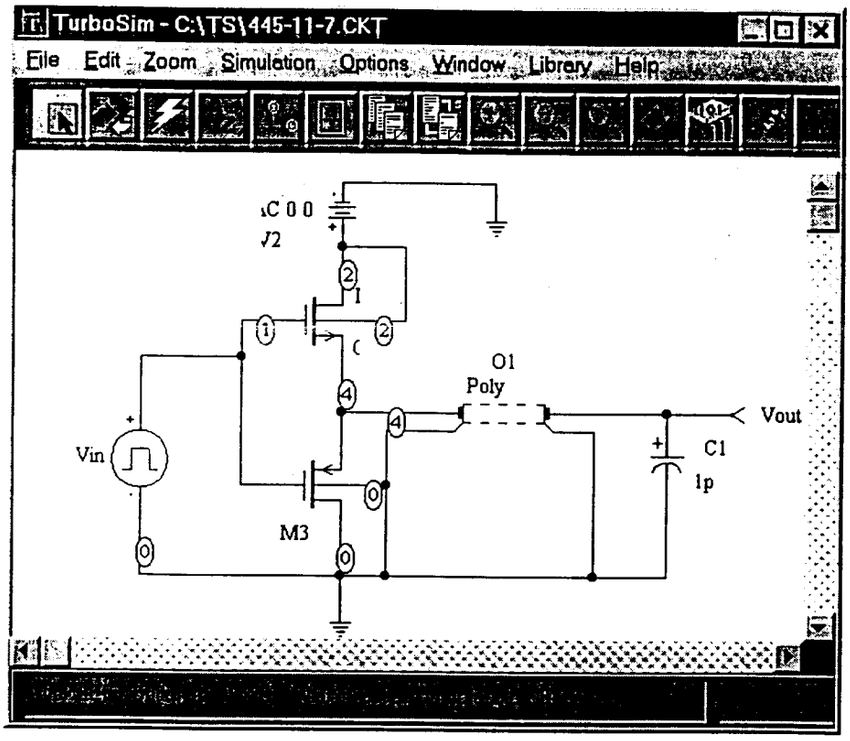
$t_{PHL} + t_{PLH} = 3\times(32k\Omega)\times(9.6fF + 11.16\times14.4fF) \approx 16.35ns < 20ns$



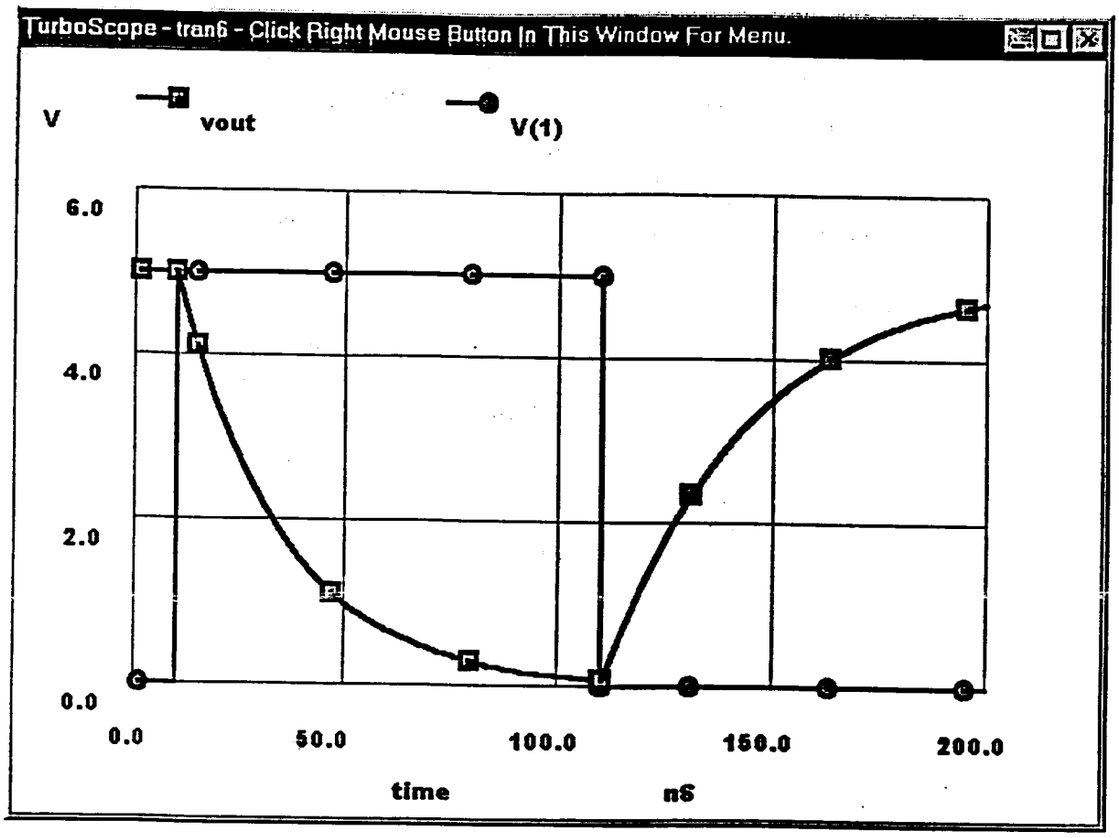
Problem 11.7

For 1mm poly, from appendix A, the unit resistance and capacitance are r = 21Ω and c = 58aF (neglecting fringe capacitance). n = 1000 for unit length equal to 1μm. Using eq. (11.30), for a minimum-size inverter,

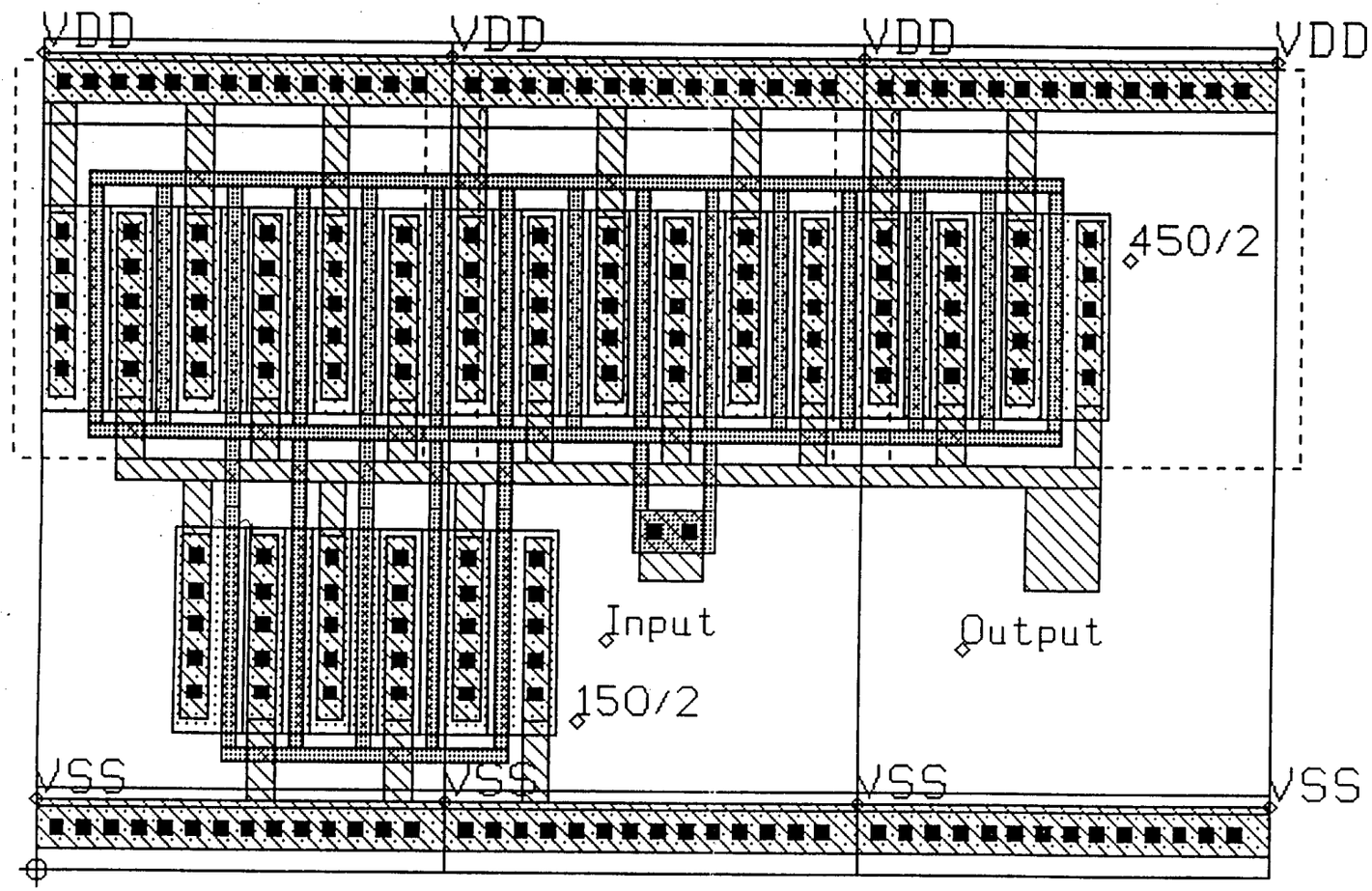
$$t_{PHL} + t_{PLH} = (8k\Omega+24k\Omega)(9.6fF+58fF+1pF)+.35\times21k\Omega\times58fF + (21k\Omega)\times1pF$$
$$\approx 55.6ns$$




```
*** Top Level Netlist ***
C1      Vout 0 1p
M3      0 1 4 0 CMOSNB  L=2u W=3u
M4      2 1 4 2 CMOSPB  L=2u W=3u
O1      4 0 Vout 0 Poly
V2      2 0     DC 5 AC 0 0
Vin     1 0     DC 0 AC 0 0 PULSE(0 5 10n 1p 1p 100n 200ns)

***** Spice models and macro models *****

.MODEL CMOSNB NMOS LEVEL=4 ...
.MODEL CMOSPB PMOS LEVEL=4 ...
.Model Poly LTRA
+ R=21 C=0.058f LEN=1000

***** End of spice models and macro models *****

.OPTION ABSTOL=1u RELTOL=.01 VNTOL=1m
.tran 1n 200n 0
.end
```

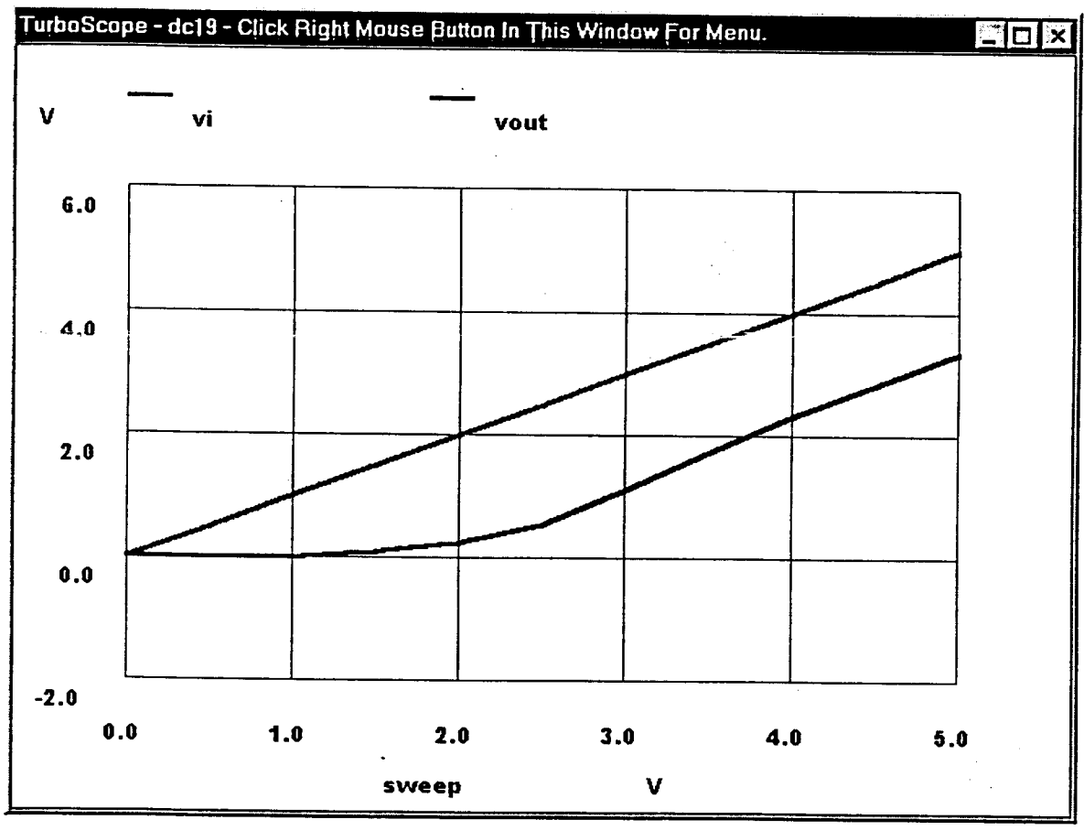

TurboScope - tran6 - Click Right Mouse Button In This Window For Menu.
V
vout
V(1)
6.0
4.0
2.0
0.0
0.0
50.0
100.0
150.0
200.0
time
nS

Problem 11.8



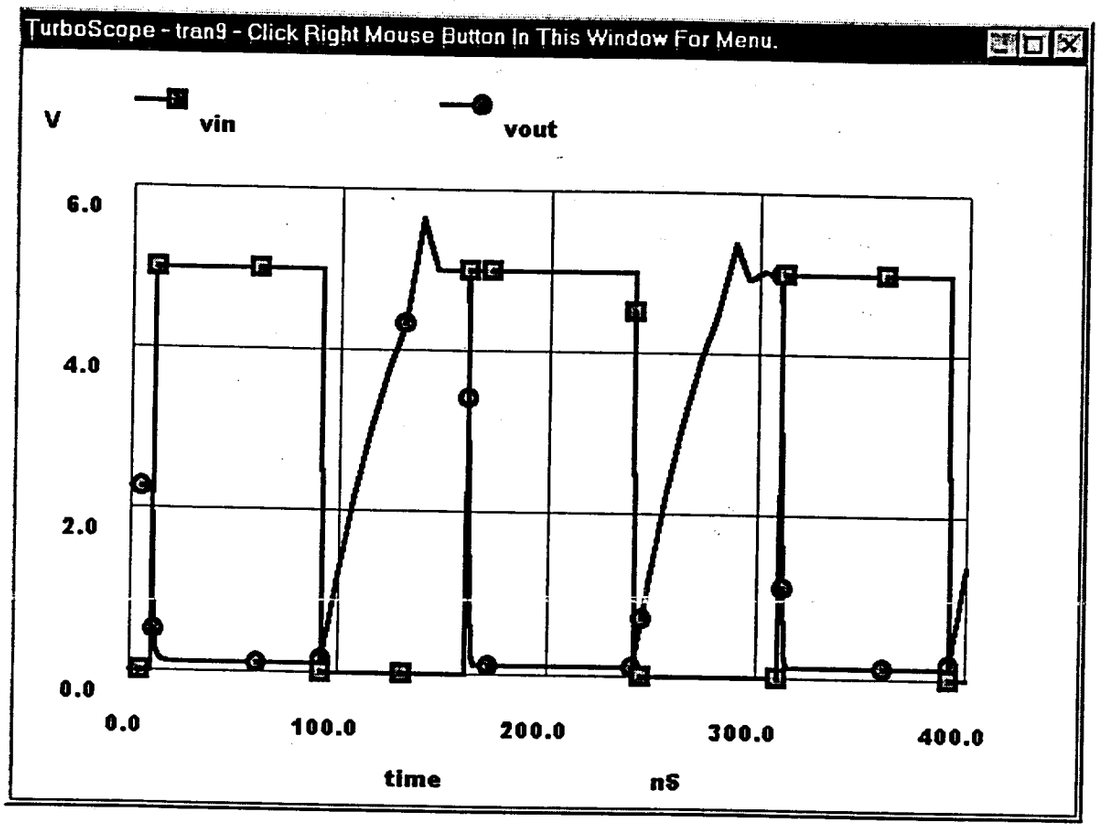
Problem 11.9

All the n-MOSFETs are minimum sized (3/2). The voltage transfer curve is shown in figure P11.9. The output voltage can swing from 0 to approximately 3.6V. For this NMOS super buffer, when Vi is low, both M2 and M3 are off. The output can be pulled down to ground through M4. When Vi is high, M2 and M3 are on, and the output will be limited to VDD - $V_{TIIN}$ ≈3.6V (w/ body effect and Vi = VDD).




Problem 11.10

For bootstrapped NMOS inverter, (Figure 11.30), if M4's size is increased to 20/20, the SPICE simulation results are shown below:




*** (TurboSim V 1.87) Netlist for C:\TS\44511-10.CKT

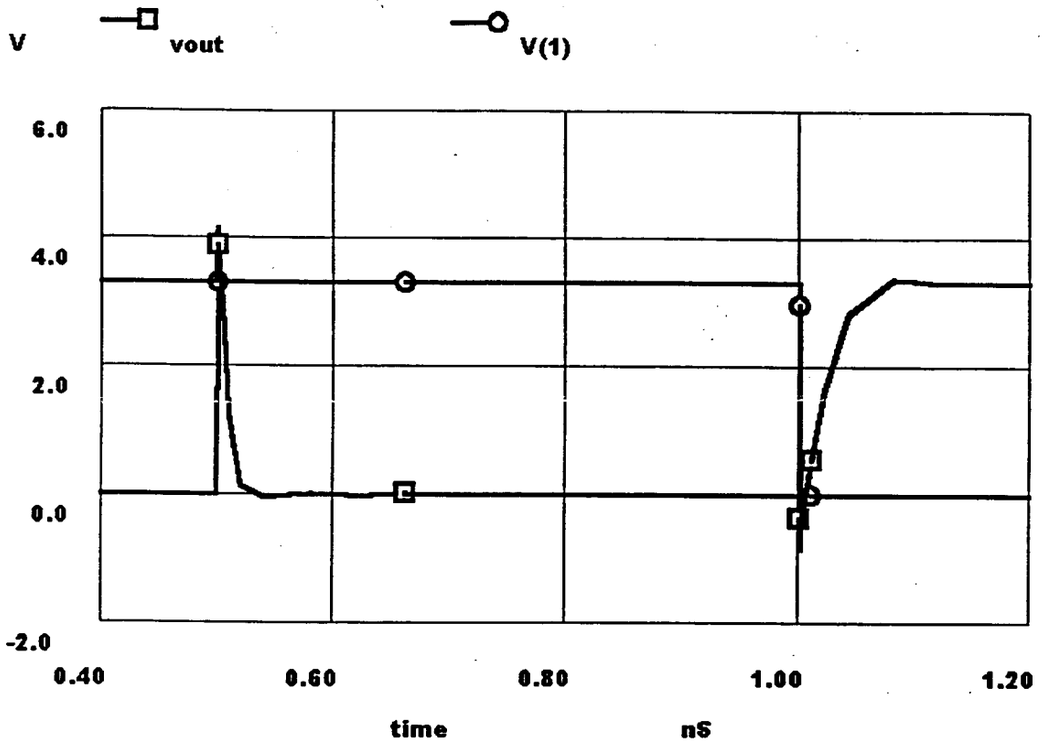
*** Top Level Netlist ***

```
M1      0 Vin Vout 0 CMOSNB  L=2u W=3u
M2      Vout 5 3 0 CMOSNB  L=8u W=3u
M3      5 3 3 0 CMOSNB  L=2u W=3u
M4      Vout 5 Vout 0 CMOSNB  L=20u W=20u
VDD     3 0      DC 5 AC 0 0
Vin     Vin 0   DC 0 AC 0 0 PULSE(0 5 10n 1n 1n 80n 150n)

.OPTION VNTOL=.1m
.tran 1n 400n 0
.end
```

Problem 11.11

For minimum-size (0.9/0.6) MOSFETs in the CMOS14TB process, from Appendix C,

$t_{PHL}$=9kΩ×0.6×2×3.7fF ≈ 40ps , $t_{PLH}$=18kΩ×0.6×2×3.7fF ≈ 80ps

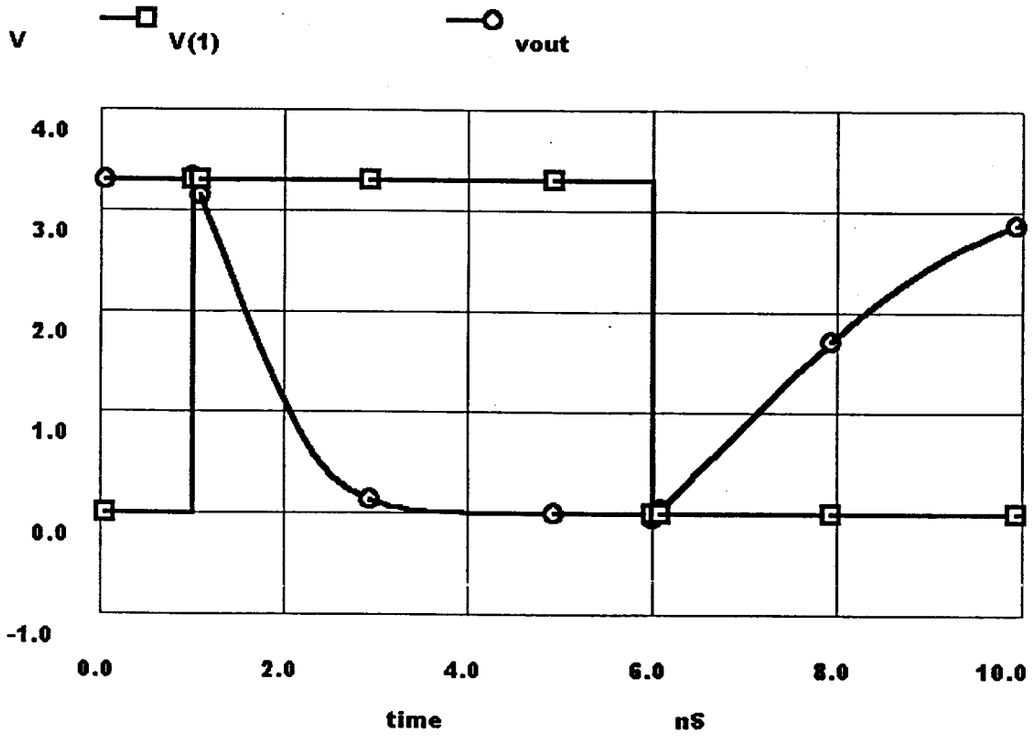



Problem 11.12

With load capacitance 100fF, for minimum-size (0.9/0.6) MOSFETs in the CMOS14TB process, from Appendix C,

$t_{PHL}$=(9kΩ/0.9)×(0.9×0.6×2×3.7fF+100fF) ≈ 1.04ns ,

$t_{PLH}$=(18kΩ/0.9)×(.9×0.6×2×3.7fF+100fF) ≈ 2.08ns




Problem 11.13