Chapter 10

Problem 10.1

For 10μm/2μm MOSFET, the effective resistance of NMOS is Rn= 12kΩ × 2/10 = 2.4kΩ, and for the PMOS, Rp = 36kΩ × 0.2 = 7.2kΩ. The capacitance between drain to ground is same for both NMOS and PMOS and equal to C_{ox} + 150fF = 166fF. From eq. (10.8) and (10.9), for NMOS,

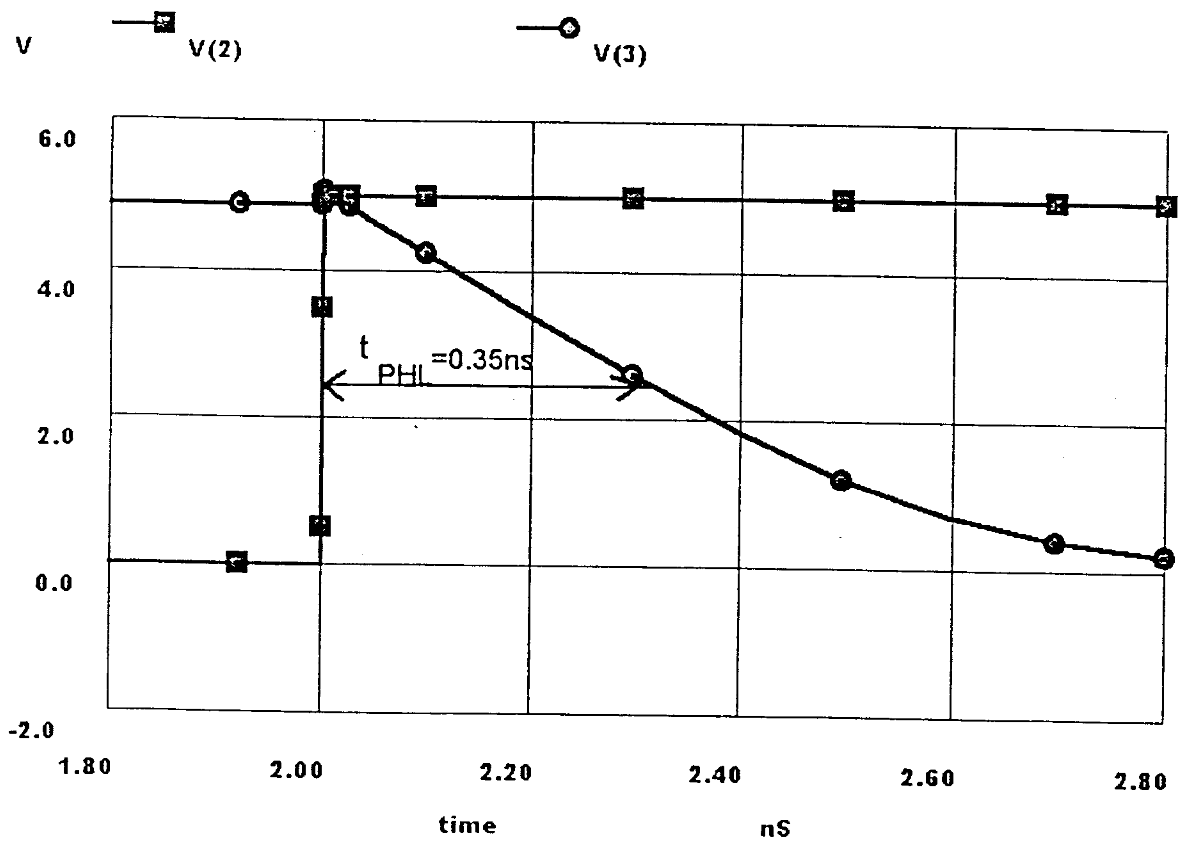
$$t_{PHL}=2.4k\Omega\times166fF \approx \underline{398ps}\ ,\ t_{HL}=2\times2.4k\Omega\times166fF \approx \underline{797ps}$$

for PMOS,

$$t_{PLH}=7.2k\Omega\times166fF \approx \underline{1.2ns}\ ,\ t_{LH}=2\times7.2k\Omega\times166fF \approx \underline{2.4ns}$$

SPICE simulation:

1) For nmos,



Problem 10.2

For CMOS14TB process (appendix C), the oxide capacitance per unit area is given by

$$C'_{ox} = (35.13\text{fF}/\mu\text{m})/0.0096\mu\text{m} \approx 3.7\text{fF}/\mu\text{m}^2$$

For the short-channel MOSFET, $I_D = I_{drive} \times W$, VDD=3.3V, the effective digital resistance

$$R = VDD/(I_{drive} \times W) = R'/W,\ \ R' = VDD/I_{drive}$$

For NMOS,

$R'_n = 3.3\text{V}/(380\mu\text{A}/\mu\text{m}) \approx$ <u>9kΩ•μm</u>; using L=0.6μm, $\tau_n = R'_n \bullet L \bullet C'_{ox} =$ <u>20ps</u>

For PMOS,

$R'_p = 3.3\text{V}/(190\mu\text{A}/\mu\text{m}) \approx$ <u>18kΩ•μm</u>; using L=0.6μm, $\tau_p = R'_p \bullet L \bullet C'_{ox} =$ <u>40ps</u>

Probelm 10.3

1) SPICE circuit and netlist

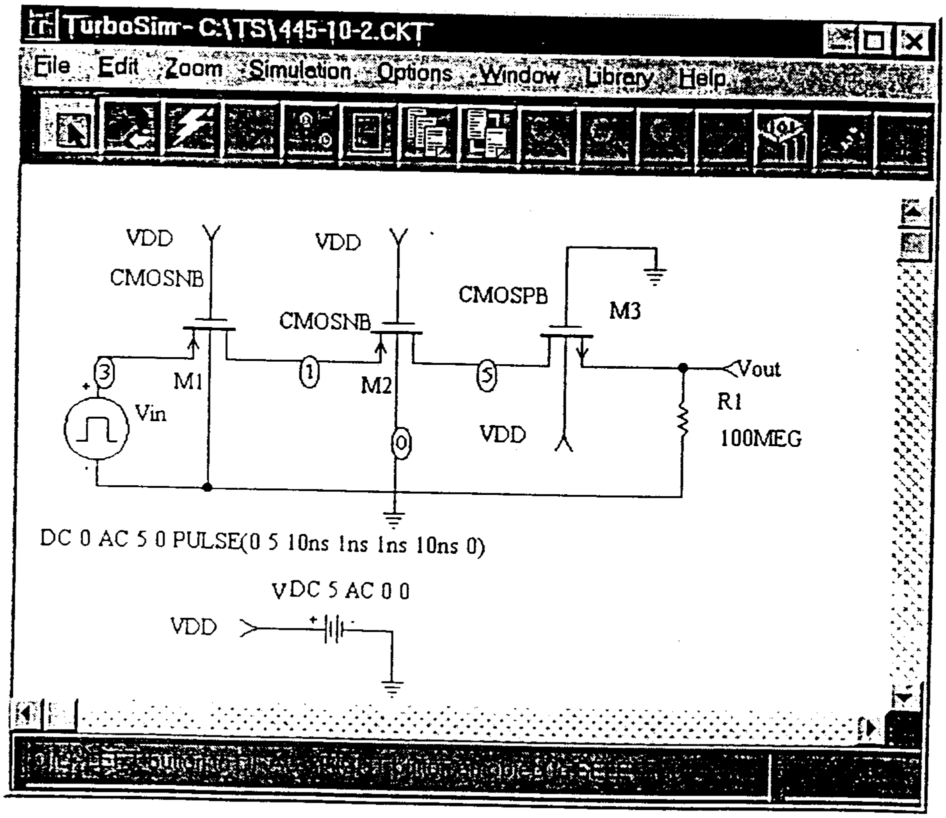
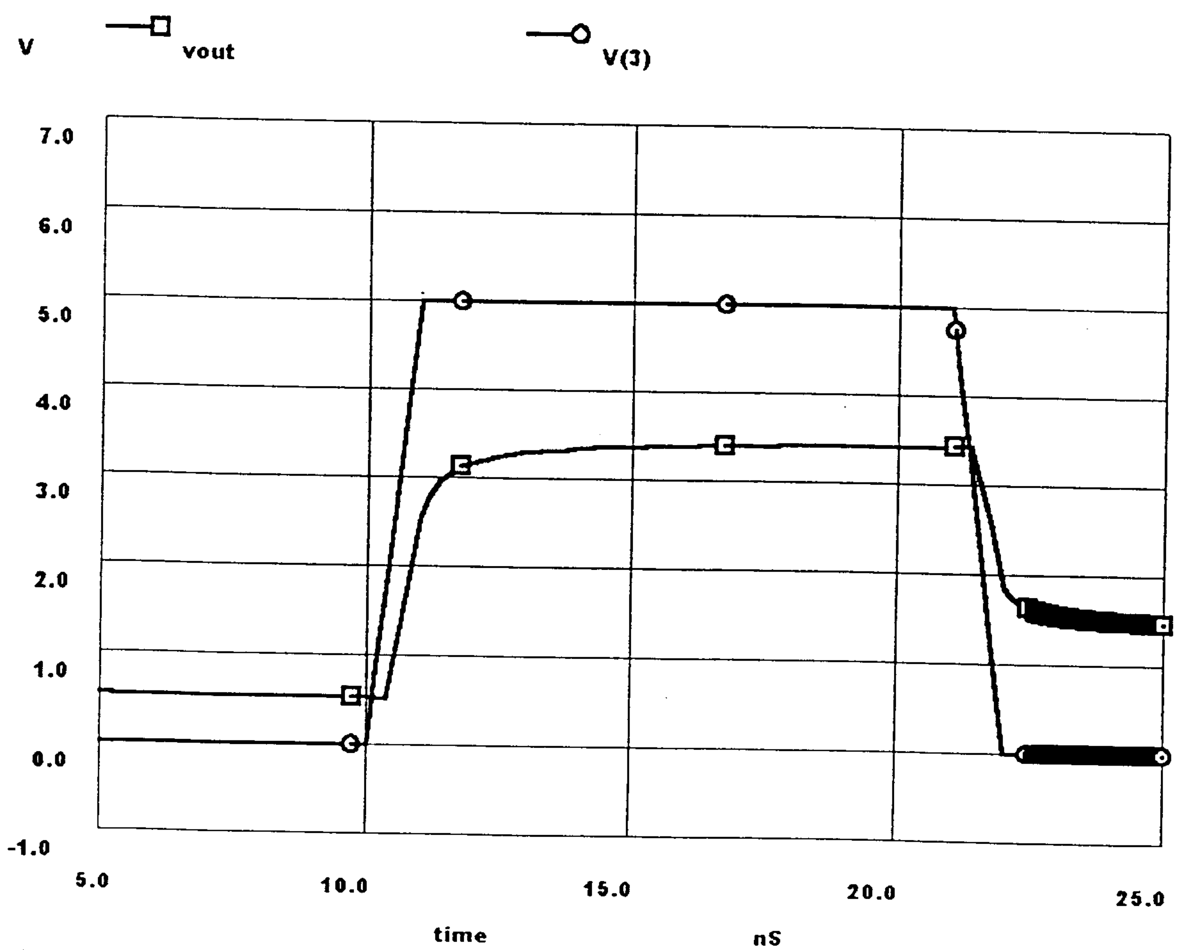


Figure P10.3 SPICE simulation circuit

```
*** (TurboSim V 1.87) Netlist for C:\TS\445-10-2.CKT
*** Top Level Netlist ***
M1      1 VDD 3 0 CMOSNB  L=2u W=3u
M2      5 VDD 1 0 CMOSNB  L=2u W=3u
M3      5 0 Vout VDD CMOSPB  L=2u W=3u
R1      0 Vout 100MEG
V       VDD 0   DC 5 AC 0 0
Vin     3 0     DC 0 AC 5 0 PULSE(0 5 10ns 1ns 1ns 10ns 0)
***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4 ... Appendix A
.MODEL CMOSPB PMOS LEVEL=4 ... Appendix A
***** End of spice models and macro models *****
.OPTION ABSTOL=1u ITL4=100 RELTOL=0.01 VNTOL=.1mv
.tran 1n 25n 0 .5n uic
.end
```

2) simulation results



3) Explain results

For the circuit shown in Figure P10.3, if any n-mosfet (m1, m2) is connected to logic low or p-mosfet, m3 to logic high, the output will be high impedence. For all three mosfets are ON (as connected shown in Fig. P10.3), from the SPICE simulation results,

a. Input from low to high (0-5V), output is from 0.8V to 3.3V. For input = high, the terminal of m1 which connected to input is drain, and the source voltage of m1 is at least VDD-Vthn to keep m1 open (i.e. VGS≥Vthn). M2 and m3 pass this voltage to output with body effects. Therefore, the output voltage is VDD-Vthn = 3.3V.

b. Input from high to low (5V-0), output is from 3.4V to 1.5V. For input = low, the left terminal of m3 which connected to m2 is drain, since the gate of m3 is connected to low. The output voltage is equal to VSG (≥Vthp), i.e. the threshold voltage of p-mosfet m3, 1.5V(with body effects).

c. The delay time t_{PLH} is greater than the t_{PHL} of the output waveform.

Problem 10.4, 10.5

For one of the n-mosfet, the time constant

$$\tau_n = R'_n \bullet L^2 \bullet C'_{ox} = 12k\Omega \times 4 \times 800aF = 38.4ps;$$

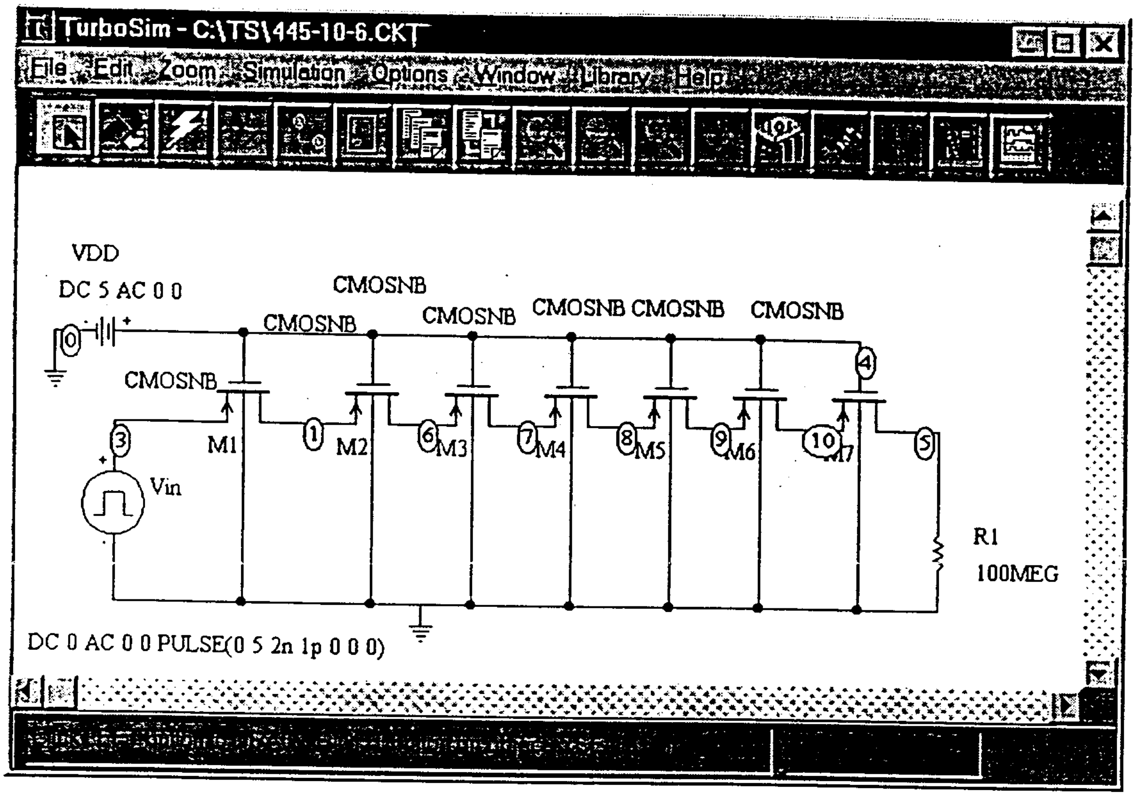
for seven n-mosfets connected in series, $td = \tau_n \bullet N^2 = \underline{1.88ns}$

For one of the p-mosfet, the time constant

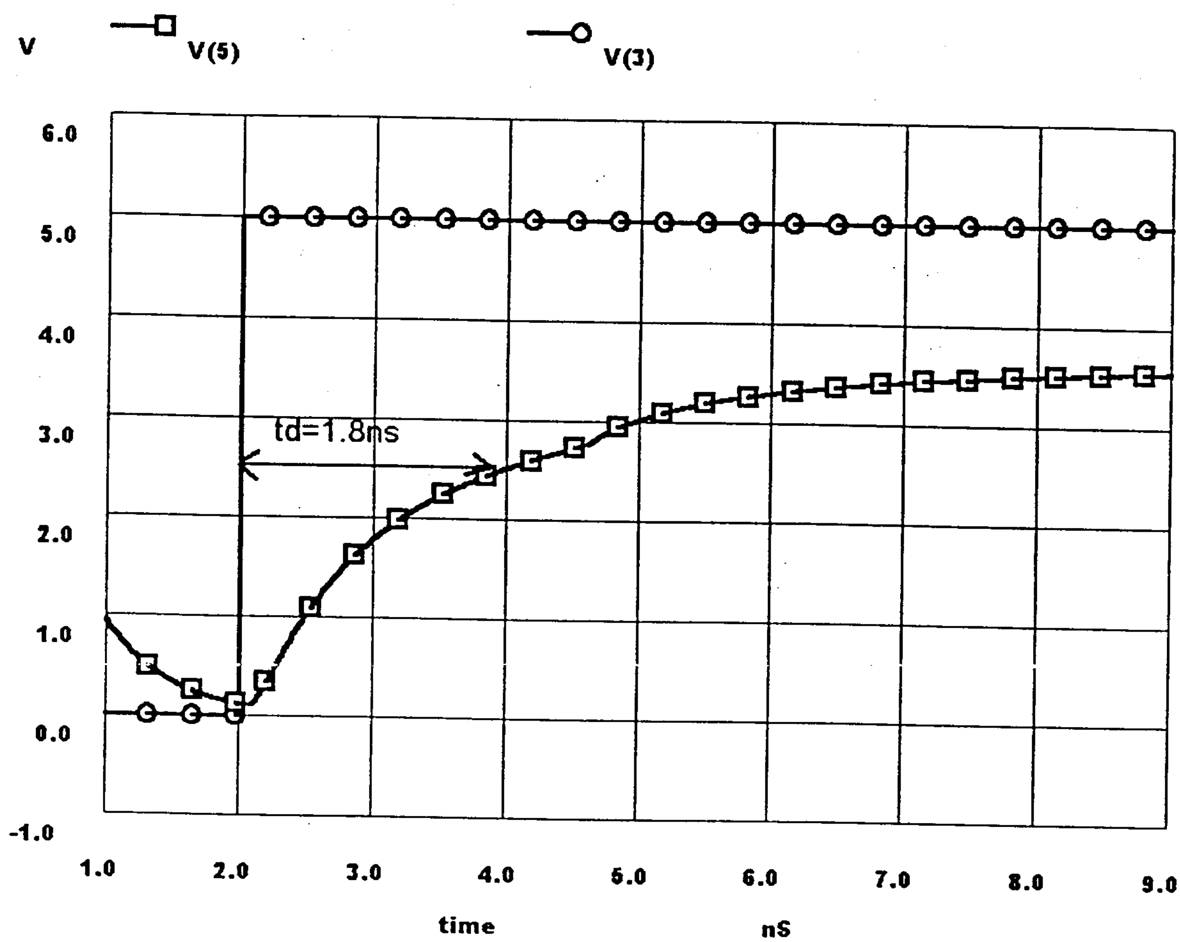
$$\tau_p = R'_p \bullet L^2 \bullet C'_{ox} = 36k\Omega \times 4 \times 800aF = 115.2ps;$$

for seven p-mosfets connected in series, $td = \tau_p \bullet N^2 = \underline{5.64ns}$

Problem 10.6




```
*** Top Level Netlist ***
M1     1 4 3 0 CMOSNB  L=2u W=10u
M2     6 4 1 0 CMOSNB  L=2u W=10u
M3     7 4 6 0 CMOSNB  L=2u W=10u
M4     8 4 7 0 CMOSNB  L=2u W=10u
M5     9 4 8 0 CMOSNB  L=2u W=10u
M6     10 4 9 0 CMOSNB  L=2u W=10u
M7     5 4 10 0 CMOSNB  L=2u W=10u
R1     0 5 100MEG
VDD    4 0     DC 5 AC 0 0
Vin    3 0     DC 0 AC 0 0 PULSE(0 5 2n 1p 0 0 0)
***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4 ...appendix A
***** End of spice models and macro models *****
.OPTION ABSTOL=1u ITL4=100 RELTOL=0.01 VNTOL=.1mv
.tran 1n 10ns 0 .01n uic
.end
```



Problem 10.7

For 3μm/2μm MOSFET, the effective resistance of NMOS is Rn= 12kΩ × 2/3 = 8kΩ, and for the PMOS, Rp = 24kΩ. The capacitance between drain to ground is same for both NMOS and PMOS and equal to C_{ox} + 1pF ≈ 1pF. From eq. (10.8) and (10.9), for NMOS,

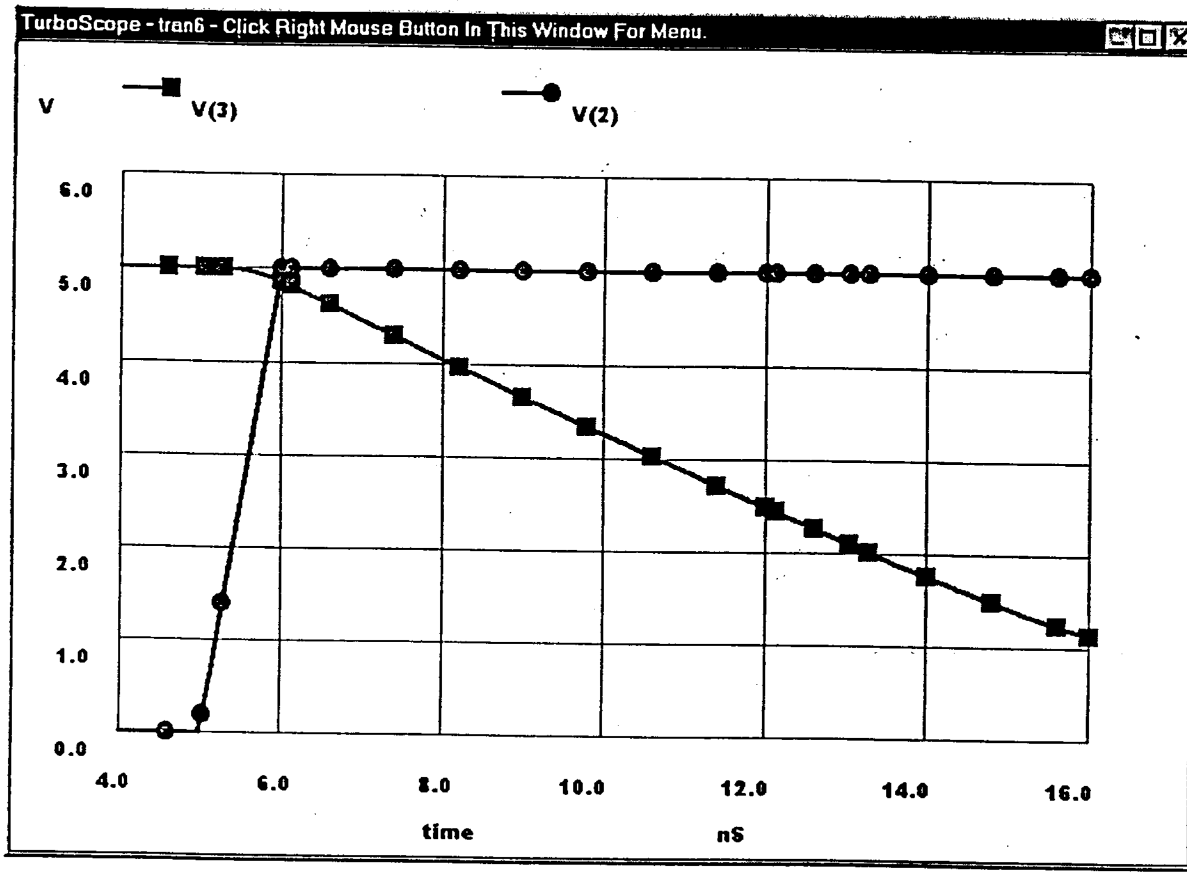
t_{PHL}=8kΩ×1pF = 8ns , t_{HL}=2×8kΩ×1pF = 16ns

for PMOS,

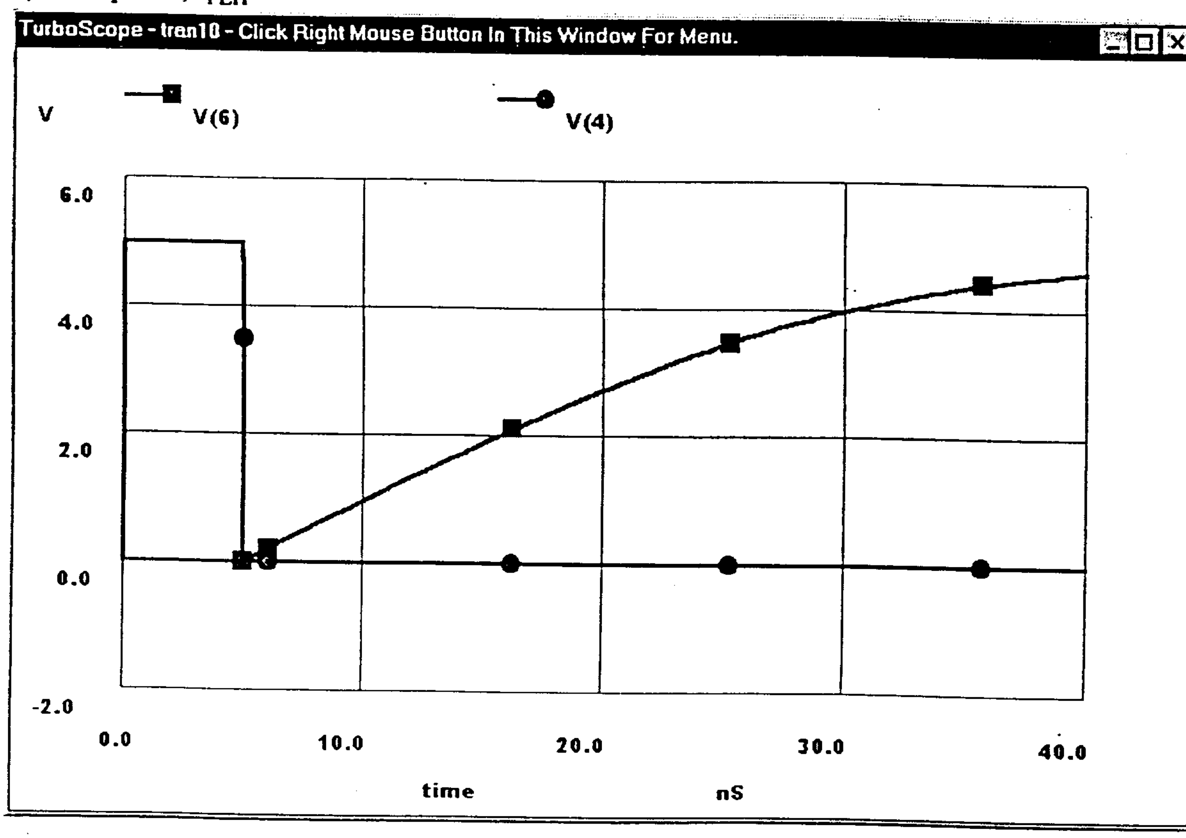
t_{PLH}=24kΩ×1pF = 24ns , t_{LH}=2×24kΩ×1pF = 48ns

SPICE simulation:

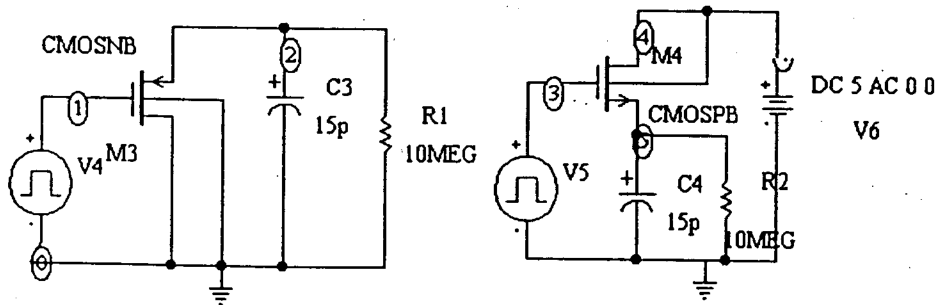
1) For nmos, t_{PHL}= 7ns



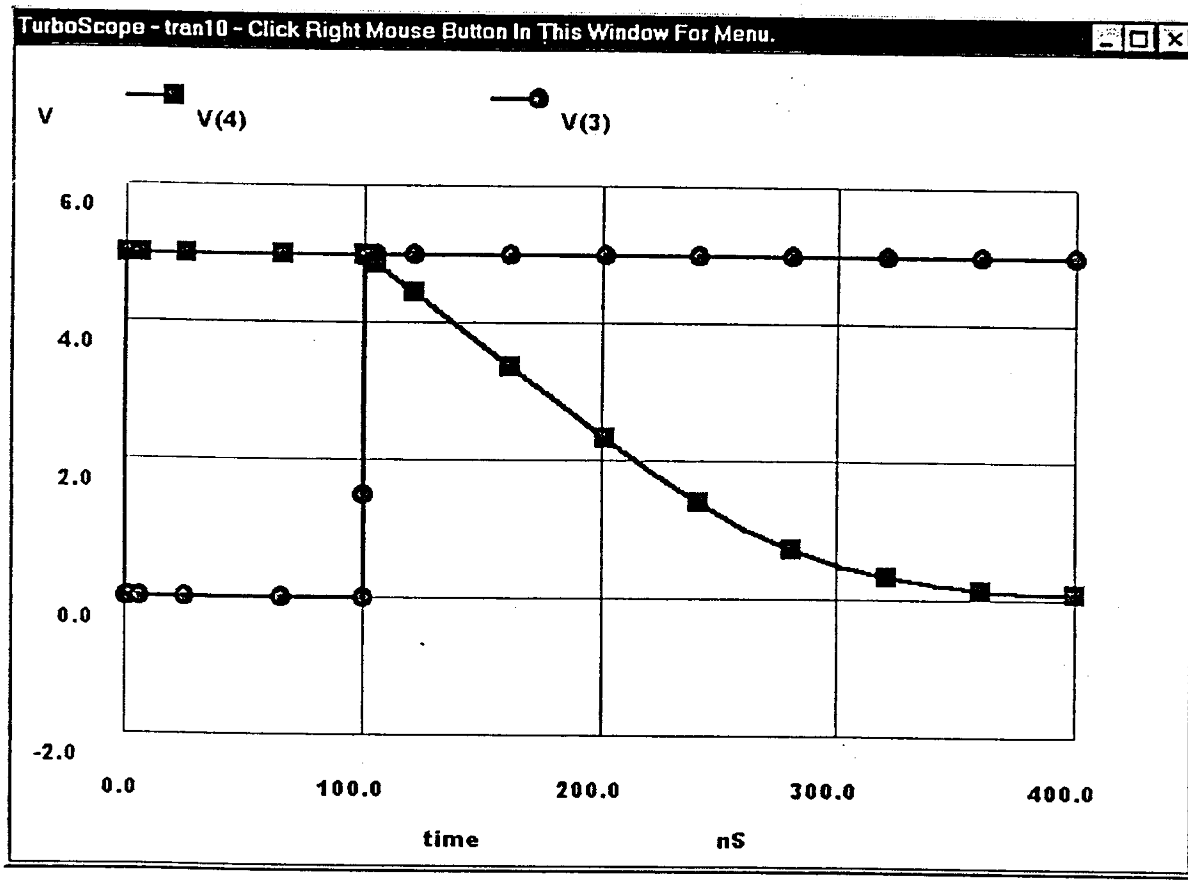
2) For pmos, t_{PLH}= 18ns

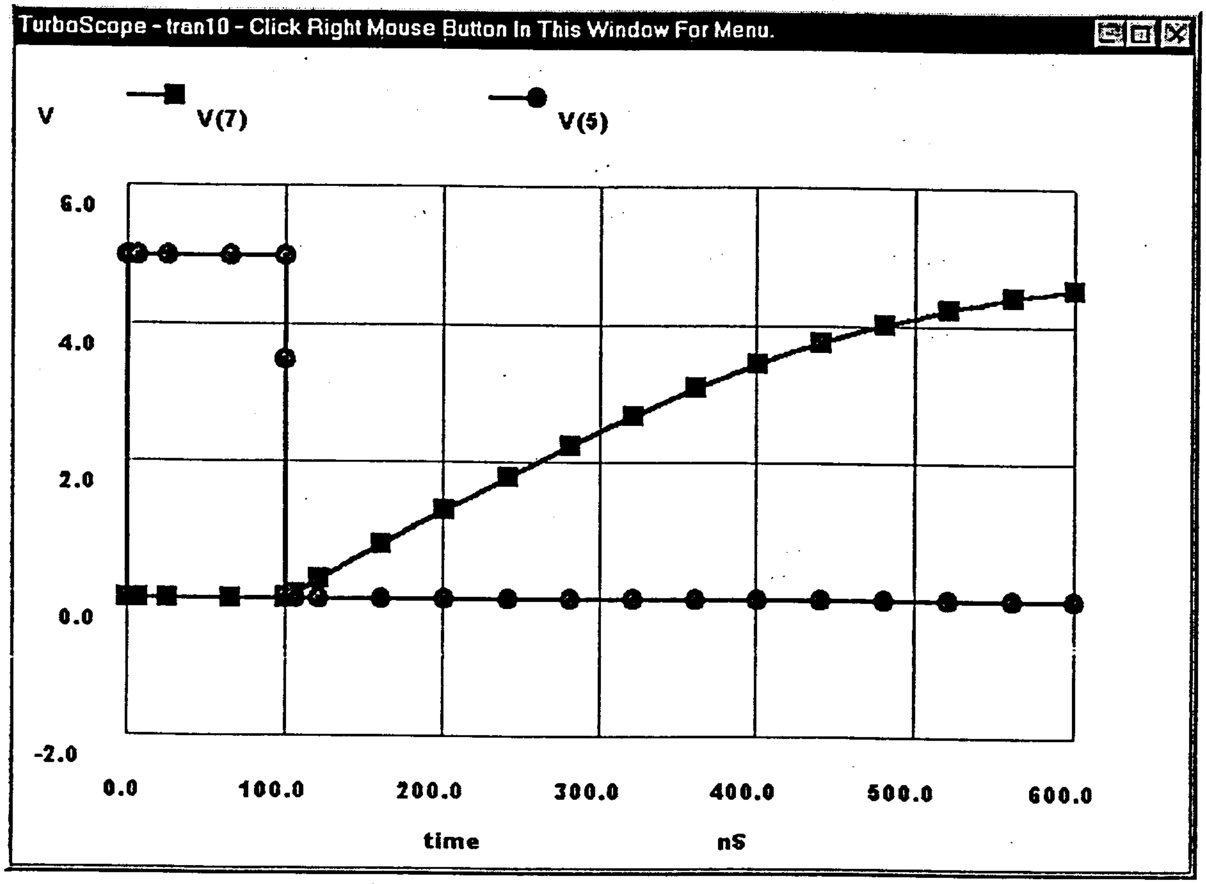


Problem 10.8



For nmos, $t_{PHL} \approx 8k\Omega \times 15pF = 120ns$; for pmos, $t_{PLH} \approx 360ns$





Problem 10.9

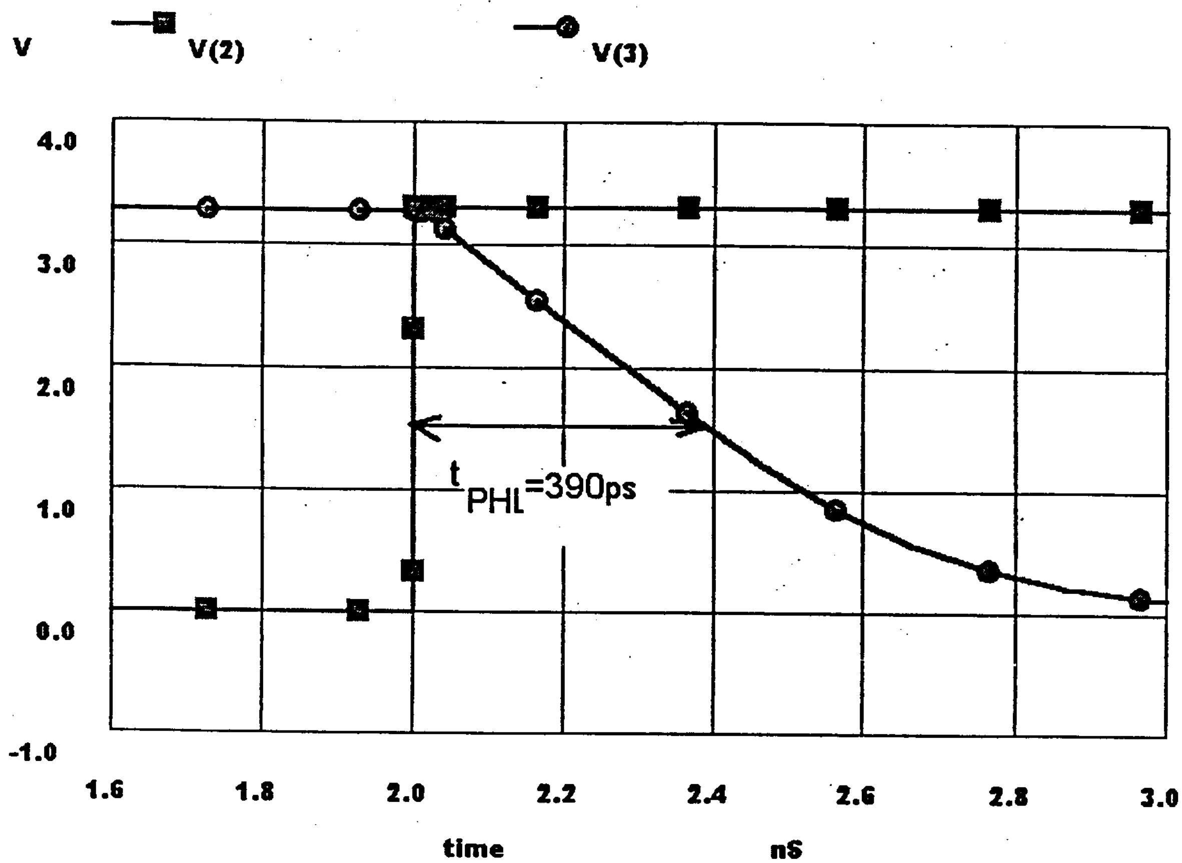
For 0.9µm/0.6µm MOSFET, the effective resistance of NMOS is Rn= 9kΩ /.9 = 10kΩ, and for the PMOS, Rp = 18kΩ /0.9 = 20kΩ. The capacitance between drain to ground is same for both NMOS and PMOS and equal to 3.7fF×0.6×.9 + 50fF = 52fF. From eq. (10.8) and (10.9), for NMOS,

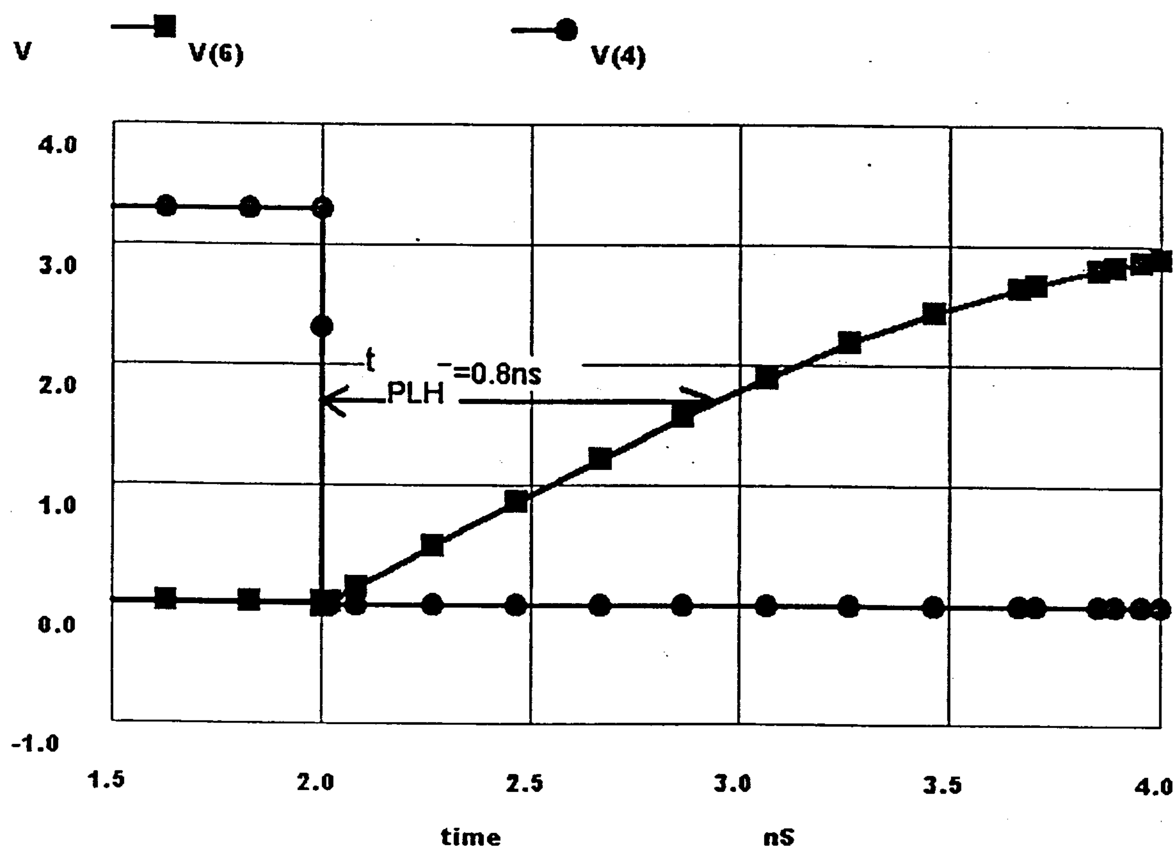
t_{PHL}=10kΩ×52fF = 520ps , t_{HL}= 1.04ns

for PMOS,

t_{PLH}=20kΩ×52fF = 1.04ns , t_{LH}= 2.08ns

SPICE simulation:


V
V(2)
V(3)
4.0
3.0
2.0
1.0
0.0
-1.0
t_{PHL}=390ps
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
time
nS


V
V(6)
V(4)
4.0
3.0
2.0
1.0
0.0
-1.0
t_{PLH}=0.8ns
1.5
2.0
2.5
3.0
3.5
4.0
time
nS